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Original Article

An Integrated Approach of CNT Front-end Amplifier towards Spikes Monitoring for Neuro-prosthetic Diagnosis

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Abstract The future neuro-prosthetic devices would be required spikes data monitoring through sub-nano-scale transistors that enables to neuroscientists and clinicals for scalable, wireless and implantable applications. This research investigates the spikes monitoring through integrated CNT front-end amplifier for neuro-prosthetic diagnosis. The proposed carbon nanotube-based architecture consists of front-end amplifier (FEA), integrate fire neuron and pseudo resistor technique that observed high electrical performance through neural activity. A pseudo resistor technique ensures large input impedance for integrated FEA by compensating the input leakage current. While carbon nanotube based FEA provides low-voltage operation with directly impacts on the power consumption and also give detector size that demonstrates fidelity of the neural signals. The observed neural activity shows amplitude of spiking in terms of action potential up to 80 μV while local field potentials up to 40 mV by using proposed architecture. This fully integrated architecture is implemented in Analog cadence virtuoso using design kit of CNT process. The fabricated chip consumes less power consumption of 2 μW under the supply voltage of 0.7 V. The experimental and simulated results of the integrated FEA achieves 60 GΩ of input impedance and input referred noise of 8.5 nv/$\sqrt{\text{Hz}}$ over the wide bandwidth. Moreover, measured gain of the amplifier achieves 75 dB midband from range of 1 KHz to 35 KHz. The proposed research provides refreshing neural recording data through nanotube integrated circuit and which could be beneficial for the next generation neuroscientists.

Keywords: Front-end amplifier (FEA), Integrate fire neuron, Neuro-prosthetic, Carbon nanotube (CNT), Pseudo resistor

Introduction

The neuromorphic engineering has recently become very popular towards the spike-based models of neurons. It is known that silicon neurons have been too much investigated and emulate the electrophysiological behaviors of real neurons using hybrid analog/digital very large scale integrated (VLSI) circuits. However, several neurons in the cortex of brain are complex systems that about to be 100 billion neurons, each with an average of 10^4 synapses and which required significant technological challenges[1]. The best nanotechnological solution is carbon nanotubes who behave as metallic wires with ballistic transport characterics and used in various FETs section to avoids scaling performance of silicon. The single-walled carbon nanotubes can easily avoid most of the fundamental scaling limitations of silicon[2]. Figure 1 shows typical blocks of the neuro-prosthetic diagnosis where neural recording is amplified through nanotube integrated chip (IC) and delivered to the wireless applications. This research mainly focuses on the nanotube based front-end amplifier (FEA) block for signal detection within neural activity monitoring systems. A front-end amplifier enables neuroscientists

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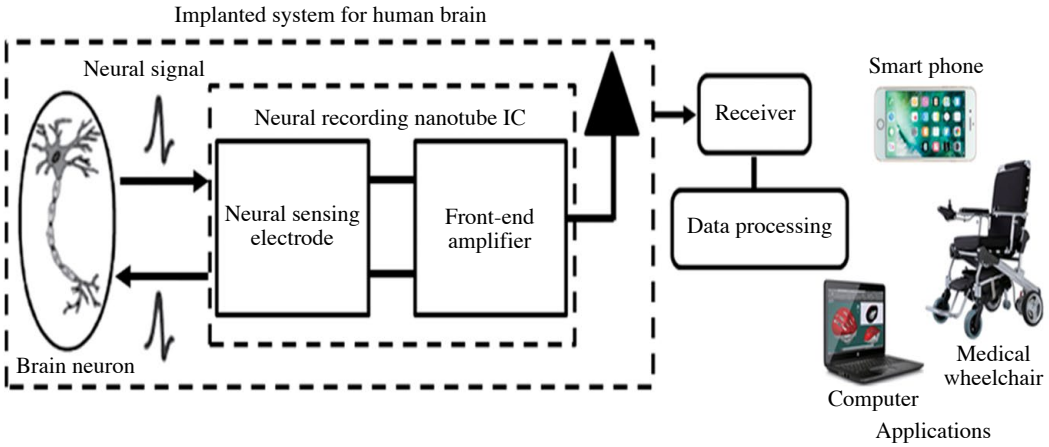


Figure 1. The typical flow block diagram of neuro-prosthetic application where neural recording nanotube IC captured neural data from neurons. And recorded data is amplified and delivers to the wireless-based applications.

to simultaneously record and observe large arrays of neural data using multiple electrodes and multi-channel monitoring systems[3-5]. Additionally, future research in disease and neuro-prosthetic devices can be enabled by acquiring neural activity data through high density array sensing[6]. As per described[7], neural activity generated electrically observable signals through analogue front-end model which are low in both amplitude as well as frequency. Generally, neural signal is typically comprised into two components, the Action potential (AP) known as neural spikes. The APs have amplitude ranging from 5 μV to 50 μV across frequencies of 300 Hz to 7.5 KHz. While another component is Local field potentials (LFP) having amplitudes ranging from 1 mV to 10 mV across frequency range of 25 mHz to 100 Hz. Moreover, some essential parameters such as interface impedance, bandwidth, input referred noise and power consumption could be improves performance of the FEA. The typical sensor seen impedance of the FEA in bio-signal detection varies from a few kΩ to few MΩ[8-11]. With regards to the FEA in bio-signal detection, the input impedance should be higher therefore attenuation can be lower caused by interface. Although, a low input noise FEA lowers the overall noise figure and increase signal to noise ratio of the entire neural sensing system. Still several authors reported their research on front-end amplifier within neural activity monitoring system without considering the various issue factors such as low area IC, suitability for implanted devices and scalability. For example, the instrumentation amplifier has been widely used for printed circuit board systems due to its high input impedance and easy of gain adjustment, although, it is not suitable for implanted devices because of large form factor[12]. A capacitive feedback biasing-based instrumentation amplifier negate the large chip area of resistors and simultaneously rejecting the DC offset. This topology has become very popular in neural recording applications but its input impedance is however limited by operational amplifier design due to its large input gate leakage current[13,14]. Moreover, several techniques are provided trade-off between the high input impedance and the low input referred noise such as chopper stabilization technique[15,16] but its drawback to suffer narrow bandwidth as compared to broader bandwidths that are required in implantable devices. A chopping instrumentation amplifier provided high input impedance and low input referred noise but its power consumption and circuit complexity are relatively too high[17]. In this paper, an integrated approach of CNT FEA towards spikes monitoring for neuro-prosthetic application is proposed. The proposed FEA considering of pseudo resistor technique and voltage amplifier with integrate fire neuron that achieves highest input impedance of 60 GΩ. This proposed technique also provides better exercise of neural spikes monitoring which are high in both amplitude as well as in frequency. A nanotube integrated FEA demonstrated best scaling performance as compared to silicon transistors which could be overcome issues such as minimize the chip area, scalability and suitability for brain implantation. The paper work is organized as follows: section II includes results and discussion of the CNT FEA while design and consideration of the nanotube FEA are followed in the section III. Finally, conclusion is brief in the section IV.

Results and Discussion

Performance Evaluation of Neural Activity

In this section, performance evaluation of CNT FEA

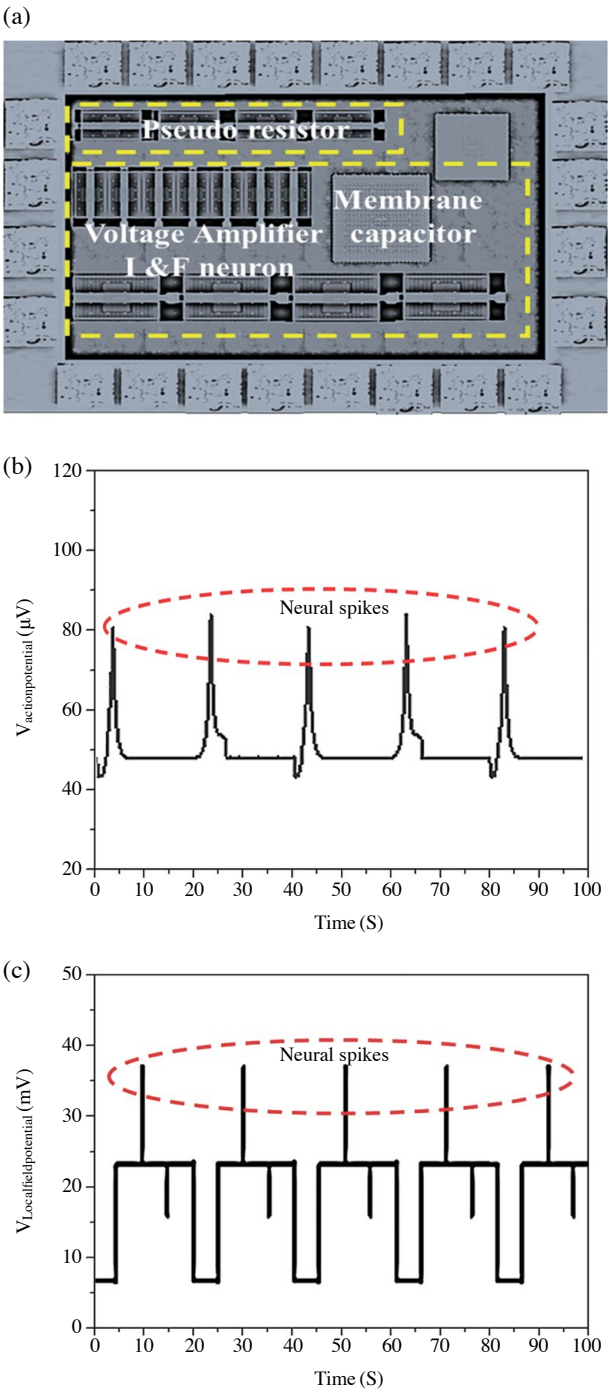


Figure 2. The proposed integrated FEA using CNT process with its (a) microchip photograph with all testing pads (b) simulated neuron spiking indicates action potential using first feedback when $V_{mem} > V_{th}$ and (c) simulated neuron spiking indicates local field potential using second feedback when $V_{mem} > V_{th}$.

would be discussing. An integrated FEA is implemented and fabricated using CNT process in a 32 nm wafer fab. A microchip photograph of the proposed FEA is shown in Figure 2(a) where area of chip is calculated as $0.012*0.015$ mm^2. These nanotube-based transistors enable to FEAs for miniaturization and implantable feature. A single-walled CNT is embedded between source and drain sections of FETs which provides less chip area as compared to conventional CMOS based FEAs. The simulated and measured observations are commencing with the monitoring of neural spikes where action potential (AP) and local field potential (LFP) voltages are examined. Figure 2(b) shows action potential spikes having maximum achievable amplitude whose range varies from 45 μV to 85 μV when membrane voltage exceeds the threshold voltage. An action potential is obtained at V_{out} to the transistor CN_{F4} through first feedback. As our design consideration, we choose input amplitude of 45 μV at the frequency of 1 KHz. Here every time, neural spikes reset the threshold voltage to a higher value therefore action potential must grow by a larger amount and time between spikes increases. The action potential voltage represents read-out neural spikes where peak points are circled in the red color. Similarly, another observation is to calculate local field potential having maximum peak to peak amplitude varying from 15 μV to 36 μV and which is shown in Figure 2(c). The LFP is also obtained at V_{out} to the transistor CN_{F3} through second feedback. The achieved amplitude range of LFP is same as our expected input amplitude of 15 μV at 1 KHz. The two feedbacks provide outputs into transistors CN_{F3} and CN_{F4} and which are controlled by two current sources: (1) sodium current I_{NA} and (2) potassium current I_K. It is clear at the point of observation that both monitored spikes are high in amplitude and frequency as compared to conventional CMOS ones. Additionally, measured input impedance achieves value of 60 GΩ with pseudo resistor technique and can be seen in Figure 3(a). It is because of pseudo resistor compensates the input leakage current and provides the higher impedance of FEA. This higher input impedance of FEA lowers the attenuation caused by sensor seen interface. The measured and simulated plotting of input impedance are made good correlation with each other. However, experimental result for input referred noise of the proposed FEA is shown in Figure 3(b) where value of 8.5 nv/$\sqrt{\text{Hz}}$ is achieved at 10 KHz. The lowest input referred noise provides minimum noise figure and enhance signal to noise ratio of the entire neural sensing system. The input referred noise are measured by using (Tektronix RSA3408A, spectrum analyzer) with testing board environment. Figure 3(c) shows the measured amplifier gain and bandwidth from 1 KHz to 35 KHz. The achieved midband gain is around 75 dB which is similar to our design specifications. The measurement of gain is done by Texas instrument equipment using

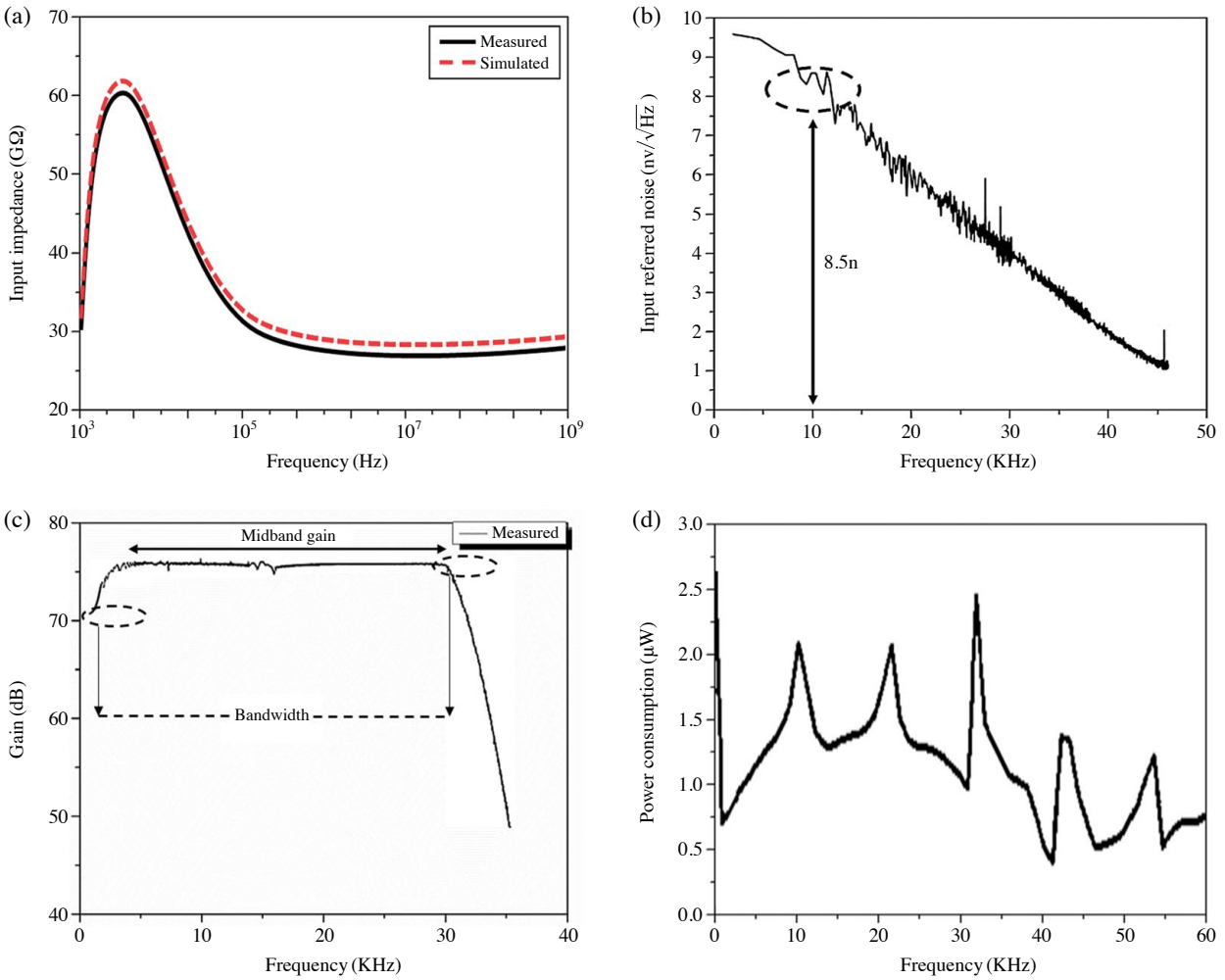


Figure 3. Experimental results of the proposed FEA with its (a) variation of input impedance with respect to frequency (b) lower input referred noise at 10 KHz (c) measured gain of the amplifier and (d) tested power consumption including all testing pads and benches.

on-chip test bench. The proposed FEA consumes less power consumption of 2.1 μW at the 10 KHz including all testing pads, board and benches. The measured power consumption of the fully integrated FEA is shown in Figure 3(d). The performance of nano-tube based FEA is compared with other reported papers which is shown in Table 1.

Conclusion

In this paper, integrated approach of CNT front-end amplifier towards spikes monitoring for neuro-prosthetic diagnosis is investigated. The proposed FEA architecture included pseudo resistor and voltage amplifier with integrate fire neuron that achieves ballistic performance as compared to conventional CMOS based ICs. The fabricated chip achieved input impedance of 60 GΩ and 8.5 nv/$\sqrt{\text{Hz}}$ of input-referred noise while power consumption of 2.1 μW with chip area of 0.012*0.015 mm^2. This research provides sub-nanoscale spikes monitoring method which could be useful for neuroscientists and clinicals in terms of scalable, implantable and wireless applications.

Designs and Consideration

Performance of CNTFET towards Spike Monitoring

An expected next computing technology demands less than 10 nm channel length-based transistors that could be embedded into integrated circuit chip and beneficial towards the neuro-prosthetic diagnosis with miniatur-

Table 1. Comparison performance of the proposed FEA with other reported ones.

Parameters	[8]	[17]	[21]	This work
Technology or process	0.35 μm	0.18 μm	0.5 μm	CNT 9 nm diameter
Technique	Instrumentation	Chopper stabilization	Capacitive feedback	Pseudo resistor with Voltage I&F
Supply voltage (V)	3	1	3.3	0.7
Power (μW)	930	13	4.95	<2
Gain (dB)	47	–	–	Midband gain of 75
Bandwidth (Hz)	100-12 K	0.3-1 K	800 K (Gain = 0)	1-30 K
Input impedance (Ω)	–	–	>50 TΩ	>60 G
Input referred noise ($v/\sqrt{Hz}$)	0.68 μ	4.4 μ	28 n	8.2 n
Chip area (mm^2)	0.08	0.076	–	0.012*0.015

– Not calculated

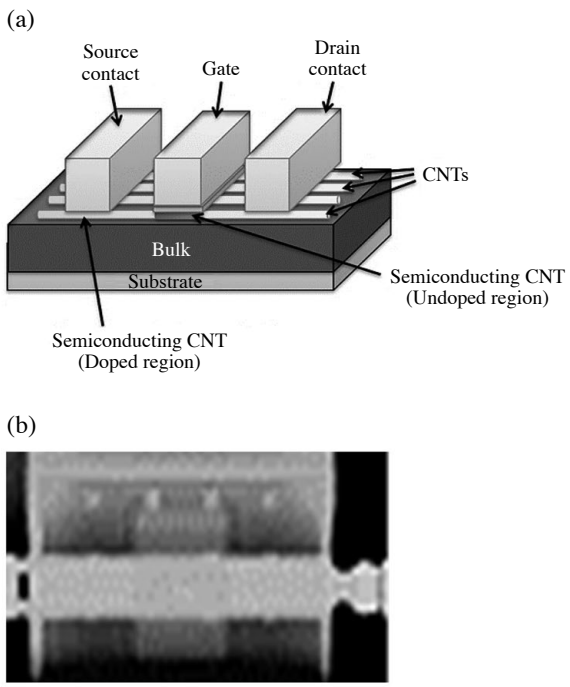


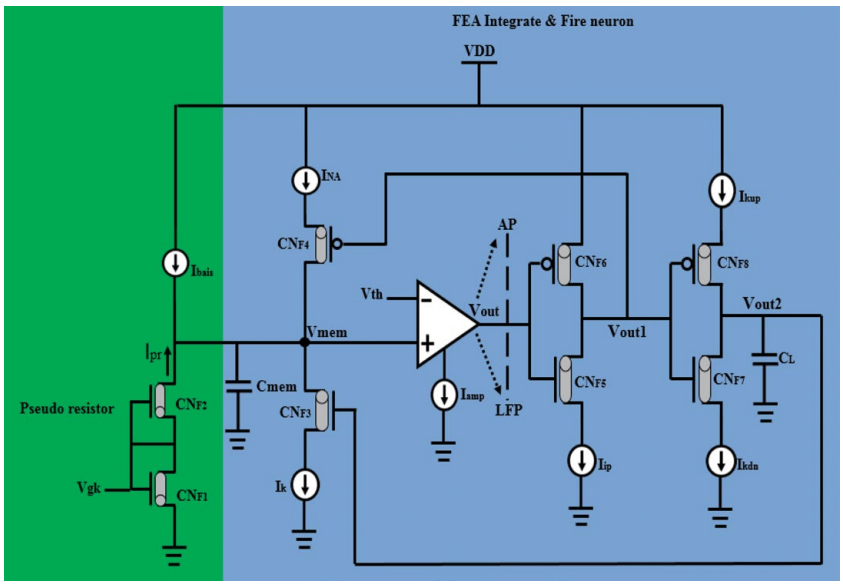
Figure 4. Carbon nanotube FET with its (a) cross-section schematic view (b) fabricated and microchip photograph.

ization and implantable features. It is well known that carbon nanotubes consist of single atomic layer of graphene rolled into 1-2 nm diameter seamless cylinder and provides ballistic carrier transport[18,19]. Although, its ability to maintain gate control of the current in a CNT transistor thus avoiding short-channel effects and should be better than for other competing structures, such as realizable nanowires or fins. In the sub-nanoscale era, CMOS circuit design technique are become very robust and crucial due to its substantially increased leakage current and sensitivity to process variations in manufacturing. In fact, when device physical gate length is reduced to below 25 nm, leakage current and device parameters become most important considerations for device optimization therefore it is more difficult to further improve device/circuit performance. The schematic diagram of CNTFET with its cross-section view and microchip photograph are shown in Figure 4(a) and 4(b) respectively. The CNTFET consists of semiconducting nanotube, acting as conducting channel and bridging between source and drain contacts. As compared with CMOS transistors, CNTFETs show a high performance and improved potential due to its small feature size and high-current capability. The intrinsic gate delay (CV/I) of CNTFET is 13 times better than the (CV/I) performance of a bulk MOSFET because driving current ability of each CNT is about 50% and effective gate capacitance of each CNT per gate is about 4% as compared to bulk CMOS[20]. Due to this, expected performance towards neuro-prothesis diagnosis provides better spikes monitoring as compared to CMOS technology era.

Integration and Technique

This section describes design and method of spikes monitoring technique using CNT based FEA for neuroprosthetic diagnosis. Figure 5(a) shows schematic of integrated CNT based FEA where spike event, gain, bandwidth and interface impedance are examined using this proposed structure. While equivalent circuit model of operational amplifier (op-amp) used in proposed schematic is shown in Figure 5(b) which provides voltage amplification output to the followed inverter stages. The proposed schematic consists of pseudo resistor for large input resistance while FEA integrate fire neuron for spikes monitoring which are high in both amplitude as well as frequency. The pseudo resistors comprise two carbon nanotube field effect transistors naming as CN_{F1} and CN_{F2} back to back and to create large resistance with acceptable layout. The pseudo resistor stage provides pseudo leakage current I_{Pr} in nanoampere (nA)

(a)



(b)

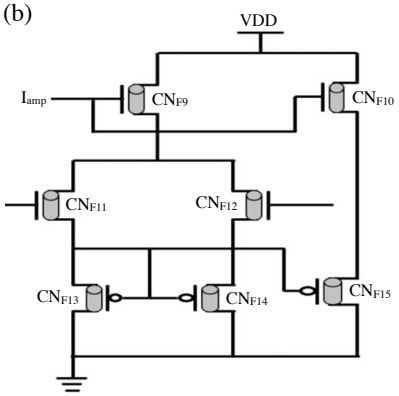


Figure 5. The integrated CNT FEA with its (a) Proposed schematic where neural spikes monitoring using two feedback approaches at the output of op-amp and (b) Equivalent models of operational amplifier used in FEA.

addition with I_{bais} to the FEA integrate fire neuron for high amplification operation. The FEA integrate fire neuron circuit provides spikes event when membrane potential V_{mem} exceeds the threshold voltage and that depends on the nanotube geometry of transistors and also nanoscale process characterics. Here, we consider brain neuron as a biological neuron where sodium and potassium tissues playing an important role for examination of the spike monitoring. The analysis of FEA integrate fire neuron commences with membrane of biological neuron which can be modelled by capacitance C_{mem} of this circuit while gate voltage V_{gk} of CNFET that controlling the membrane leakage current. As per operation of FEA integrate fire neuron, in the absence of any input V_{mem} gives sleeping potential by leakage current. The excitatory input (I_{bais}) add charge to the membrane capacitance C_{mem} while other inputs are remove charge from the same capacitance C_{mem}. When excitatory input is larger than leakage current is injected, the V_{mem} will increase from its sleeping potential. As V_{mem} exceeds the value with comparison of V_{th} using basic amplifier then action and local field potentials would be created. These created potentials will act as similar way in a biological neuron. The upswing of spike is created by increasing the conductance of sodium while downswing of spike by decreasing the conductance of potassium. It noting here that two feedbacks are used in the proposed schematic which are controlling the sodium current I_{NA} and the potassium current I_K. In addition, two inverters naming as CN_{F5}, CN_{F6} and CN_{F7}, CN_{F8} provides low and high output operations as per the low noise op-amp output. The current I_{Kup} controlling the speed at which capacitance C_L to be charged by the second inverter while I_{Kdn} controlling at which capacitance C_L to be discharged. During analysis, it is observed that op-amp schematic playing an important role for spike monitoring that are managed by using whole circuit topology. The gain bandwidth W_{GB} of the op-amp can be expressed in the equation (1).

$$W_{GB} = \sqrt{2K_p\left(\frac{W}{L_{CNT}}\right)I_{DS}} \tag{1}$$

Here, W and L_{CNT} are width and CNT length of the corresponding transistor while I_{DS} is the drain to source current. Also, overall open loop gain of the op-amp can be expressed in the equation (2).

$$A_{op\text{-}amp} = \frac{G_{m12}}{G_{ds12}+G_{ds14}} \cdot \frac{G_{m15}}{G_{ds15}+G_{ds10}} \tag{2}$$

Where

$$G_{ds} = I_D * \lambda \tag{3}$$

G_{ds} is transconductance of nanotube transistor, I_D is the drain current and λ is channel length parameter depends on the nanotube manufacturing process. The input referred voltage noise of the FEA integrate fire neuron consists of thermal and flicker noise that can be expres-

Table 2. Dimension values of integrated front-end amplifier.

Components	Values (W/L) nm
CN_{F1}, CN_{F5} & CN_{F11}	0.025/9
CN_{F2}, CN_{F4} & CN_{F15}	0.122/9
CN_{F6} & CN_{F9}	0.082/9
CN_{F10}	0.046/9
CN_{F8}	0.021/9
CN_{F9} & CN_{F10}	0.057/9
CN_{F3}, CN_{F7} & CN_{F12}	0.051/9
CN_{F13}	0.045/9
CN_{F14}	0.022/9

sed in equation (4)

$$\overline{V_{n,FEA}^2} = \overline{V_{n,thermal}^2 + V_{n,flicker}^2} \tag{4}$$

The thermal noise is calculated as in equation (5) and (6) respectively.

$$\overline{V_{n,thermal}^2} = \frac{48KT}{9} * \frac{1}{G_{CNF3}^2} * \left[G_{CNF3} + G_{CNF13} + \frac{G_{CNF15} + G_{CNF10}}{2G_{CNF15}^2 (r_{0F12} \parallel r_{0F14})} \right] \tag{5}$$

$$\simeq \frac{48KT}{9} * \frac{1}{G_{CNF3}^2} * (G_{CNF3} + G_{CNF13}) \tag{6}$$

While flicker noise is calculated as in equation (7).

$$\overline{V_{n,flicker}^2} = \frac{2K_p}{W_{CNF4} L_{CNF3} C_{ox} f} + \frac{2K_n}{W_{CNF3} L_{CNF3} C_{ox} f \left(\frac{G_{CNF11}}{G_{CNF3}} \right)^2} \tag{7}$$

Here, K is the process dependent constant and C_{ox} is gate oxide capacitance of the carbon nanotube field effect transistor. Also, input referred current noise of the FEA integrate fire neuron can be calculated as in equation (8).

$$\overline{I_n^2} = \left[(2\pi f)^2 C_{mem}^2 \overline{V_n^2} \right] \Delta f \tag{8}$$

C_{mem} is membrane capacitance of the input device, V_n^2 is the input-referred voltage noise and f are the frequency over the wide bandwidth. The proposed schematic is implemented and analyzed into analog cadence virtuoso using CNT process. The dimension values of all components for proposed FEA is shown in Table 2.

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