IETE Journal of Research

ISSN: 0377-2063 (Print) 0974-780X (Online) Journal homepage: https://www.tandfonline.com/loi/tijr20

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To cite this article: Yajunath Kaliyath & Tonse Laxminidhi (2019) A 1.8 V 8.62 µW Inverter-based Gain-boosted OTA with 109.3 dB dc Gain for SC Circuits, IETE Journal of Research, 65:6, 749-757, DOI: 10.1080/03772063.2018.1464968

To link to this article: https://doi.org/10.1080/03772063.2018.1464968

Published online: 14 Jun 2018.

IETE JOURNAL OF RESEARCH
2019, VOL. 65, NO. 6, 749–757
https://doi.org/10.1080/03772063.2018.1464968

A 1.8 V 8.62 µW Inverter-based Gain-boosted OTA with 109.3 dB dc Gain for SC Circuits

Yajunath Kaliyath and Tonse Laxminidhi

Department of Electronics and Communication Engineering, National Institute of Technology Karnataka, Surathkal, Mangalore, Karnataka, India

ABSTRACT

This paper presents a low-power inverter-based gain-boosted operational transconductance amplifier (OTA) for switched capacitor (SC) circuits operating at higher supply voltage (> 1 V). The proposed OTA is implemented using UMC 180 nm CMOS technology with a supply voltage of 1.8 V and it offers a high dc gain with a unity gain bandwidth (UGB) suitable for audio applications. All the transistors of the proposed OTA are operated in sub-threshold region to minimize the power consumption. Gain-boosting technique is employed to achieve a higher dc gain. The post-layout simulations demonstrate the robust performance of the proposed OTA, which delivers a high dc gain of 109.3 dB and a UGB of 5.29 MHz at 81° phase margin (PM) with a capacitive load of 2.5 pF for a typical process corner at room temperature (27°C). The proposed OTA draws a quiescent current (I_Q) of 4.79 µA, resulting in a power consumption of 8.62 µW.

KEYWORDS

Gain-boosting; High gain; Inverter-based; Low power; OTA; Switched capacitor

1. INTRODUCTION

Switched capacitor circuits are used in the discrete-time implementation of most of the analog and mixed signal integrated circuit (IC) designs such as filters and $\Delta\Sigma$ modulators [1,2]. An OTA is the basic building block in a SC circuit and it accounts for a large fraction of the total power consumed by the IC. Further, the dc gain of an OTA determines the accuracy of charge transfer in the SC circuits [2]. So, SC circuits require an OTA that offers a high dc gain in order to ensure an accurate charge transfer. Folded-cascode topology has been the preferred choice for OTA implementation, as it offers a high dc gain; but, they consume a lot of power when operated at higher supply voltages [3–5]. Recently, inverter-based OTA's have been reported to replace the traditional OTA's in SC applications [6–8]. Design simplicity, area efficiency and power efficiency (at lower supply voltages) are the main advantages of an inverter-based OTA. However, these inverter-based OTA's are suitable for only low voltage applications ($VDD < 1$ V) because they consume a lot of power when operated at higher supply voltages ($VDD > 1$ V) [6,8].

SC circuit based data converters, operating at supply voltages greater than 1 V, are used in the design of several portable, battery powered electronic applications such as digital microphones [9,10], bio-sensors [11–13], image sensor [14], data acquisition systems [15,16], hearing aids [17–19], etc. Such applications require low-power designs, which would result in a relatively cooler devices with longer battery run time. So, an OTA that delivers high dc gain with lower power consumption will help in realizing the objective of low-power design, but designing such an OTA is quite challenging.

In this work, a novel low-power solution for designing an OTA, based on inverter and operating at higher supply voltage, has been proposed for SC circuits. It offers high dc gain and UGB suitable for audio applications. The transistors are operated in sub-threshold region to lower the power consumption. Gain-boosting technique has been employed to achieve higher dc gain. A preliminary work on this has been presented in [20]. This work is an extension with a refined design. The novelty of the proposed work when compared to that presented in [20] are the following.

- The proposed OTA offers about two folds enhancement in bandwidth for the same capacitive load while consuming 22% less power.
- The proposed OTA is designed to be stable without the need for any explicit compensating capacitor. Moreover, the proposed OTA achieves a higher phase margin of 81° as against 63° in [20]. Note that the OTA

presented in [20] uses four capacitors for frequency compensation.
- The relaxation on compensating capacitor requirement resulted in an enhancement of slew rate by 3.4 times, that too while consuming 22% less power.

This paper also discusses the design and stability issues with necessary mathematical analysis. The robustness of the design has been evaluated through post layout and Montecarlo simulations in this work.

The rest of the paper is organized as follows. Section 2 explains the design of the proposed OTA. The implementation of SC integrator using inverter-based OTA is outlined in Section 3. Results and discussions are presented in Section 4. Comparison with other published works are made in Section 5 and conclusions are drawn in Section 6.

2. PROPOSED OTA

The complete schematic of the proposed low-power inverter-based gain-boosted OTA is shown in Figure 1. Transistor pairs *M2p*, *M3p* and *M2n*, *M3n* form two source follower circuits with active load and they act as level shifters. These source follower circuits are used to bias *M1p* and *M1n* transistors in sub-threshold region, where the bias currents are relatively low, and thereby reducing the quiescent current drawn from the supply (*VDD*). The source followers are biased and sized such that they draw very low quiescent current from the supply.

Transistors *M4p*, *M5p*, *M5n* and *M4n*, *M6p*, *M6n* form two gain-boosting stages and they are used for achieving a higher dc gain. The transistors used in the gain-boosting stages are also operated in sub-threshold region in order to minimize the power consumption by carefully sizing and biasing them. The biasing voltages $V_{bias,p}$ and $V_{bias,n}$ are choosen such that $|V_{GS}|$ of *M3p*, *M6p* and *M3n*, *M5n* transistors are lesser than their respective $|V_{TH}|$. The bias voltages $V_{bias,p}$ and $V_{bias,n}$ are generated from a common-mode reference voltage V_{cm} ($= VDD/2$) as shown in the biasing circuit block in Figure 1. The input and output nodes of the proposed OTA settles to a common-mode voltage of V_{mid} when connected in feedback configuration and with proper sizing, V_{mid} is chosen to be close to $VDD/2$ for achieving maximum possible output swing.

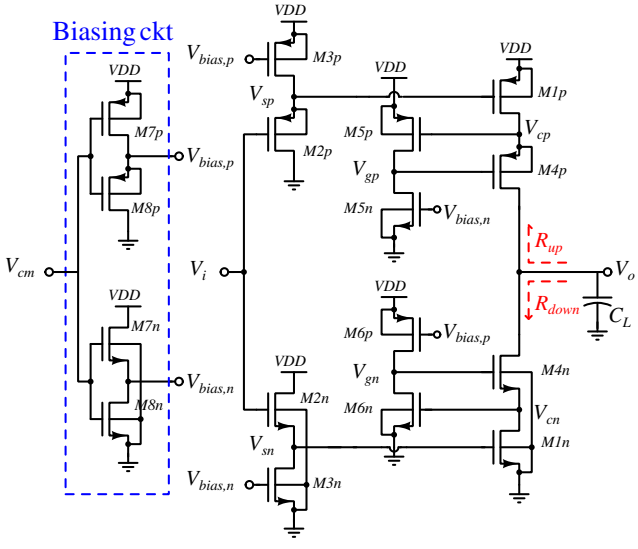

Figure 1: Schematic of proposed OTA

The small signal gain of the proposed OTA is given by (1). The body effect of *M2n* and *M4n* are neglected for the purpose of mathematical simplicity.

$$A_v = -G_m \cdot R_{out}, \tag{1}$$

$$G_m \approx g_{m_{1p}} A_{v1} + g_{m_{1n}} A_{v2}, \tag{2}$$

$$A_{v1} = \frac{g_{m_{2p}}(r_{o_{2p}} \parallel r_{o_{3p}})}{1 + g_{m_{2p}}(r_{o_{2p}} \parallel r_{o_{3p}})}, \tag{3}$$

$$A_{v2} \approx \frac{g_{m_{2n}}(r_{o_{2n}} \parallel r_{o_{3n}})}{1 + g_{m_{2n}}(r_{o_{2n}} \parallel r_{o_{3n}})}, \tag{4}$$

$$R_{out} = R_{up} \parallel R_{down}, \tag{5}$$

$$R_{up} \approx r_{o_{1p}} r_{o_{4p}} g_{m_{4p}} g_{m_{5p}} (r_{o_{5p}} \parallel r_{o_{5n}}), \tag{6}$$

$$R_{down} \approx r_{o_{1n}} r_{o_{4n}} g_{m_{4n}} g_{m_{6n}} (r_{o_{6p}} \parallel r_{o_{6n}}), \tag{7}$$

where G_m and R_{out} are the overall transconductance and the output resistance of the OTA respectively, A_{v1} and A_{v2} are the small signal voltage gains of the upper and lower source follower stages respectively, $r_{o_{XX}}$ and $g_{m_{XX}}$ are the output resistance and the transconductance of the transistors *Mxx* respectively. From (1), it is evident that proposed OTA can achieve a very high dc gain by carefully biasing and sizing the transistors.

2.1 Stability Analysis

In SC circuits, OTA's are used in negative feedback configuration and therefore it is necessary that the proposed OTA is stable in the closed loop configuration. The location of the open loop poles of the OTA decides the closed loop stability. Closed loop stability can be achieved if the OTA's frequency response is made to follow a first order response within its UGB. The location of the poles of the

proposed OTA and the constraints for ensuring closed loop stability are presented as follows.

The dominant pole of the OTA occurs at the output node (V_o) and is given by (8).

$$p_1 = -\frac{1}{R_{out}C_{out}}, \tag{8}$$

where C_{out} is the total capacitance at the output node (V_o) of the OTA.

The UGB of the OTA is given by (9)

$$w_u = \frac{G_m}{C_{out}}. \tag{9}$$

The non-dominant poles occurring at the cascode nodes V_{cp} and V_{cn} are given by (10) and (11) respectively.

$$p_2 = -\frac{1}{R_{v_{cp}}C_{v_{cp}}}, \tag{10}$$

$$p_3 = -\frac{1}{R_{v_{cn}}C_{v_{cn}}}, \tag{11}$$

$$R_{v_{cp}} \approx r_{o_{1p}} \parallel \left(\frac{r_{o_{4p}} + R_{down}}{1 + G_{m_{4p}}r_{o_{4p}}}\right), \tag{12}$$

$$R_{v_{cn}} \approx r_{o_{1n}} \parallel \left(\frac{r_{o_{4n}} + R_{up}}{1 + G_{m_{4n}}r_{o_{4n}}}\right), \tag{13}$$

$$G_{m_{4p}} \approx g_{m_{4p}}g_{m_{5p}}\left(r_{o_{5p}} \parallel r_{o_{5n}}\right), \tag{14}$$

$$G_{m_{4n}} \approx g_{m_{4n}}g_{m_{6n}}\left(r_{o_{6p}} \parallel r_{o_{6n}}\right), \tag{15}$$

where $R_{v_{cp}}$, $R_{v_{cn}}$ and $C_{v_{cp}}$, $C_{v_{cn}}$ are the effective output resistances and total capacitances at the cascode nodes V_{cp} and V_{cn}, respectively.

From (10) and (11), it is evident that $|p_2|, |p_3| \gg |p_1|$ ($\because R_{out} \gg R_{v_{cp}}, R_{v_{cn}}$ and $C_{out} \gg C_{v_{cp}}, C_{v_{cn}}$), which means that the poles contributed by the cascode nodes are far away from the dominant pole. Further, to ensure a first order roll-off, poles p_2, p_3 should satisfy (16) so that they lie beyond the UGB of the OTA. This can be achieved by carefully biasing and sizing the transistors.

$$|p_2|, |p_3| > w_u. \tag{16}$$

The non-dominant poles contributed by the input source follower stages at nodes V_{sp} and V_{sn} are given by (17) and (18) respectively.

$$p_4 \approx -\frac{1}{[(1/g_{m_{2p}}) \parallel r_{o_{3p}}]C_{v_{sp}}}, \tag{17}$$

$$p_5 \approx -\frac{1}{[(1/g_{m_{2n}}) \parallel r_{o_{3n}}]C_{v_{sn}}}, \tag{18}$$

where $C_{v_{sp}}$ and $C_{v_{sn}}$ are the total capacitances at the nodes V_{sp} and V_{sn}, respectively.

Clearly, $|p_4|, |p_5| \gg |p_1|$, which means that these poles are far away from the dominant pole. Further, these poles have to satisfy (19) in order to ensure a first order roll-off for the OTA, which can be achieved by carefully biasing and sizing the transistors in the source follower circuit.

$$|p_4|, |p_5| > w_u. \tag{19}$$

If either one of (16) or (19) is not met, then the OTA has to be frequency compensated for ensuring closed loop stability, which was the case in [20]. However, the proposed OTA has been designed carefully through proper transistor sizing to ensure closed loop stability without the need for any explicit frequency compensation.

3. SC INTEGRATOR USING INVERTER-BASED OTA

The proposed OTA is validated for its application in a pseudo-differential SC integrator. Figure 2 shows a parasitic insensitive pseudo-differential inverter-based SC integrator circuit with auto-zeroing technique [7].

The operation of the SC integrator is as follows. Initially, the integrating capacitors (C_i) are reset in the ϕ_{rst} phase. In ϕ_1 phase, the input is sampled onto the sampling capacitors (C_s) and the voltage difference between V_{mid} and V_{cm} is stored across the the offset-storing capacitors (C_{off}) in order to make the nodes V_{xp} and V_{xn}, a virtual ground during the charge transfer (ϕ_2) phase. In the ϕ_2 phase, the charge stored in the sampling capacitors are transferred to the integrating capacitors.

The transfer function of the SC integrator in the z-domain is given by (20)

$$\frac{V_{o,diff}(z)}{V_{i,diff}(z)} = \frac{C_s}{C_i}\frac{z^{-1/2}}{1 - z^{-1}}. \tag{20}$$

A passive common-mode feedback circuit (CMFB) is used to minimize the effects of mismatch between the two branches of the pseudo differential configuration. It also helps in minimizing the effects of charge injection.

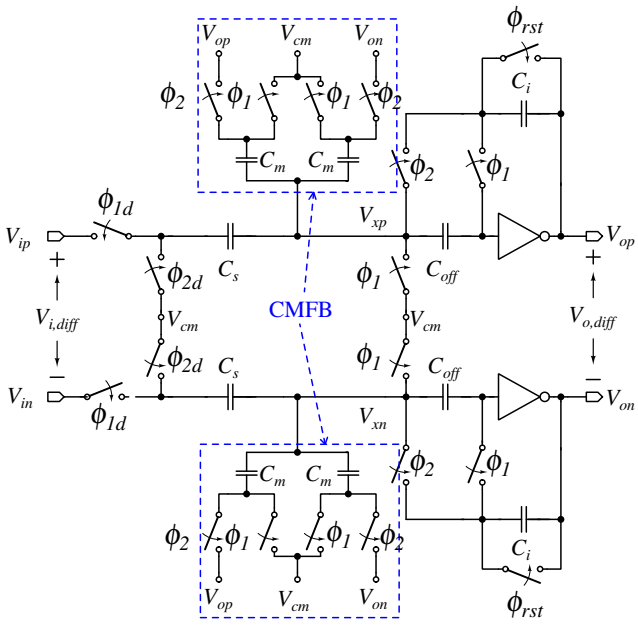

Figure 2: Pseudo-differential inverter-based SC integrator

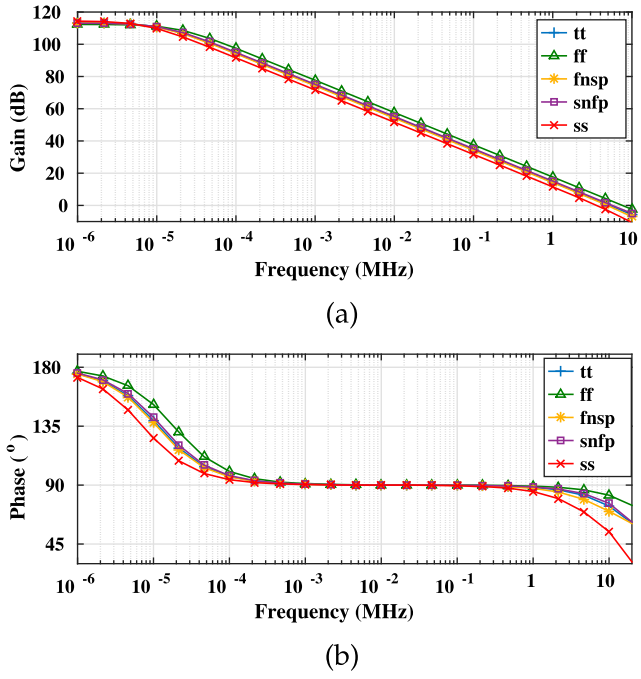

Figure 3: (a) Magnitude and (b) phase response of the proposed OTA

4. RESULTS AND DISCUSSIONS

The proposed OTA has been designed in UMC 180 nm CMOS technology and it is operated on a supply voltage of 1.8 V with a load capacitance (C_L) of 2.5 pF.

4.1 Performance of the Proposed OTA

The performance of the proposed OTA across different process corners is evaluated to verify the robustness of the design. The frequency response of the proposed OTA for different process corners at room temperature are shown in Figure 3 and the key features are summarized in Table 1.

Table 1: Performance of the proposed OTA across process corners

Process corner	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (µA)	V_{mid} (mV)
tt	113.3	81.2	5.31	4.78	900.0
ss	114.4	73.6	3.60	2.08	896.1
ff	112.3	84.2	7.59	12.85	905.4
fnsp	113.3	78.6	4.91	5.44	892.4
snfp	113.1	82.1	5.70	5.30	908.5

From Table 1, it can be noted that the proposed OTA maintained a dc gain in excess of 110 dB across the process corners. It is also observed that the proposed OTA offered more than sufficient phase margin across the process corners. At slow-slow (ss) corner, the UGB has degraded by 32% when compared to a typical (tt) corner. However, the UGB offered is quite sufficient for audio applications. A three fold increase in the quiescent current consumption is observed at fast-fast (ff) corner when compared to a typical corner. This is due to the fact that currents in transistors are decided by the biasing voltages $V_{bias,p}$ and $V_{bias,n}$, which vary with process corners. However, it is quite low considering that the OTA is operated at a higher supply voltage of 1.8 V. Further, it is also observed that the variation in V_{mid} is limited to less than 10% and therefore the the output swing of the OTA is not severely affected.

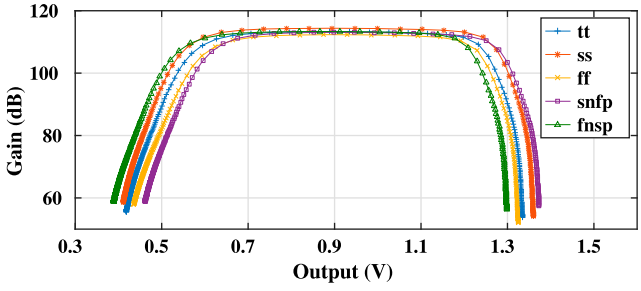

Figure 4: Gain vs output voltage of the proposed OTA

Figure 4 shows the plot of gain versus output voltage of the OTA for different process corners at room temperature. It can be observed that the OTA offers a gain in excess off 100 dB across corners for an output swing of ±350 mV around V_{mid}.

Figure 5 shows the output noise spectrum of the proposed OTA. The total integrated output noise (from 1 Hz to 10 MHz) of the OTA is found to be 19.76 µV.

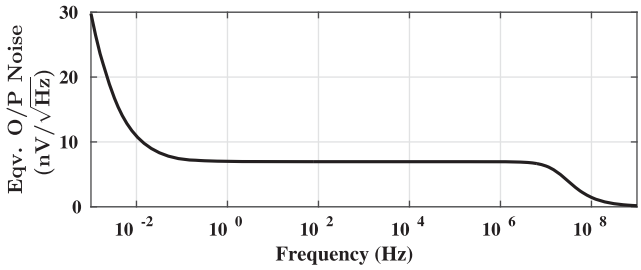

Figure 5: Output noise spectrum of the proposed OTA

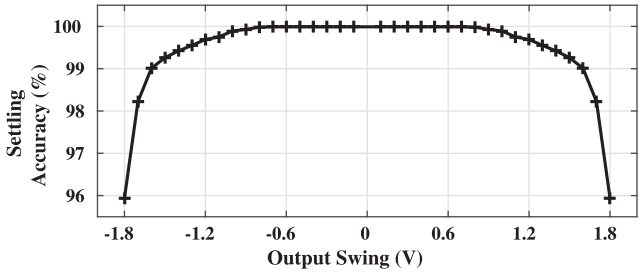

Figure 6: Settling accuracy vs. output swing

4.2 Performance of SC Integrator

In the SC integrator circuit, $C_s = C_i = C_{off} = 1$ pF and $C_m = 0.5$ pF have been used for evaluating OTA's performance. The settling accuracy of the SC integrator completely depends on the dc gain of the OTA. Figure 6 shows the plot of settling accuracy vs output swing of the pseudo-differential SC integrator for a typical process corner at room temperature. The integrator achieves the best settling accuracy of 99.99% for a maximum differential output transition of ±600 mV and maintains a settling accuracy of 99.9% for a maximum differential output voltage of ±900 mV.

Figure 7 shows the step response of the pseudo-differential SC integrator for a 200 mV differential output transition for different process corners at room temperature. The integrator settles faster in the ff corner and exhibits a slower settling in ss corner when compared to a typical corner. The integrator takes 0.3, 0.39 and 0.48 µs for ff, tt and ss corners, respectively for achieving a settling accuracy of 99.99%.

4.3 Layout and Post-layout Simulations

The layout of the proposed OTA is shown in Figure 8. It occupies an area of 71.30 µm × 21.04 µm. The OTA's performance has been evaluated on the RC extracted net list.

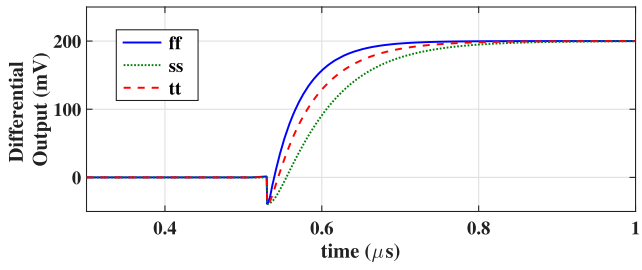

Figure 7: Step response of pseudo-differential SC integrator

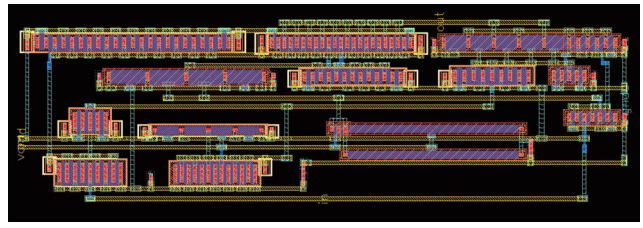

Figure 8: Layout of the proposed OTA

Table 2: Post-layout performance across process corners

Process corner	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (µA)	V_{mid} (mV)
tt	109.3	80.5	5.29	4.79	900.2
ss	111.8	71.8	3.57	2.08	896.2
ff	108.8	83.7	7.56	12.85	905.6
fnsp	101.4	78.1	4.87	5.48	893.4
snfp	112.3	81.1	5.68	5.30	908.5

The performance metrics of the layout extracted OTA for different process corners, at room temperature (27°C), are presented in Table 2. The dc gain of the OTA is found to be slightly lower than that of a pre-layout (schematic) simulation. This is attributed to the leakage in the dummy transistors that are added to maintain symmetry in the environment seen by each transistor finger. All other performance metrics remain almost the same. Therefore, the post-layout performance of the OTA is considered robust against process variations.

The post-layout performance of the proposed OTA at different supply voltages, for a typical process corner at room temperature, is presented in Table 3 and it is observed that the OTA manages to offer high dc gain, sufficient phase margin, adequate UGB and draws low quiescent current.

The post-layout performance of the proposed OTA at different temperatures for a typical process corner is presented in Table 4 and it is worth noting that the proposed OTA offers a dc gain in excess of 80 dB even at 70°C temperature. The quiescent current consumed by the OTA is still low, considering that the OTA is operated at 1.8 V supply.

Table 3: Post-layout performance at different supply voltages

Supply (V)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (µA)	V_{mid} (mV)
1.71 (−5%)	111.1	77.1	4.15	2.92	854.5
1.755 (−2.5%)	110.3	78.9	4.70	3.72	877.3
1.8	109.3	80.5	5.29	4.79	900.2
1.845 (+2.5%)	108.1	81.7	5.91	6.21	923.2
1.89 (+5%)	106.8	82.7	6.58	8.09	946.3

Table 4: Post-layout performance at different temperatures

Temp (°C)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (µA)	V_{mid} (mV)
−10	113.7	67.6	4.63	2.61	899.4
27	109.3	80.5	5.29	4.79	900.2
50	97.4	83.7	5.27	7.82	902.0
70	84.6	84.7	5.22	12.25	910.6

Table 5: Post-layout performance with variations in V_{cm}

V_{CM} (mV)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (µA)	V_{mid} (mV)
882 (−2%)	110.3	81.4	5.34	4.88	886.8
891 (−1%)	109.8	81.0	5.32	4.81	893.5
900	109.3	80.5	5.29	4.79	900.2
909 (+1%)	108.7	79.9	5.25	4.81	906.9
918 (+2%)	108.0	79.2	5.21	4.89	913.7

Since the biasing voltages $V_{bias,p}$ and $V_{bias,n}$ are generated from the common-mode reference voltage (V_{cm}), the effect of variation in the V_{cm} voltage on the performance of the OTA is evaluated. Table 5 summarizes the performance of the OTA with the variations in V_{cm} voltage for a typical process corner at room temperature. The performance of the proposed OTA is found to be robust under the variations in the common-mode reference voltage (V_{cm}).

4.4 Monte Carlo Analysis

Mismatch between transistors can effect the performance of the OTA, especially for a pseudo-differential architecture. Hence, a Monte Carlo simulation has been carried out on the layout extracted net list to verify the robustness of the design against process mismatch.

Figures 9–13 show the distribution of dc gain, UGB, PM, I_Q and V_{mid} respectively for 500 samples (N) along with their respective mean (μ) and standard deviation (σ). The plots reveal that the proposed OTA is robust even with local mismatches.

The key performance metrics of the proposed OTA obtained from the post-layout simulations for a typical process corner at room temperature (27°C) are summarized in Table 6.

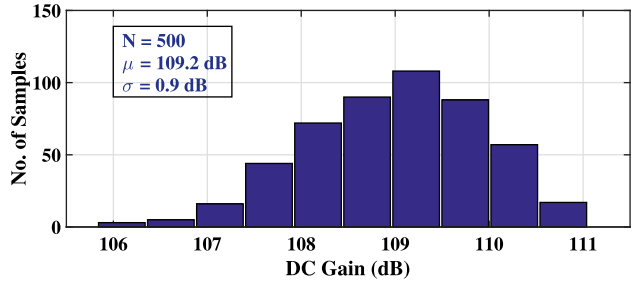

Figure 9: Distribution of DC gain

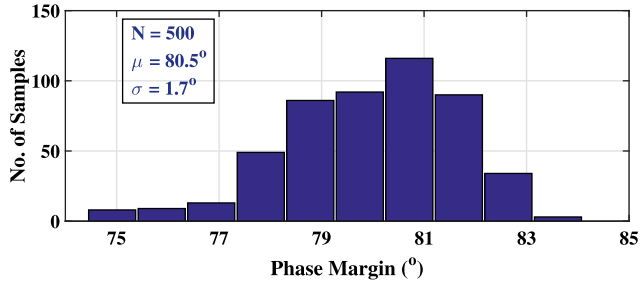

Figure 10: Distribution of PM

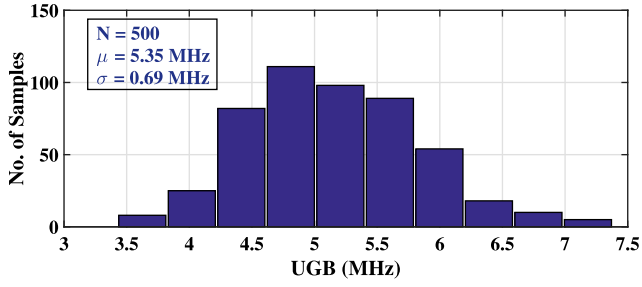

Figure 11: Distribution of UGB

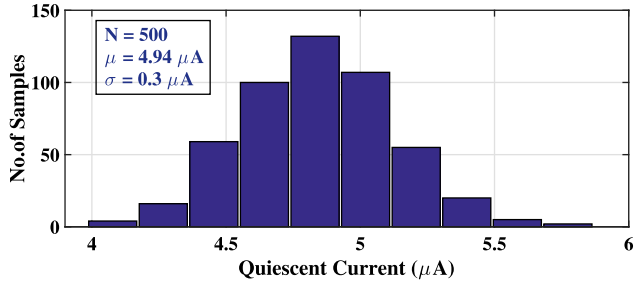

Figure 12: Distribution of quiescent current (I_Q)

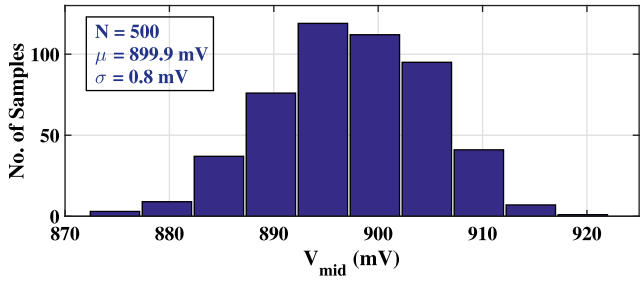

Figure 13: Distribution of V_{mid}

Table 6: Summary of proposed OTA's performance

Parameter	Value
Technology (nm)	180
Supply (V)	1.8
DC gain (dB)	109.3
PM (°)	81
GM (dB)	30.2
UGB (MHz)	5.29
Input referred noise (µV/$\sqrt{\text{Hz}}$)	121.1 @ 10 KHz
Output swing (mV) (@ 1% THD)	±442
Average slew rate (V/µs)	41.3
I_Q (µA)	4.79
Power (µW)	8.62
C_L (pF)	2.5

5. COMPARISON

Table 7 compares the performance of the proposed OTA with other works operating on 1.8 V.

The performance of the proposed OTA is also compared with OTA's operating on lower supply voltage and it is presented in Table 8. Figure of Merit (FOM)[24] used for comparison is given by (21). The higher the FOM, the more power efficient is the design.

$$\text{FOM} = \frac{\text{UGB (MHz)}.C_L(\text{pF})}{I_Q(\text{mA})}. \tag{21}$$

From Table 7, it is evident that the proposed OTA offers the highest dc gain while consuming very low power when compared with other works and therefore achieves a higher FOM. It is worth noting from Table 8 that the power consumption of the proposed OTA is even lower than that of the OTA's operating on lower supply voltages and thereby resulting in a higher FOM. So, from these comparisons it is evident that the proposed OTA is very power efficient.

Table 7: Comparison of proposed OTA with OTA's operating on 1.8 V

	[3]	[4]	[5]	[21]	[22]	[23]	This work
Technology (nm)	180	180	180	180	180	180	180
DC Gain (dB)	87.7	90.7	67.0	77.0	74.0	72.0	109.3
PM (°)	74	82	69	45	–	50	81
UGB (MHz)	24.8	995	581	475	160	86.5	5.3
C_L (pF)	1	0.5	0.25	3	1.75	200	2.5
Power (μW)	573.5	12600	920	5100	362	11900	8.6
FOM $(\text{kV})^{-1}$	78	71	284	503	773	2616	2792

Table 8: Comparison of proposed OTA with OTA's operating on lower supply voltage

	[24]	[25]	[26]	[27]		[28]	This work
Technology (nm)	130	350	180	65		50	180
Supply (V)	1	±0.5	0.7	0.5	0.35	0.4	1.8
DC Gain (dB)	60	88.3	57.5	46	43	60	109.3
PM (°)	72	66	60	57	56	70	81
UGB (MHz)	3.7	11.7	3	38	3.6	2.5	5.3
C_L (pF)	95	15	20	3		10	2.5
Power (µW)	187	197	25.4	182	17	24	8.62
FOM $(\text{kV})^{-1}$	1880	891	1653	313	222	422	2792

6. CONCLUSION

A low-power inverter-based OTA for SC circuits has been proposed. The proposed OTA delivers a high dc gain while consuming low power even under the presence of process, voltage and temperature (PVT) variations. Post-layout simulations and Montecarlo simulations prove the robustness of the proposed OTA. The proposed OTA is area and power efficient making it suitable for portable, battery operated applications.

ACKNOWLEDGEMENTS

The authors would like to thank MeitY, Government of India, for providing the EDA tool through SMDP-VLSI project.

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Authors

Yajunath Kaliyath received his BTech degree in electronics and communication engineering from Lakireddy Bali Reddy College of Engg., Mylavaram, India (affiliated to JNTUK, Kakinada) in 2009 and MTech degree in VLSI design from NITK, Surathkal, India in 2012. Presently, he is working towards the PhD degree in the Department of Electronics and Communication Engineering at NITK, Surathkal, India. His research interests include low power analog IC design.

Corresponding author. Email: yajunath@gmail.com

Tonse Laxminidhi received his BE degree in electrical engineering from NMAM Institute of Technology, Nitte, India (affiliated to Mangalore University) in 1996; MTech degree from KREC, Surathkal, India (affiliated to Mangalore University) in 1998 and PhD degree from Indian Institute of Technology, Madras, India in 2008. He joined the Department of Electronics and Communication Engineering, NITK Surathkal as a faculty in 2000 and currently, he is an associate professor in the department. His research interests include analog and mixed signal design and power management circuits.

Email: laxminidhi_t@yahoo.com