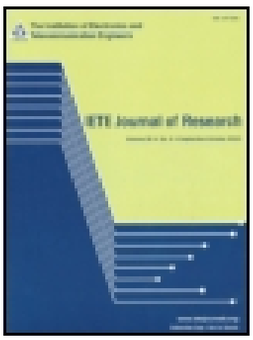

IETE Journal of Research

ISSN: 0377-2063 (Print) 0974-780X (Online) Journal homepage: https://www.tandfonline.com/loi/tijr20

A 0.8-V, 55.1-dB DR, 100 Hz Low-Pass Filter with Low-Power PTAT for Bio-Medical Applications

G. Hanumantha Rao & S. Rekha

To cite this article: G. Hanumantha Rao & S. Rekha (2019): A 0.8-V, 55.1-dB DR, 100 Hz Low-Pass Filter with Low-Power PTAT for Bio-Medical Applications, IETE Journal of Research, DOI: 10.1080/03772063.2019.1682074

To link to this article: https://doi.org/10.1080/03772063.2019.1682074

Published online: 29 Oct 2019.

IETE JOURNAL OF RESEARCH
https://doi.org/10.1080/03772063.2019.1682074

A 0.8-V, 55.1-dB DR, 100 Hz Low-Pass Filter with Low-Power PTAT for Bio-Medical Applications

G. Hanumantha Rao and S. Rekha

Department of Electronics and Communication Engineering, National Institute of Technology Karnataka, Surathkal Mangalore, 575025 Karnataka, India

ABSTRACT

This paper presents a power efficient transconductor-capacitor ($G_m - C$) filter for front-end processing of bio-medical signals. A low voltage, low-power transconductor with improved output resistance is proposed. It offers a transconductance (G_m) of 5.85 nS while operating at a supply voltage (V_{dd}) of 0.8 V. Furthermore, a low-power Proportional to Absolute Temperature (PTAT) current reference circuit is designed to bias the transconductor and to make G_m independent of temperature. It follows PTAT characteristics in the temperature range of -20°C to 70°C and is less sensitive to V_{dd} variations. A second-order Butterworth low-pass filter (LPF) with a cutoff frequency of 100 Hz is implemented to validate the proposed transconductor and the PTAT circuit. The filter is designed in UMC 65 nm CMOS process and it takes an area of 0.065 mm^2. While consuming a power of 47 nW, it offers a dynamic range (DR) of 55.1 dB. Figure-of-merit (FoM) of the filter is as low as 4.2×10^{-13} J, which is found to be on par with the filters reported in the literature.

KEYWORDS

Bulk-driven transistor; low-frequency filters; low voltage and low-power transconductor; PTAT current

1. INTRODUCTION

Low-frequency filters are one of the essential building blocks in front-end processing of biological signals. A typical biological data acquisition system [1] is shown in Figure 1, where pre-amplifier amplifies the signal to a higher level. The filter removes the noise outside the frequency band of interest. Bio-potentials such as electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) fall in the frequency range of 10 mHz to 10 kHz [2]. To process these signals in this frequency range, the cutoff frequency of the filter should be as low as the band width of these signals. Additional requirements of such filter are low voltage and low power.

Active-RC and transconductance-C ($G_m - C$) are the two main topologies to design continuous-time filters. The expressions for their cutoff frequency are $1/2\pi RC$ and $G_m/2\pi C$. In Active-RC filters, large capacitors and resistors, which occupy more silicon area, are required to get low-cutoff frequencies. Hence, active-RC filters are generally not preferred for low-frequency applications. In $G_m - C$ filters, either capacitance must be high or G_m must be low achieve low bandwidth. A large equivalent capacitance can be achieved in a small chip area by using capacitor multiplier circuits [3,4]. But these circuits introduce non-linearity and generate extra noise.

Current division and current cancelation are two important G_m reduction techniques proposed in [5]. These techniques have been used in [6–8] to implement transconductors with low G_m. However, these techniques consume more power. DC gains of the filters designed in [7,8] are −10.5 dB and −8 dB respectively due to finite output resistance of the transconductors used in their designs. Another amplifier has to be used in order to increase the gain, which in turn increases the power consumption. A transconductor with a G_m of 0.1 nS is implemented in [9] by cascading transconductance and transimpedance amplifiers. But this circuit has the drawbacks of higher power consumption and finite offset voltage. A transconductance reduction technique using input voltage attenuation is proposed in [10] and a second-order LPF of cutoff frequency in the range of 0.73–76 Hz is designed using the proposed transconductor. Although achieved dynamic range (DR) is 64 dB, the power consumption of this filter is on the higher side (0.9 μW). A 0.9 nW, 101 Hz, fourth-order LPF using flipped voltage followers (FVFs) is proposed in [11]. A 4.26 nW, 100 Hz, fourth-order filter using sub-threshold buffers is proposed in [12]. In [13], a 1.5 V, 100 Hz, fourth-order filter using sub-threshold current-reuse biquads is proposed. These filter designs [11–13] are based on source followers or voltage followers which are very simple in structure

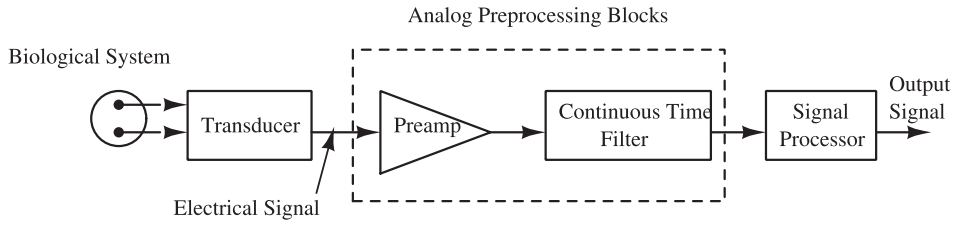

Figure 1: Typical biological data acquisition system

and hence consume less power. In [14], a second-order filter is designed using a tunable bulk-driven transconductor using 180 nm CMOS process. Even though the supply voltage used for this design is 0.5 V, the power dissipation is 248 nW.

In this paper, a low voltage, low-power transconductor with low G_m and improved output resistance is proposed. Furthermore, a low-power proportional to absolute temperature (PTAT) current reference circuit is designed to make G_m of the transconductor independent of temperature. A second-order Butterworth LPF with a cutoff frequency of 100 Hz is implemented using the proposed transconductor and PTAT current reference. Organization of the paper is as follows. Design and simulations of the proposed transconductor and PTAT current reference are discussed in Section 2. Section 3 presents the implementation of the filter and its simulation results. Section 4 concludes the paper.

2. DESIGN OF THE TRANSCONDUCTOR

In this work, bulk-driven transistors [15] operating in sub-threshold region are used to get low G_m. In bulk-driven circuits, the input signal is applied to the bulk-terminal. This lowers the threshold voltage of the transistor and hence increases the signal swing. Gate-degeneration [16] technique is also used to reduce G_m further. When the transconductor is operating in sub-threshold region, the gate and bulk transconductances (g_m and g_{mb}) are given by the following [17]:

$$g_m = \frac{I_D}{\eta V_T} \tag{1}$$

$$g_{mb} = (\eta - 1)g_m \tag{2}$$

where η is the sub-threshold slope factor. g_{mb} is typically 20–40% of the g_m [17].

Output conductance of the transconductor (g_o) should be as low as possible. If g_o is comparable to G_m, there will be a reduction in the filter DC gain as well as deviation in the cutoff frequency and quality factor of the filter. This is justified by equations given in Section 3. Cascode transistors can be used to reduce output conductance (increase the output resistance). However, these cascode transistors reduce signal swing. Composite transistor [18] shown in Figure 2 can be used to reduce output conductance without reducing signal swing. It can be treated as a single transistor (M_1) with transconductance, g_{m1} [18] and increased output resistance given as in (3) [18]

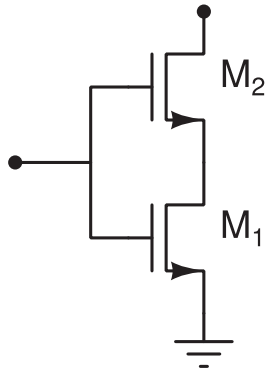

Figure 2: Composite transistor

$$r_{comp} = g_{m2}r_{o2}r_{o1} \tag{3}$$

Hence, the composite transistors can be used in the output stage of the transconductor block to reduce the output conductance without consuming extra power.

2.1 Proposed Transconductor

A fully differential proposed transconductor is shown in Figure 3. The circuit is biased by the PTAT current source (explained in Section 2.2) through transistor M_{13}. Here, gate terminals of the input transistors, M_1 and M_3 are connected to their respective drain terminals (gate degeneration). Composite transistors ($M_5 - M_6$, $M_7 - M_8$, $M_9 - M_{10}$ and $M_{11} - M_{12}$) are used in the output stage to increase the output resistance of the transconductor. Supply voltage and input common mode voltage used are 0.8 V and 0.4 V respectively. The output common mode voltage is set to 0.4 V by using a common mode feedback (CMFB) circuit shown in Figure 4. This CMFB circuit is based on the circuit given in [19], where PMOS

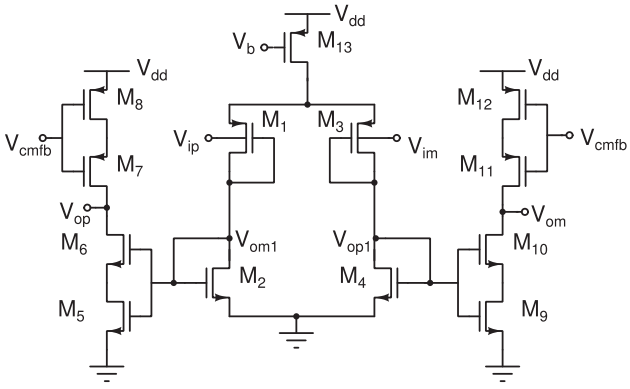

Figure 3: Proposed transconductor

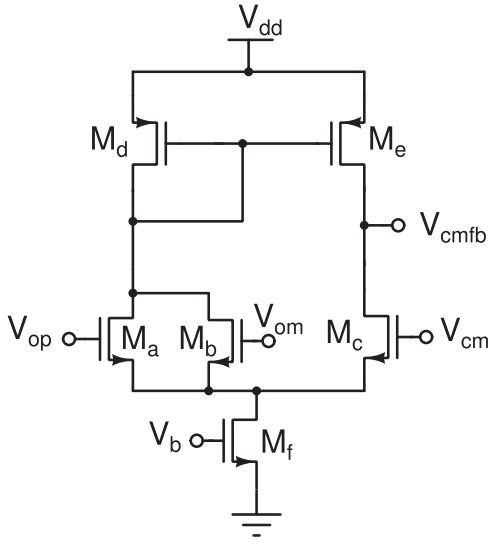

Figure 4: CMFB circuit

input transistors are used. A PTAT current of 4.5 nA, generated from the proposed PTAT current reference circuit (Section 2.2), is mirrored to the transistor, M_f. Difference of currents in the two legs of the CMFB circuit generates a voltage (V_{cmfb}) which in turn controls the currents in the transconductor thereby closing the negative feedback loop.

2.1.1 Small Signal Analysis

The small signal equivalent of left-half of the proposed transconductor is shown in Figure 5, where r_x ($= g_{m6}r_{o6}r_{o5}$) and r_y ($= g_{m7}r_{o7}r_{o8}$) are output resistances of the composite transistors $M_5 - M_6$ and $M_7 - M_8$ respectively. The effective transconductance, G_m, can be derived as

$$G_m = \frac{i_{op}}{v_{ip}} = \frac{\frac{g_{m5}}{g_{m2}}g_{mb1}}{1 + \frac{1}{g_{m2}r_{o1}} + \frac{g_{m1}}{g_{m2}}} \tag{4}$$

As $g_{m2}r_{o1} \gg 1$, $g_{m1} = g_{m2}$ (as the same current flows through M_1 and M_2, their transconductances become equal as per Equation (1)) and $g_{m2} = g_{m5}$ (as the same current is mirrored from M_2 to M_5), (4) is simplified to (5)

$$G_m \approx \frac{g_{mb1}}{2} \tag{5}$$

The expressions for the output resistance (r_{out}) and DC gain (A_V) of the transconductor are given by (6) and (7) respectively.

$$r_{out} = \frac{1}{g_o} = r_x \parallel r_y = (g_{m6}r_{o6}r_{o5}) \parallel (g_{m7}r_{o7}r_{o8}) \tag{6}$$

$$A_V = G_m r_{out} = \frac{g_{mb1}}{2}[(g_{m6}r_{o6}r_{o5}) \parallel (g_{m7}r_{o7}r_{o8})] \tag{7}$$

From (6) and (7), it can be seen that the output resistance and the DC gain of the proposed transconductor are increased by $g_m r_o$ times compared to a simple transconductor where single transistor is used in the output stage.

2.2 PTAT Current Reference Circuit

Thermal voltage, V_T ($= (kT/q)$) is directly proportional to the temperature. For a constant drain current, g_{mb} is inversely proportional to the temperature as per Equations (1) and (2). As the temperature increases, g_{mb} reduces and vice versa. This can be compensated by biasing the transconductor with a PTAT current source. With this, the current generated is directly proportional to the temperature and hence makes G_m (Equation (5)) of the transconductor independent of temperature. This makes cutoff frequency of the filter independent of the temperature as explained in Section 3.

The PTAT current reference circuit shown Figure 6(a) is based on the beta-multiplier circuit [20,21]. All the transistors are operating in sub-threshold region. Gates of M_A and M_B are connected to their drains and given as inputs to the error amplifier shown in Figure 6(b). The error amplifier output drives the gates of M_C and M_D. This makes the drain voltages of both M_A and M_B equal and hence currents through M_A and M_B are equal. This arrangement will also reduce the dependency of I_{PTAT} on V_{dd}. The expression for I_{PTAT} including the body effect of M_B is given by (8) [20,21])

$$I_{PTAT} = \frac{V_T ln(p)}{R} \tag{8}$$

where $p = (W/L)_B/(W/L)_A$.

In this design "p" is chosen as 1.5. It can be seen from (8) that the current is directly proportional to temperature

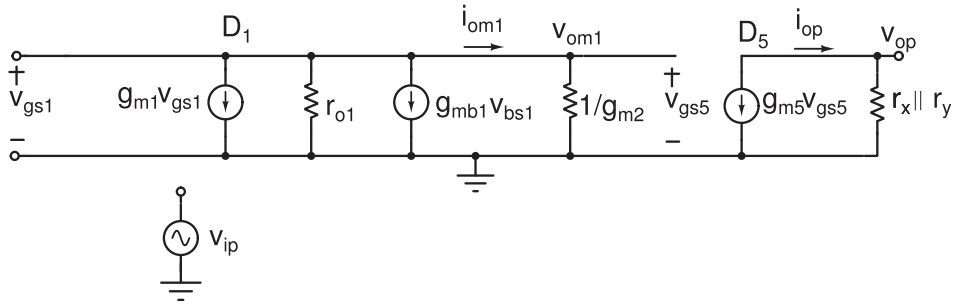

Figure 5: Small signal equivalent of the proposed transconductor (left half)

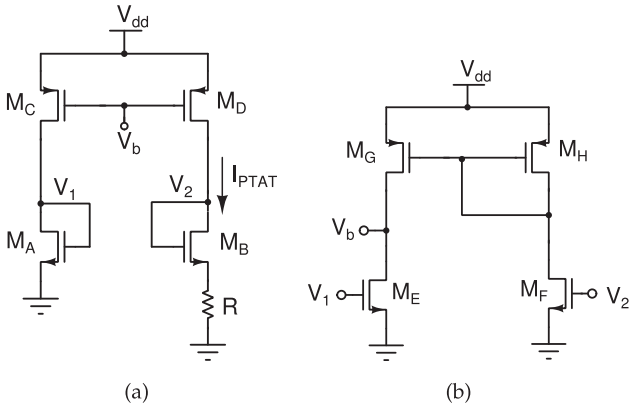

Figure 6: (a) PTAT current reference and (b) error amplifier

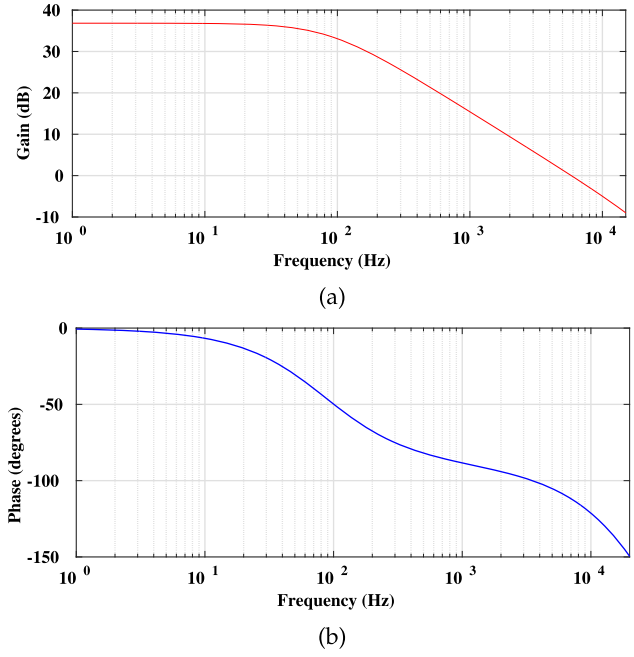

Figure 7: Magnitude and phase response of the proposed transconductor

for a fixed resistor, R. This PTAT circuit can be used to compensate for the change in G_m across the temperature variations. Transistor sizes are adjusted to generate an I_{PTAT} of 4.5 nA and this current is mirrored as the bias current to the transconductor (Figure 3) as well as to the CMFB circuit (Figure 4) through transistors M_{13} and M_f respectively.

2.3 Simulation Results

The proposed transconductor and the PTAT current reference are designed using UMC 65 nm CMOS technology and post-layout simulations are performed using Cadence Virtuoso. Figure 7(a,b) shows the magnitude and phase responses of the transconductor respectively. Transconductor offers a DC gain of 36.8 dB and the unity gain bandwidth (UGB) of 5.8 kHz under no load condition. Observed phase margin is 72°.

Table 1 presents various parameters of the proposed transconductor. It offers a G_m of 5.85 nS for an I_{PTAT} of 4.5 nA. The power consumption of the transconductor is as low as 7.2 nW.

Input/output parasitic capacitances (C_i and C_o) and conductances (g_i and g_o) of the transconductor are given in Table 2. It can be seen that g_i and g_o values are negligible compared to G_m value. g_o is reduced to 50 pS (from 3.3 nS in the case of single transistor in the output stage of the transconductor) due to composite transistors in the output stage of the transconductor. Hence, these g_i and g_o values will not reduce the DC gain of the filter as explained in Section 3.

Table 1: Transconductor parameters

Parameters	Simulated values
Technology	UMC 65 nm
V_{dd}	0.8 V
DC gain	36.8 dB
UGB	5.8 kHz
Phase margin	72°
G_m	5.85 nS
Power Consumption	7.2 nW †

†Excluding CMFB and PTAT current reference

Table 2: Input/output parasitic capacitances and conductances of the transconductor

g_i	g_o	C_i	C_o
0.01 nS	0.05 nS	0.04 pF	0.11 pF

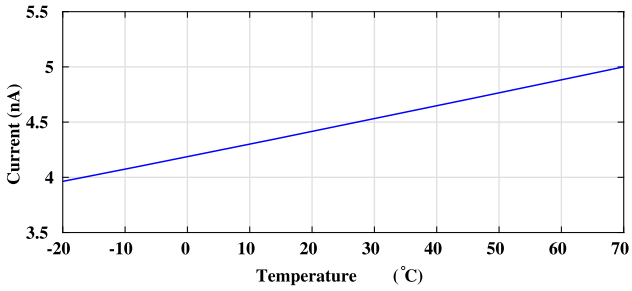

Figure 8: I_{PTAT} versus temperature

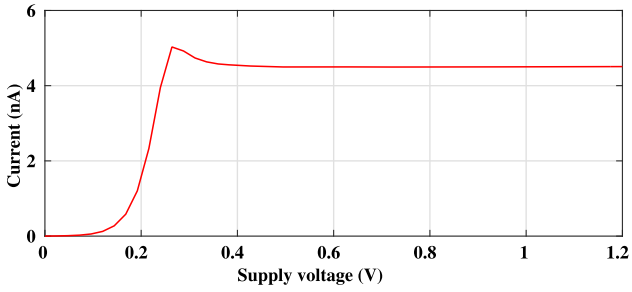

Figure 9: I_{PTAT} versus supply voltage

The designed PTAT current reference circuit offers a current of 4.5 nA at room temperature (27°C) for an off chip resistor, R = 3 MΩ. In Figure 8, I_{PTAT} is plotted against the temperature and it can be seen that the current varies linearly with temperature in the range of −20°C to 70°C. Figure 9 shows the current variation with supply voltage. It can be seen that I_{PTAT} is constant in the supply voltage range of 0.4–1.2 V. The designed PTAT circuit can be operated down to a supply voltage of 0.4 V.

2.3.1 Variation of G_m with Temperature

Figure 10 shows the G_m variation with temperature when the transconductor is biased by a constant current of 4.5 nA instead of a PTAT current source. As the temperature increases, G_m reduces almost linearly. G_m is 6.4 and 5.5 nS at −20°C and 70°C respectively. This leads to a deviation of +9.4% and −6% at −20°C and 70°C respectively.

Figure 11 shows the G_m variation with temperature when the transconductor is biased by the proposed PTAT current reference circuit. It can be seen that G_m is almost independent of temperature up to 50°C. The maximum deviation of +1.8% occurs at 70°C. This deviation is due

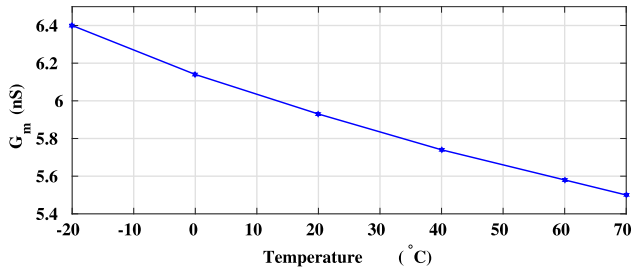

Figure 10: G_m variation when the transconductor is biased by a constant current

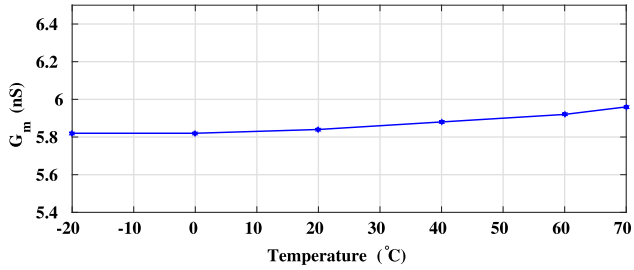

Figure 11: G_m variation when the transconductor is biased by a PTAT current

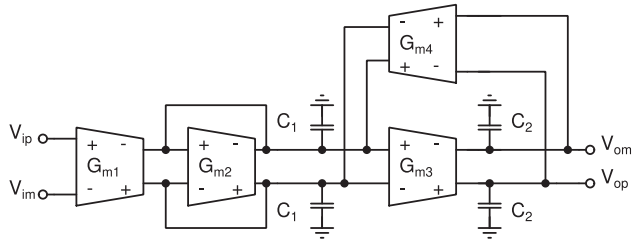

Figure 12: $G_m - C$ bi-quad filter

to the deviation of I_{PTAT} current from its PTAT characteristics. The total power consumption of the PTAT current reference circuit is 11.4 nW at room temperature.

3. FILTER REALIZATION

A second-order Butterworth LPF of cutoff frequency of 100 Hz is implemented using the proposed transconductor and PTAT current reference circuit. Figure 12 shows a standard fully differential $G_m - C$ bi-quad [22]. If the output is taken at V_{op} (or V_{om}), it gives a second-order LPF characteristics.

If the input–output parasitic capacitances and conductances of the transconductor are considered, the expressions for cutoff frequency (f_o'), DC gain (A_o') and Quality-factor (Q_o') are given by (10), (9) and (11) respectively

[14,22]

$$f_o' = \frac{1}{2\pi}\sqrt{\frac{(g_o+g_i)(G_{m2}+2g_i+3g_o)+G_{m3}G_{m4}}{C_1'C_2'}} \quad (9)$$

$$A_o' = \frac{G_{m1}G_{m3}}{(g_o+g_i)(G_{m2}+2g_i+3g_o)+G_{m3}G_{m4}} \quad (10)$$

$$Q_o' = \sqrt{C_1'C_2'}\frac{\sqrt{(g_o+g_i)(G_{m2}+2g_i+3g_o)+G_{m3}G_{m4}}}{(3g_o+2g_i)C_2'+(g_o+g_i)C_1'+G_{m2}C_2'} \quad (11)$$

where $C_1' = C_1 + 3C_o + 2C_i$ and $C_2' = C_2 + C_o + C_i$.

As g_i and g_o values (Table 2) are very small compared to G_m (5.85 nS), they can be neglected in (10), (9) and (11). C_i and C_o can be accommodated along with C_1 and C_2. The new expressions for the DC gain, cutoff frequency and quality factor, if all the transconductors have equal G_m values, are given by (12), (13) and (14) respectively

$$A_o = 1 \quad (12)$$

$$f_o = \frac{G_m}{2\pi\sqrt{C_1'C_2'}} \quad (13)$$

$$Q_o = \sqrt{\frac{C_1'}{C_2'}} \quad (14)$$

C_1 and C_2 are taken as 6 and 12.6 pF to get Butterworth response ($Q_o = 1/\sqrt{2}$). Two CMFB circuits, one for G_{m1}, G_{m2} and G_{m4} blocks and second one for G_{m3} block are used in the filter circuit.

3.1 Simulation Results & Discussion

The second-order Butterworth LPF is designed and laid out (shown in Figure 13) using UMC 65 nm CMOS technology and post-layout simulations are performed in Cadence Virtuoso. The filter takes an area of 0.065 mm^2 (278 µm × 235 µm). In the layout, MIM capacitors are used. The magnitude response of the filter for an I_{PTAT} of 4.5 nA is shown in Figure 14. DC gain and cutoff frequency are −0.14 dB and 100 Hz respectively. The roll-off rate of the filter is −40 dB/decade.

As shown in Figure 15, cutoff frequency can be linearly tuned from 10 Hz to 1 kHz by varying I_{PTAT} from 0.45 nA to 45 nA. Hence, it can be fit into the required bandwidth of different biological signals. I_{PTAT} can be varied by using the off chip resistor, R.

A sinusoidal signal of frequency 25 Hz is fed into the filter to test its linearity. Figure 16 shows the harmonics in the output of the filter. Total harmonic distortion (THD) is found to be 1% (−40 dB) for an input

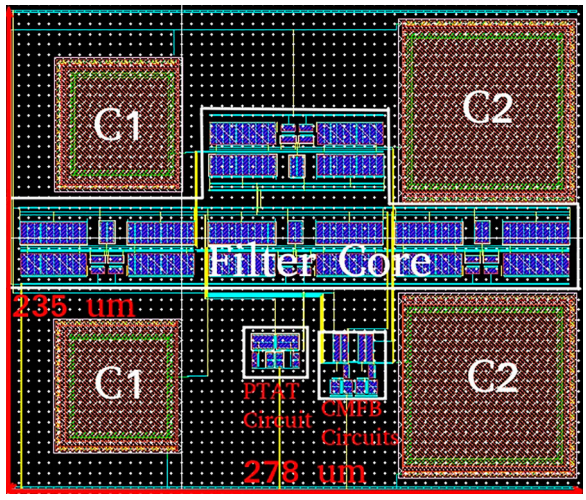

Figure 13: Layout of the filter with CMFB and PTAT circuits

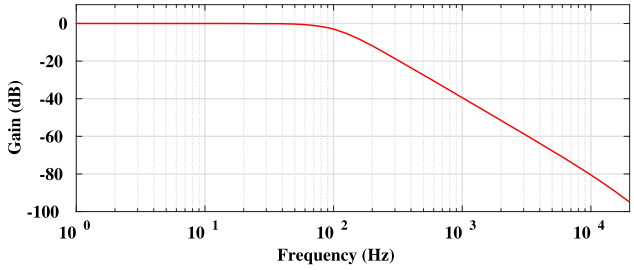

Figure 14: Magnitude response of the filter

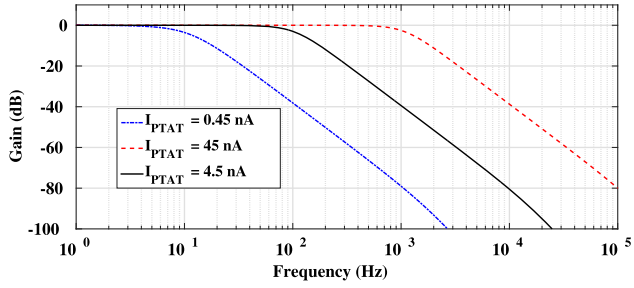

Figure 15: Cutoff frequency tuning of the filter

voltage of 580 mVpp. Third-order harmonic distortion (HD3) of −42 dB is observed for the same input voltage. Two input signals with the same amplitude and different frequencies 20 and 30 Hz are applied to the filter to check its inter modulation behavior. For an input voltage of 280 mVpp, third-order inter modulation distortion (IMD3) of 40 dBc is observed as shown in Figure 17.

Noise plot is shown in Figure 18. Input referred noise (*IRN*) integrated over the frequency range 1–100 Hz is found to be 360 µVrms. The DR is calculated as 55.1 dB.

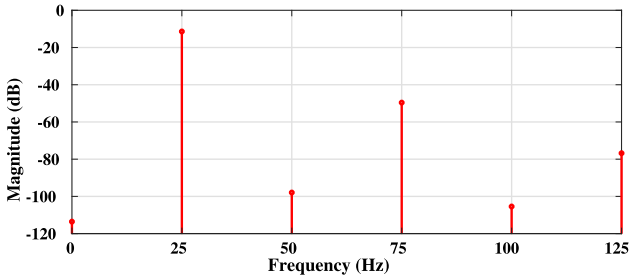

Figure 16: Harmonics of the filter

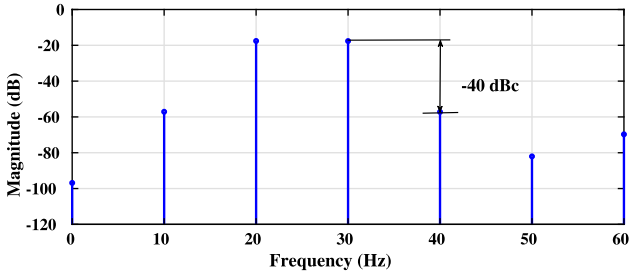

Figure 17: Inter modulation distortions of the filter

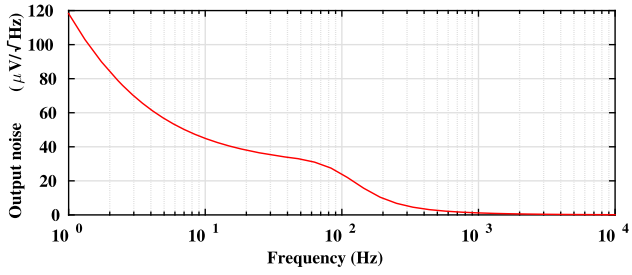

Figure 18: Noise plot of the filter

Figure-of-Merit (FoM) given in (15) [23] is used to check energy efficiency of the filters. Lower value of FoM indicates better energy efficiency

$$FoM = \frac{P}{Nf_oDR} \tag{15}$$

where P, f_o and N are power dissipation, cutoff frequency and order of the filter respectively. FoM of the proposed filter is 4.12×10^{-13} J.

The comparison of the proposed filter with other similar designs is given in Table 3. It can be seen that FoM of the proposed filter is better than the FoM of the $G_m - C$ filters in [7,8,14,24–26]. Filters in [11–13] are based on source followers or voltage followers (single branch filters). They generally consume very low power compared to $G_m - C$ filters. However, the input signal swing of the filters in [11–13] is less than the proposed filter. Even with the supply voltage of 0.8 V, the proposed filter is better in terms of input signal swing compared to all, except [24] ([24] uses a supply voltage of 3 V). The DR of the filter is better compared to all, except [13,25]. However, the design in [25] consumes more power. The DC gain of the filter is almost 0 dB, thanks to the composite transistors. The DC gain of the filters in [7,8,24,25] is less than 0 dB due to finite output resistance of the transconductors used in these designs.

IRN of the proposed filter is more compared to filters listed in Table 3. However, it is within the limit as explained below in connection with ECG signal processing. The limit on *IRN* is calculated by using (16) [7]

$$IRN_{\max} = \frac{V_{in,rms}}{10^{SNR(dB)/20}} \tag{16}$$

The maximum and minimum signal levels of ECG are 4 mV and 100 μV [2] respectively. For ECG signal the SNR must be more than 38 dB [7]. For the proposed design, $V_{in,rms}$ is 205 mVrms ($580/2\sqrt{2}$). By using (16), $IRN_{\max}$ for the proposed filter is calculated as 2580 μVrms. But *IRN* of the proposed filter is only 360 μVrms which is very much below IRN_{max} (2580 μVrms).

Table 3: Comparison of the proposed work with other designs from the literature

Parameter	[7]* (2009)	[24]† (2012)	[25]† (2013)	[26]‡ (2016)	[14]‡ (2018)	[8]* (2018)	[11]* (2018)	[12]* (2018)	[13]* (2019)	This work†
Technology (nm)	180	350	250	130	180	180	350	350	350	65
V_{dd} (V)	1	3	±0.8	0.9	0.5	1	0.6	0.9	1.5	0.8
Filter order	5	4	5	2	2	5	4	4	4	2
DC gain (dB)	−10.5	≈ −7	≈ −4	5.99	≈0	−8	−2.77	−0.05	−0.09	−0.14
Cutoff frequency (Hz)	250	40	243	48	456	50	101	100	100	100
Power (nW)	453	750	3×10^4	800	248	350	0.9	4.26	5.25	47
V_{inpp} for 1% THD (mV)	100	735	100	7	180	86	130	70	110	580
IRN (μVrms)	≈300**	500	36	17.38**	160**	97	46.27††	80.5††	39.38††	360**
DR (dB)	50	54	65	43.8	52	49.9	47	48.2	56.9	55.1
Active area (mm^2)	0.13	–	0.09	–	–	0.12	0.168	0.11	0.1	0.065
FoM (J) ($\times 10^{-13}$)	11.5	93.5	138	538	6.83	44.8	0.1	0.4	0.19	4.12

*measured, †post-layout simulation, ‡schematic simulation, **integrated over 1 – f_o, ††integrated over 1 – $2f_o$.

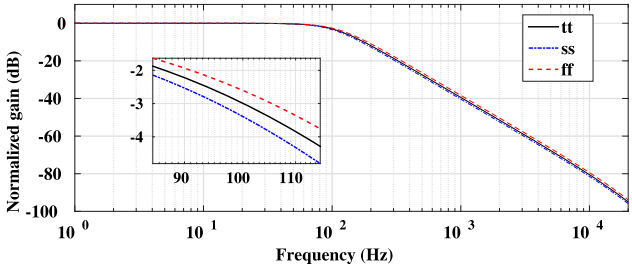

Figure 19: Frequency response for different process corners showing worst case deviation

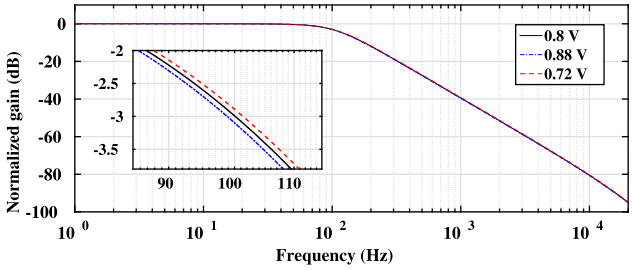

Figure 20: Frequency response for different supply voltages

Considering IRN_{max} limit of 2580 µVrms and IRN of 360 µVrms of the proposed design, output referred noise of the pre-amplifier circuit should not exceed 2220 µVrms (2580 µVrms – 360 µVrms). The gain of the pre-amplifier should be sufficiently large in order to amplify the minimum ECG signal (100 µV) above the noise level at the input of the filter. This will give us the minimum gain of the pre-amplifier ($Gain_{\min}$). As per (17), $Gain_{\min}$ is calculated to be 36.5 in the present case. For this gain, IRN of the pre-amplifier is calculated as 61 µVrms (2220 µVrms/36.5).

$$Gain_{\min} = \frac{\text{IRN}_{\max}}{\text{RMS of minimum ECG signal}} \tag{17}$$

The maximum gain of the pre-amplifier ($Gain_{\max}$) is decided by the maximum input signal of the filter. From (18), $Gain_{\max}$ is calculated to be 72.5. For this gain, IRN of the pre-amplifier is calculated as 30.6 µVrms (2220 µVrms/72.5).

$$Gain_{\max} = \frac{V_{\text{in, max}}}{\text{RMS of maximum ECG signal}} \tag{18}$$

The above-described analysis can be applied for the processing of EEG and EMG signals also.

The proposed circuit offers wide input linear range, thanks to the bulk driven structure. However, due to the lower transconductance of input transistors, IRN is at the higher side. But this value is well within the limits as explained above.

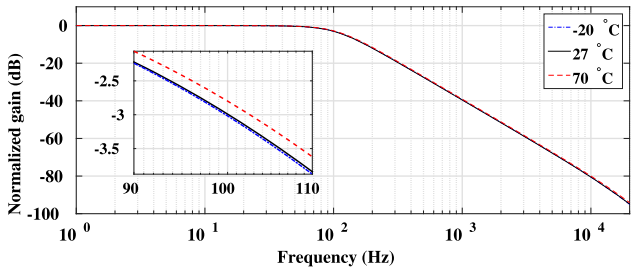

Figure 21: Frequency response for different temperatures

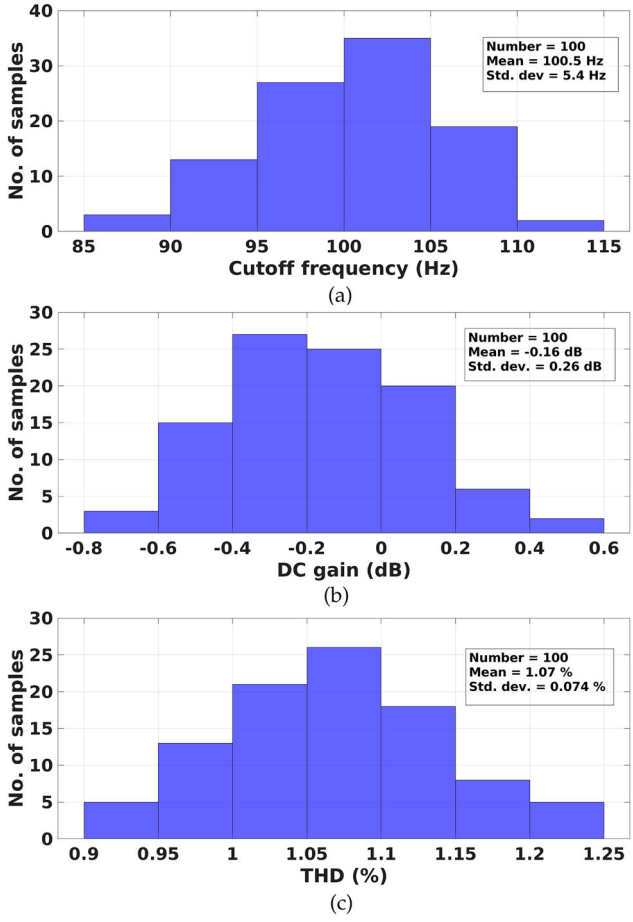

Figure 22: Monte Carlo simulations of (a) cutoff frequency, (b) DC gain and (c) THD

3.1.1 Effect of PVT Variations on Cutoff Frequency

The frequency response of the filter across the process corners is shown in Figure 19. Gain is normalized to 0 dB to compare the results. Cutoff frequency is 96 Hz and 105 Hz in "ss" and "ff" corners respectively. Worst case deviation occurs in "ss" and "ff" corners. Hence, the deviation in cutoff frequency is $< 5\%$. For a $\pm$ 10% variations in V_{dd}, cutoff frequency variation is only $\pm$ 1% as shown in Figure 20. The frequency response of the filter for different temperatures is shown in Figure 21. Cutoff frequency is 99.8 Hz and 102 Hz at −20°C and

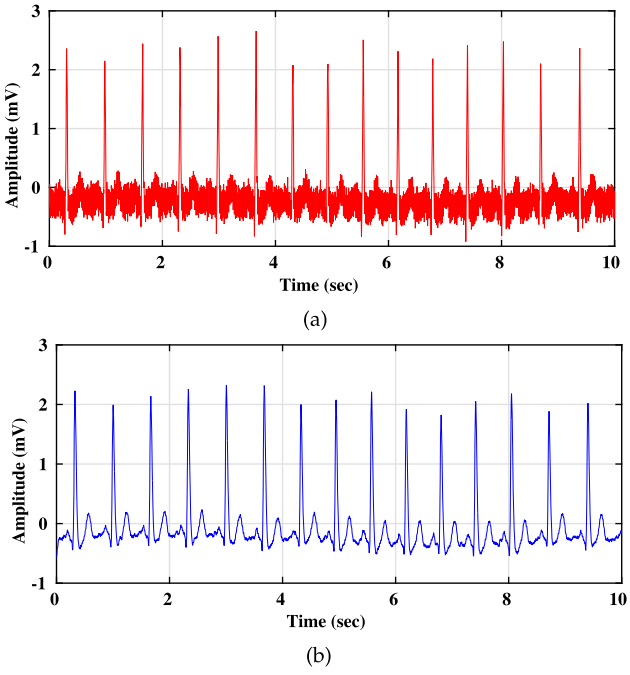

Figure 23: ECG signal (a) before filtering and (b) after filtering

70°C respectively. The deviation of 2 Hz at 70°C is due to the deviation of PTAT current from its actual value. These results show the robustness of the design across PVT variations.

To check the deviation in filter parameters (cutoff frequency, DC gain and THD) across transistor process and mismatch variations, Monte Carlo simulations are performed for 100 runs. As shown in Figure 22(a), the mean and standard deviation of cutoff frequency are 100.5 and 5.4 Hz respectively. The mean value of DC gain is −0.16 dB with 0.26 dB standard deviation as shown in Figure 22(b). Figure 22(c) shows the Monte Carlo simulations of THD when the 580 mVpp and 25 Hz sinusoidal input signal is applied to the proposed filter. The mean value of THD is 1.07% with 0.074% standard deviation.

3.1.2 ECG Signal Testing

To demonstrate the functionality of the proposed LPF, an unfiltered ECG signal obtained from [27] is applied. Figure 23(a,b) show a sample of unfiltered ECG and corresponding filtered output respectively. This portrays a successful ECG detection.

4. CONCLUSION

A low voltage, low-power transconductor is proposed and a low-power PTAT current reference circuit is designed to bias the proposed transconductor. G_m variation with temperature is reduced by biasing the transconductor with PTAT current. A second-order Butterworth LPF with a cutoff frequency of 100 Hz is implemented using the proposed transconductor and the PTAT current reference circuit. The filter operates with a supply voltage of 0.8 V and consumes a power of 47 nW. The DR and FoM are 55.1 dB and 4.12×10^{-13} J respectively. The proposed filter can be a strong candidate in the front-end processing of bio-medical signals where power is the main constraint.

ACKNOWLEDGMENTS

The EDA tools used for this work are supported under SMDP project funded by MeitY, Government of India.

DISCLOSURE STATEMENT

No potential conflict of interest was reported by the authors.

ORCID

G. Hanumantha Rao http://orcid.org/0000-0003-4453-2722

REFERENCES

1. S. Solís-Bustos, J. Silva-Martínez, F. Maloberti, and E. Sánchez-Sinencio, "A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter for medical applications," *IEEE Trans. Circuits Syst. II: Analog Digital Signal Process.*, Vol. 47, no. 12, pp. 1391–1398, Dec. 2000. doi:10.1109/82.899631

2. J. Webster, *Medical Instrumentation: Application and Design*. Hoboken: John Wiley & Sons, 2009.

3. C.-H. Chen, et al., "A 2.4 Hz-to-10 kHz-tunable biopotential filter using a novel capacitor multiplier," in *Proceedings of PrimeAsia, Shanghai*. IEEE, 2009, pp. 372–375.

4. M. A. Al-Absi, E. S. Al-Suhaibani, and M. T. Abuelmaatti, "A new compact CMOS C-multiplier," *Analog Integr. Circuits Signal Process.*, Vol. 90, no. 3, pp. 653–658, 2017. doi:10.1007/s10470-016-0822-1

5. J. Silva-Martinez and J. Salcedo-Suñer, "IC voltage to current transducers with very small transconductance," *Analog Integr. Circuits Signal Process.*, Vol. 13, no. 3, pp. 285–293, 1997. doi:10.1023/A:1008286718560

6. A. Veeravalli, E. Sánchez-Sinencio, and J. Silva-Martínez, "Transconductance amplifier structures with very small transconductances: A comparative design approach," *IEEE J. Solid-State Circuits*, Vol. 37, no. 6, pp. 770–775, June 2002. doi:10.1109/JSSC.2002.1004582

7. S.-Y. Lee and C.-J. Cheng, "Systematic design and modeling of a OTA-C filter for portable ECG detection," *IEEE Trans.*

Biomed. Circuits Syst., Vol. 3, no. 1, pp. 53–64, Feb. 2009. doi:10.1109/TBCAS.2008.2007423

8. C.-Y. Sun and S.-Y. Lee, "A fifth-order Butterworth OTA-C LPF with multiple-output differential-input OTA for ECG applications," *IEEE Trans. Circuits Syst. II: Express Briefs*, Vol. 65, no. 4, pp. 421–425, Apr. 2018. doi:10.1109/TCSII.2017.2695366

9. R. Rieger, A. Demosthenous, and J. Taylor, "A 230-nW 10-s time constant CMOS integrator for an adaptive nerve signal amplifier," *IEEE J. Solid-State Circuits*, Vol. 39, no. 11, pp. 1968–1975, Nov. 2004. doi:10.1109/JSSC.2004.835818

10. C. Sawigun and W. A. Serdijn, "A modular transconductance reduction technique for very low-frequency Gm-C filters," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Seoul, May 2012, pp. 1183–1186.

11. C. Sawigun and S. Thanapitak, "A 0.9-nW, 101-Hz, and 46.3-μVrms IRN low-pass filter for ECG acquisition using FVF biquads," *IEEE Trans. Very Large Scale Int. Syst.*, Vol. 26, no. 11, pp. 2290–2298, Nov. 2018. doi:10.1109/TVLSI.2018.2863706

12. S. Thanapitak and C. Sawigun, "A subthreshold buffer-based biquadratic cell and its application to biopotential filter design," *IEEE Trans. Circuits Syst. I: Reg. Pap.*, Vol. 65, no. 9, pp. 2774–2783, Sept. 2018. doi:10.1109/TCSI.8919

13. C. Sawigun and S. Thanapitak, "A nanopower biopotential lowpass filter using subthreshold current-reuse biquads with bulk effect self-neutralization," *IEEE Trans. Circuits Syst. I: Reg. Pap.*, Vol. 66, no. 5, pp. 1746–1757, May 2019. doi:10.1109/TCSI.8919

14. G. H. Rao and S. Rekha, "Low voltage, low power Gm-C filter for low frequency applications," *J. Low Power Electron.*, Vol. 14, no. 2, pp. 266–274, June 2018. doi:10.1166/jolpe.2018.1558

15. A. Guzinski, M. Bialko, and J. Matheau, "Body driven differential amplifier for application in continuous-time active-C filter," *Proc. ECCD*, Vol. 87, pp. 315–319, 1987.

16. R. Sarpeshkar, R. F. Lyon, and C. Mead, "A low-power wide-linear-range transconductance amplifier," *Analog Integr. Circuits Signal Process.*, Vol. 13, no. 1–2, pp. 123–151, 1997. doi:10.1023/A:1008292213687

17. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge university press, 2013.

18. L. H. Ferreira, T. C. Pimenta, and R. L. Moreno, "An ultra-low-voltage ultra-low-power weak inversion composite MOS transistor: Concept and applications," *IEICE Trans. Electron.*, Vol. 91, no. 4, pp. 662–665, Jan. 2008. doi:10.1093/ietele/e91-c.4.662

19. S. Rekha and T. Laxminidhi, "Common mode feedback circuits for low voltage fully-differential amplifiers," *J. Circuits Syst. Comput.*, Vol. 25, no. 10, pp. 1650124, 2016. (12 pages). doi:10.1142/S0218126616501243

20. B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: Tata McGraw-Hill, 2002.

21. R. J. Baker and C. Boyce, "Circuit design, layout, and simulation," in *IEEE Press Series on Microelectronic Systems*, 2005.

22. R. Schaumann, H. Xiao, and V. V. Mac, *Design of Analog Filters*, 2nd ed. New York: Oxford University Press, Inc., 2009.

23. T.-T. Zhang, et al., "15-nW biopotential LPFs in 0.35 μm CMOS using subthreshold-source-follower biquads with and without gain compensation," *IEEE Trans. Biomed. Circuits Syst.*, Vol. 7, no. 5, pp. 690–702, Oct. 2013. doi:10.1109/TBCAS.2013.2238233

24. Y.-T. Liu, D. Y. Lie, W. Hu, and T. Nguyen, "An ultralow-power CMOS transconductor design with wide input linear range for biomedical applications," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, May 2012, pp. 2211–2214.

25. S. A. Mahmoud, A. Bamakhramah, and S. A. Al-Tunaiji, "Low-noise low-pass filter for ECG portable detection systems with digitally programmable range," *Circuits Syst. Signal Process.*, Vol. 32, no. 5, pp. 2029–2045, Oct. 2013. doi:10.1007/s00034-013-9564-9

26. R. Arya and J. P. Oliveira, "Gm-C biquad filter for low signal sensor applications," in *Proceedings of 23rd IEEE International Conference on Mixed Design of Integrated Circuits and Systems*, Lodz, June 2016, pp. 207–210.

27. A. L. Goldberger, et al., "PhysioBank, physioToolkit, and physioNet: Components of a new research resource for complex physiologic signals," *Circulation*, Vol. 101, no. 23, pp. e215–e220, 2000. (June 13), circulation Electronic Pages: Available: http://circ.ahajournals.org/content/101/23/e215.full PMID:1085218; doi:10.1161/01.CIR.101.23.e215.

Authors

G. Hanumantha Rao was born in Guntur, India. He received B.Tech. degree in Electronics & Communication from KL College of Engineering, India and M.Tech. in VLSI Systems from NIT Trichy, India. Since 2015, he is pursuing his Ph.D. in National Institute of Technology Karnataka, Surathkal, India. His research interests include low voltage, low-frequency continuous-time filters.

Corresponding author. Email: hanu.vnk@gmail.com

S. Rekha was born in Puttur, India. She received the B.E. degree in Instrumentation Technology from SJCE Mysore, India and M.Tech. in Industrial Electronics from NITK (KREC) Surathkal, India. She obtained her Ph.D. degree from the Department of Electronics & Communication Engineering, NITK Surathkal, India. Since 2007 she has been an Assistant Professor with the National Institute of Technology Karnataka, Surathkal, India. Her research interests include analog and digital VLSI design.

Email: rsbhat 99@yahoo.com