Moment based Delay Modelling for On-Chip RC Global VLSI Interconnect for Unit Ramp Input

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***Abstract*— The Elmore delay has been the metric of choice for the performance driven design applications. But the accuracy of the Elmore delay is insufficient. This paper presents an accurate and efficient model to compute the delay metric of on-chip high speed VLSI interconnects for ramp inputs. The proposed delay metric is based on the distributed RC interconnect model. For optimization like physical synthesis and static timing analysis, efficient interconnect delay computation is critical. In this paper, a delay metric using RC-out has been formulated which computes the delay at the output node. The proposed model is based on the first three moments of the impulse response. Two pole RC model is developed based on the first, second and third moments' effect onto the delay calculation for interconnect lines. This two pole approach permits the pre-characterization of the interconnect delay. The empirical D3M metric is shown to be a typical case. The proposed metric also provides an expression for impulse response. The SPICE simulation results justify the accuracy and efficacy of the proposed model.**

Keywords- Delay Modelling, On-Chip Interconnect, RC Segments, Ramp Input, VLSI

I. INTRODUCTION

Interconnects constitute a dominant source of circuit delay for modern chip designs. As the CMOS technology scales further, on-chip interconnects with lower width-to-height aspect ratio are dominating the physical design. Due to the ever-increasing speed and complexity of very-large-scale integration (VLSI) circuits, the modelling and simulation of VLSI macro models such as interconnects, require high accuracy and efficiency. As CMOS technologies shift towards deep sub-micron (DSM) technologies, interconnect networks are becoming increasingly dominant in terms of total path delay [1]. The model order reduction techniques [2] compute the dominant poles and the corresponding residues by matching the moments of the circuit impulse response. The response of the interconnect network is then represented as the sum of exponential functions. The Elmore delay [3] approximation is the most widely used delay model in the performance driven design of RC interconnect. However, Elmore delay can not accurately estimate the delay for RC interconnects lines [4]. The Elmore constant, or first moment of the impulse response [3], has been for a long time the de-facto standard delay metric for interconnect for performance driven design optimization. The mean value of delay is taken as an approximation to the time at which the output voltage of the interconnect v(t), for a ramp input, reaches 50% of its final value.

$$\tau_D = \int_0^\infty t v'(t) dt \tag{1}$$

Since interconnect resistance is higher, its shielding effect [5] is more important. Elmore delay, neglecting the resistance shielding, does not capture the correct sensitivity, which is very crucial. This can lead to unacceptably large errors due to the fact that it tends to neglect the screening of the downstream capacitance of the interconnect by its resistance [6-7].

Interconnect delay computation is critical tasks which may be executed millions of time during floor planning, placement and routing [8]. A number of new interconnect delay metrics are proposed recently. Most of these are based on the assumption that matching the first three moment of the impulse response [8] result in a circuit that can describe accurately the electrical behaviour of the linear RC circuit which models the interconnects. In [9], the authors have proposed an explicit RC circuit delay model using the first three moments. In [10], the delay metric is based on comparing the impulse response to the gamma distribution. In [11], the gamma distribution is selected to model the normalized homogenous portion of the step response. While the Elmore delay is provably an upper bound for the 50% delay of large class of RC tree response. The tightness of the bound varies significantly from one node to create higher order (2-pole) moment matching models from which the delay can be approximated explicitly [10]. The result is a delay metric in terms of the first three moment of the impulse response which provides accuracy similar to two pole models. These metrics are more accurate, thereby, prohibiting the use of higher order Krylov space methods [12]. AWE [13] is proposed with partial pade capability that produces provably stable two-pole models using the moments at the driven point and load end. In [14], a closed form expression for delay using first three circuit moments of the impulse response has been presented based on double pole approximation. In current mode signalling technique [15], an equivalent lumped element model can predict the step response of an interconnect line for both current and voltage mode signalling. The mean of an RC circuit can be calculated in a recursive way, and the resulting equivalent Elmore delay is in a simple closed form. Alpert *et*

al. [6] proposed two RC delay metrics which is virtually simple and fast as the Elmore metric.

This paper is organized as follows: Section II discusses the proposed delay model for on-chip interconnects line. Section III presents and discusses the simulation results. Finally section IV concludes the paper.

II. PROPOSED DELAY MODEL

Let us consider the RC circuit as shown in Figure 1, which is a two stage RC model for estimation of the output response in an interconnect line.

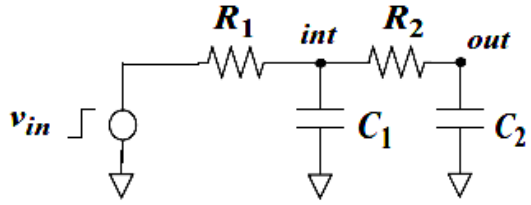

Figure 1. The RC Circuit.

Kirchoff's Voltage Law is applied in loop 1 and loop 2, respectively.

For loop 1,

$$v_{in} - i_1 r_1 - \frac{(i_1 - i_2)}{c_1 s} = 0$$

$$\text{or, } v_{in} = i_1\left(r_1 + \frac{1}{c_1 s}\right) - \frac{i_2}{s c_1} \tag{2}$$

For loop 2,

$$\frac{i_1}{s c_1} - i_2\left[\frac{r_1 c_1 c_2 s + c_1 + c_2}{c_1 c_2 s}\right] = 0 \tag{3}$$

$$\text{and } v_0 = \frac{i_2}{s c_2} \tag{4}$$

Solving (2), (3) and (4) yields,

$$i_2 = \frac{v_{in} s c_2}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1} \tag{5}$$

Using (5) in (4) results in (6).

$$\frac{v_0}{v_{in}} = \frac{1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1} \tag{6}$$

Let h(t) is the time domain impulse response of the RC circuit. The corresponding transfer function $h(s)$ is expressed in term of RC interconnects' parameters.

$$h(s) = \frac{1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1} \tag{7}$$

Consider a transfer function h(s) of the RC circuit, and assume that a sufficient number of its moment is calculated form the circuit [8].

$$h(s) = \frac{1}{1 + a_1 s + a_2 s^2} = 1 + m_1 s + m_2 s^2 \tag{8}$$

The first three moments of the transfer function can be expressed in term of resistance and capacitances.

$$m_1 = -[r_1 c_1 + (r_1 + r_2) c_2] \tag{9}$$

$$m_2 = -[r_1 r_2 c_1 c_2 - [r_1 c_1 + (r_1 + r_2) c_2]^2] \tag{10}$$

$$m_3 = [r_1 c_1 + (r_1 + r_2) c_2]\,[2 r_1 c_1 r_2 c_2 - (r_1 c_1 + (r_1 + r_2) c_2)^2] \tag{11}$$

The transfer function of the circuit can be expressed in term of its moment [13].

$$h(s) = \frac{1}{\left[m_2 - \frac{m_3}{m_1}\right] s^2 - m_1 s + 1} \tag{12}$$

Hence, its poles, in the form of first three moments, are sufficient to describe the transfer function. The stable two poles (S2P) approximation consist for transfer function h(s) and finding the poles form the driving point moments [8], hence its poles are:

$$p_{1,2} = \frac{m_1 \pm \sqrt{m_1^2 - 4\left[m_2 - \left(\frac{m_3}{m_1}\right)\right]}}{2\left[m_2 - \left(\frac{m_3}{m_1}\right)\right]} \tag{13}$$

In the following discussions, two extreme cases are discussed regarding relationships between two poles, i.e., dominant and coincident poles.

From (8) we have,

$$H(s) = \frac{1}{1 + a_1 s + a_2 s^2}$$

Thus the output for infinite unit ramp input will be given as

$$V_{out}(s) = \frac{1}{T_R} \cdot \frac{1}{s^2} \cdot \frac{1}{1 + a_1 s + a_2 s^2} \tag{14}$$

or,

$$V_{out}(s) = \frac{1}{T_R} \cdot \frac{1}{s^2}\left[\frac{k_1}{s - p_1} + \frac{k_2}{s - p_2}\right] \tag{15}$$

A. *Case 1. For dominant pole(i.e., $p_1 >> p_2$)*

Thus, neglecting the second term in equation (15), we get

$$V_{out}(s) = \frac{1}{T_R} \cdot \frac{1}{s^2}\left[\frac{k_1}{s - p_1}\right] \tag{16}$$

$$\text{or, } V_{out}(s) = \frac{1}{T_R}\left[\frac{A}{s} + \frac{B}{s^2} + \frac{c}{s - p_1}\right] \tag{17}$$

Solving for A, B and C from equation (16) we get

$$A = -\frac{k_1}{p_1^2};\ B = -\frac{k_1}{p_1};\ C = \frac{k_1}{p_1^2}$$

Thus the time domain analysis of the Vout will be

$$V_{out}(t)=\frac{1}{T_R}\left(-\frac{k_1}{p_1^2}-\frac{k_1}{p_1}t+\frac{k_1}{p_1^2}e^{p_1 t}\right) \quad (18)$$

Now determining the delay for 50% threshold voltage we get,

$$0.5=\frac{1}{T_R}\left(-\frac{k_1}{p_1^2}-\frac{k_1}{p_1}t+\frac{k_1}{p_1^2}e^{p_1 t}\right) \quad (19)$$

Solving for t_D from equation (19) by expanding the exponential up to three terms we get,

$$t_D=\sqrt{\frac{T_R}{k_1}} \quad (20)$$

where the value of k1 is given by[3]

$$k_1=\frac{1-m_1 p_2}{p_1-p_2}p_1^2 \quad (21)$$

putting the values of p_1 and p_2 from equation (13) into equation (12), we get

$$k_1=\frac{1}{\sqrt{m_1^2-\left(m_2-\frac{m_2}{m_1}\right)}} \quad (22)$$

now putting the value of k_1 from (22) into (20) we get

$$t_D=\frac{\sqrt{T_R}}{\sqrt[4]{m_1^2-\left(m_2-\frac{m_2}{m_1}\right)}} \quad (23)$$

B. Case 2. Coincident poles

In this condition both poles are equal i.e., $P_1=P_2$. This occurs when the discriminator in (13) is zero. Therefore, from (13) we have,

$$m_1=4\left[m_2-\left[\frac{m_3}{m_1}\right]\right] \quad (24)$$

Hence the double pole p of the transfer function can be expressed in term of first three moments as,

$$p=4\left(\frac{\sqrt{m_2-\frac{m_3}{m_1}}}{m_1^2}\right) \quad (25)$$

So, the transfer function of the RC circuit for step response at node out is

$$\frac{v_{out}}{v_{in}}=\frac{1}{r_1r_2c_1c_2s^2+[r_1c_1+(r_1+r_2)c_2]s+1}=\frac{1}{((s-p)^2)}$$

In the case of ramp input, the output will be

$$V_{out}(s)=\frac{1}{T_R}\frac{1}{s^2(s-p)^2}$$

or, $$V_{out}(s)=\frac{1}{T_R}\left[\frac{k_1}{s}+\frac{k_2}{s^2}+\frac{k_3}{s-p}+\frac{k_4}{(s-p)^2}\right] \quad (26)$$

Now solving for values of k_1,k_2, k_3 and k_4 from (26), we get

$$k_1=\frac{2}{p^3}, \qquad k_2=\frac{1}{p^2}$$

$$k_3=\frac{-2}{p^3}, \qquad k_4=\frac{1}{p^2}$$

Thus the time domain equation for V_{out} will be

$$V_{out}(t)=\frac{1}{T_R}\left[\frac{2}{p^3}+\frac{1}{p^2}t-\frac{2}{p^3}e^{pt}+\frac{1}{p^2}te^{pt}\right] \quad (27)$$

Now the delay t_D for 50% response will be

$$0.5=\frac{1}{T_R}\left[\frac{2}{p^3}+\frac{1}{p^2}t_D-\frac{2}{p^3}e^{pt_D}+\frac{1}{p^2}t_De^{pt_D}\right] \quad (28)$$

Now solving equation (28) for t_D, we get

$$t_D\approx\sqrt[3]{\frac{T_R}{p}} \quad (29)$$

Putting value of p from equation (25) into (29)
We get,

$$t_D=\left(\frac{T_Rm_1^2}{4\left(\sqrt{m_2-\frac{m_3}{m_1}}\right)}\right)^{1/3} \quad (30)$$

Equation (23) and (30) present the required expression for 50% delay for the output node. From the both equations, it is found that D3M is more accurate in predicting the 50% delays to the output of RC interconnect.

III. Simulation Results and Discussions

The accuracy of our model (23) an (30) d is established using the circuit illustrated in figure 1. The 50% delay at output node of the circuit is computed using (23) and (30). These delay values are compared with HSPICE and Elmore equivalent simulation for different value of C. In figure 2 the output voltage at output node is plotted as dotted curve when the RC model is simulated with the circuit simulator SPICE and a ramp input voltage is applied to input node. It can also be analysed that delay values are higher at out node for ramp input comparable to step input at output node on the interconnect line. These curves are obtained for the ramp input.

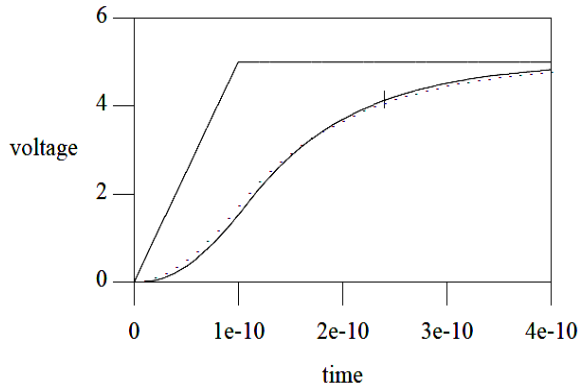

Figure 2. Output voltage waveform when ramp signal is applied at input node.

TABLE I. COMPARISON BETWEEN ELMORE , PROPOSED DELAY AND SPICE RESULT FOR THE DOMINANT POLE

C (pF)	SPICE 50 % Delay (ns)	Equivalent Elmore model (ns)	Proposed model (ns)
125	32	31	34
175	44	40	44
225	61	67	59
275	69	68	71
300	73	71	72
350	81	83	82
400	93	95	98
450	112	109	119
500	132	123	145

The comparative result of the proposed models for output node with SPICE delay and Elmore delay for the different values of C is illustrated in the TABLE I-II. From the table we can analyze that the possible errors in the value of delay obtained in both cases with that of SPICE value is less than 10%

TABLE II. COMPARISON BETWEEN ELMORE, PROPOSED DELAY AND SPICE RESULT FOR COINCIDENT POLE

C (pF)	SPICE 50 % Delay (ns)	Equivalent Elmore model (ns)	Proposed model (ns)
125	73	75	74
175	87	84	90
225	92	97	95
275	108	106	110
300	123	127	122
350	142	158	148
400	161	165	169
450	182	169	192
500	201	212	211

IV. CONCLUSIONS

In this work, an accurate delay metric for resistive interconnect is presented, that computes the delay along the interconnect. It is based on the first three moments of the impulse response. Two pole RC model is developed based on first, second and third moment effect into the delay estimate for interconnect lines. Proposed model is applicable to any type of interconnect as this approach is not based on the analogy of the impulse response to a particular Probability Distribution Function (PDF). Verification with measurement data from various industrial nets demonstrates the validity of this model. Since all elements are frequency independent, it is fully compatible with transient analysis and wide-band design.

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