Estimation of Interconnect Metrics using State Space Approach

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Abstract—In this paper, we propose models for single and coupled on-chip global interconnect lines by distributed RLGC parameters using state space approach. Models for single and coupled lines are validated by comparing with SPICE simulations. Interconnect performance metrics are obtained from the proposed models for 65 nm, 90 nm, 130 nm and 180 nm technology nodes based on PTM values. In case of coupled interconnect lines, the effect of mutual inductance and coupling capacitance is considered in addition to the distributed *RLGC* parameters. The proposed models are generic in nature and illustrated by applying our modeling approach to four coupled interconnect lines.

I. INTRODUCTION

The downscaling of Complementary Metal Oxide Semiconductor (CMOS) technology into nanometer dimensions and multi Giga Hertz (GHz) regime has made on-chip interconnects play an important role in determining the performance of the integrated circuits. International Technology Roadmap for Semiconductors (ITRS) [1] 2007 report predicts that by 2013, high performance integrated circuits will have more than three billions of transistors per chip, 12 metal layers, total interconnect length increases to 4000 m/cm^2 and switching speed in the range of tens of pico seconds or even less than that. Growing complexity and the stringent design requirements in today's Deep Sub-Micron (DSM) systems have made the necessity of accurate understanding and modeling of the intermediate and global interconnect lines critical than ever.

Previously, global interconnect lines were modeled as just a single lumped capacitance and the small resistive component was neglected for wider interconnect geometries [2]. With the continuous scaling of technology, the cross sectional area of the interconnect lines has decreased and the length increased due to increase in the chip area resulting in a significant increase in wire resistance. These effects are modeled as lumped *RC* circuit and later as distributed *RC* circuit [3] when the signals are transmitted at high (nearing GHz) frequencies. Sakuri has derived expressions to find interconnect delay for the distributed RC network based on boundary conditions [3].

As the Very Large Scale Integrated (VLSI) circuit design reaches DSM regime, interconnect delay dominates gate delay [4] and the inductance of the interconnect line starts to dominate the delay behavior [5]. Several types of delay estimation models are proposed by considering interconnects as distributed *rlc* elements ([6]- [9]). Interconnect delay

estimation is improved in [10] by incorporating transport delay with ABCD matrix.

In all these papers, interconnect lines are modeled by *rlc* sections and transfer functions are obtained by approximating to the lower order. The expressions for the time delay calculation is derived from the reduced transfer functions. When global interconnect lines with large lengths are considered, higher order transfer functions are required to have better accuracy in the interconnect metrics calculation. Hence approximating the transfer function to lower order leads to inaccurate estimation of the interconnect metrics such as delay, rise time and cut-off frequency. Further, analysis of the coupled lines by considering the electric and magnetic coupling effects between them as well as to derive the expression for the transfer function becomes complex when previously described methods are used.

In this paper, we have developed models for single and coupled interconnect lines with distributed *RLGC* parameters using state space approach by taking into account the effect of dielectric losses and electric and magnetic coupling. Generalized state matrices are formed in case of single and coupled interconnect lines. The elements of the state space matrices developed in this method are in the form of a regular structure. Hence the matrix can be written to the required sizes in a modular fashion by looking at the required number of segments. The proposed models can be extended to any number of coupled lines without any additional mathematical derivations.

The rest of this paper is organized as follows. Transmission line model of interconnect in GHz frequency is given in section II. Section III gives the generalized state matrices for single and coupled interconnect lines. Section IV gives the simulation results. The conclusions are given in section V.

II. MODELING OF INTERCONNECTS

A uniform single interconnect system of length d is shown in Fig. 1. Consider a small line element Δx at any position x along the interconnect line. Since Δx is sufficiently small, we can model this section as a lumped *RLGC* circuit as shown in Fig. 2.

The loop and node equations for the circuit in Fig. 2 are

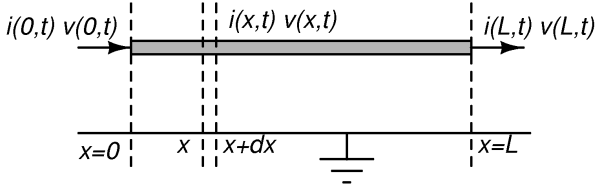$$v(x,t) = l\Delta x \frac{\partial i(x,t)}{\partial t} + r\Delta x i(x,t) + v(x+\Delta x, t) \quad (1)$$
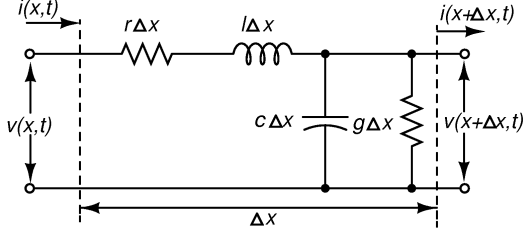
Fig. 1. A simple interconnect line system

Fig. 2. Equivalent circuit of an infinitesimal section.

$$i(x,t) = c\Delta x\frac{\partial v(x+\Delta x,t)}{\partial t} + g\Delta x v(x+\delta x,t) + i(x+\Delta x,t) \tag{2}$$

Since interconnect to substrate losses dominate beyond 10 GHz, these losses are modeled using the conductance term (g) in Eq. 2 above. Differentiating Eq. 1 and 2 and letting $\Delta x \to 0$, we obtain

$$\frac{\partial v(x,t)}{\partial x} = -[ri(x,t) + l\frac{\partial i(x,t)}{\partial t}] \tag{3}$$

$$\frac{\partial i(x,t)}{\partial x} = -[gv(x,t) + c\frac{\partial v(x,t)}{\partial t}] \tag{4}$$

Applying Laplace transformation to Eq. 3 and Eq. 4, we get,

$$\frac{\partial V(x)}{\partial x} = -[r + sl]I(x) \tag{5}$$

$$\frac{\partial I(x)}{\partial x} = -[g + sc]V(x) \tag{6}$$

A. State Space Based Interconnect Modeling

An interconnect network can be modeled as a linear, time invariant system using descriptor state space equations shown in Eq. 7 and Eq. 8.

$$\boldsymbol{E}\dot{x}(t) = \boldsymbol{A}x(t) + \boldsymbol{B}u(t) \tag{7}$$

$$\boldsymbol{y(t)} = \boldsymbol{C}x(t) + \boldsymbol{D}u(t) \tag{8}$$

where $\dot{x}(t)$ and $x(t)$ are n dimensional state derivative and variable vectors, $u(t)$ and $y(t)$ are $m \times 1$ input and $p \times 1$ output vector variables, $\boldsymbol{E}$ and $\boldsymbol{A}$ are descriptor and state matrices of dimension $n \times n$, $\boldsymbol{B}$ is the input vector matrix of dimension $n \times m$, $\boldsymbol{C}$ is the output vector of dimension $p \times n$ and $\boldsymbol{D}$ is the feed-through vector of dimension $p \times m$. In our system model, there is no direct coupling between input and output i.e. $\boldsymbol{D} = 0$. Depending upon m and p values, the system can be SISO (Single Input Single Output) or MIMO (Multiple Input Multiple Output).

B. Procedure to find State Space Matrices

Following steps are used to find state space matrices.
1) In the proposed model, the state space description of an interconnect line is represented by *rlgc* network. The physical state variables in this system include inductor currents and capacitor voltages.
2) State variables in the state vector $x(t)$ in Eq. 7 are obtained from the equivalent distributed *RLGC* model of the circuit.
3) The nodal and loop equations containing capacitor voltages and inductor currents are obtained and expressed as matrices shown in Eq. 7 and Eq. 8.
4) The elements of matrix E represent the capacitive and inductive coupling among state variables.
5) The elements of matrix A represent resistance and conductance among state variables. Matrices B, C, D are input, output and feed-through matrices.

III. PROPOSED MODELS

A. Model for Single Interconnect line

Fig. 3(a) shows the 3D view of an isolated single interconnect line and its equivalent RLGC model is shown in Fig. 4(a).
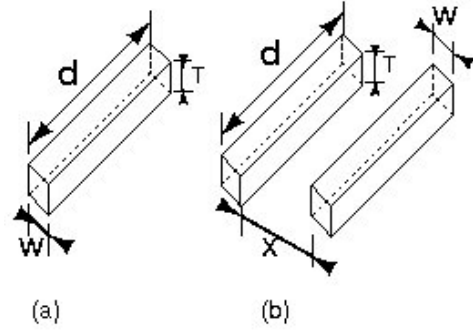

Fig. 3. Structures of (a) Single and (b) Coupled interconnect line

Using the procedure given in II-B, state matrices are formed as shown below.

$$\mathbf{E_{sing}} = \begin{bmatrix} \mathbf{E_{11}} & 0 \\ 0 & \mathbf{E_{22}} \end{bmatrix} \tag{9}$$

$$\mathbf{A_{sing}} = \begin{bmatrix} \mathbf{A_{11}} & \mathbf{A_{12}} \\ \mathbf{A_{21}} & \mathbf{A_{22}} \end{bmatrix} \tag{10}$$

The structure of the state space matrices presented in Eq. 9 and 10 are given below.

Entry e_{ij} of $\mathbf{E_{11}}$ are defined as,

$$e_{i,j} = \begin{cases} L_i, & i=j \\ 0, & \text{otherwise} \end{cases}$$

e_{ij} of $\mathbf{E_{22}}$ are defined as,

$$e_{i,j} = \begin{cases} C_i, & i=j \\ 0, & \text{otherwise} \end{cases}$$
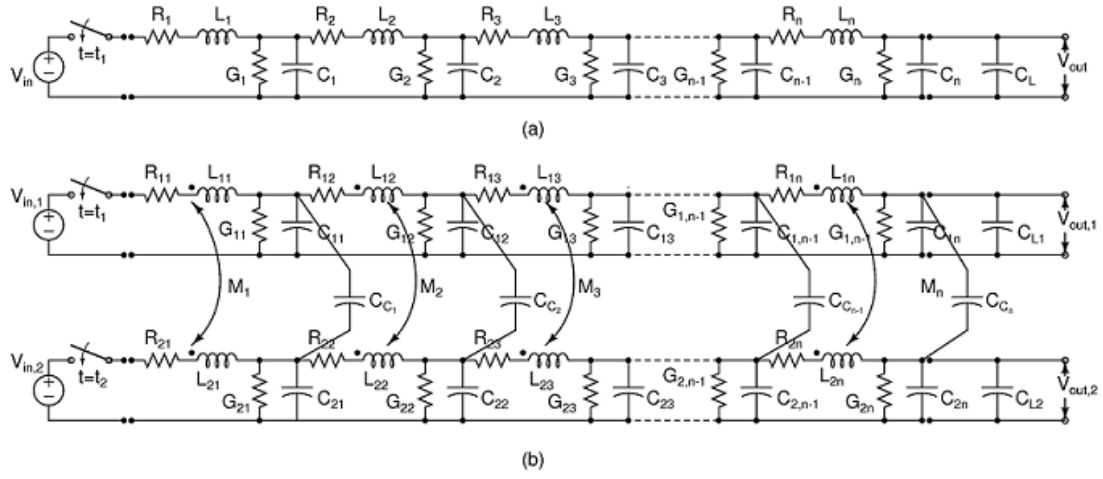
Fig. 4. Generalized models of interconnect (a) Single line (b) Coupled line

a_{ij} of $\mathbf{A_{11}}$ are defined as,

$$a_{i,j} = \begin{cases} -R_i, & \text{i=j} \\ 0, & \text{otherwise} \end{cases}$$

a_{ij} of $\mathbf{A_{12}}$ are defined as,

$$a_{i,j} = \begin{cases} -1, & \text{i=j} \\ 1, & \text{i=(j-1)} \\ 0, & \text{otherwise} \end{cases}$$

a_{ij} of $\mathbf{A_{21}}$ are defined as,

$$a_{i,j} = \begin{cases} 1, & \text{i=j} \\ -1, & \text{i=(j+1)} \\ 0, & \text{otherwise} \end{cases}$$

a_{ij} of $\mathbf{A_{22}}$ are defined as,

$$a_{i,j} = \begin{cases} -G_i, & \text{i=j} \\ 0, & \text{otherwise} \end{cases}$$

B. Proposed Model for Coupled Lines

Closely placed interconnect lines are considered for modeling as shown in Fig. 3(b). Crosstalk occurs between neighboring lines and this adversely affects the system level timings and integrity of the signal. To model this effect, mutual inductance and coupling capacitances between the interconnect lines are considered as shown in Fig. 4(b). Loop equations for the mutual inductance (M) are applied such a way that if both the currents defined going into the dots (the sign of M), will be positive else negative. The effect of leakage from the interconnect to the substrate is modeled using G. Using the procedure given in section II-B, state matrices are formed as shown below.

$$\mathbf{E_{coup}} = \begin{bmatrix} \mathbf{E_{C11}} & \mathbf{E_{C12}} & 0 & 0 \\ \mathbf{E_{C21}} & \mathbf{E_{C22}} & 0 & 0 \\ 0 & 0 & \mathbf{E_{C33}} & \mathbf{E_{C34}} \\ 0 & 0 & \mathbf{E_{C43}} & \mathbf{E_{C44}} \end{bmatrix} \quad (11)$$

$$\mathbf{A_{coup}} = \begin{bmatrix} \mathbf{A_{C11}} & 0 & \mathbf{A_{C13}} & 0 \\ 0 & \mathbf{A_{C22}} & \mathbf{A_{C23}} & 0 \\ \mathbf{A_{C31}} & 0 & \mathbf{A_{C33}} & 0 \\ 0 & \mathbf{A_{C42}} & 0 & \mathbf{A_{C44}} \end{bmatrix} \quad (12)$$

Each entry in Eq. 11 and 12 are matrices and the elements are defined as given below.

Entry e_{ij} of $\mathbf{E_{C11}}$ are,

$$e_{ij} = \begin{cases} L_{1k}, & \text{i=j and k=[1,n]} \\ 0, & \text{i} \neq \text{j} \end{cases}$$

e_{ij} of $\mathbf{E_{C12}}$ and $\mathbf{E_{C21}}$,

$$e_{ij} = \begin{cases} M_k, & \text{i=j and k=[1,n]} \\ 0, & \text{i} \neq \text{j} \end{cases}$$

e_{ij} of $\mathbf{E_{C33}}$,

$$e_{ij} = \begin{cases} C_{1k} + C_{c_k}, & \text{i=j and k=[1,n]} \\ 0, & \text{i} \neq \text{j} \end{cases}$$

e_{ij} of $\mathbf{E_{C34}}$ and $\mathbf{E_{C43}}$,

$$a_{ij} = \begin{cases} -C_{c_k}, & \text{i=j and k=[1,n]} \\ 0, & \text{i} \neq \text{j} \end{cases}$$

e_{ij} of $\mathbf{E_{C44}}$,

$$a_{ij} = \begin{cases} C_{2k} + C_{c_k}, & \text{i=j and k=[1,n]} \\ 0, & \text{i} \neq \text{j} \end{cases}$$

Elements a_{ij} of $\mathbf{A_{C11}}$ is

$$a_{ij} = \begin{cases} -R_{1k}, & i=j \text{ and } k=[1,n] \\ 0, & i \neq j \end{cases}$$

a_{ij} of $\mathbf{A_{C13}}$ and $\mathbf{A_{C23}}$,

$$a_{ij} = \begin{cases} -1, & i=j \\ 1, & i=(j\text{-}1)>1 \\ 0, & i \neq j \end{cases}$$

a_{ij} of $\mathbf{A_{C22}}$,

$$a_{ij} = \begin{cases} -R_{2k}, & i=j \text{ and } k=[1,n] \\ 0, & i \neq j \end{cases}$$

a_{ij} of $\mathbf{A_{C31}}$ and $\mathbf{A_{C42}}$,

$$a_{ij} = \begin{cases} 1, & i=j \\ -1, & i=(j+1)>1 \\ 0, & i \neq j \end{cases}$$

a_{ij} of $\mathbf{A_{C33}}$,

$$a_{ij} = \begin{cases} -G_{1k}, & i=j \text{ and } k=[1,n] \\ 0, & i \neq j \end{cases}$$

Entries a_{ij} of $\mathbf{A_{C44}}$,

$$a_{ij} = \begin{cases} -G_{2k}, & i=j \text{ and } k=[1,n] \\ 0, & i \neq j \end{cases}$$

IV. SIMULATION RESULTS

The minimum number of *rlgc* segments required to model the interconnect [11] is given in Eq. 13.

$$N_{min} \geq \frac{10 \cdot d}{t_r v} \tag{13}$$

where d is the length of the interconnect line, v is the propagation velocity through the transmission line and t_r is the rise (or fall) time of the signal. In our example, we have considered an interconnect length of 2.5 mm, dielectric permittivity as 2.2, C_L=0.5 pF and 16 *rlgc* segments (calculated based on Eq. 13). Inductance, mutual inductance and coupling capacitance values are calculated using closed form expressions ([12] - [13]). Interconnect parameters are calculated based on the physical parameters given in ITRS 2007 [1] for different technology nodes and is given in Table I for a length of 2.5 mm.

Models for single and coupled interconnect lines are validated by comparing their responses with SPICE simulations. From Fig. 5 and 6, it is observed that the models responses are matching with the SPICE simulations.

To find the accuracy of our model in estimating the delay, we have considered an isolated single line of Fig. 3(a) with its generalized model shown in Fig. 4(a). State space matrices are formed as per the procedure given in section II-B and the corresponding transfer function is formed. Interconnect delay (50%) is measured from the response plot of the transfer

TABLE I
VALUES USED IN THE PROPOSED MODELS

Element	Technology				Units
	180 nm	130 nm	90 nm	65 nm	
R	55	76.38	91.65	101.85	Ω
L	4.149	4.214	4.243	4.258	nH
C	201.715	197.81	207.06	205.07	fF
C_c	203.85	223.6	220.99	183.05	fF
G	0.30	0.33	0.41	0.56	$amho$
M	0.29	0.31	0.32	0.34	nH

function for step input in MATLAB. A comparison between our model with other models ([14] and [10]) is listed in Table II for different source resistances. It can be seen from Table II that the model presented in this paper is more accurate than the other models.
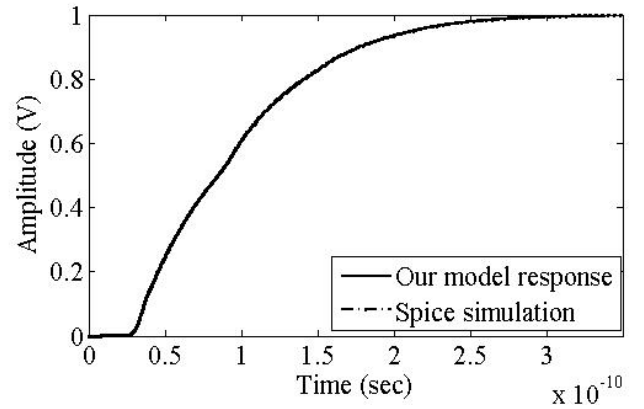

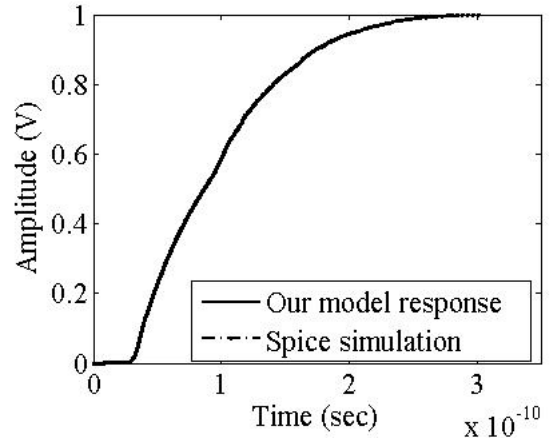Fig. 5. Single line model response compared to Spice simulation

Fig. 6. Coupled line model response compared to Spice simulation

Interconnect performance metrics (50% time delay (t_d), rise time (t_r) and cut-off frequency (f_c)) are obtained from the models responses for different technology nodes are given in Table III. Fig. 7 shows the frequency response of the proposed

TABLE II
COMPARISON OF TIME DELAY WITH OTHER DELAY MODELS

R_s	C_L		Delay Models					
			Ref. [14]		Ref. [10]		Our model	
		Spice	t_d	Error in	t_d	Error in	t_d	Error in
(Ω)	(pF)	(ps)	(ps)	%	(ps)	%	(ps)	%
40	0.176	33.9	39.9	15	36.3	6.6	34.6	2
50	0.176	38.9	44.1	11.8	40.6	4.2	39.1	0.5
75	0.176	51.9	54.8	5.3	53	2	52.08	0.3

TABLE III
PROPOSED MODELS RESPONSE

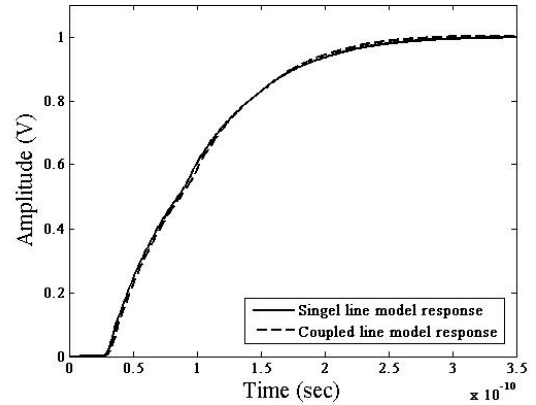| Technology	Proposed Models	t_d (ps)	t_r (ps)	f_c (GHz)
180 nm	Single	71	88	15.3
	Coupled	73	87	13.2
130 nm	Single	78	111	11
	Coupled	89	104	9.8
90 nm	Single	82	127	6.05
	Coupled	84	125	5.51
65 nm	Single	86	141	3.8
	Coupled	88	136	3.6

Fig. 8. Time domain response for the proposed models at 65nm technology node

models for 65nm technology node. Fig. 8 shows the time domain response curves for the proposed models obtained using 65nm technology parameters.

From Table III, it can be seen that time delay and rise time through the interconnect increases as the technology node decreases. The effect of Mutual inductance and coupling capacitance increases the signal propagation delay.
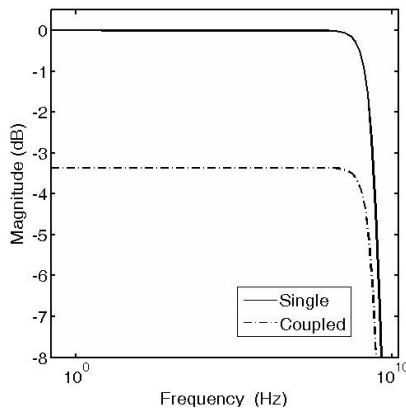

Fig. 7. Frequency domain response for the proposed models at 65nm technology node

Models for any length of single and coupled interconnect lines can be written using our proposed modular approach. The developed models are easily extendable to any number of cou-

pled interconnect lines. This is illustrated by developing state space matrices for four coupled interconnect system shown in Fig. 9. Coupling effects between non-consecutive lines are neglected since electric and magnetic coupling between non-consecutive lines is usually very weak relative to that between consecutive lines. In our example, we have considered four *RLGC* sections and step signals as the inputs for line 1 and line 3 (aggressor lines).

State matrices are determined for the four coupled interconnect system shown in Fig. 9 by extending the Eq. 11 and 12 as in Eq. 14 and 15. Each entry in Eq. 14 and 15 are matrices and the elements are defined as given in section III-B. Model response of the system is shown in Fig. 10. In our example, line 2 and line 4 are the victim lines and the coupled noise voltage in these lines are plotted in Fig. 10.

$$
\mathbf{E_{4coup}} =
\begin{bmatrix}
\mathbf{E_{11}} & \mathbf{E_{12}} & 0 & 0 & 0 & 0 & 0 & 0 \\
\mathbf{E_{21}} & \mathbf{E_{22}} & \mathbf{E_{23}} & 0 & 0 & 0 & 0 & 0 \\
0 & \mathbf{E_{32}} & \mathbf{E_{33}} & \mathbf{E_{34}} & 0 & 0 & 0 & 0 \\
0 & 0 & \mathbf{E_{43}} & \mathbf{E_{44}} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \mathbf{E_{55}} & \mathbf{E_{56}} & 0 & 0 \\
0 & 0 & 0 & 0 & \mathbf{E_{65}} & \mathbf{E_{66}} & \mathbf{E_{67}} & 0 \\
0 & 0 & 0 & 0 & 0 & \mathbf{E_{76}} & \mathbf{E_{77}} & \mathbf{E_{78}} \\
0 & 0 & 0 & 0 & 0 & 0 & \mathbf{E_{87}} & \mathbf{E_{88}}
\end{bmatrix}
\tag{14}
$$

Fig. 9.   Four coupled interconnect lines

V. CONCLUSION

State space approach is used to model single and coupled interconnect lines. Generalized state matrices are formed and validated by comparing with SPICE simulations. In comparision to the existing models, our model is found to be close to the SPICE model. In case of coupled interconnect lines, matrices are formed by considering mutual inductances, coupling capacitances and dielectric losses. Interconnect metrics are determined from the proposed models for 180 nm, 130 nm, 90 nm and 65 nm technology nodes. The models are valid for wide range of operating frequencies. Simulation results indicate dominance of interconnect delay at lower technologies. The generic nature of our modeling approach is illustrated by writing the state space matrices for four coupled interconnect lines.

$$A_{4coup} = \begin{bmatrix} A_{11} & 0 & 0 & 0 & A_{15} & 0 & 0 & 0 \\ 0 & A_{22} & 0 & 0 & 0 & A_{26} & 0 & 0 \\ 0 & 0 & A_{33} & 0 & 0 & 0 & A_{27} & 0 \\ 0 & 0 & 0 & A_{44} & 0 & 0 & 0 & A_{48} \\ A_{51} & 0 & 0 & 0 & A_{55} & 0 & 0 & 0 \\ 0 & A_{62} & 0 & 0 & 0 & A_{66} & 0 & 0 \\ 0 & 0 & A_{73} & 0 & 0 & 0 & A_{77} & 0 \\ 0 & 0 & 0 & A_{84} & 0 & 0 & 0 & A_{88} \end{bmatrix} \tag{15}$$
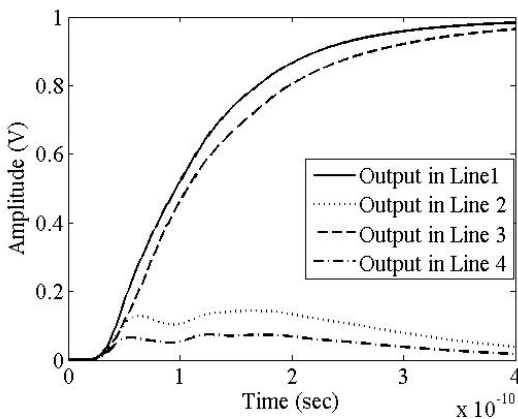

Fig. 10.   Model response for four coupled interconnect system in different interconnect lines

Using the proposed modular approach, we can model any number and any length of coupled interconnect lines. Our method does not requires separate mathematical derivations to find the expressions for the time delay in case of more than two coupled interconnect lines. Crosstalk voltage in the victim lines of the coupled interconnect system can be measured from the response plots.

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