Low Voltage, Low Power Transconductor for Low Frequency G_m-C Filters

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Abstract. A low voltage, low power bulk-driven transconductor for low frequency Transconductance-C ($G_m - C$) filters is proposed. The transconductor is designed in UMC 180 nm technology with supply voltage of 0.5 V. The transconductance (G_m) is tunable from 12 nS to 100 nS, which is suitable for low frequency $G_m - C$ filters. The power consumption is 120 nW. As an application, a 2^{nd} order Butterworth low pass filter (LPF) with cutoff frequency tunable from 110 Hz to 960 Hz is designed.

Keywords: Bulk-driven · Low-voltage · Low-power
Low-frequency filters

1 Introduction

Continuous time (CT) filters are one of the important building blocks of analog pre-processing in wearable and implantable medical devices such as heart rate detectors, breathing detectors, cardiac-pacemakers, cochlear implants etc. They are used to limit the frequency band and to eliminate the out-of-band noise. As the signals involved in the above mentioned applications are of low frequency, typically 10 mHz to 10 KHz [1], it is mandatory to design such filters with low cutoff frequency. The other major requirements of these filters are low power consumption, low noise and less area as these medical devices are portable and battery operated.

The popular topologies of CT filters are Active-RC and $G_m - C$ structures. To design Active-RC filters with low cutoff frequency, large resistors and capacitors are required, which occupy a large area on the chip. Hence, simple Active-RC filters are not suitable for low frequencies. However, certain circuit techniques have been developed such as current steering [2,3], Pseudo resistor based Active-RC filter [4,5], R-2R ladder network [6,7] based filter etc., for low frequencies. But all these techniques have their own limitations as far as power, area, thermal noise, high sensitivity to changes in bias voltage etc., are concerned. In general, $G_m - C$ filters are preferred over Active-RC filters for low frequencies.

In $G_m - C$ filters, the cutoff frequency is determined by $\frac{G_m}{2\pi C}$. To get low cutoff frequency, either G_m should be low or capacitor should be large. But,

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large capacitors occupy more area on the chip. By using impedance scaler circuits [8,9] the capacitance value can be increased with less silicon area. But these circuits not only consume extra power but also produce extra noise. Therefore, a transconductor with small G_m is preferred for the realization of low frequency filters. Current division and current cancellation techniques to reduce G_m are reported in [9,10]. These techniques require more power and suffer from offset voltage. Floating-gate transistors [11,12] capacitively attenuate the input voltage and reduce the G_m. But, these transistors occupy more silicon area and need extra processing steps.

According to ITRS-2015 (International Technology Road map for Semiconductors), by about the year 2024, the power supply for digital circuits will be at 0.55 V. The main motive for this scaling of supply voltage is to reduce the dynamic power of digital logic circuits. Analog circuits have to work with these low supply voltages as they exist along with digital circuits in a typical System-on-chip (SoC). But the supply voltage scaling in analog circuits, results in the reduction of signal swing, and hence reduces dynamic range. As the threshold voltage (V_{th}) of the transistors is scaled at a slower rate than supply voltage, this problem is magnified. Thus, the existing analog circuits should be modified in order to have the same or even better performance under low voltage conditions.

In order to avoid above mentioned problems, bulk-driven transistors [13] can be used, where the signal is applied to the bulk terminal rather than the gate terminal. This reduces the V_{th} of transistor and allows rail-to-rail input voltage swing even under low supply voltages such as 0.5 V. The bulk transconductance is typically 0.2–0.4 times that of gate transconductance, which is the major requirement for the low frequency $G_m - C$ filters. The transconductance can be reduced further by current scaling circuits. Therefore, a low voltage, low power transconductor with low G_m can be realized by using bulk-driven input transistors and current scaling circuits.

This paper proposes the design of fully differential tunable bulk-driven transconductor. As an application a 2^{nd} order Butterworth LPF is designed to demonstrate the performance of the transconductor. The rest of the paper is organized as follows. In Sect. 2, design of tunable bulk-driven transconductor is discussed. Section 3 deals with the simulation results. Finally conclusions are drawn in Sect. 4.

2 Transconductor Design

2.1 Tunable Bulk-Driven Transconductor

A tunable single ended bulk-driven transconductor is shown in Fig. 1, where V_{in} and V_o represent input and output voltages respectively. V_{in} is given to the bulk terminal of the input transistor M_1. I_{in} represents the current of transistor M_1 and I_o represents the output current. The transistor M_1 is biased by a constant current of 10 nA that is mirrored by constant current source I_{DC}. M_2 mirrors the current I_{in} to M_3 through Variable Gain Current Mirror [14] with a current gain K.

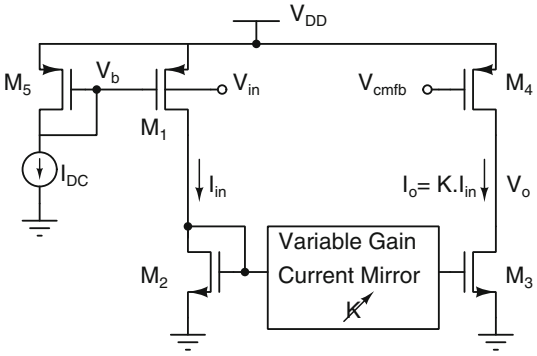


Fig. 1. Tunable single ended bulk-driven transconductor

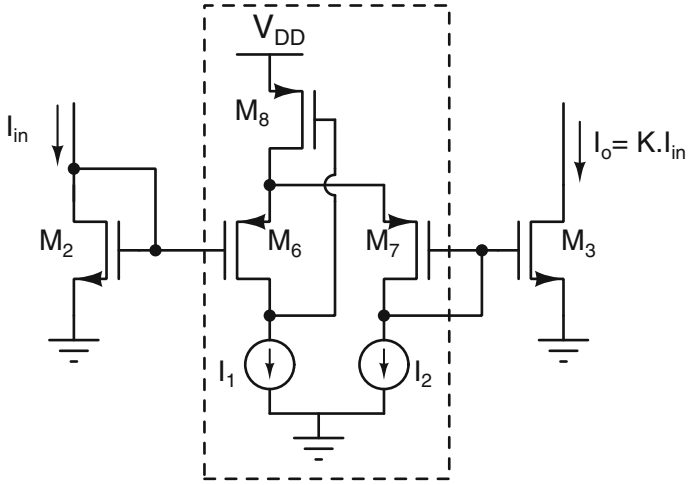


Fig. 2. Variable gain current mirror

The Variable Gain Current Mirror circuit is shown in Fig. 2. The currents I_1 and I_2 are generated from a reference current source (not shown in Figure). M_2, M_3, M_6 and M_7 are biased in the weak-inversion region and form trans-linear loop [15]. The relation among the gate-source voltages of M_2, M_3, M_6 and M_7 can be expressed as (1).

$$V_{GS2} + V_{SG6} = V_{SG7} + V_{GS3} \tag{1}$$

For an NMOS transistor operating in weak-inversion region, the drain current can be written as

$$I_{Dn} = A_n e^{B_n(V_{GSn} - V_{tn})}(1 - e^{\frac{-V_{DSn}}{V_T}}) \tag{2}$$

where,

$$A_n = \mu_n C_{ox} \frac{W}{L}(m_n - 1)V_T^2$$

$$B_n = \frac{1}{m_n V_T}$$

$V_T = \frac{kT}{q}$, is the volt-equivalent of temperature and m_n is sub-threshold slope factor and its value lies between 1.1 and 1.4. For $V_{DSn} \geq 4V_T$, the current I_{Dn} can be assumed to be independent of V_{DSn} i.e. $(1 - e^{-\frac{-V_{DSn}}{V_T}}) \approx 1$. Then (2) can be simplified to (3).

$$I_{Dn} \approx A_n e^{B_n(V_{GSn} - V_{tn})} \tag{3}$$

Similarly, the drain current for a PMOS can be written as (4)

$$I_{Dp} \approx A_p e^{B_p(V_{SGp} - |V_{tp}|)} \tag{4}$$

From the Eqs. (3) and (4), V_{GSn} and V_{SGp} can be derived as (5) and (6) respectively.

$$V_{GSn} = \frac{1}{B_n} \ln(\frac{I_n}{A_n}) + V_{tn} \tag{5}$$

$$V_{SGp} = \frac{1}{B_p} \ln(\frac{I_p}{A_p}) + \mid V_{tp} \mid \tag{6}$$

The transistors M_2, M_3 and M_6, M_7 in the Fig. 2 are matched. By substituting (5) and (6) in (1), the relation among the currents I_{in}, I_o, I_1 and I_2 can be derived as (7)

$$I_o = K.I_{in} \tag{7}$$

where $K = (\frac{I_1}{I_2})^{\frac{m_p}{m_n}}$ is the current gain.

When $I_1 = I_2$, the current gain is 1 as $V_{SG6} = V_{SG7}$, $V_{GS2} = V_{GS3}$. When $I_1 > I_2$, the current gain is >1 as $V_{SG6} > V_{SG7}$, $V_{GS2} < V_{GS3}$. When $I_1 < I_2$, the reverse is true and the current gain is < 1. Therefore the output current of the transconductor can be scaled by varying the currents I_1 or I_2, which in turn scales the effective transconductance of the circuit.

2.2 Fully Differential Bulk-Driven Transconductor

A fully differential tunable bulk-driven transconductor is shown in Fig. 3. The input transistors M_1 and M_2 are biased by using a current source of 10 nA (not shown in the Figure). M_5-M_{10} and current sources I_1, I_2 form Variable Gain Current Mirror. All the transistors are operating in weak-inversion region. C_c is used as compensating capacitor to improve the phase margin.

The output differential current, i_{od} is given by (8)

$$i_{od} = K.g_{mb}.v_{id} \tag{8}$$

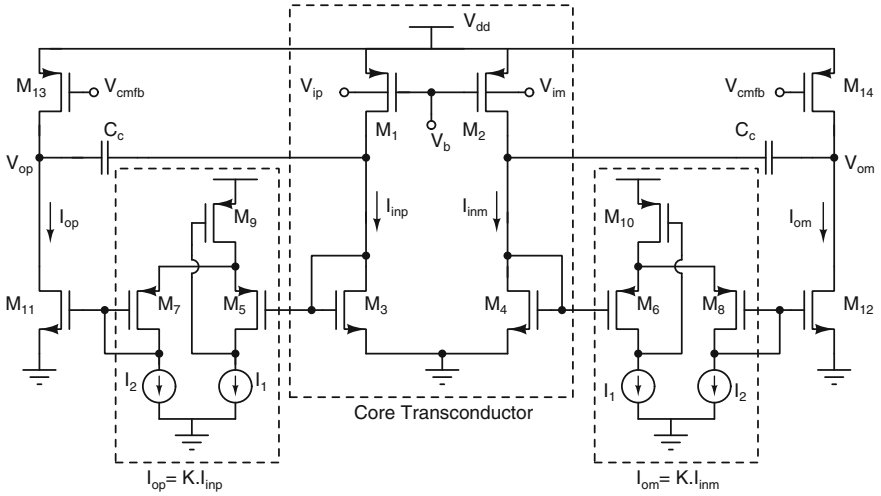
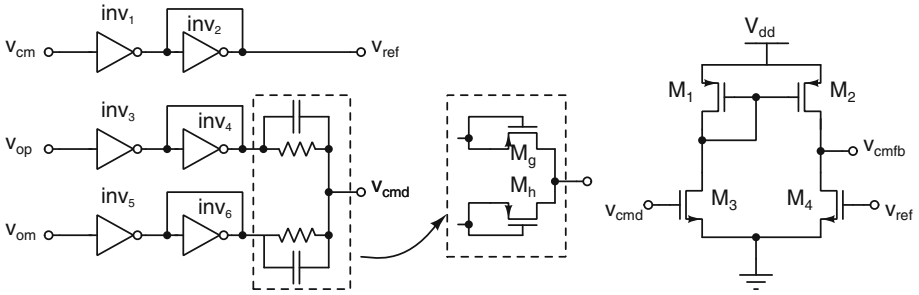


Fig. 3. Fully differential bulk-driven transconductor



(a) Common mode detector (b) Error amplifier

Fig. 4. CMFB circuit [16]

where $i_{od} = I_{op} - I_{om}$ is the output differential current, g_{mb} is the bulk-driven transconductance of the input transistor M_1 or M_2 and $v_{id} = V_{ip} - V_{im}$ is the input differential voltage.

The effective transconductance G_m is given by (9)

$$G_m = K.g_{mb} \tag{9}$$

The voltage gain of the transconductor is given by (10)

$$A_v = K.g_{mb}.(r_{11} \parallel r_{13}) \tag{10}$$

where r_{11} and r_{13} are small signal output resistances of M_{11} and M_{13} respectively.

The transconductor uses a supply voltage of 0.5 V. The input common mode voltage (V_{cm}) is fixed at 0.25 V. Gates of M_{13} and M_{14} are biased with a common

mode feedback voltage (V_{cmfb}) which sets the output common mode voltage to 0.25 V. A common mode feedback (CMFB) circuit proposed in [16] (Fig. 4) is used in this work. In Fig. 4(a), inverters 3 to 6 along with transistors M_g and M_h form common mode detector. Inverters 3 and 5 sense the output voltages of the transconductor. Inverters 4 and 6 have their outputs shorted to inputs. This arrangement reduces the gain of sensing inverters, thus enhancing the linearity of the sensing inverters and entire CMFB circuit. Transistors M_g and M_h are connected such that they offer high resistance along with a capacitor. This arrangement gives the average (V_{cmd}) of the sensed voltages. V_{cmd} is compared with the reference voltage V_{ref} using a simple error amplifier shown in Fig. 4(b). The error amplifier output voltage V_{cmfb} is fed back to the transconductor to set the output common mode to the reference voltage (V_{cm}).

3 Simulation Results

The transconductor is designed and simulated in UMC 180 nm technology. G_m tuning of the transconductor is done by varying I_1 from 2 nA to 18 nA by fixing I_2 at 10 nA. This varies the current gain, K and hence G_m. The simulated G_m against the input differential voltage for different I_1 values is shown in Fig. 5. G_m is tuned from 12 nS to 100 nS by fixing I_2 at 10 nA and varying I_1 from 2 nA to 18 nA in steps of 4 nA. The values of I_1 and I_2 can be digitally controlled by using current splitting circuits implemented as in [17]. It is observed that an equal increment in I_1, gives almost an equal increment in G_m.

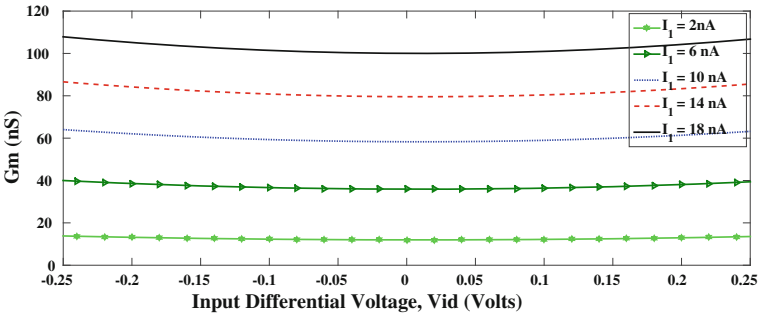


Fig. 5. G_m tuning

The magnitude and phase response of the proposed transconductor are shown in Fig. 6. The open loop DC gain is 30.3 dB, unity-gain frequency is 4.6 KHz and the phase margin is 80°. To test the linearity, the transconductor is connected in unity feedback configuration. The total harmonic distortion (THD) is less than −40 dB for an input signal of 1 V_{pp} differential. Table 1 lists the parameters of the proposed transconductor. A performance comparison of the proposed transconductor with other similar works found in the literature is given in Table 2. It can

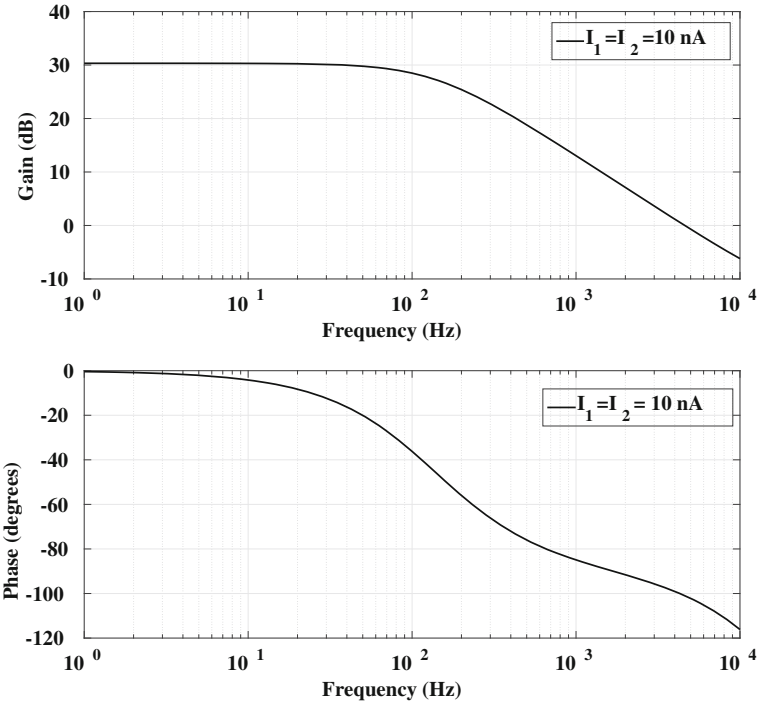


Fig. 6. Frequency response of the transconductor

Table 1. Parameters of the transconductor

Parameter	Simulated values
Technology (μm)	0.18
Supply voltage (volts)	0.5
Transconductance (nS)	12–100
DC Gain(dB)	30.3
UGB (KHz)	4.6
Phase margin (degrees)	80
V_{in-pp} for 1% THD (volts)	1.0
Input referred noise at 100 Hz ($\frac{\mu V}{\sqrt{Hz}}$)	3.6
Input referred noise from 50 Hz–5 KHz (μV)	50
Dynamic range (dB)	77
Power (nW)	120[a]

[a]At $I_1 = 18$ nA and $I_2 = 10$ nA, including CMFB

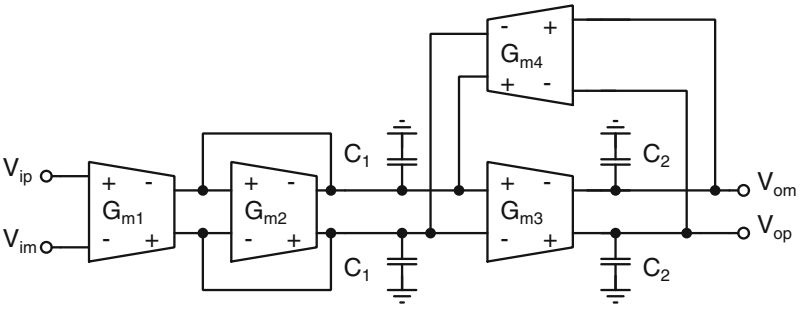


Fig. 7. $G_m - C$ biquad

Table 2. Comparison of the proposed transconductor with other similar works

Parameters	[14]	[18]	[12]	[19]	This work
Technology (μm)	0.18	0.35	0.8	1.2	0.18
Supply voltage (volts)	0.8	0.8	1.5	1.35	0.5
DC gain (dB)	72.2	61	-	-	30.3
G_m (nS)	300–3000	66 n	0.46–82	16.6	12–100
UGB (KHz)	15 with C_L=20 pF	0.195 with C_L=25 pF	-	-	4.6
Phase margin (degrees)	90	81	-	-	80
Input referred noise ($\mu VRMS$)	-	80	110	17.29	50
V_{in-pp} for 1% THD (volts)	1.6	0.1	1.2	0.24	1
Dynamic range (dB)	75	52.9	73	73.9	77
Power (μW)	8.3	0.040	≈1	1.35	0.12

be seen that, performance of the proposed transconductor is better in terms of power and G_m tunability. Hence, it can be very efficiently used for low voltage, low frequency filters.

A fully differential 2^{nd} order Butterworth LPF, shown in Fig. 7 [20], is designed and simulated to evaluate the performance of the proposed transconductor. The cutoff frequency of the filter is tuned from 110 Hz to 960 Hz as shown in Fig. 8. The filter cutoff frequency can be tuned to the required value by controlling the currents I_1 and I_2, so that it fits into the desired frequency range of

different bio-potentials such as electromyogram (EMG), electroencephalogram (EEG), electrocardiogram (ECG) etc.

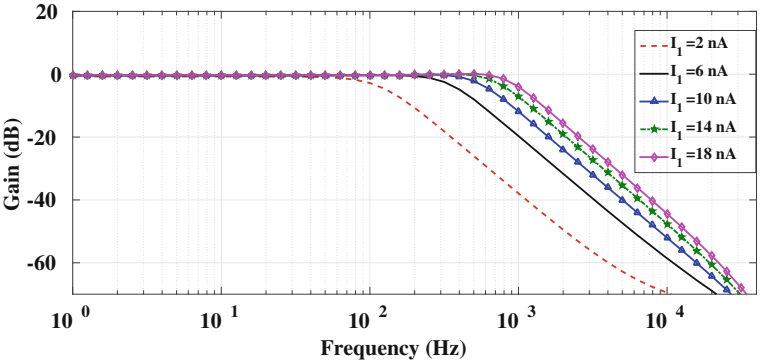


Fig. 8. Frequency response of the filter

4 Conclusion

A fully differential low voltage, low power bulk-driven transconductor for low frequency $G_m - C$ filters is presented. It offers 30.3 dB DC gain, 4.6 KHz unity gain frequency and 80° phase margin. The transconductor consumes a power of 120 nW with 0.5 V supply. A 2^{nd} order Butterwoth LPF with the cutoff frequency tunable from 110 Hz to 960 Hz is designed as an application of the proposed transconductor. By adjusting the currents I_1 and I_2, the cutoff frequency can be tuned to fit into the desired frequency range of different bio-potentials. Filter response closely matches with ideal 2^{nd} order filter response upto an attenuation of 60 dB.

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References

1. Webster, J.: Medical Instrumentation: Application and Design. Wiley, Hoboken (2009)
2. Wong, A., Pun, K.-P., Zhang, Y.-T., Hung, K.: A near-infrared heart rate measurement IC with very low cutoff frequency using current steering technique. IEEE Trans. Circ. Syst. I Regul. Pap. **52**(12), 2642–2647 (2005)
3. Li, H., Zhang, J., Wang, L.: 5 mHz highpass filter with-80 dB total harmonic distortions. IET Electron. Lett. **48**(12), 698–699 (2012)
4. Shiue, M.-T., Yao, K.-W., Gong, C.-S.A.: Tunable high resistance voltage-controlled pseudo-resistor with wide input voltage swing capability. Electron. Lett. **47**(6), 377 (2011)

5. Tajalli, A., Leblebici, Y.: Power and area efficient MOSFET-C filter for very low frequency applications. Analog Integr. Circ. Signal Process. **70**(1), 123–132 (2012)
6. Alzaher, H.A., Tasadduq, N., Mahnashi, Y.: A highly linear fully integrated powerline filter for biopotential acquisition systems. IEEE Trans. Biomed. Circ. Syst. **7**(5), 703–712 (2013)
7. Roy, S.D.: On resistive ladder networks for use in ultra-low frequency active-RC filters. Circ. Syst. Signal Process. **34**(11), 3661–3670 (2015)
8. Silva-Martinez, J., Vazquez-Gonzalez, A.: Impedance scalers for IC active filters. In: Proceedings of IEEE International Symposium on Circuits and Systems 1998, pp. 151–154 (1998)
9. Solis-Bustos, S., Silva-Martnez, J., Maloberti, F., Sinchez-Sinencio, E.: A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter for medical applications. IEEE Trans. Circ. Syst. II Analog Digital Signal Process. **47**(12), 1391–1398 (2000)
10. Silva-Martinez, J., Salcedo-Suer, J.: IC voltage to current transducers with very small transconductance. Analog Integr. Circ. Signal Process. **13**(3), 285–293 (1997)
11. Rodriguez-Villegas, E., Yfera, A., Rueda, A.: A 1.25-V micropower Gm-C filter based on FGMOS transistors operating in weak inversion. IEEE J. Solid-State Circ. **39**(1), 100–111 (2004)
12. Mourabit, A.E., Lu, G.N., Pittet, P.: Wide-linear-range subthreshold OTA for low-power, low-voltage, and low-frequency applications. IEEE Trans. Circ. Syst. I Regul. Pap. **52**(8), 1481–1488 (2005)
13. Guzinski, A., Bialko, M.A., Matheau, J.C.: Body driven differential amplifier for application in continuous-time active-C filter. In: Proceedings of ECCD 1987, pp. 315–319 (1998)
14. Yodtean, A., Thanachayanont, A.: Sub 1-V highly-linear low-power class-AB bulk-driven tunable CMOS transconductor. Analog Integr. Circ. Signal Process. **75**(3), 383–397 (2013)
15. Serrano-Gotarredona, T., Linares-Barranco, B., Andreou, A.G.: A general translinear principle for subthreshold MOS transistors. IEEE Trans. Circ. Syst. I Fundam. Theory Appl. **46**(5), 607–616 (1999)
16. Rekha, S., Laxminidhi, T.: Common mode feedback circuits for low voltage fully-differential amplifiers. J. Circ. Syst. Comput. **25**(10), 1650124 (2016)
17. Linares-Barranco, B., Serrano-Gotarredona, T.: On the design and characterization of femtoampere current-mode circuits. IEEE J. Solid-State Circ. **38**(8), 1353–1363 (2003)
18. Cotrim, E.D., de Carvalho Ferreira, L.H.: An ultra-low-power CMOS symmetrical OTA for low-frequency Gm-C applications. Analog Integr. Circ. Signal Process. **71**(2), 275–282 (2012)
19. Veeravalli, A., Sanchez-Sinencio, E., Silva-Martnez, J.: Transconductance amplifier structures with very small transconductances: a comparative design approach. IEEE J. Solid-State Circ. **37**(6), 770–775 (2002)
20. Schaumann, R., Xiao, H., Mac, V.V.: Design of Analog Filters, 2nd edn. Oxford University Press, Inc., New York (2009)