Design and Development of SiGe HBT based High Gain Amplifier for GPS Application

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Abstract **– A two stage high gain small signal amplifier for GPS based receiver application is designed and realised using SiGe Hetrojunction Bipolar transistor (HBT). The measured gain and noise figure is 33.5 dB and 2.9dB respectively at Vce of 2V, and total current of 10mA. The circuit is fabricated on microstrip configuration using RT duroid substrate of dielectric constant 10.5 and height 50 mils. This circuit is being used in satellite based GPS receiver.**

Index Terms **– SiGe, HBT, Microstrip amplifier, Si BJT, GPS.**

I. INTRODUCTION

Si based BJT is suitable for L and S band amplifier for medium to moderate gain application, but now a day's SiGe HBT devices [1] is replacing BJTs due to improved current transport properties [2-3]. The HBT is similar to the standard bipolar transistor except base emitter junction formed by two different materials. With HBT improved injection efficiency can be achieved by the energy band–gap difference at the junction. This allows the base layer to be more heavily doped, causing reduction in base resistance, and this reduces the transit time of the device and increases its frequency response and gain. In SiGe HBT base layer has the sloping concentration of germanium across its thickness, which creates an electric field to reduce the transit time of electron moving from the base into collector. Table-1 shows [4] the comparison between Si and SiGe technology for f_T, f_{max} and noise figure.

The small signal amplifier in addition to bias circuitry consists of transistor, and input-output matching network. For medium to moderate gain applications the circuit should be biased in linear region and bias circuitry should not disturb RF performance of the network. This can be achieved with proper selection of reactive elements, either in lumped or distributed form to isolate DC and RF circuitry. For the linear amplifier the bipolar devices are operated in common emitter configuration because of maximum power gain. The proposed circuit is a part of GPS receiver for space application that uses the GPS data to determine the position and velocity of the spacecraft in the LEO earth orbit.

II. AMPLIFIER DESIGN

In order to characterise the behaviour of any two port network at microwave frequencies scattering parameters (S parameters) are very useful. The most important design considerations in a microwave transistor amplifier are stability, gain, bandwidth, noise and DC requirements. The design starts with the set of the specifications and selection of suitable device. Then a systematic mathematical solution is used to design the circuit to meet the requirement. For microwave amplifier design S parameters at different bias points are required. These are either measured at the device fabrication level or provided by the manufacturer.

The design of the RF amplifier [3-9] starts with the measurement of transistor stability at the desired frequency band. J.M. Rollett [5] determined a stability factor K from the scattering parameters of the transistor as given in equation 1.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad (1)$$

And $|\Delta| < 1$, where Δ, the determinant of the scattering matrix, is

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}|$$

The significance of the stability factor K is that a device is unconditionally stable for all passive and active source and load terminations when K >1. If the circuit is potentially unstable (K<1), then circuit is stabilized either by using resistive loading or adding negative feedback, but with later approach one has to sacrifice with gain and noise figure.

After establishing the stability, circuit is matched for maximum transducer power gain, the condition for this is

$\Gamma_{in} = \Gamma_s^*$ and $\Gamma_{out} = \Gamma_L^*$

where

$$\Gamma_S = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad (2)$$

and

$$\Gamma_L = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \qquad (3)$$

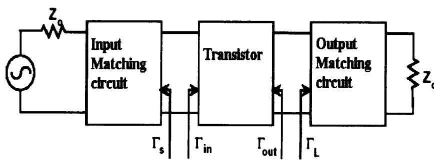

Fig.1. Building Blocks of Amplifier

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Definitions of Γ is represented in the figure 1. By solving equation 2 and 3 simultaneously gives the values Γ_S and Γ_L required for simultaneous conjugate match.

III. CIRCUIT REALISATION

The circuit is realised by using SiGe BJT part number BFY 405 from Infineon technologies [10]. It is a low current and low noise figure micro-X packaged device suitable for amplifier application up to 12 GHz with a power gain and noise figure of 23 dB and 1.15 dB respectively at 1.8 GHz. Resistor divider network with grounded emitter is selected for bias where base resistor is controlling the collector current. Schematic diagram of the single stage amplifier is shown in figure 2. The circuit is biased in linear region with Vce 2V and current 5mA each stage. Resistive loading with resistor value of 75 Ohm at collector side is used to make circuit stable. The effect of this loading on stability factor and gain is shown in figures 3 and 4. The maximum gain reduced from 23 to 18dB.

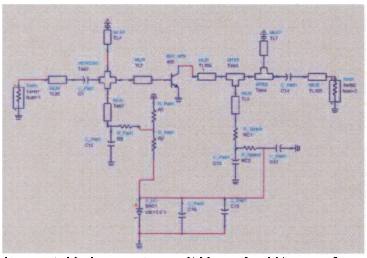

Fig.2. Circuit Schematic of Single Stage Amplifier

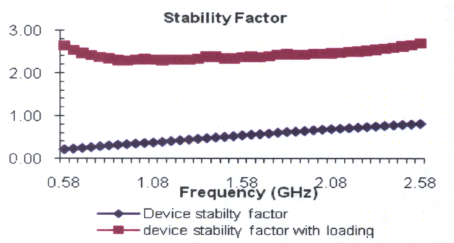

Fig.3. Effect on Stability factor with resistive loading

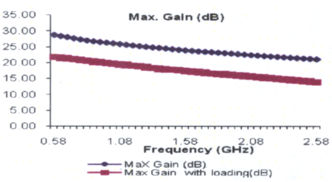

Fig.4. Effect on Max. Gain with resistive loading

The amplifier circuit is fabricated on RT duroid [11] substrate of dielectric constant 10.5 and 50 mil height in microstrip configuration. Conjugate matching using open circuit single stub is used at input and output of the device. Base and collector voltages were applied through short circuit high impedance $\lambda/4$ lines that act as an inductor and open circuit for RF at the intersection with main transmission line to avoid flow of RF towards DC supply side. The simulated frequency is 1.575GHz with return loss bandwidth of 120 MHz and gain was 17 dB each stage. The simulation is carried out by the help of Agilent ADS circuit simulator [12]. The simulated result for single stage is shown in figure 5.

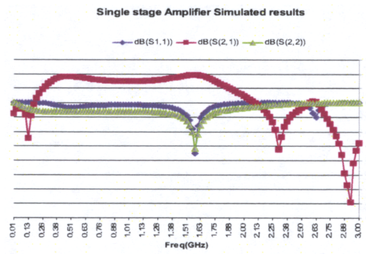

Fig.5. Simulated results of Single stage amplifier

The Same stage is cascaded for double stage and the results are shown in figure 6.

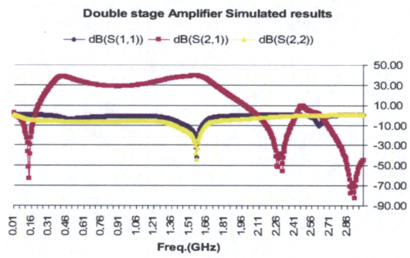

Fig.6. Simulated results of Double stage amplifier

Fabricated circuit is shown in figure 7. Its size is 72.2mm by 36.5 mm. The measured gain and return loss plot is shown in figure 8.

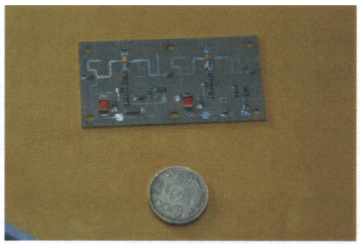

Fig.7. Fabricated Circuit

The measured gain and return loss is 33.75 dB and 18 dB respectively at 1.575 GHz. The total current drawn by the circuit is 10 mA at 2V, Vce. The measurement and simulated responses match closely. This circuit was subjected to hot and cold test and there is no variation of current and gain with temperature over -25 to +60 degree C. The one dB compression measurement is also carried out, the plot of this is shown in figure 9. The measured output P1 dB point is -2 dBm.

IV. CONCLUSION

A two stage high gain amplifier has been designed and developed, the measurement of gain and one dB compression point was carried out. The results of gain and return loss match closely with that of the designed values. The observed deviation in the measured results is due to dielectric, conductor losses and resistive loading. This circuit is used as a buffer gain stage in the satellite based GPS receiver. The overall circuit noise figure including LNA is 1.2 dB.

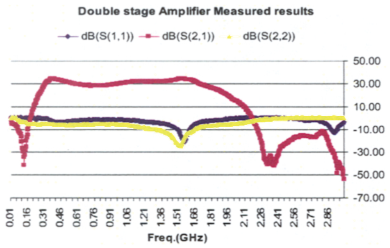

Fig.8. Measured results of two stage amplifier

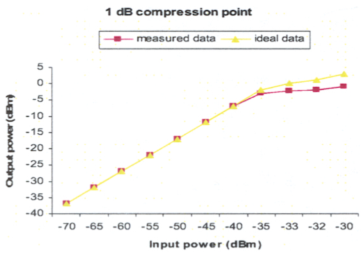

Fig.9. P1 dB point measurement

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