A Compact 10-bit Nonbinary Weighted Switched Capacitor Integrator Based SAR ADC Architecture

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***Abstract*—A compact switched capacitor integrator (SCI) based successive approximation register (SAR) analog to digital converter (ADC) for data acquisition system is presented. This technique requires an operational transconductor amplifier (OTA), a comparator and four equal sized capacitors of moderate value for fully differential approach and the architecture is resolution independent. The reference voltage is generated by charge sharing between a reference capacitor and the input capacitor of a switched capacitor (SC) integrator. The DAC voltage for comparison is generated by accumulating the charges on the SC integrating capacitor. ADC being fully differential nature has wide input range and it is parasitic insensitive to a large extent. As a stand alone data converter it has small capacitance spread and hence its input capacitance is easy to drive. A 10 bit 0.9 MHz sampling rate SAR ADC is designed using 180 nm CMOS technology, operating at 1.8 V supply, has effective number of bits (ENOB) of 9.5 at Nyquist frequency. The ADC occupies small die area compared to SAR with a binary weighted capacitor array.**

***Index Terms*—Analog to Digital Converter (ADC), Successive Approximation Register (SAR), Low power, Charge sharing, Switched Capacitor, Nonbinary.**

I. Introduction

Binary weighted successive approximation ADC has been the most preferred ADC architecture for applications demanding low power and low to medium resolutions. ADC resolution mainly depends on DAC resolution. For every bit increase in DAC resolution, total DAC capacitance doubles which in turn limits the size of the unit capacitor for a given area requirement. To meet accuracy requirement and to minimize KT/C noise, a unit capacitor should be of a reasonable size. Especially in charge redistribution SAR ADCs, DAC capacitors are used to sample the input signal as well. Hence for medium resolution applications, total input capacitance of ADC becomes appreciably large value. On the other hand nonbinary weighted DAC overcomes this problem as there are only fixed number of unit capacitors to be used in DAC irrespective of resolution of ADC. Due to reduced number of unit capacitors in DAC, mismatch errors are greatly reduced. Also there is no need of explicit sample and hold circuit as it can be absorbed into the SC integrator. There are quite a few SCI based nonbinary ADCs reported in the literature. In [1], a similar approach being used for design of resolution independent SCI based 5 V, 100 kHz sampling rate SAR ADC, but the unit capacitor used is of the order of few pico farads, which in turn increases area and power consumption. Because of fully differential operation the linearity is ensured. A SCI based ADC in [2] uses dual power supply voltage for nonbinary DAC structure. Due to single-ended architecture of the DAC and non-ideality of the switches, the SNDR (signal to noise and distortion ratio) is found to be degraded. Noise shaping SAR ADC [3] uses few unit capacitors but takes 50 percent extra time per conversion over conventional SAR ADC. An SCI based SAR ADC architecture using 2 unit capacitors at each part of the differential OTA is proposed in this work which has bare minimum control logic except the registers required to store the data bits. The remaining paper is organized as follows. Section 2 explains proposed SAR architecture. Section 3 includes details regarding OTA and comparator used in the architecture. Section 4 and section 5 gives the simulation results of ADC and conclusion respectively.

II. Proposed SAR Architecture

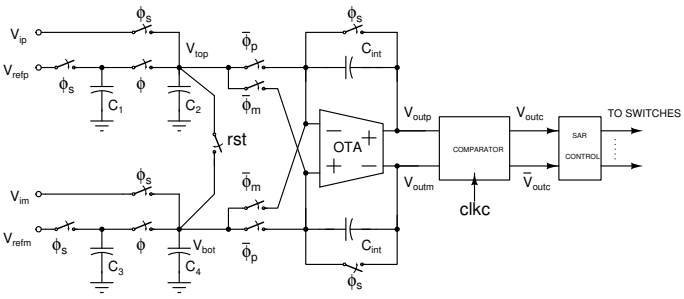

Fig. 1. Schematic of proposed SCI based ADC

Figure 1 illustrates the proposed data converter. Pair of unit capacitors C_1, C_2 and C_3, C_4 form a passive charge sharing capacitors, used for obtaining charge equivalent to binary fractions of positive reference voltage V_{refp} and negative reference voltage V_{refm} respectively. The capacitor C_{int} is used as integrating capacitor. The comparator output V_{outc} is the ADC output bit at successive clock cycles and is fed into simple control circuit which further generates control signal to operate switches according to successive approximation algorithm. Normally, $C_1 = C_2 = C_3 = C_4 = C_{int}$. Step by step operation of ADC is as follows.

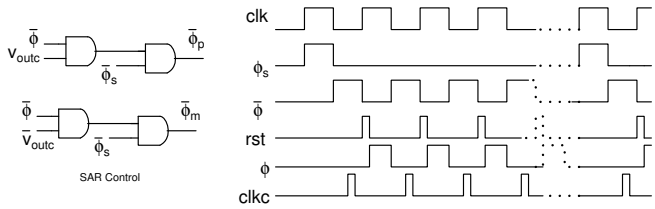

Fig. 2. SAR control and Timing details

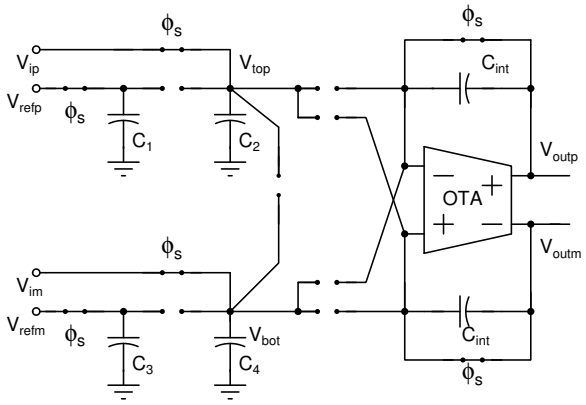

Fig. 3. Sampling phase

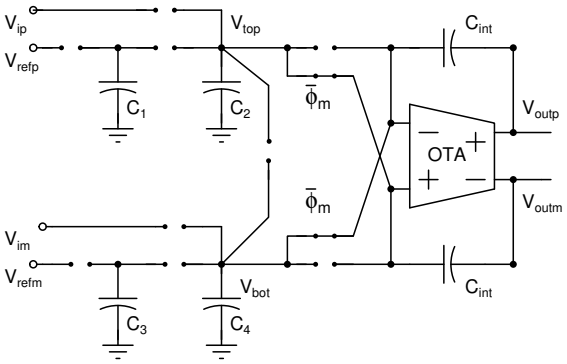

Fig. 4. First $\overline{\phi}$ phase

- **Sampling**: Assuming all capacitors are initially discharged, ϕ_s raised to high so that V_{ip} and V_{im} is sampled on to C_2 and C_4 respectively, V_{refp} and V_{refm} is sampled on to C_1 and C_3 respectively and C_{int} is discharged as shown in Figure 3. The output of the integrator, V_{outp} = V_{outm} = V_{cm}.
- **Charge integration and comparison**: During first $\overline{\phi}$ phase, $\overline{\phi}_m$ is set to '1' (since V_{outc} = '0' initially) so that V_{ip} and V_{im} are integrated on to respective integrated capacitors C_{int} as in Figure 4. Therefore V_{outp} = $-V_{im}$, V_{outm} = $-V_{ip}$. For fully differential operation,
V_{ip} = $-V_{im}$ = V_i and V_{refp} = $-V_{refm}$ = V_{ref}. Therefore one can write V_{outp} = V_i and V_{outm} = $-V_i$. At the end of this phase the comparator is enabled to decide upon MSB. If differential output of the integrator is positive, V_{outc} becomes '1' else '0'.
- **Charge sharing phase**: The 'rst' signal is set to '1' just before next ϕ phase, so that both C_2 and C_4 are discharged. This is done so as to discharge both C_2 and C_4 to common-mode levels before next clock cycle begins. This is important because, any charge left over on these capacitors at the end of the integration phase due to the finite gain of the OTA, will be carried over to the remaining clock cycles of the conversion cycle, corrupting the reference voltages.
When ϕ goes high, then V_{top} becomes V_{refp}/2 and V_{bot} becomes V_{refm}/2. Based on comparator output of previous cycle, V_{top} and V_{bot} voltages are transferred to integrating capacitor during next $\overline{\phi}$ phase. i.e., If previous V_{outc} = '1' (MSB) (for V_i >0) (Figure 5),
then V_{outp} = - V_{im} - V_{refp}/2 and V_{outm} = - V_{ip} - V_{refm}/2.
i.e., V_{outp} = V_i - V_{ref}/2 and V_{outm} = -V_i + V_{ref}/2.
If V_{outc} = '0' (MSB) (for V_i <0),
then V_{outp} = -V_{im} - V_{refm}/2 and V_{outm} = -V_{ip} - V_{refp}/2.
i.e., V_{outp} = V_i + V_{ref}/2 and V_{outm} = -V_i - V_{ref}/2.
Next ϕ phase, the charges remained in C_1, C_3 are further shared on to C_2, C_4 respectively. This process of charge sharing and integration of these charges on to appropriate integrating capacitor happens until all bits are evaluated. V_{outp} - V_{outm} continuously decrease and converge towards zero at the end of conversion period.

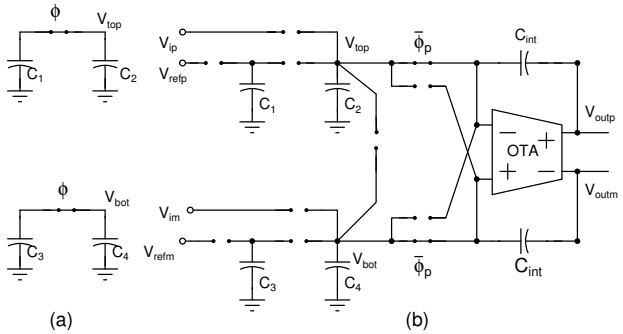

Fig. 5. (a) First ϕ phase (b) Second $\overline{\phi}$ phase, V_{outc} = '1' (MSB)

The charge sharing process is made parasitic insensitive by matching parasitic at the charge sharing nodes using dummy switches. The clock phases for conversion and

the simple control circuit for the above operation are shown in Figure 2. Note that digital control logic uses only four AND gate and D-registers of 10 numbers. The clock phases are appropriately delayed to prevent signal dependent charge injection.

III. OTA FOR SCI SAR ADC

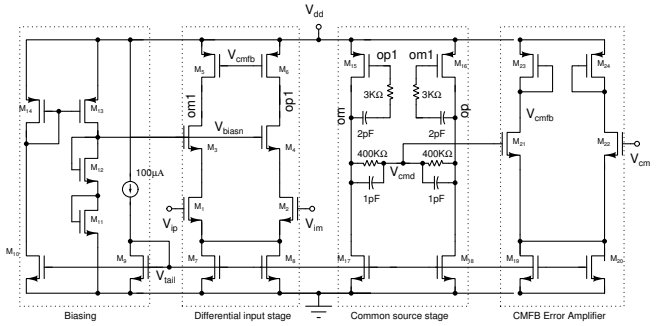

Fig. 6. Schematic of OTA used for SCI ADC

In order to improve the dynamic range and noise performance, a fully differential OTA is designed for SCI based ADC as shown in Figure 6. The two stage OTA has cascode differential amplifier as first stage and a common source second stage. The transistors M_1- M_8 form first stage differential amplifier with cascoded NMOS device and PMOS current source load. Gate bias of PMOS current source load is controlled by common mode feedback (CMFB) circuit. PMOS common source second stage provides additional gain for OTA. Both input and output common mode voltage of OTA is fixed at 0.9 V. Output common mode voltage at second stage of OTA is compared with reference common mode voltage of 0.9 V using error amplifier formed by M_{19}- M_{24} to obtain V_{cmfb} voltage for first stage. A simple Miller RC compensation is used to stabilize the circuit. Differential operation takes care of offset voltage due to signal independent channel charge injection. To address the noise causing input offset at the OTA and disturbing the common mode voltage, a common mode feedback as well as offset correction is employed in this architecture. An autozeroing technique [4] is employed as in Figure 7, which essentially stores offset voltage on to a capacitor during signal sampling phase (ϕ_s) and feeding back the stored offset to cancel the offset voltage from the signal path during hold phase ($\overline{\phi_s}$). The overall OTA DC gain obtained is 75.1 dB for typical process corner with unity gain bandwidth of 84 MHz.

IV. SIMULATION RESULTS

The proposed fully differential SCI based SAR ADC has been designed in UMC 180 nm CMOS process to operate on 1.8 V supply. The ADC has input voltage swing of 1 V peak to peak with a common mode voltage of 0.9 V. The area occupied is 0.05 mm^2 (267 μm X 188 μm). The simulation results shows that, ADC achieved a conversion speed of 0.9 MS/s in 10-bit resolution. The total capacitors used in the DAC is $6C$

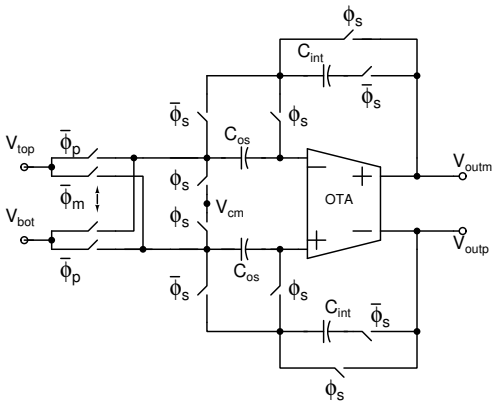

Fig. 7. Schematic of offset correction in OTA

where, C is the unit capacitor of value 300 fF. The unit capacitor of this order is used to limit the thermal noise at the output of integrator. Compared to conventional charge redistribution DAC architecture which requires $1024\,C$ for 10-bit resolution, this DAC offers large savings in terms of area, headroom on capacitor mismatch and parasitic requirements. From static performance of ADC (code density test) in 10 bit, DNL and INL of the ADC at 0.9 MS/s sampling speed is found to be within 0.3 LSB/-0.6 LSB and 0.7 LSB/ -0.1 LSB respectively and is shown in Figure 8 & Figure 9 respectively. The output spectrum of the ADC for an input full-scale sine

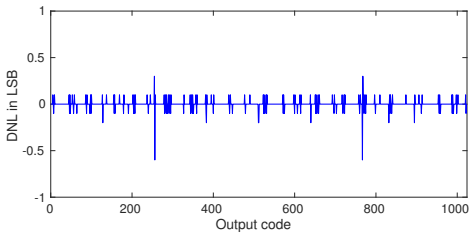

Fig. 8. DNL error

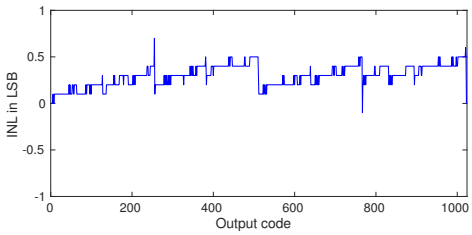

Fig. 9. INL error

wave at 10.65 KHz (near DC) and 450.9 KHz (at Nyquist) are shown in Figure 10 & Figure 11, for which the SNDRs of 61.7 dB (ENOB = 9.95) and 59.02 dB (ENOB = 9.5) are obtained, respectively. The total power consumption of ADC is 739 μW, where major share of power is consumed

Ref.	Tech. (µm)	V_{dd} (V)	F_s (MS/s)	ENOB (@fin)	P_{diss} (µW)	FOM (fJ/conv.)	Area (mm^2)	AE (μm^2/code)	C_u (fF)	C_{tot} (pF)
[6] [1]	0.18	1.5	0.128	12.81	74.2	81.2	0.25	480.08	4000	24
[7] [1]	0.18	1.8	1	9.4	131	193	0.24	480.24	20	5.12
[8][2]	0.18	1	0.82	7.41	30.9	221	0.128	752.62	-	-
[9] [2]	0.13	1.2	1	8.39	147.6	2170	0.18	536.57	15	15
[1] *[1]	0.18	5	0.1	8.63	2035	256000	0.316	797.62	2000	13
[10] [1]	0.045	1.25	1000	6.48	73000	80	0.16	179.24	5	0.6
This work *[1]	**0.18**	**1.8**	**0.91**	**9.5**	**734**	**924.7**	**0.05**	**69.32**	**300**	**1.8**

[1]Nonbinary DAC [2]Binary weighted capacitive array DAC * simulation result

TABLE I

COMPARISON WITH AVAILABLE LOW POWER, LOW VOLTAGE, SAR ADCS IN THE LITERATURE.

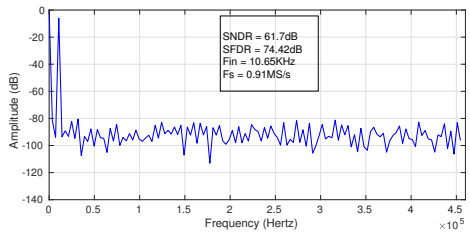

Fig. 10. FFT spectrum of 10 b ADC for an input frequency of 10.65 KHz

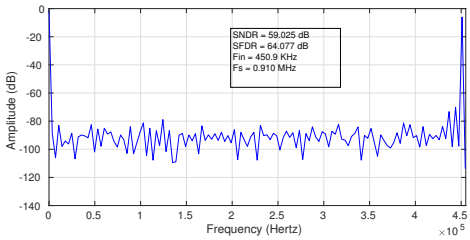

Fig. 11. FFT spectrum of 10 b ADC for an input frequency of 450.9 KHz

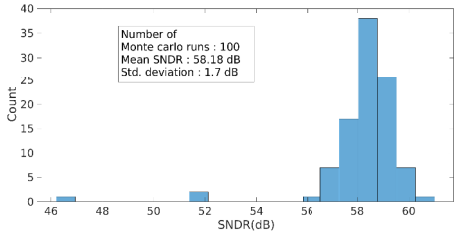

Fig. 12. Mean and sigma SNDR against mismatch in OTA

by OTA. To verify ADC performance against mismatch in OTA, a Monte Carlo simulations of 100 runs are carried on the extracted netlist. Figure 12 shows the histogram plot of SNDR variations. The mean and sigma values of SNDR are 58.18 dB and 1.7 dB respectively. The plot shows the offset voltage correction incorporated in OTA has a great impact on the ADC performance to a large extent. The designed SCI based SAR ADC performance is compared with some of the SAR ADCs in the literature as shown in the Table I. It can be seen that the proposed SAR ADC has the figure of merit (FOM) comparable with some of the SAR ADCs found in the literature. A lower FOM indicates higher power efficiency. Moreover the designed ADC occupies small area compared to few state of art designs.

V. CONCLUSION

An area efficient 10-bit nonbinary weighted SAR ADC is presented. The ADC has SCI DAC implemented with only six unit capacitors and therefore, there is an area advantage over the conventional binary weighted capacitor array architecture. Though the OTA required for the ADC demanded a higher power, with a careful design of OTA, the overall efficiency is maintained on par with the existing 10-bit architectures. The DAC architecture proposed is resolution independent and also parasitic independent to a large extent. The simulation results of the ADC designed in 180 nm CMOS process operating on 1.8 V supply offered an ENOB of 9.9 at near DC and 9.5 at nyquist frequency. The proposed ADC is suitable for modern instrumentation systems and data acquisition systems.

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