A 0.5 V, 1 nA Switched Capacitor PTAT Current Reference Circuit

Hanumantha Rao G.* and Rekha S.†
Dept. of Electronics and Communication Engineering,
National Institute of Technology Karnataka,
Surathkal, India - 575025
Email: *hanu.vnk@gmail.com and †rsbhat_99@yahoo.com

***Abstract*—This paper presents a low voltage, low power Proportional to Absolute Temperature (PTAT) current reference circuit. Switched capacitor is used instead of a large resistor, which in turn reduces the area of the circuit and makes the circuit less process sensitive. The proposed circuit has been designed using UMC 65 nm CMOS technology and simulated in Cadence Virtuoso. It generates a reference current (I_{ref}) of 1 nA at 0.5 V supply voltage (V_{dd}) at room temperature (27°C) and follows PTAT characteristics in the temperature range of -10°C to 80°C. The total power consumption of the circuit is as low as 1.5 nW. The supply voltage sensitivity of I_{ref} is 2.7 %/V, which shows that the proposed circuit is less sensitive to supply voltage variations.**

***Index Terms*—Low voltage, Low power, PTAT current, Switched capacitor**

I. Introduction

As the technology is getting scaled down and the demand for portable or battery operated devices is getting increased, it becomes necessary to operate the circuit under low voltages and currents. Current references are necessary building blocks for biasing analog circuits such as filters, oscillators, phase locked loops, etc. These circuits require a stable current reference that is used to set the operating point. As the circuit performance varies depending upon the operating point, the current reference should be stable enough to be independent of variations in process, supply voltage. Depending on the application, circuits need a temperature independent or Proportional to Absolute Temperature (PTAT) current reference. Sub-threshold (weak-inversion) based log-domain and Transconductance-Capacitor ($G_m - C$) filters are such kind of circuits that require PTAT current reference.

The cutoff frequency (f_o) of the sub-threshold log-domain and $G_m - C$ filters is given by (1) [1], [2].

$$f_o = \frac{G_m}{2\pi C} = \frac{I_o}{2\pi\eta V_T C} \tag{1}$$

where I_o, η and V_T are bias current, sub-threshold slope factor and thermal voltage respectively. Thermal voltage (V_T) is given by

$$V_T = \frac{kT}{q} \tag{2}$$

where k, T and q are Boltzmann constant, absolute temperature and charge of the electron respectively.

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As V_T is directly proportional to temperature, f_o varies with temperature. This variation is more in low frequency filters as the bias current (I_o) required is in the range of nAs. To maintain f_o constant with temperature, I_o must be a PTAT current.

Beta-multiplier based PTAT current reference circuits given in [3]–[5] have good PTAT current characteristics. However, when these circuits are exploited to work with low supply voltages and expected to generate low reference currents of the order of nA, the value of the resistance increases. It occupies large area and also the control over temperature coefficient of resistance is very difficult. Extensive research has been done on the conventional circuit of PTAT to overcome these limitations [6]–[8]. In [8], authors use a self-cascode structure to replace the resistance. Although the supply variation rejection is improved, current versus temperature linear characteristic has been sacrificed. In [1], [9], switched capacitors are used to replace the resistance. In these designs, PTAT voltage is converted to PTAT current by using op-amp based voltage to current converter. However, power dissipation is a major issue in these designs.

In this paper, a PTAT current reference circuit, which uses switched capacitor instead of a large resistor is proposed. The proposed circuit provides good PTAT current characteristics and stability for changes in the supply voltage. It operates with a supply voltage of 0.5 V and consumes less power. The paper is organized as follows. Details of the proposed circuit is given in Section II. Simulation results are explained in Section III. Conclusions are drawn in Section IV.

II. Proposed Circuit

A simple beta-multiplier circuit [5] is shown in Fig. 1. It is generally used as Constant-G_m biasing circuit [5] if all the transistors are operating in strong-inversion saturation region ($V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$). If all the transistors are operating in weak-inversion saturation ($V_{GS} < V_{th}$ and $V_{DS} \geq 3V_T$), it gives a PTAT current as explained later in this Section.

The equation of drain current in weak-inversion region [10] is given as

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}-V_{th}}{\eta V_T}} (1 - e^{\frac{-V_{DS}}{V_T}}) \tag{3}$$

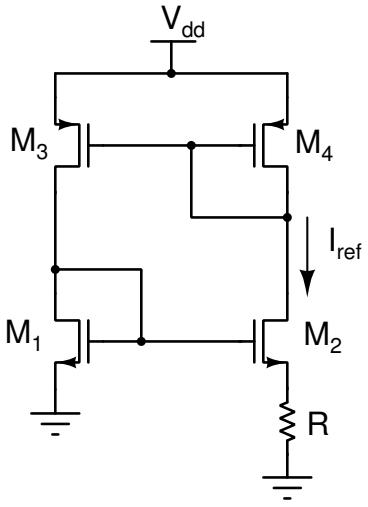

Fig. 1. Beta-multiplier circuit

where $I_{D0} = \mu_n C_{ox}(\eta - 1)V_T^2$; μ_n and C_{ox} are mobility of the electron and capacitance per unit area presented by the gate oxide respectively. Remaining terms have their usual meanings. For $V_{DS} \geq 3V_T$ (weak-inversion saturation region), (3) can be approximated to (4).

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS} - V_{th}}{\eta V_T}} \tag{4}$$

From Fig. 1, V_R (voltage across R) can be expressed as follows.

$$V_R = V_{GS1} - V_{GS2} \tag{5}$$

Using (4), gate-source voltages of M_1 and M_2 can be expressed as in (6) and (7) respectively.

$$V_{GS1} = \eta V_T ln(\frac{I_{D1}}{I_{D0}(\frac{W}{L})_1}) + V_{th1} \tag{6}$$

$$V_{GS2} = \eta V_T ln(\frac{I_{D2}}{I_{D0}(\frac{W}{L})_2}) + V_{th2}^{'} \tag{7}$$

$V_{th2}^{'}$ can be written as in (8) [11] to include the body effect of M_2.

$$V_{th2}^{'} = V_{th2} + (\eta - 1)V_{SB} = V_{th2} + (\eta - 1)(V_R) \tag{8}$$

By substituting (6) and (7) in (5) and by assuming $V_{th1} = V_{th2}$, V_R can be derived as

$$V_R = I_{ref}.R = V_T ln(p) \tag{9}$$

where $p = \frac{(W/L)_2}{(W/L)_1}$.
Therefore, I_{ref} can be written as

$$I_{ref} = \frac{V_T ln(p)}{R} \tag{10}$$

If the resistor, R is assumed to be thermally stable, then I_{ref} is directly proportional to temperature and hence it follows PTAT characteristics.

To design a PTAT current of 1 nA using beta-multiplier circuit shown in Fig. 1, a resistor of 10 MΩ approximately is required for p = 1.5. These large resistors occupy huge area on the chip and also are more process dependent. This limits the accuracy of I_{ref}. In systems where a precise clock frequency is available, the resistor, R in Fig. 1 can be replaced by a switched capacitor equivalent to achieve higher accuracy. The clock can be obtained from the digital circuits as they co-exist with analog circuits in a typical SoC (System-on-chip).

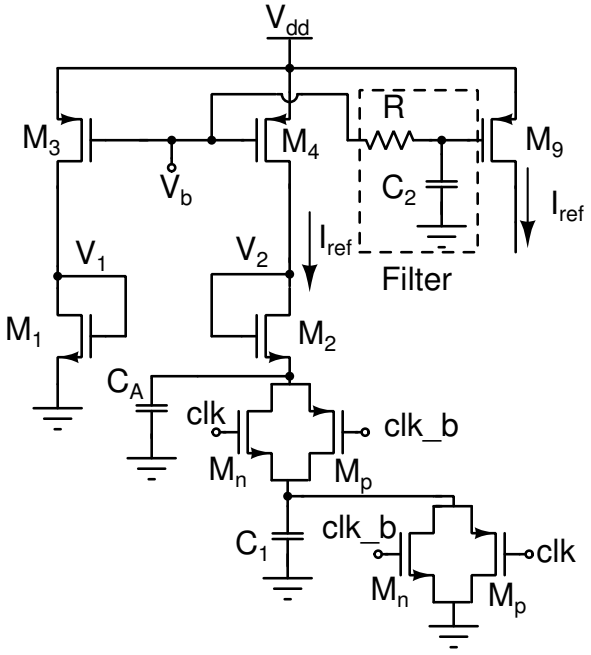

Fig. 2. Proposed PTAT current reference circuit

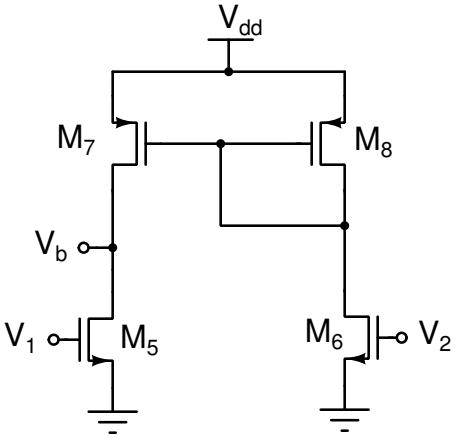

Fig. 3. Error amplifier

The proposed PTAT current reference circuit is shown in Fig. 2. In this circuit, all the transistors are operating in weak-inversion region. The size of M_2 is chosen as 1.5 times the size of M_1 to get p = 1.5. Here, the resistor is replaced by a switched capacitor formed by C_1 and transmission gate

switches (formed by M_n and M_p). The size of M_p is chosen as 4 times the size of M_n to make the on resistance of the transmission gate independent of the voltage across it. Two complementary clocks ('clk' and 'clk_b') of same frequency (f_{clk}) are used for the switching operation. When 'clk' is high ('clk_b' is low), C_1 charges and it discharges when 'clk' is low ('clk_b' is high). The average resistance (R_{eq}) of the switched capacitor is given as in (11) [5].

$$R_{eq} = \frac{1}{f_{clk} C_1} \tag{11}$$

where f_{clk} denotes frequency of the clock used for switching operation.

By substituting R_{eq} (11) in place of R in (10), we get

$$I_{ref} = V_T f_{clk} C_1 ln(p) \tag{12}$$

From (12) it can be seen that, I_{ref} is directly proportional to C_1. For the currents in the range of nAs, the capacitor can be a small value by appropriately choosing f_{clk} and 'p'.

The error amplifier shown in Fig. 3 makes the drain voltages of both M_1 and M_2 equal and hence currents through M1 and M2 are equal. This arrangement will also reduce the dependency of I_{ref} on V_{dd}. The capacitor C_A is used to shunt the high frequency switching noise (ripples) to ground. Additionally, a simple low pass filter formed by R and C_2 is added to remove ripples further in the reference current. The sizes of all the transistors are given in Table I.

TABLE I
SIZES OF THE TRANSISTORS IN FIG. 2 AND FIG. 3

Transistors	W/L (μm/μm)
M_1	4/3
M_2	6/3
M_3, M_4 and M_9	20/3
M_n	1/1
M_p	4/1
M_5, M_6	2/3
M_7, M_8	6/3

f_{clk} is chosen as 100 kHz. The capacitors, C_1, C_2 and C_A are taken as 0.8 pF, 0.1 pF and 10 pF respectively. The resistor, R is taken as 1 kΩ.

By substituting (12) in (1),

$$f_o = \frac{f_{clk} C_1}{2\pi\eta C} ln(p) \tag{13}$$

From (13), it can be seen that f_o is independent of temperature. The process variations in f_o can be reduced by properly laying out the capacitors C_1 and C.

III. SIMULATION RESULTS

The proposed PTAT current reference circuit is designed using UMC 65 nm CMOS process and simulated using Cadence Virtuoso. Periodic steady state (PSS) analysis in Cadence Spectre simulator is used to plot the reference current. A clock frequency of 100 kHz is used throughout the simulations. At $V_{dd} = 0.5$ V and room temperature (27°C), the circuit generates a reference current of 1 nA as shown in Fig. 4. In this figure, the average reference current is plotted for one clock period (10 μs) using PSS analysis.

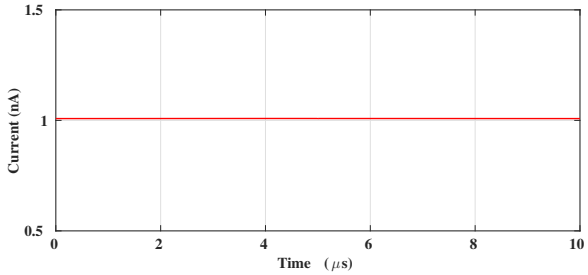

Fig. 4. I_{ref} at V_{dd}= 0.5 V and room temperature

Figure 5 plots I_{ref} with respect to temperature in the range of -10°C to 80°C for V_{dd} = 0.5 V and in 'tt' corner. It can be seen that I_{ref} varies linearly with temperature. Hence, I_{ref} follows a PTAT characteristics.

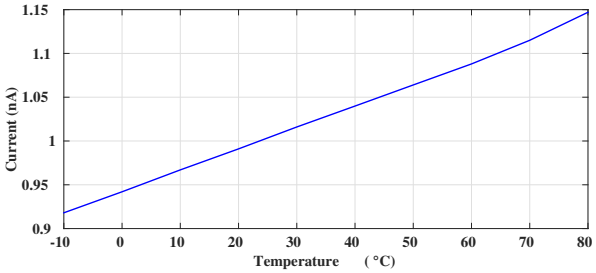

Fig. 5. I_{ref} vs. Temperature plot

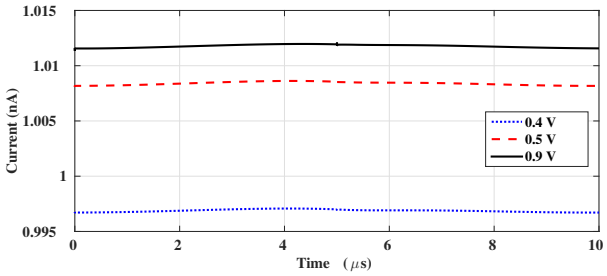

Fig. 6. I_{ref} for different supply voltages

In Fig. 6, I_{ref} is plotted for V_{dd} values of 0.4 V, 0.5 V and 0.9 V at room temperature and in the 'tt' corner. I_{ref} is 0.998 nA and 1.012 nA for 0.4 V and 0.9 V respectively. From the above values, the supply voltage sensitivity of I_{ref} is calculated as 2.7 %/V. The circuit can be operated in a supply voltage range of 0.4 V - 0.9 V. Figure 7 plots I_{ref} in different process corners (ss, ff, tt, fnsp and snfp) at room temperature and V_{dd} = 0.5 V. Maximum deviation of I_{ref} occurs in 'ss' and 'ff' corners. I_{ref} is 1.03 nA and 0.982 nA in 'ss' and 'ff' corners respectively. The maximum deviation is less than $\pm$2.8 %.

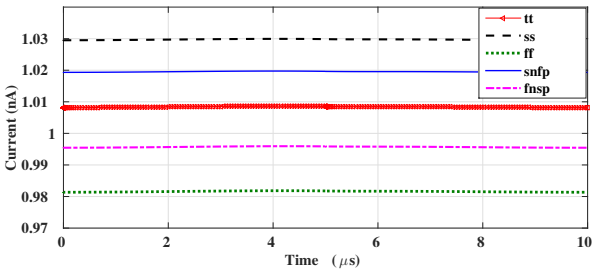

Fig. 7. I_{ref} across the process corners

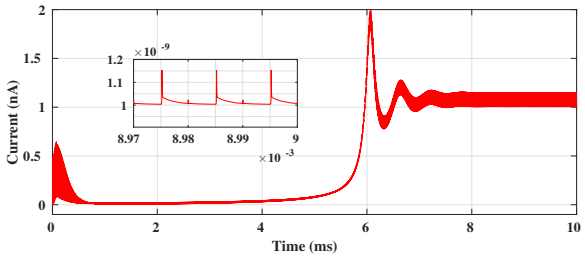

Fig. 8. Transient response of the current at the source of M_2 (Fig. 2)

Figure 8 shows the transient response of the current at the source of M_2. It contains ripples of magnitude about 0.15 nA. The transient response of the ripple free current flowing through M_9 is shown in Fig. 9. The settling time is approximately 8 ms, which can be reduced by adding a start-up circuit to the proposed PTAT circuit.

TABLE II
COMPARISON OF THE PROPOSED WORK WITH OTHER SIMILAR WORKS

Parameter	[8]	[12]	[13]	This work
Technology (μm)	1.5	0.18	0.04	0.065
Supply voltage (V)	1.2	1.2	1	0.5
Reference current (nA)	0.4	6	100	1
Power (nW)	2	–	350	1.5
Supply voltage sensitivity (%/V)	6	6.47	2.9	2.7

The proposed circuit consumes a power of 1.5 nW at room temperature and V_{dd} = 0.5 V. A performance comparison of the proposed circuit with the state-of-the-art PTAT current reference circuits is given in Table II. The proposed PTAT circuit operates with lowest supply voltage and has the lowest supply voltage sensitivity among the papers listed. This circuit

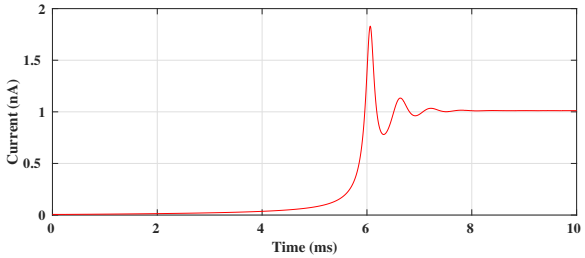

Fig. 9. Transient response of the current flowing through M_9 (Fig. 2)

can be used as a biasing circuit in low voltage, low frequency log-domain and $G_m - C$ filter circuits to make the cutoff frequency of the filter independent of temperature.

IV. Conclusion

In this paper, a low voltage, low power switched capacitor PTAT current reference circuit is proposed. Simulation results show that the proposed circuit provides ultra low power operation, less sensitive to supply voltage variations and can operate at supply voltages down to 0.4 V in UMC 65 nm CMOS technology. The reference current follows PTAT characteristics in the temperature range of -10°C to 80°C. The power consumed by this circuit is as low as 1.5 nW at 0.5 V supply voltage. The proposed PTAT circuit can be used as biasing circuit in low voltage, low frequency log-domain and $G_m - C$ filter circuits.

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