

Transition Metal Oxides Based Devices for Nonvolatile Resistive Random Access Memory Applications

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

STERIN N. S.

Reg. No: 158023; Roll No. PH15F06



DEPARTMENT OF PHYSICS

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA

SURATHKAL, MANGALORE-575025

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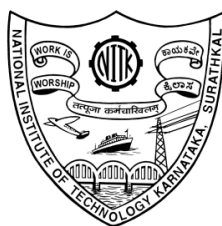
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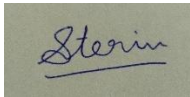
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DECLARATION

By the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled “**Transition Metal Oxides Based Devices for Nonvolatile Resistive Random Access Memory Applications**”, which is being submitted to the *National Institute of Technology, Karnataka, Surathkal* in partial fulfilment of the requirements for the award of the *Degree of Doctor of Philosophy in Physics* is a *bonafide report of the research work carried out by me*. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.



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May 2022

CERTIFICATE

This is to *certify* that the Research Thesis entitled “**Transition Metal Oxides Based Devices for Nonvolatile Resistive Random Access Memory Applications**”, submitted by **STERIN N. S.** (Register Number: 158023PH15F06) as the record of the research work carried out by him, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of *Doctor of Philosophy*.



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Abstract

Resistive-random-access-memory (RRAM) is envisioned as a promising candidate for next-generation memory applications due to its simple structure, non-volatility, and fast switching speed. RRAM – in principle a transistor analogue – is a two-terminal device wherein an active material (in the form of a dielectric thin film of thickness down to few tens of nanometer)) is sandwiched between two conducting electrodes. Sweeping the dc bias voltage between the terminals, the resistance value of such a device can be toggled between two distinct resistance or current levels. Such phenomenon is called resistive switching (RS).

In this work, *firstly*, we have fabricated and tested the RS behavior of non-volatile nature in a number of devices with mainly two architectures: (1) W-tip/Cu_xO/Pt/Ti/SiO₂/Si and (2) Cu-contact-pad/Cu_xO/Pt/Ti/SiO₂/Si. The device type (1) showed coexistence of two bipolar resistive switching modes, commonly known as eight-wise (8w) and counter-eight-wise (c8w), in their current-voltage (*I-V*) characteristics. We report considerably high ON/OFF ratio of 10⁵ and stable retention time 15 × 10³ sec. The formation and annihilation of metallic Cu nanofilaments was argued as the plausible reason behind the observed resistive switching events. The onset of quantized conductance steps in the typical conductance plots (in units of quanta of conductance $2e^2/h$, where e and h are electronic charge and Planck's constant, respectively) – a phenomenon usually observed in narrow conductive channel – was exploited to provide an “indirect” proof for formation of metallic Cu-based filaments or channels during switching. On the contrary, in device type (2), we observed only “regular” bipolar switching. The operating voltage was less than 1 V in both the devices – implying its potential low-power applications. We assessed the underlying conduction mechanism in depth and also using a simple model theoretically estimated the lateral size of the tiny conductive nanofilaments formed during the switching events. Copper being a cost-effective and widely available substance, our results indicate that Cu_xO based cells can be a feasible and useful route for non-volatile resistive memories.

Secondly, we have demonstrated uniform, repetitive and stable RS phenomenon on a low-cost two-terminal metal-insulator-metal stack fabricated using a highly redox-active vanadium based polyoxometalate (POM) molecular clusters, [V₁₀O₂₈]⁶⁻ – belonging to polyoxovanadate (POV) family. The RS was observed to be unipolar and non-volatile in nature, and occurred at a fairly low operating bias voltage (less than 2 volts), making it suitable for low-power operations. We attribute the switching event to the cycling between formation and rupture of tiny conductive nanofilaments formed due to trapping and de-trapping of positively charged

ionized oxygen vacancy sites present in the active switching layer of $[V_{10}O_{28}]^{6-}$. POMs, in their rich abundance, are highly stable early transition metal oxide nanosized clusters, capable of storing as well as releasing a large number of electrons. In addition, they can undergo fast and reversible redox reactions (both in solid and liquid electrolyte media) in “stepwise” manner – a property that makes them a promising candidate for ultra-fast and multi-level non-volatile molecular memory for high-density data storage. Preliminary investigations on our POV based memory cells resulted in device resistance ratio ~ 25 , endurance for more than 200 cycles and stable retention time around 2200 sec, in fully open-air condition.

Thirdly, we have initiated building an array of RRAM cells on indium-tin-oxide (ITO) coated *flexible* polyethylene-terephthalate (PET) substrate. The switching layer was taken as sputter deposited Cu_xO thin film as in the second work described right above. Thermally deposited aluminum dots acted as top contact and ITO as bottom contact. A few preliminary studies on transport properties have been reported in this dissertation. Also, described are the future directions for building robust and stable resistive memory for flexible and wearable electronic circuitry.

Keywords: RRAM, Resistive switching, Polyoxometalate, Copper oxide, Quantized conductance, Flexible memory.

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Nomenclature

Symbol	Description
M	Metal
M^{z+}	Metal cation
O_l^{--}	Oxygen ion at the anion lattice position
$V_A^{\cdot\cdot}$	Doubly ionized oxygen vacancy
e	Charge of electron
V_A^{\cdot}	Singly ionized oxygen vacancy
V_A	Unionized oxygen vacancy
A^*	Richardson constant
J	Current density
V	Voltage
Φ_b	Energy barrier height
ϵ_r	Dielectric constant
ϵ_0	Permittivity of vacuum space
d	Film thickness
k	Boltzmann's constant
T	Absolute temperature
m_o	Free electron mass
m^*	Effective mass of electron
h	Planck's constant
E	Electric field across the dielectric
θ	Ratio of free carrier density to total carrier density
E_t	Trap energy level
g_n	Degeneracy of the energy state in the conduction band

N_t	Concentration of trap centres
N_c	Density of states in the conduction band
μ	Electronic mobility
n	Free carrier density in the insulator matrix
n_0	Thermally generated free electrons
τ_d	Dielectric relaxation time
τ_c	Carrier transit time
ν	Frequency of incident X-ray photon
E_k	Kinetic energy of the photoelectrons
E_b	Binding energy
G	Electrical conductance
I	Current
I_{cc}	Compliance current
μ_O^0	Standard chemical potential of oxygen
R	Gas constant
p	Oxygen partial pressure
p^0	Standard pressure of 1 atm
F	Faraday constant
φ	Electrostatic potential.
Φ_a	Activation energy
Φ_a'	Bias-dependent activation energy
λ	Jump length for the oxygen anions (O_2^-)

List of abbreviations

Abbreviation	Full form
NVM	Non-volatile memory
DRAM	Dynamic-random-access-memory
SRAM	Static-random-access-memory
FeRAM	Ferroelectric-random-access-memory
PCRAM	Phase-change-random-access-memory
RRAM	Resistive-random-access-memory
ITRS	International Technology Roadmap for Semiconductors
RAM	Random-access-memory
ROM	Read-only memory
CMOS	Complementary-metal-oxide-semiconductor
RS	Resistive switching
M-I-M	Metal-insulator-metal
HRS	High-resistance-state
LRS	Low-resistance-state
ECM	Electrochemical metallization
VCM	Valence change mechanism
MIS	Metal-insulator-semiconductor
SCLC	Space-charge-limited-current
OV	Oxygen vacancy
POM	Polyoxometalate
8w	8 wise
c8w	counter 8 wise

CRS	Complementary resistive switching
<i>I-V</i>	Current-Voltage
BRS	Bipolar resistive switching
TE	Top electrode
BE	Bottom electrode
QPC	Quantum point contact
POV	Polyoxovanadate
SDV	Sodium decavanadate
ITO	Indium-tin-oxide
PEN	Polyethylene-naphthalate
PET	Polyethylene-terephthalate
F-N	Fowler-Nordheim

CHAPTER 1

INTRODUCTION

Overview: This chapter gives a brief introduction to the existing memory technologies in general and RRAM in particular. Different aspects of RRAM have been discussed. Also, discussed in a nutshell are the advantages of using RRAM over FLASH, FERAM, PCRAM, etc. Extensive literature survey on different RRAM studies have also been included in this chapter. Finally, we provide with the scope and objectives followed by organization of this dissertation.

1.1. Introduction

The sequential acts of sensing, interpreting/processing and acting can be seen as the foundation of all information processing techniques. These activities cannot be carried out unless the item of interest is remembered (which is commonly known as *non-volatility*) for long enough time for the required operations to be carried out. Based on the principle of functioning, the memories, in general, can be sub-divided into two categories – *volatile* and *nonvolatile*. Non-volatile memories (NVMs) have the ability to preserve its contents even when the external power is turned off (e.g., flash memory). In contrast, volatile memories (e.g., dynamic-random-access-memory (DRAM) and static-random-access-memory (SRAM)) need a constant power source to remember the state, and they lose the stored data when power goes off. Rapid miniaturization of today’s omnipresent charge-based memory devices such as DRAM and flash-memory have resulted in many technological and physical limitations: excessive power consumption, high fabrication cost, low programming speed and the approach of the tunnel limit for the source-drain current (ITRS 2013). Significant progress, both in theory (Dirkmann et al. 2018) as well as in experiments (Waser 2012), has been made in recent years to realize this objective. The quest for realizing the fundamental limit in complementary-metal-oxide-semiconductor (CMOS) based electronics has pushed physicists and engineers to address those obvious limitations – further miniaturization (difficulty in achieving length scales sub 20 nm), high operating voltage (~ 12 V), low endurance ($< 10^6$) and low programming speed (μ s to write and ms to erase), among others (ITRS 2013) (Lee 2017). The reportedly increasing interest for realizing next generation NVMs is perceived to have overcome some of those

bottlenecks (Wong and Salahuddin 2015) (Banerjee 2020). There is an urgent need for an appropriate, non-charge-based memory technology to find a suitable alternative in order to go beyond von Neumann computing (Lee et al. 2020a). Ferroelectric-random-access-memory (FeRAM) (Lin et al. 2020), phase-change-random-access-memory (PCRAM) (Jiao et al. 2020) and resistive-random-access-memory (RRAM) (Zahoor et al. 2020) (Das et al. 2020) are the prominent emerging memory technologies.

Historically, integrated circuit (IC) technology has increased functional density exponentially. Gordon Moore first predicted in 1965 that the number of transistors per microchip in computer architecture would double every year. He revised his prediction 10 years later and said that this number would double every two years. This has been popularly called Moore's law. However, in recent times the pace has slowed down and many, therefore, say that we have reached the end of Moore's law or prediction. The International Technology Roadmap for Semiconductors (ITRS) has been driven by this so-called Moore's law (Moore 1975). At every three years of interval, the semiconductor device industry advances by technological growth, with new generation of product lines, referred to as a technology node, resulting in miniaturization of feature size (F) 0.7 times smaller than that of the previous generation (Ogirima 1993) (Schulz 2012). Data for five nodes included in the ITRS were: Year 2004 (90 nm), 2007 (65 nm), 2010 (45 nm) and 2013 (32 nm) (ITRS 2013). Semiconductor memories are broadly classified as random access memories (RAMs) and read-only memories (ROMs). The writing and reading times are faster in RAM than those in ROM. In year 1966, Dr. Robert Dennard of IBM's Thomas J. Watson Research Center invented dynamic RAM (DRAM), or field-effect transistor memory (Klein 2016). It was the low-cost memory with high-performance characteristics which was required to find its way into computing systems. Structurally, DRAM is one transistor and one capacitor (1T1C) per cell. DRAM is a volatile technology that keeps information with charge stored on a capacitor. A logic ONE can be represented by charge levels greater than a certain threshold amount, while a logic ZERO can be represented by charge levels less than another threshold amount. In the presence of natural noise levels, the two critical levels are chosen to ensure an unambiguous understanding of logic ZERO

or ONE. (The higher charge level is referred to as logic ONE in this case. However, the definition of ONE or ZERO is arbitrary). The second candidate ROM also faces many limitations in terms of storage capacity, speed, number of write/erase cycle. ROMs are classified as One-Time Programmable ROM (OTPROM), Erasable Programmable ROM (EPROM), Ultraviolet EPROM (UVEPROM), Electrically Erasable Programmable ROM (EEPROM), as shown in the flow chart of Figure 1.1 (Jeong et al. 2012). It is important to note that all those aforementioned memory technologies possess inherent shortcomings such as scaling, low-memory density, volatility, low retention and poor endurance (Lee 2017).

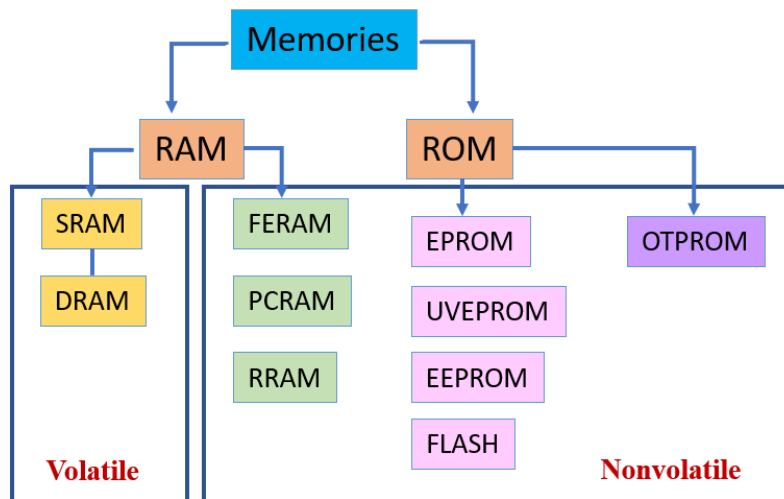


Figure 1.1 Categories of conventional memories and emerging memories.

1.2 Different types of NVMs

As already explained above, NVMs are capable of storing data even when the memory cells are kept in powered-off condition. This is an important aspect for realizing energy-efficient electronics and high-performance computing. It can thereby reduce the weight and increase the performance speed of portable personal electronic devices such as laptops, mobile phones and other wearable gadgets. Therefore, NVM cells are presently being subject of intense research both in academia as well as in industry. Examples of NVMs

include FLASH memory. Forthcoming prominent NVM technologies include FeRAM (Lin et al. 2020), PCRAM (Jiao et al. 2020) and RRAM (Zahoor et al. 2020) (Das et al. 2020).

1.2.1 FLASH memory

Masuoka *et al.* of Toshiba proposed the first modern FLASH EEPROM at the IEEE International Electron Devices Meeting held in year 1984 (Masuoka et al. 1987). The word FLASH was coined to describe how easily the entire memory array could be erased. This labeling is used to describe all EEPROM devices that delete a block or a page of data at the same time. A memory array stacked with a large number of FLASH cells makes up a FLASH memory architecture. A basic FLASH memory cell is made up of a storage transistor with a floating gate and a control gate which are separated from the rest of the transistor by a thin dielectric or oxide layer. The electrical charge is stored in the floating gate, which regulates the flow of current in the cell, as shown in figure 1.2. To change the threshold voltage of the storage transistor, electrons can be added or removed from the floating gate. Changing the voltage has an impact on whether a cell is programmed as ONE or ZERO (Luo 2019).

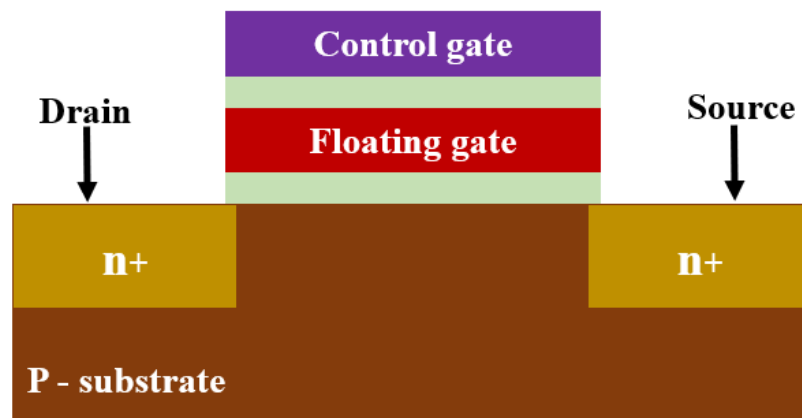


Figure 1.2 Schematic diagram of FLASH memory cell.

The evolution of FLASH is a fascinating example of how engineers could tackle the scaling problem in novel ways. Although improved lithographic capability has become available with each generation of technology in last several decades, further

miniaturization of the fundamental portion of a FLASH memory (which actually stores charge) appears challenging. Engineers put on efforts on locating and reducing the amount of space devoted to non-memory components of the array (e.g., contacts, separation between cells, etc.). Introduction of multibit cell was a key strategy in the battle to keep the area per bit low (Sugizaki et al. 2003). FLASH memories are used as secondary storage media because of their long write/erase time (1 ms/0.1 ms) and higher capacity. The need for permanent data storage was fulfilled so far by the CMOS FLASH memory. However, FLASH memory encounters many limitations such as low retention, low endurance, and the high operating voltage (5V), making it undesirable to consider it a future memory storage device, as shown in the Table 1.1. To keep scaling on this evolutionary course new structures and materials along with new processes must be created. Quest for realizing novel memory device with simple cost-effective structure, low power consumption, high speed, long retention, high endurance, high scalability, high data storage density and compatibility with existing CMOS technology (Meena et al. 2014) (Lee et al. 2020a) (Banerjee 2020) is still underway.

Table 1.1 provides comparative study between existing memory and upcoming prototype memory technology.

		Baseline technologies					Prototypical technologies		
		DRAM		SRAM	FLASH		FeRAM	PCRAM	RRAM
		Stand-alone	Embedded		NOR	NAND			
<i>Storage mechanism</i>		Charge on a capacitor		Inter-locked state of logic gates	Charge trapped in floating gate or in gate insulator		Remnant polarization on a ferroelectric capacitor	Reversibly changing amorphous and crystalline phases	Nano-filament formation
<i>Feature size F, nm</i>	2013	36	65	45	45	16	180	45	5 nm
	2026	9	20	10	25	>10	65	8	< 5nm
<i>Cell Area</i>	2013	6F ²	(12-30)F ²	140F ²	10F ²	4F ²	22F ²	4F ²	4F ²
	2026	4F ²	(12-50)F ²	140F ²	10F ²	4F ²	12F ²	4F ²	4F ²
<i>Read Time</i>	2013	<10 ns	2 ns	0.2 ns	15 ns	0.1 ms	40 ns	12 ns	---
	2026	<10 ns	1 ns	70 ps	8 ns	0.1 ms	<20 ns	<10 ns	---
<i>W/E Time</i>	2013	<10 ns	2 ns	0.2 ns	1 us/10ms	1/0.1 ms	65 ns	100 ns	10 ns
	2026	<10 ns	1 ns	70 ps	1 us/10ms	1/0.1 ms	<10 ns	<50 ns	<10 ns
<i>Retention Time</i>	2013	64 ms	4 ms	---	10 yr	10 yr	10 yr	>10 yr	10 yr
	2026	64 ms	1 ms	---	10 yr	10 yr	10 yr	>10 yr	>10 yr
<i>Write Cycles</i>	2013	>1E16	>1E16	>1E16	1E5	1E5	1E14	1E9	1E12
	2026	>1E16	>1E16	>1E16	1E5	1E5	>1E15	1E9	>1E12
<i>Write Operating Voltage (V)</i>	2013	2.5	2.5	1	8-10	15-20	1.3-3.3	3	<1
	2026	1.5	1.5	0.7	8	15	0.7-1.5	<3	<0.5
<i>Read Operating Voltage (V)</i>	2013	1.8	1.7	1	4.5	4.5	1.3-3.3	1.2	0.1 – 0.2
	2026	1.5	1.5	0.7	4.5	4.5	0.7-1.5	<1	0.1

Table 1.1 Details of current baseline and future prototypical memory technologies (ITRS 2013: <http://www.itrs2.net>).

1.2.2 Other emerging NVMs

Present-day solid-state memories (SRAM, DRAM, FLASH memory) are built following the traditional transistor microfabrication process flow. As the scaling of transistor is becoming slower and slower, the semiconductor fraternity is in quest of some promising *non-transistor* based memory technologies which can potentially replace the existing trend (Meena et al. 2014). FeRAM, PCRAM and RRAM are a few examples in that respect (Banerjee 2020). Below we briefly outline them.

(a) Ferroelectric-Random-Access-Memory (FeRAM)

FeRAM is a prototype NVM with a ferroelectric layer-based capacitor. It stores information as an electric polarization state of the ferroelectric material (Shin and Son 2018). The changes in the polarization of ferroelectric materials under high electric field condition ($E > E_c$, E_c : coercive field) are hysteretic in nature (Park et al. 2018a). The polarization state will be memorized by the dipoles within the ferroelectric capacitor even after the removal of the field. The two distinguishable polarization states can be denoted as binary 0 or 1. FeRAM is highly non-volatile in nature compared with DRAM and it can hold the stored information for up to 10 years with an endurance of 10^{14} cycles. Relative to FLASH memory it offers low power consumption (3.3 V to write and 1.5 V to read) and fast write speed (65 ns) (ITRS 2013). However, despite several superior qualities, FeRAM has scalability issue. Unlike DRAM and FLASH memory, it stores less data in the same space leading to need of a large memory cell area for enhanced data storage.

(b) Phase-Change-Random-Access-Memory (PCRAM)

PCRAM is one of the emerging non-volatile memory technologies in which a chalcogenide glass is sandwiched between two electrodes. The reversible transition between crystalline and amorphous phases of chalcogenide material brings change in the resistivity. The transition from the high-resistive amorphous phase to the low-resistive crystalline phase is called SET switching and the reverse transition from crystalline to amorphous phase is called RESET switching. The pristine PCRAM device will be in the

crystalline phase due to the high processing temperature. Under the application of an external current pulse the PCRAM will reset into the high-resistive amorphous phase (Shen et al. 2019). To set the PCRAM back into low-resistive crystalline phase, an electric pulse (to achieve a temperature between crystallization and melting temperature) is applied. PCRAM is faster than FLASH memory with an operating speed of 100 ns. It possesses long retention (>10 years) and good endurance (10^9) at small dimensions (ITRS 2013).

1.3 Why do we need Resistive-Random-Access-Memory (RRAM)?

Charge-based memories, such as DRAM and FLASH memory will suffer from performance degradation as the scaling limit is approached (Waser 2012). As devices are scaled down, charge-storage-based methods must be able to reliably store only a few electrons over several years. Among all other possible alternatives, the RRAM is considered to be very useful due to its remarkable features such as excellent scalability, low operational voltage (< 3 V), high endurance, simple structure, ease of fabrication and process compatibility with existing CMOS (Waser et al. 2009) (Lee et al. 2020)

In contrast to charge-based memories, RRAM devices use more stable and durable methods of maintaining their states (Kwon et al. 2010) (Waser et al. 2009). Although resistive switching phenomena were observed more than four decades ago (Hickmott 1962) (Hickmott 1965) (Chopra 1965) (Argall 1968) (Dearnaley et al. 1970), current research on resistive switching only started after year 2000. Intensive research on RRAM began after the introduction of NiO memory cells integrated with conventional CMOS in a one-transistor, one-resistor (1T1R) device structure in 2004 by Samsung Electronics Ltd (Baek et al. 2004).

RRAM works based on the principle of resistive switching (RS) wherein the resistance of the device can be toggled between different and distinct states. The pioneering study on RS event was conducted in 1960s by Hickmott (Hickmott 1962) by studying the (negative) resistance changes of aluminum oxide film interposed between two metal electrodes. There

was no noticeable breakthrough research in the following two decades. Only recently (post 2000s), research on RS driven devices has received fresh impetus – mostly with a view to realizing high performance NVMs (Jeong et al. 2012). The memory cells that work based on this phenomenon of RS is termed as *resistive memory* or *resistive-random-access-memory*, popularly known as RRAM (Waser et al. 2009).

Unlike conventional MOS transistors, RRAM is a two-terminal device. A thin layer of oxide (typically a few tens of nm thick) material is sandwiched between two metal contacts. In addition, RRAM is capable of modulating and retaining its internal state variable(s) on demand (Zidan et al. 2018) (Prezioso et al. 2015). Ability to form 3D stacking has made RRAMs an effective tool for extremely high-density data storage applications (Hou et al. 2019). The operational parameters shown in the Table 1.2 confirm that RRAM can be considered as a potential candidate for future memory technology.

		Electrochemical Metallization Bridge	Metal Oxide: Bipolar Filament	Metal Oxide: Unipolar Filament	Metal Oxide: Bipolar Nonfilamentary
<i>Storage mechanism</i>		Electrochemical filament formation	Valence change filament formation	Thermochemical effect filament formation	Change in tunneling characteristics at or near the interface
<i>Feature size F, nm</i>	Best projected	<5 nm	<5 nm	not available	<10 nm
	Demonstrated	20 nm (GeSe), 30 nm (CuS)	5 nm	35 nm	40 nm
<i>Cell Area</i>	Best projected	4F ²	4F ²	4F ²	4F ²
	Demonstrated	4F ²	4F ²	4F ²	4F ²
<i>Read current (HRS/LRS)</i>	Best projected	not available	not available	not available	not available
	Demonstrated	not available	~ 100 pA/~10 nA	1 nA/20 nA	<100 nA
<i>Write/erase time</i>	Best projected	<1 ns	<1 ns	not available	< 10 ns
	Demonstrated	<1 ns	<1ns	10 ns	10 ns
<i>Retention Time</i>	Best projected	>10 yr	>10 yr	>10 yr	>10 yr
	Demonstrated	>10yr	>10 yr	>10 yr	4hr
<i>Write Cycles</i>	Best projected	>10 ¹¹	>10 ¹²	not available	>10 ⁶
	Demonstrated	10 ¹⁰	10 ¹²	10 ⁶	10 ⁶
<i>Write Operating Voltage (V)</i>	Best projected	<0.5 V	<1 V	not available	not available
	Demonstrated	0.6 V	1-3 V	1-3 V	2 V
<i>Read Operating Voltage (V)</i>	Best projected	<0.2 V	0.1 V	not available	0.1 V
	Demonstrated	0.2 V	0.1-0.2 V	0.4 V	0.5 V
<i>Key advantages</i>		-Scalability -Endurance -Speed -Low energy operation	-Scalability -Endurance -Speed -CMOS compatibility	-High ROFF\RON ratio	-Uniform switching -Adjustable current -No forming -Nonlinearity in both states
<i>Key research challenges</i>		-Operation and reliability model development -Random telegraph noise (RTN) -Improved memory controller design -CMOS processing compatibility -Select device	-Need better understanding of detailed physical mechanisms - Random telegraph noise (RTN) -Improved reliability and uniformity -Select device	-Lower erase current/energy -Detailed understanding of physical mechanisms - Improved reliability and uniformity -Select device	-Improved retention -Need better understanding of detailed physical mechanisms - Improved reliability and uniformity -Select device

Table 1.2 Details of RRAM performance parameters, demonstrated and projected values (ITRS 2013: <http://www.itrs2.net>).

1.4 Basic working principle of RRAM cell

RRAM is a two-terminal device with capacitor geometry having metal-insulator-metal (M-I-M) structure. A schematic diagram of RRAM device is shown in Figure 1.3. An active dielectric material (or solid electrolyte in form of thin film) is sandwiched between two conducting electrodes. The initial resistance of the pristine insulator will be a high value. To activate the RS, a pretreatment process is necessary which will switch the device from a high-resistance state (HRS) to a low-resistance state (LRS). This process is called electroforming. Electroforming can be done by applying a voltage between the two metal contacts. This high voltage initiates the forming of the conductive filament leading to the decrease in resistance of the matrix with several orders of magnitude. The sudden drop in resistance surges the current to a high value; this high dissipation of power may result in the permanent breakdown of the dielectric. A current compliance value should be set to avoid a permanent breakdown. Many commercial voltage sources provide a current limiting technique called the current compliance function, by limiting the current to a particular value. Thereby, one can save the device from permanent breakdown. The electroforming process is needed to bring the device to the switching regime, called as mild breakdown. There is no widely accepted theory in deciding the thickness or other properties of dielectric and the requirement of electroforming. Applying an electric field between the terminals (or electrodes), the electrical resistance of the device can be alternately switched between a high resistance state (HRS) and a low resistance state (LRS). They can be assigned to binary “0” and “1” levels, respectively. Switching event from HRS to LRS (device OFF → device ON) is known as SET process and that from LRS to HRS (device ON → device OFF) is known as RESET process. Based on the dielectric material and the type of switching, the set and reset voltages can be higher or lower and can be of positive or negative polarity. Situations wherein SET and RESET happen in the same polarity of bias voltage are called “unipolar” RS (Mukherjee 2019). If SET and RESET happen in opposite bias polarity, the switching is named “bipolar” RS (Xu et al. 2008). A compliance current (generally a few mA) is needed (when the device ramps up from HRS to LRS) to prevent complete dielectric breakdown of the switching dielectric medium as considerably

high electric current flows through the device at LRS. It is important to note that both unipolar and bipolar switching events are *nonvolatile* in nature owing to the fact that even after removing the applied bias the resistance values will remain at whichever state it was set to.

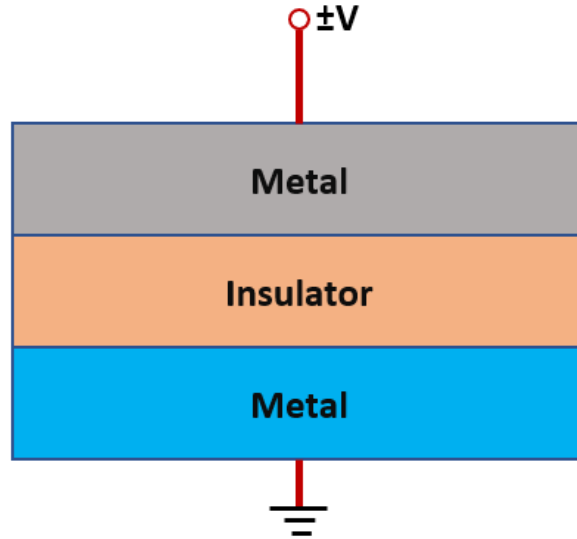


Figure 1.3 Schematic representation of Metal-Insulator-Metal device used for RRAM applications.

(a) Unipolar resistive switching

In unipolar RS, the direction of switching is dependent on only the amplitude of the applied bias. Therefore, the SET and RESET happen at the same polarity of applied electric stimuli (or bias), as shown in Figure 1.4. Mostly, unipolar switching is theorized taking help of the so-called *filamentary model*, where the RESET occurs due to Joule heating in the filament (Zhang et al. 2020). Unipolar switching behavior have been reported in mostly binary transition metal oxides (TMOs), such as TiO_2 (Yoon et al. 2012), Ta_2O_5 (Sahu et al. 2017), HfO_2 (Lee et al. 2013), CoO (Wang et al. 2010), NiO (Ahn and Son 2021), SrTiO_3 (Thakre and Kumar 2018), etc.

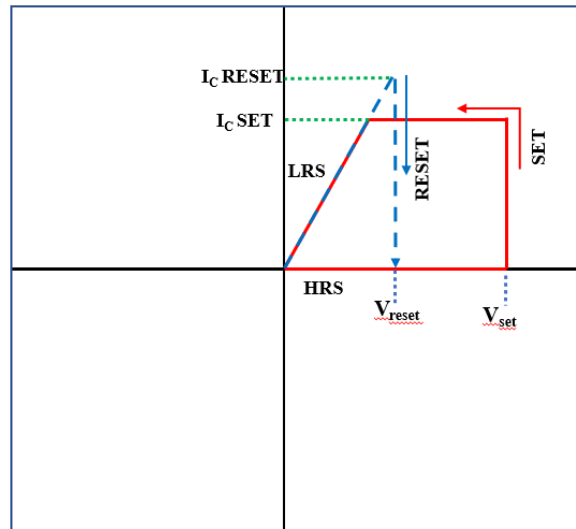


Figure 1.4 Unipolar resistive switching.

(b) Bipolar resistive switching

Unlike the previous case, bipolar switching is characterized by the change in switching direction as a function of change in polarity of the applied electric bias voltage. This makes SET and RESET to occur at opposite voltage polarities, as shown in Figure 1.5. Bipolar RS has been observed in memory cells made of both TMOs (such as WO_x (Hsu et al. 2021), Al_2O_3 (Sokolov et al. 2017) and a few inorganic perovskites (such as SrZrO_3 (Hyun et al. 2021)).

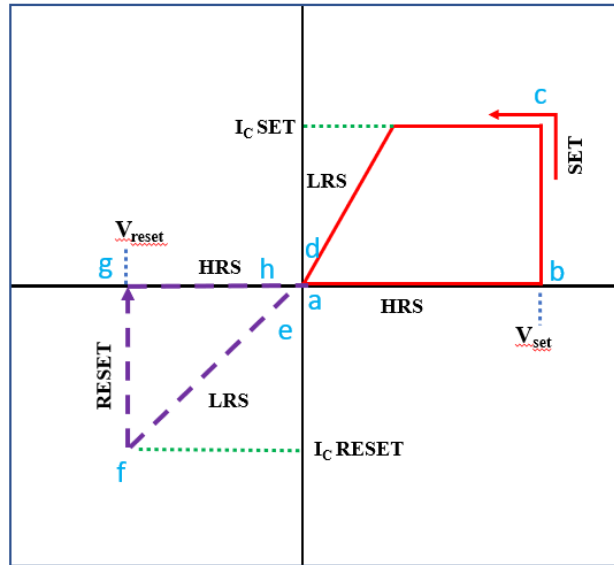


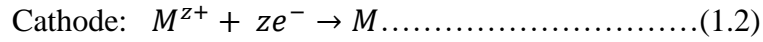
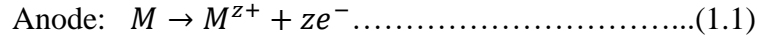
Figure 1.5 Bipolar resistive switching.

Memory cells are broadly classified as electrochemical metallization cell (ECM) and valence change mechanism (VCM).

1.5 Electrochemical metallization (ECM) cell

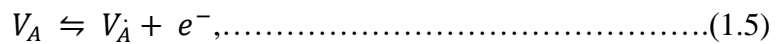
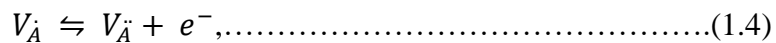
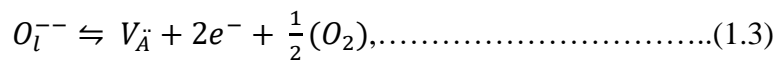
The ECM memory cells are fabricated using an active electrode (M) such as Ag, Cu, Ni, and an inactive counter electrode of Pt, W, Au with a thin film in between. A positive electrode (anode) acts as an ion source that maintains charge neutrality in the oxide matrix. Most devices have the structure in the form of a solid electrolyte between ion supplying anode and electron supplying cathode. When an electric field is applied to the active electrode, the metal undergoes anodic dissolution and form metal ion (M^{z+}). Under the influence of a high electric field, the metal cation drifts toward the counter electrode across the solid electrolyte, which undergoes reduction and electrocrystallization at the electrode and forms M . This cathodic deposition reaction deposits the metal atoms and grow towards the active electrode. Due to the formation of metal nanofilament, the resistance of the solid matrix changes to a low resistance value. The cell retains its low resistance state until a

sufficient voltage of opposite polarity is applied (Menzel et al. 2015). The cathodic and anodic reaction can be represented as: (Lee et al. 2015a)



1.6 Valence change mechanism (VCM)

The VCM cells consist of a metal electrode of high work function, which forms a Schottky interface with the dielectric layer on one face and another counter electrode that makes ohmic interface with the same dielectric layer on the other face. The resistive switching in the VCM cells relies on the redox reaction in the cation sublattice due to the formation of oxygen vacancies (ions). Hence, the local conductivity of the oxide matrix will on application of electric stimuli. The oxygen vacancy formation occurs at the electrode-insulator interface and it alters the electrostatic potential barrier (due to Schottky effect) locally. The generation and movement of oxygen vacancies may lead to the transformation of the phase of the active dielectric matrix. In VCM cells, an electroforming process is required to initiate the redox process. During the forming process, oxygen was extracted from the oxide matrix by leaving the oxygen vacancies behind. This oxidation reaction causes a reduction reaction in the cation sublattice through the change of valence state. In the presence of an electric field, the oxygen vacancies migrate towards the cathode interface and accumulate there. The oxygen vacancies migrate in the direction of the electric field, and the filament grows towards the anode electrode. The formation of oxygen vacancies ca be expressed as: (Lee et al. 2015a) (Menzel et al. 2015)



where O_i^{--} is an oxygen ion at the anion lattice position, e^- is conduction electron, V_A^{--} is a doubly ionized oxygen vacancy, V_A^- is a singly ionized oxygen vacancy, V_A is unionized oxygen vacancy, and $\frac{1}{2}(O_2)$ is the atom of an oxygen ion in the ambient gas.

1.7 Device performance metrics

Any memory technology is judged by a few important device performance metrics. A few important performance metrics of RRAM are: operating speed, operating voltage, endurance, retention time, resistance ratio or memory window, present and future scaling trends, and device yield.

(a) Operating speed

By examining the RRAM device response (e.g., voltage or current via the device structure) to applied electric stimuli with the help of an oscilloscope, switching speed can be measured. It is important to separate the intrinsic device speed from parasitic RC delays in the device structure. The dependence of switching yield on applied electric pulse width can be obtained by array testing. The operating speed is defined by the shortest pulse for the minimum acceptable switching yield.

(b) Operating voltage

A device operating at high voltage is generally unwanted in any technological application. This causes high power consumption, heat dissipation, and reliability issues. The issues relating to high-power consumption faced by FLASH memory can be overcome only when RRAM programming and erasing voltage is less than few volts (preferably around 1 V or less).

(c) Endurance and retention

The usefulness of a memory cell is determined on its ability to retrieve its stored information (or internal state variables) in either non-volatile or quasi-stable manner. The particular internal state can be resistivity, polarization, degree of magnetization, optical transmission, electrical permittivity, or some other properties. Such internal states can be

controllably tailored applying electric, magnetic, thermal, optical, or some other stimuli. It is noteworthy that the degree to which a device can be considered nonvolatile cannot be defined precisely. Though we may be able to play with the internal state of a memory cell with a great deal of precision between two extremes, yet it will be of very little utility should the intermediate states are not clearly distinguishable. This amounts to the need of maximization of the range between the internal state extrema. This is the way forward to realize greater distinguishability between intermediate states. A memory cell can no longer be called non-volatile if its intermediate states fluctuate or degrade significantly over time in absence of the stimulus. The duration for which the internal states of the cell remain stable and distinguishable is known as the *retention time*. Retention is normally a function of temperature and it goes down with increase of temperature. Another important performance parameter is the *endurance*. Endurance is defined as the highest number of switching cycles a device can go through before its electrical properties start to deviate outside of the permitted limits (commonly referred to as the operation window). One operating cycle in resistive memory consists of one set and one reset transition. Maximizing both endurance and retention time is paramount to device performance. RRAMs should reach endurance cycles between 10^4 and 10^7 to compete with present FLASH memories (Waser et al. 2009). FLASH has the potential to offer over ten years of retention time, so the RRAM should also possess the same.

(d) Resistance ratio (or memory window)

Resistance ratio is also known as “memory window”. This is a very important parameter of RRAMs since it is direct measure of how precisely programming or erasing can be done. HRS and LRS levels must be distinguishable enough in order for successful programming which requires a resistance ratio more than at least 10 times (Waser et al. 2009). More than 10^6 to 10^7 memory window has been demonstrated so far (Sharma et al. 2015).

(e) Scaling trends

The attractive feature of oxide-based RRAMs is its potential scalability to the nanometer regime. The size of conductive filaments formed during switching event can be as low as 10 nm. Therefore, in principle, one can expect to scale down feature size of RRAM cells down to sub-10 nm dimensions. In recent years, metal-oxide-based RRAM devices with sub-100 nm feature size have been fabricated using optical lithography (Nio et al. 2009), nanoimprint lithography (Yang et al. 2008) and e-beam lithography (Niu et al. 2016).

(f) Device yield

In general, most of the materials used in RRAM are nonstoichiometric oxides. Such devices show low yield owing to the challenge in controlling the oxygen concentration. The methods proposed to increase the device yield are: (a) using stoichiometric oxides, (b) using suitable electrode material, (c) utilizing doping techniques and (d) introducing metal nanocrystals (Wang and Yan 2019).

1.8 Resistive switching mechanisms

The working mechanisms of the RRAM devices are divergent and not yet clearly understood. Various models have been proposed to explain the behavior of RS events. Among those, the concept of the formation/rupture of conductive filaments (CFs), commonly known as the “filament model” has been widely explored. Some other prominent transport models which can be verified using current-voltage (I-V) curve fitting are space charge-limited current (SCLC) (Guo et al. 2015), Schottky emission (Bai et al. 2014) and Poole-Frenkel emission (Lee et al. 2015). We briefly elucidate each of these models below.

1.8.1 Formation and rupture of conductive nanofilament

A few commonly exploited mechanisms for RS in RRAMs can be listed as: the formation and rupture (or dissolution) of conductive nanofilaments inside the functional oxide layer, charge trap/detrapping (Yu et al. 2011), and oxygen vacancy migration (Menzel et al. 2015). Formation and dissolution of the nanometer-size conductive channels are of two types: electrochemical and thermochemical effects (Wang and Yan 2019). In the thermochemical effect, the rupture of conductive filaments (CFs) is connected with Joule heating. As a result of injection of the electrons, reaction takes place between the conducting electrode material and the dielectric thin film. This results in gradual onset of tiny CFs made of aligned defects, which can be either the oxygen vacancies (OVs) or the electrode metal ions transported into the insulating oxide film. For the SET process, the electrons will be trapped by the defects in the oxide film (on application of electric field), and those tiny conductive channels (current paths) are formed. The RESET voltage induces a high current in those as-formed filaments and causes severe heating in them, and as a result, the filaments rupture. The device comes to the HRS. In the electrochemical switching mechanism, the CFs are created by the redox reactions in solid-state electrolytes. In this case, an oxidizing anode (such as Ag or Cu) and an inert cathode (such as Pt or W) are used (Tappertzhofen et al. 2011) (Du et al. 2016). When a positive voltage is applied to the anode, chemical reactions oxidize the metal atoms into cations. As these cations are highly mobile particles, they speed through the ion conductive layer to the inert cathode, where they will get reduced to metal atoms. CFs are formed with that process and the device switches to LRS. Upon changing the bias polarity, the electrochemical conductive bridge will rupture and finally reset the device back to HRS. This gives us one complete sweep. The bipolar switching mechanism is often attributed to this mechanism (Lee et al. 2015) (Waser et al. 2009).

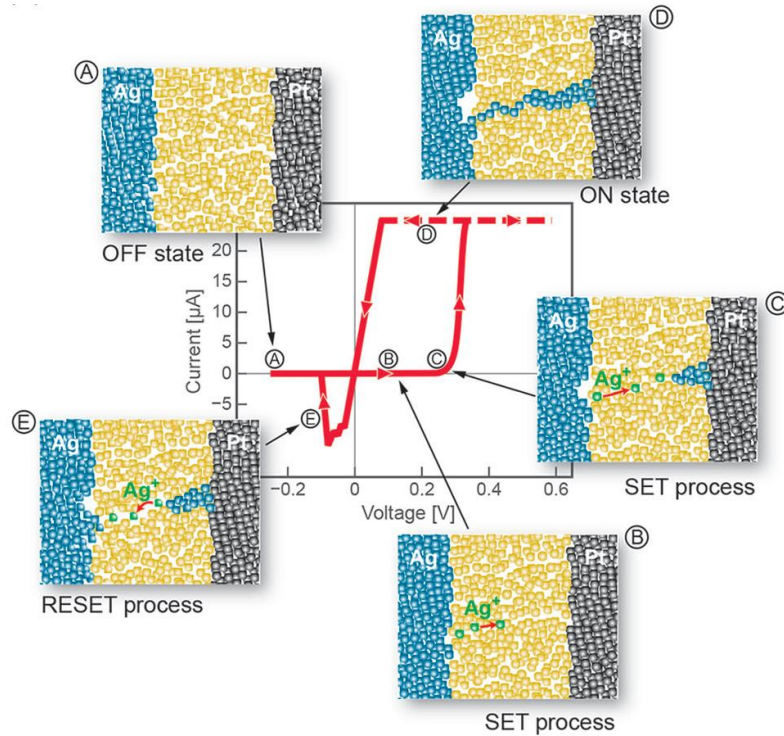


Figure 1.6 Demonstration of formation and dissolution of nanometer size conductive paths or channels that enable RRAM cells to switch between two distinct resistance states at different bias regimes. The letters (A →E) within the circles mean different stages of those tiny filaments (Menzel et al. 2015).

1.8.2 Schottky emission

Schottky emission is connected to the electron transport which overtops a potential barrier (at the interface of metal and insulator), the height of which is reduced under high electric field condition. The thermally energized electrons in the metal can acquire sufficient energy to overcome the barrier height at the interface. The image force reduced the energy barrier height, and this phenomenon is called the Schottky effect. Such emission of electrons from the metal to the oxide is called Schottky emission, shown in Figure 1.7 The equation to represent Schottky emission is (Chiu 2014),

$$J = A^*T_2 \exp \left[\frac{-q \left(\phi_b - \sqrt{\frac{qV}{4\pi\epsilon_0\epsilon_r d}} \right)}{KT} \right] \dots\dots\dots(1.6)$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m_0} \dots\dots\dots(1.7)$$

where A^* is the Richardson constant, J is the current density, V is the applied voltage, ϕ_b is energy barrier height, ϵ_r is the dynamic (optical) dielectric constant of the insulating film, ϵ_0 is the permittivity of vacuum space, d is the film thickness, k is Boltzmann's constant, T is absolute temperature, q is charge on electron, m_0 is free electron mass, m^* is effective electron mass in the dielectric and h is Planck's constant. The effective thickness of the switching layer (d) and the energy barrier height (ϕ_b), E is the electric field across the dielectric, can be obtained from the slope and intercept of \sqrt{V} vs $\ln(\frac{J}{T^2})$ plot, respectively. The slope is $\frac{q}{KT} \sqrt{\frac{q}{4\pi\epsilon_0\epsilon_r d}}$ and the intercept is $(\ln A^* - \frac{q\phi_b}{KT})$. Here, $\ln A^*$ can be ignored because it is much smaller than $\frac{q\phi_b}{KT}$. We can confirm the Schottky emission mechanism by the fitting of $V^{\frac{1}{2}}$ vs $\ln(J)$ (Bai et al. 2014) (Chu et al. 2014).

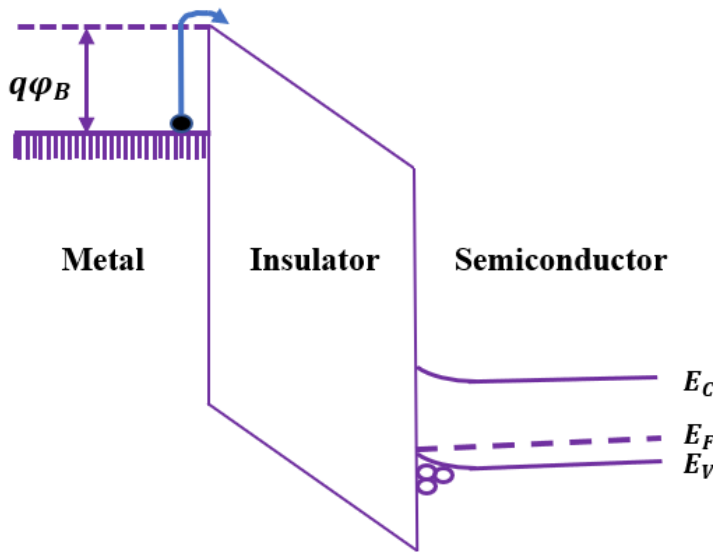


Figure 1.7 Pictorial representation of energy band diagram of Schottky (or thermionic) emission in metal-insulator-semiconductor (M-I-S) heterostructure. E_c , E_F and E_v represent conduction band minima, Fermi energy and valence band maxima, respectively. $q\phi_B$ is Schottky barrier height.

It is important to note that Schottky emission is also known thermionic emission. Two other commonly observed transport mechanisms are thermionic-field emission and field emission. Thermionic-field is intermediate of *pure* thermionic and *pure* field emission transport mechanism. A comparative depiction of all these three types of transport mechanisms is shown in Figure 1.7.

1.8.3 Space-charge-limited-current

The mechanism behind the space-charge-limited-current (SCLC) is based on the shallow traps in the metal oxide layer. SCLC is somewhat similar to transport events in vacuum diode. The typical I - V characteristics of the SCLC mechanism consists of three parts: the ohmic region $J_{ohm} \propto V$, trap-filled limit current ($J_{TFL} \propto V^2$), the Child's square law region ($J_{child} \propto V^2$) (Guo et al. 2015). We consider V_{tr} and V_{TFL} as the transition voltages at the ohmic region and TFL region respectively, as shown in Figure 1.8.

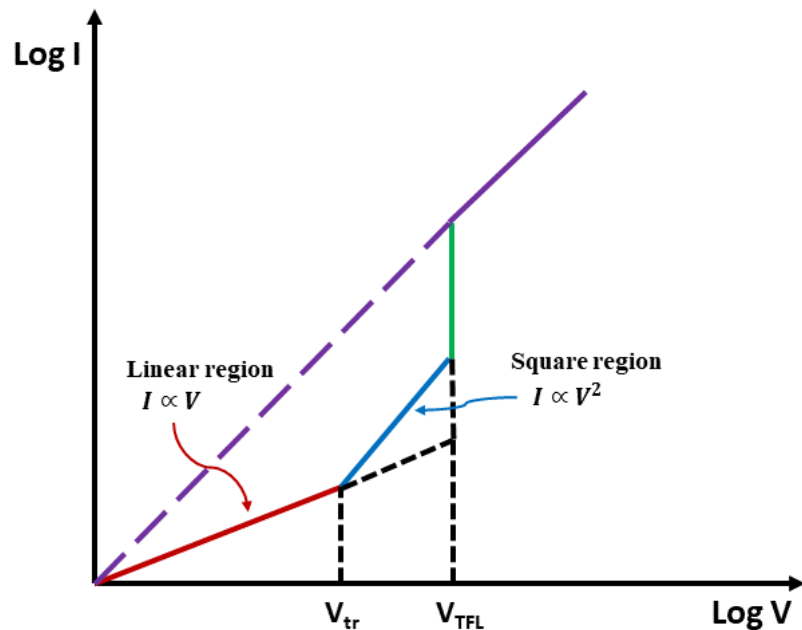


Figure 1.8 A current-voltage (I - V) characteristics of SCLC model. V_{tr} is transition voltage. V_{TFL} is trap-filled limit voltage.

The current densities for different regions can be expressed as (Chiu 2014),

$$J_{Ohm} = qn_0\mu\frac{V}{d}, \dots\dots\dots(1.8)$$

$$J_{TFEL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3}, \dots\dots\dots(1.9)$$

$$J_{Child} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3}, \dots\dots\dots(1.10)$$

$$V_{tr} = \frac{8}{9} \times \frac{qn_0d^2}{\varepsilon\theta}, \dots\dots\dots(1.11)$$

$$\theta = \frac{N_c}{g_n N_t} \exp\left(\frac{E_t - E_c}{kT}\right), \dots\dots\dots(1.12)$$

$$V_{TFEL} = \frac{qN_t d^2}{2\varepsilon}, \dots\dots\dots(1.13)$$

$$\tau_c = \frac{d^2}{qn\mu\theta}, \dots\dots\dots(1.14)$$

$$\tau_d = \frac{\varepsilon}{qn\mu\theta}, \dots\dots\dots(1.15),$$

where, J is the current density, ε is the dielectric constant, n_0 is the concentration of the free charge carriers in thermal equilibrium, N_c is the density of states in the conduction band, d is the thickness of the dielectric, g_n denotes the degeneracy of the energy levels in the conduction band, T is the absolute temperature, V is the applied voltage, θ is the ratio of free carrier density to total carrier density, E_t is the trap energy level, μ is the electronic mobility, k is the Boltzmann's constant, q is the electronic charge, n is the concentration of the free carrier in the insulator.

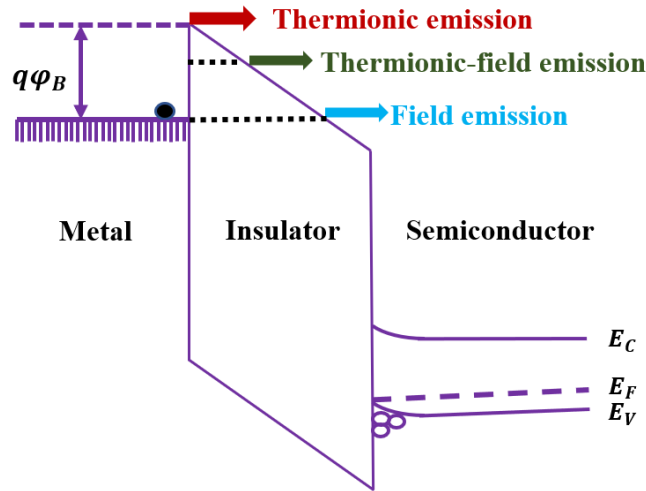


Figure 1.9 A single platform which shows schematics of thermionic emission, thermionic-field emission and field emission transport models.

When the applied bias voltage is low ($V < V_{tr}$), we will have more thermally generated free electrons (n_0) than the injected electrons from the electrode (n). As a result, the $J - V$ curve obeys Ohm's law, and the slope of the $\log I - \log V$ (or $\log J - \log V$) curve is 1. During the transition from ohmic to SCLC, the dielectric relaxation time (τ_d) and the carrier transit time (τ_c) become equal at the transition voltage (V_{tr}). Departure of ohmic conduction and onset of SCL conduction occur when one approaches this limiting bias V_{tr} . When $V < V_{tr}$, the thermally generated carrier density is larger compared to the injected carriers. The injected carriers will then get redistributed inside the dielectric medium in order to maintain charge neutrality. Those injected carriers will travel across the dielectric. This redistribution of carriers is called dielectric relaxation. The ohmic behavior is observed only when the space charge carriers are trapped. As we increase the applied voltage, the number of injected electrons increases rapidly. Those injected electrons are then transported into the thin oxide film and are partially captured by the trap sites present in the oxide matrix, while the others contribute to the total current. The transport process at this stage is called trap-controlled SCLC. As the applied voltage is increased further, i.e., $V > V_{tr}$, τ_c and τ_d decrease with increasing V , which finally results in the increase in free carriers in the dielectric. At this stage, the injected electrons will dominate the thermally

generated electrons and the I - V curve would correspond to trap-filled SCLC mechanism (denoted by J_{TFL} in eq. 1.9).

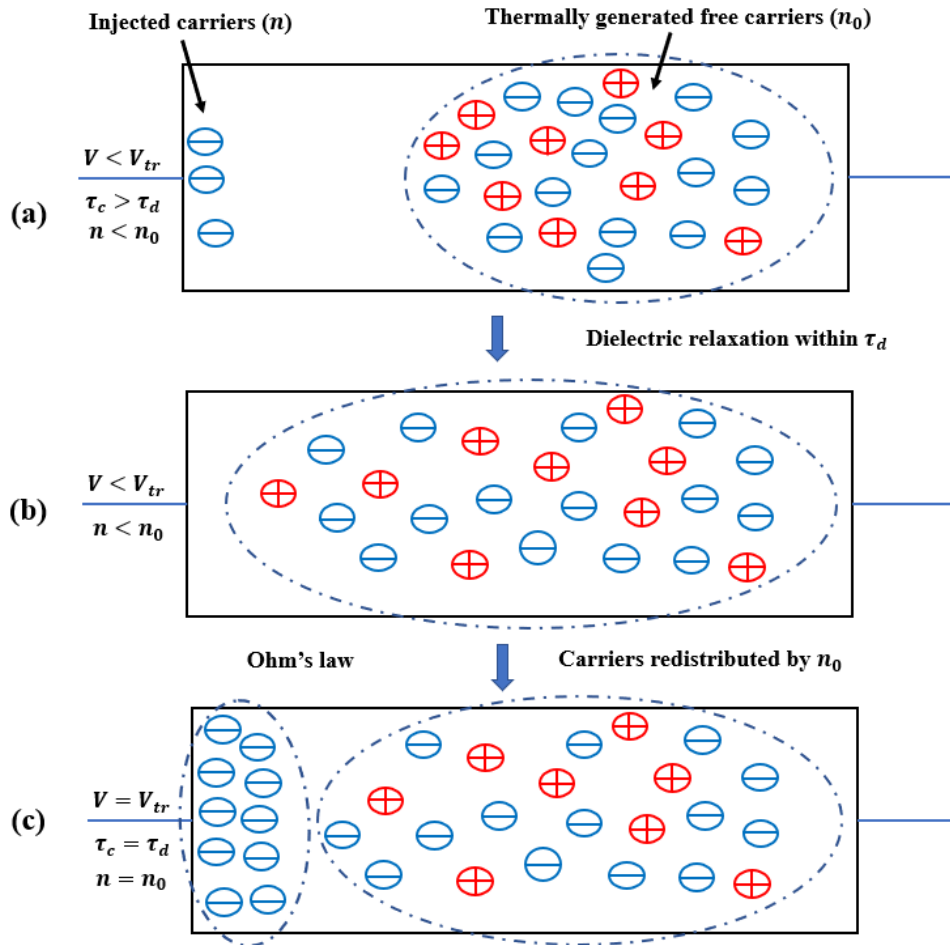


Figure 1.10 A schematic representation of charge carriers' distribution in insulating film under carrier weak electric stimulus ($V \leq V_{tr}$) in SCLC. (a) Very weak injection ($V < V_{tr}$, $n < n_0$, $\tau_c > \tau_d$), (b) dielectric relaxation and carriers' redistribution on increasing the bias and (c) weak injection at V_{tr} ($V = V_{tr}$, $n = n_0$, $\tau_c = \tau_d$). V_{tr} is the transition voltage at which the cell starts departing the Ohmic transport regime. n is the injected carrier concentration; n_0 the concentration of thermally generated free carriers in insulating matrix; τ_c the carrier transit time; τ_d the dielectric relaxation time.

After all the traps are filled, the injected carriers can move freely in the oxide material; as a result, the resistance of the cell rapidly jumps to LRS. In the LRS regime, the current is fully controlled by the space charge, which limits further injection of free carriers in the oxide layer (Chiu 2014). The I - V curve follows Child's law ($I \propto V^2$). When the slope of $\log I$ - $\log V$ curve changes from 1 to 2, it confirms the onset of $I \propto V^2$ (SCLC). Figure 1.8, Figure 1.10, and Figure 1.11 show the distribution of carriers in SCLC, (a) High electric field ($V > V_{tr}$, $n < n_0 < N_t$, $\tau_c < \tau_d$), (b) Trap-filled-limited conduction ($V_{tr} < V < V_{TFL}$, $n < n_0 < N_t$), (c) SCLC conduction ($V > V_{TFL}$, $n_0 > N_t$).

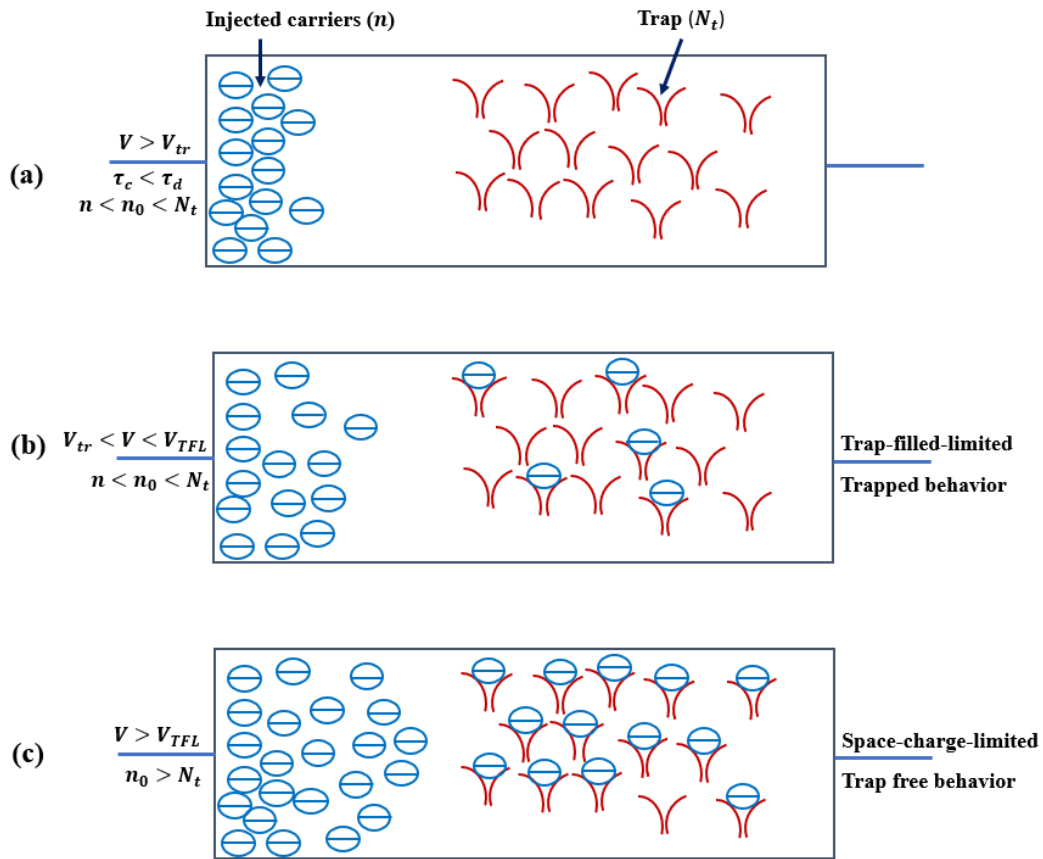


Figure 1.11 Schematic representation of carriers' transport within the dielectric film under carrier strong injection ($V > V_{tr}$) in SCLC. (a) Strong injection ($V > V_{tr}$, $n < n_0 < N_t$, $\tau_c < \tau_d$), (b) trap-filled-limited ($V_{tr} < V < V_{TFL}$, $n < n_0 < N_t$): parts of traps are filled up (trap control), and (c) space-charge-limited ($V > V_{TFL}$, $n_0 > N_t$): all traps are filled up (trap free). Ohmic conduction departs at bias V_{tr} and TFL conduction departs

at bias V_{TFL} (See Figure 1.8); n is the injected carrier concentration; n_0 is the concentration of thermally generated free carriers; N_t is the trap density; τ_c is the carrier transit time; τ_d is the dielectric relaxation time.

1.8.4 Poole-Frenkel emission

Poole-Frenkel emission is another mechanism which is controlled with traps. It is related to field enhanced thermal excitation of trapped electrons into the conduction band of the dielectric, as shown in Figure 1.12. Here, the electrons hop between trap states caused by defects (Lee et al. 2015b). For Poole-Frenkel emission the current density is described as (chiu 2014),

$$J = q\mu N_c E \exp \left[\frac{-q \left(\phi_T - \sqrt{\frac{qE}{\pi \epsilon_i \epsilon_0}} \right)}{KT} \right] \dots \dots \dots (1.16),$$

where μ is the mobility of charge carriers, N_c is the density of states in the conduction band, $q\phi_T$ is the trap energy level, and the other notations are the same as mentioned before. It is clear that the Poole-Frenkel mechanism can be confirmed by the curve of $\ln \left(\frac{J}{V} \right) - V^{\frac{1}{2}}$.

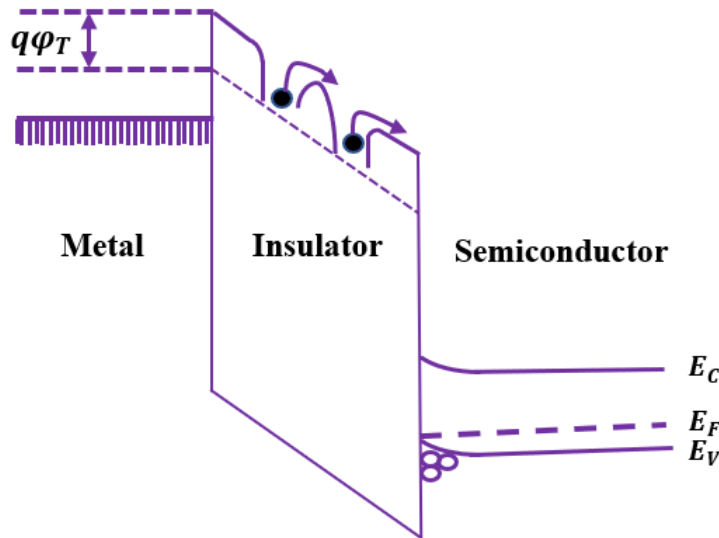


Figure 1.12 Schematic energy band diagram of Poole-Frenkel emission in metal-insulator-semiconductor structure.

As discussed above, the SCLC, Schottky emission and Poole-Frenkel emission models can be verified from I - V curve fitting data. It is interesting to note that the conduction process in general depends on bias voltage and temperature, making it clear that the exact conduction mechanism can be identified experimentally by temperature- dependent charge transport measurement.

1.9 Literature survey

The concept of resistive switching (RS) based memories arose as an aftermath of the path-breaking results on electrical transport of aluminum oxide (Al_2O_3) thin film in early 1960s (Hickmott 1962). In that article, Hickmott reported the hysteretic current-voltage response for the first time in Al_2O_3 based metal-insulator-metal (M-I-M) structure. On application of bias voltage between the two metal contacts in the M-I-M structure, a sudden drop in resistance was observed, which he called “negative resistance”. In year 1968, Ovshinsky reported sudden change in resistance values in an amorphous semiconductor (made of 40% tellurium, 30% arsenic, 12% silicon and 10% germanium) thin film of a few micron thickness. Ovshinsky named it as *unusual memory effect* (Ovshinsky 1968). Most of these early research findings presumed this phenomenon as negative differential resistance. Later in year 1969, Hickmott observed switching of resistance values between two distinct states followed by a sudden dielectric breakdown in his Nb_2O_5 film based device (Hickmott 1969). The breakdown happened as he could not apply bias controllably. This was, to our knowledge, the first ever report on RS effect. This finding became incentive for many scientists to exploit this RS phenomenon (observed in several binary transition metal oxides) in order to build NVMs around late 1960s and early 1970s. In 1972, G. N. Jackson fabricated a capacitor type structure using lead-zirconate dielectric medium and aluminum electrodes. He termed it a *bistable switchable memory device* (Jackson 1972). Jackson succeeded in sweeping the memory states of the device between HRS and LRS, repeatedly back and forth. The first report on switching, what today’s researchers termed as ECM, dates back to year 1976. Hirose et al. observed the formation and rupture of dendrites-like structures in $\text{Ag}/\text{Ag}_2\text{S}_3/\text{Au}$ memory cells (Hirose et al. 1976).

These are lateral devices operated in bipolar mode. After this, we see a down-time in this avenue of research on RS based devices, which lasted for nearly two decades. The phenomenal growth of silicon-based technology and particularly the development of silicon-based FLASH memories in the 80s and 90s overshadowed the progress of resistive memories. The slow progress in understanding the underlying RS mechanisms, lack of technological sophistication for depositing good quality oxide thin films and characterization methods kept the potential of the resistive memory technology dormant until the end of the 90s (Lee et al. 2015). In the year 2000, Beck et al. observed the RS event in Cr-doped SrZrO₃ perovskite thin film (Beck et al. 2000). This was a breakthrough finding in the field of RS. They observed a metastable property of device ON and device OFF states even when the previously applied electric field was withdrawn. In the following years, many intense and path-breaking research efforts could be seen in this area in academia and industry. The research in this field mushroomed after the successful integration of NiO memory cell into conventional CMOS devices by I. G. Baek et al. at Samsung Electronics in year 2004 (Baek et al. 2004). With the remarkable progress in material processing techniques in the last few decades, resistive memory started to attract the research community's interest all over again as a non-volatile, low power, high density, and multi-bit operating memory (Bai et al. 2014). A current major hindrance to make this technology commercially viable is the lack of reproducibility and uniformity of the RS effect (Kim et al. 2014b). This is the result of the fact that although it is known that RS is caused by point defects (Traversa et al. 2013) (Rodenbücher et al. 2013), the specific types of defects that are responsible for the switching process are poorly understood. Various types of defects may exist in typical materials that are used for these devices (Yang et al. 2008), making it a challenging phenomenon to control and study. The commercialization of RRAMs is strongly reliant on a thorough understanding of the underlying switching kinetics. The growth of nanofilaments is random nature and pinpointing the tiny switching region is highly challenging in RRAM. The advancements in fabrication and characterization techniques in the early 2000s helped in properly comprehending the nanoscale materials and devices. A tremendous progress has been achieved in

understanding the switching mechanism behind RRAMs during the last two decades. By thorough understanding of switching mechanisms, many significant techniques were developed to optimize the performance of RRAMs such as imaging techniques (in situ TEM) (Huang et al. 2014), electrode engineering (Yang and Rhee 2007), interface studies (Yong et al. 2021), heterostructures (Xia et al. 2020), doping (Wang et al. 2019), etc. In the diverse metal oxide systems, a wide range of kinetics have been proposed as the possible mechanism of RS. From the beginning, there has been only a rudimentary understanding of the ECM mechanism. Szot et al., in 2006, studied the RS characteristics in SrTiO₃ based ECM cell (Au/SrTiO₃/AFM-tip) (Szot et al. 2006). The phenomenon behind the bistable switching in ECM cell was explained by the movement of oxygen ions and a corresponding valence change in the cation sublattice. To broaden the periphery of classification of nanionically driven redox-based memory cells, an another class, called *valance-change- memory* (VCM) effect, was introduced to explain bipolar metal oxide systems during those days. In 2007, Janousch et al. reported the valence change in Cr-doped SrTiO₃ by analyzing through spectroscopic evidence for the first time (Janousch et al. 2007).

The materials used in the RRAM devices can be classified into two categories: storage medium and electrode materials. In the last two decades, a variety of materials have been investigated as storage media and electrode materials. Storage media can be loosely classified as organic, inorganic and not-so-conventional materials. Because of the switching stability and ease of fabrication, inorganic materials, specifically transition metal oxides received a lot of attention in the early 2000s. The different materials that come under inorganic materials are binary oxides (SiO_x (Liu et al. 2015), HfO_x (Zhou et al. 2017), TaO_x (Lee et al. 2011a), CuO_x (Liang et al. 2014), ZrO_x (Liu et al. 2009), etc.), ternary oxides (SrRuO₃ (Skaja et al. 2016), SrZrO₃ (Guo et al. 2013), etc.), nitrides (SiN (Kim et al. 2017), AlN (Chen et al. 2013a), etc.). In 2008, M. Y. Chan et al. studied the RS characteristics in HfO₂ deposited using pulsed laser deposition technique (Au/Cr/HfO₂/Pt/SiO₂/Si) (Chan et al. 2008). They found that the switching was of bipolar nature with a switching voltage of 4.8 V and retention of 500 sec. The switching behavior was ascribed to the formation and

rupture of conducting nanofilaments formed due to the electrically-induced migration of oxygen vacancies (OVs). In 2009, Walczyk et al. observed low power unipolar RS in Au/HfO₂/TiN based device operational at 3 V. The 5 nm thick HfO₂ thin film was deposited using atomic vapor deposition and the switching mechanism was explained using contact-controlled Schottky effect (Walczyk et al. 2009). W. G. Kim et al. studied the effect of top electrode in TiO₂ based RRAM device (Kim and Rhee 2010). They used Pt//Ti/SiO₂/Si as the BE and a variety of metals (Pt, Ti, Au, Ag, Ni, Al) as TE. They argued that a Schottky contact was necessary to observe stable switching. Their switching characteristics could be controlled by changing the barrier height at the metal-insulator junction or interface. For Pt, Au and Ag, they observed formation of stable interface with TiO₂ film. In the case of Pt and Au, a high Schottky contact was formed and they observed both bipolar and unipolar switching events. Mere unipolar switching observed with Ag (as TE) was attributed to low Schottky barrier at the Ag-TiO₂ interface. Cells with Ni, Al and Ti as TE showed unstable unipolar and bipolar switching behavior. Later in year 2010, M. Kim et al. reported bipolar RS in Pt/TiO₂/Pt based RRAM (Kim et al. 2010). They interpreted the switching events using SCLC mechanism. From these reports we can understand that the electrode materials have a considerable impact on the switching modes of the oxide based RRAMs. The switching modes can differ even when we use the same oxide thin film but different electrode materials. This implies that the switching mode is believed to be a characteristic of both the active switching oxide layer and the electrode/oxide interfaces, rather than the intrinsic properties of the oxide itself. J. Li et al. investigated single crystal SrTiO₃ perovskite thin film for memory applications (Li et al. 2016). Using temperature dependent study, they stressed on the importance of OV migration in defining the RS nature. Multi-level switching was observed by W. Chen et al. with W/Zr/HfO₂/TiN RRAM memory stack (Chen et al. 2015). They found that a multi-step forming technique could be used to suppress the over-shooting of forming current, which eventually helped them achieve switching at fairly low SET/RESET bias. Another group S. Ge et al. observed RESET voltage dependent multilevel RS behavior in a completely inorganic non-oxide CsPb_{1-x}Bi_xI₃ perovskite film (Ge et al. 2018b). Both these groups observed stable,

repetitive multi-step switching which can facilitate building of high-density memory. Non-volatile memory based on such RS event has been so far reported for variety of materials, such as inorganic perovskites (Solanki et al. 2020), organic-inorganic hybrid polymer (Ercan et al. 2017), graphene oxide (Pal et al. 2020), silicon dioxide (Lee et al. 2021), organic compounds (SD et al. 2020), Mott insulators (Kalcheim et al. 2020), ferrites (Tong et al. 2021) (Kim et al. 2020), ferroelectrics (Wang and Bai 2019), metal sulfide (Mallick et al. 2020), 2D materials such as hexagonal boron nitride (Zhuang et al. 2020) and transition metal dichalcogenides (Ge et al. 2018), binary transition metal oxides (Rasheed et al. 2021) (Abbasi et al. 2020), and other chalcogenide materials (Gogoi and Mallajosyula 2020). Bio-inspired memories using substances such as protein (Sun et al. 2019), egg albumen (Yan et al. 2019) and glucose (Park et al. 2019) have also been reported, but with limited success.

While fabricating RRAMs researchers generally concentrate on a few notable factors: cost effectiveness, yield of low switching voltage, high endurance, good retention / stability and finally process compatibility with present CMOS. RS studies were performed in a few low-cost materials such as Cu_2O , CuO and Al_2O_3 . Y. Wu et al. (2011) fabricated Pt/ Al_2O_3 /TiN memory cell by patterning the oxide layer sized $50 \text{ nm} \times 50 \text{ nm}$ using atomic layer deposition technique (Wu et al. 2014). They observed both unipolar and bipolar switching modes. The LRS was associated with the migration of oxygen ions toward the anode and formation of the CFs made of OVs. The soft-breakdown process of dielectric in their device initiated from the Pt TE or the TiN BE was responsible for observing both unipolar and bipolar RS. They reported 10 ns of switching time which is quite promising for industry application. Y. Yang et al. imaged the formation of nanofilaments using *ex-situ* transmission electron microscopy (Yang et al. 2012a). They fabricated a planar device using SiO_2 as the active material, with Ag and Pt as contacts.

Table 1.3 lists out a few notable findings on resistive memory with their performance metrics.

Storage media	Switching voltage (V)	Switching mode	ON/OFF ratio	Retention (Sec)	Endurance (# of cycles)	References
HfO ₂	< 2	Unipolar/ bipolar	>10 ³	>10 ⁴	>10 ⁵	(Ryu et al. 2019) (Yong et al. 2021)
WO _x	< 2	Unipolar/ bipolar	>10 ⁵	>10 ⁴	>10 ⁸	(Won et al. 2017) (Wu et al. 2011)
Ta ₂ O ₅	< 2	Unipolar/ bipolar	>10 ³	>10 ⁴	>10 ⁴	(Wang et al. 2018)
TiO ₂	< 1	Unipolar/ bipolar	>10 ⁵	>10 ⁵	>10 ⁴	(Srivastava et al. 2021) 2021), (Ge and Chaker 2017)
Complex oxides						
BaTiO ₃	< 3	Unipolar/ bipolar	>10 ⁴	>1000	>10 ⁵	(Au et al. 2013)
SrTiO ₃	< 5	Bipolar	>10 ⁵	--	>10 ⁶	(Choi et al. 2014) (Zhang et al. 2013)
Chalcogenides						
Cu ₂ S	< 1	Bipolar	>10 ⁶	--	>10 ⁵	(Yan et al. 2016)
Ag ₂ S	--	Bipolar	>10 ⁶	--	>10 ⁶	(Liao et al. 2010)
Nitrides						
AlN	< 5	Unipolar/ bipolar	>10 ⁵	>10 ⁵	>10 ⁶	(Chen et al. 2012) (Kim et al. 2011)
SiN	< 3	Unipolar/ bipolar	>10 ⁷	--	>10 ⁹	(Kim et al. 2013)
Not-so-conventional materials						
Polymer	< 2	Bipolar	--	>10 ⁴	50	(Hu et al. 2014)
Protein	< 10	Bipolar	6.2	5000	500	(Moudgil et al. 2018a)
Glucose	< 5	Bipolar	10 ⁴	10 ⁴	100	(Park et al. 2018)
Graphene oxide	< 3	Bipolar	10	10 ⁴	100	(Chen et al. 2018)
Egg Albumen	< 2	Bipolar	10 ²	10 ⁴	120	(He et al. 2016)

Table 1.3 A few significant reports on different types of materials used for RRAM and their corresponding device performance parameters.

Copper (Cu) is a non-toxic, easily available and also an easily oxidizable element. It is extensively used in modern semiconductor electronics industry as well (Badugu et al. 2020). There are, in general, three different oxide phases of Cu: CuO, Cu₂O and Cu₄O₃ (Rehman et al. 2018). B. Singh et al. deposited thin film of Cu₂O on Cu substrate using thermal deposition and stencil lithographic techniques, and thereafter performed charge transport measurements using a conductive-AFM (c-AFM) tip as TE (Singh et al. 2012). They fabricated devices with different area of 25 μm, 50 μm and 150 μm which showed the resistance ratio of 26, 365 and 485, respectively. The filament formation was confirmed using the atomic force micrograph obtained during the switching. C. C. Lin et al. observed RS behavior in Cu_xO based cell (Al/Cu_xO/Pt/Ti/Si) fabricated using thermal oxidation method. The SET process occurred at 3 V with a retention of 5 × 10⁶ sec (Lin et al. 2013). The filament formation was due to the migration of OVs. Q. Zhou et al. studied the RS characteristics in Cu_xO/Cu/Ta/TaN/SiO₂/Si using again c-AFM tip as TE (Zhou et al. 2013). From the c-AFM current-voltage characteristics, they concluded that the conduction in oxide matrix was due to migration of OVs and the mechanism was explained using the Poole-Frenkel model. K. Park et al. fabricated flexible memories using Ni/Cu_xO/Ni deposited on Au-coated polyethylene-terephthalate (PET) substrate (Park et al. 2016). They observed bipolar switching and their conduction mechanism was explained using again Poole-Frenkel emission. W. Duan et al. used a CdS interfacial layer between Cu₂O and Pt with device structure Pt/CdS/Cu₂O/FTO (Duan et al. 2018). This interfacial layer eliminated the failure behavior and their device operated at fairly higher voltage (~ 8 V). C. H. Huang et al. studied the RS phenomenon in p-type hydrogen treated CuO nanowires (Huang et al. 2020). They grew CuO nanowires by oxidizing copper foil exploiting the vapor–solid mechanism. An improved RS behavior with low operating voltage induced unipolar switching with a ON/OFF ratio of 10⁷ and a retention time of 10⁴ sec were reported. Oxygen ion and Cu vacancy sites played a crucial role in the filament formation. The major takeaway from the findings described above is that we must minimize the electrode-oxide contact area in order for obtaining superior device performance. A prominent group from University of Houston (Ebrahim et al. 2012) reported Cu_xO

memristive cell. However, their initial resistance of the oxide layer was considerably small (only of the order of few tens of $k\Omega$), which eventually restricted the size of the memory window. This is a major hindrance for any memory to be used in computer architecture. Also, we do not get much clue from their data on details of switching mechanism, retention, lateral dimension of the conductive channels, etc. This article served as an incentive for us to investigate thoroughly the switching characteristics of copper oxide based RRAMs. In this thesis work, we perform an in-depth study on Cu_xO (mixture of CuO and Cu_2O) based memory cells using two different electrode combinations, and explain the aspects on which we could improve on our results from that of the existing literature. Further details have been explained in Chapter 2 and Chapter 3.

Previously we explained the working of two different types of resistive memories: ECM and VCM. In ECM cell, the movement of metal ions are responsible for formation or dissolution of conductive paths or filaments via the active insulating switching layer. On the other hand, in VCM cell, the SET process evolves with the gradual development of oxygen-deficient regions in the oxide-metal interface under application of external electrical stimuli. The two metal electrodes have different oxygen affinity and/or work functions. Removal of a negatively charged oxygen ion from the oxide-lattice interface creates a donor-type point defect (an oxygen vacancy or a cation interstitial), which carries a positive charge relative to the lattice and is usually compensated by the introduction of electrons to maintain charge neutrality. Oxygen vacancy sites will then align along the applied electric field and form CFs (creating onset of SET process). As for the RESET process, when applied an appropriate bias voltage, part of the previously removed oxygen atoms/ions is recaptured by the vacancy sites causing the rupture of the CFs which results in sudden increase of resistance of the insulating matrix, thus driving the cell to HRS. In this manner, the memory cell can be reversibly switched from HRS to LRS and vice versa. Various factors, such as the oxygen affinity or roughness of the electrodes, the diffusion barriers for oxygen transport in the dielectric, or the high local current densities resulting in Joule heating up to 1000 K (Yalon et al 2012), are responsible for causing RS event making it a complex process to understand. Despite attempts of using numerous indirect

probing techniques (such as, conductive atomic force microscopy (Barman et al. 2015) (Bae et al. 2017) and in-situ transmission electron microscopy (Kim et al. 2020) to verify and locate CFs within switching material, only limited information can be obtained. Therefore, a clear and unambiguous picture about the role of oxygen vacancies in resistive switching event is still missing. The aim of one part of this thesis work is to elucidate the role and importance of oxygen vacancy driven RRAM operation.

There has been a concerted effort to exploit molecules or nanometer-size molecular clusters (Barman et al. 2019) (Li et al. 2017) (Mas-Torrent et al. 2013) (Poon et al. 2015) (Xiang et al. 2016) (Cho et al. 2017) (Cho et al. 2017), other than conventional transition metal oxides (as described above) that exhibit reversible redox property, as active material in NVM. Redox active molecules in general have one or more oxidation-reduction states and they can be made to grow on various surfaces forming self-assembled monolayer or multilayers with simple and low-cost fabrication processes. Application of an oxidation voltage will cause electron loss in such molecules, whereas a reduction voltage in opposite direction can bring the electrons back to the molecules. Due to the capability of showcasing such intrinsic alternate oxidation and reduction behavior, such type of molecules can exhibit distinct charged/discharged states, which can represent typical logic ON and OFF states, with ultra-fast switching speed and excellent endurance/retention. Owing to scalability of the molecules and naturally present multiple redox states they can be used for building high-density of memory. Such properties make the redox active molecule a potential charge-storage medium for memory applications (Barman et al. 2019) (Mas-Torrent et al. 2013) (Poon et al. 2015) (Xiang et al. 2016) (Cho et al. 2017) (Cho et al. 2017). Towards that goal, we have explored for the first time a decavanadate $[V_{10}O_{28}]^{6-}$ molecule, belonging to larger group of polyoxometalate (POM) family for building resistive memory cell. Details of structure, property and applications of such molecular clusters can be found with Chapter 2 and Chapter 4.

X. Chen *et al.* co-assembled $(H_3PW_{12}O_{40})$ POM clusters into graphene-oxide and studied the switching characteristics (Chen et al. 2018). They reported bipolar switching and explained the charge transport using SCLC mechanism. X. Chen *et al.* built RRAM

device using a Keggin-type POM cluster, $\text{H}_3\text{PW}_{12}\text{O}_{40}$ (chen et al. 2019) as switching layer. They observed bipolar RS with operating voltage of 1.2 V and could hold the cell at two distinct bistable states for considerably large duration of time, 10^4 sec. The device operation followed Fowler-Nordheim (F-N) tunneling and SCLC law. Following that, Ghosh *et al.* fabricated flexible memory using ammonium phosphomolybdate POM ($(\text{NH}_4)_3\text{PMO}_{12}\text{O}_{40}$) with gold as top and bottom contacts (Ghosh et al. 2020). To the best of our knowledge this is the first ever report on flexible resistive memory with a POM molecule as an active element. They reported bipolar RS and confirmed that the conduction happened due to Schottky and Poole-Frenkel effect.

In general, RRAMs are suitable for 3D stacking of memory layers which can eventually facilitate extremely high-density storage applications (Wang et al. 2018). Another significant application is its potential use in an artificial synaptic device inside the hardware of neuromorphic circuits which will be able to mimic biological neural activities and aim for cognitive capabilities. Neuromorphic circuits create spiking neural impulses by connecting CMOS neurons with artificial synapses in neural networks. Electronic neural networks have been created traditionally by combining CMOS circuits made of Si-based floating gate cells, that act as neurons with artificial synapses. The synaptic conductance is continuously adjusted between low and high states to design the neural network. Such research efforts can find place in much-talked-about “artificial intelligence”. RRAM could be an ideal candidate for this application because the resistance may be altered from the set state to the reset state and vice versa using the right voltage and current.

From the above cited literature, we develop an understanding that there is no complete agreement on the exact origin of switching of resistance or current values in such discrete manner (in both cases unipolar and bipolar switching) as function of electric field. Interestingly, a few recent reports (Mikheev et al. 2014) (Mikheev et al. 2015) suggest that the switching event is highly sensitive to the interfacial layer and the point defects (such as oxygen vacancy sites) near the metal/insulator junction. This clearly implies that the quality of the metal/insulator interfacial layer and its crystallinity likely play important roles in device performance. Both are largely dependent on the device fabrication conditions (such

as deposition technique used, thickness of the functional oxide layer, ambiance of the deposition chamber, substrate temperature during metallization and deposition of the oxide layer, nature of the conducting substrate and contact pad, etc.). Of late, it is suggested that a detailed study on relationship between dielectric constant of insulating material, its crystallinity and thickness could provide solid information about the origin of switching event. Therefore, in order to understand various RS mechanisms as well as to realize their superior performance, further research is paramount to study the device behavior as function of fabrication parameters.

1.10 Scope of this thesis work

RRAM devices can be characterized by studying performance parameters such as operation speed, resistance ratio, retention and endurance. Maximizing resistance ratio, endurance and retention is the one of key goals of this proposed research. From device physics standpoint, the RS and performance degradation mechanisms need to be fully elucidated, as they pertain directly to endurance and retention. This is crucial to eventually translate the research into real commercial devices. Obtaining uniformity and reproducibility in switching of RRAMs is a major engineering challenge. Furthermore, device characteristics are strongly influenced by crystallinity of the oxides (Mikheev et al. 2014) (Mikheev et al. 2015), which in thin films is a function of growth parameters (such as deposition technique used, thickness of the functional oxide layer, ambiance of the deposition chamber, substrate temperature during metallization and deposition of the oxide layer, nature of the conducting substrate and contact pad, etc.) and substrate-lattice mismatch, among other factors. Much work examining structure-property relationships is necessary, especially considering that no single device or oxide is clearly the most favorable for memory applications. Defects also affect switching and degradation, and are prevalent in oxides. Quantification of the role of point defects and their migration is necessary, especially in high electric field conditions. Structural properties are intimately related to electronic properties, and it is imperative to understand charge transport (or conduction) mechanisms as well. Charge transport encompasses many effects, such as

electronic band structure of oxide, oxide electrode band alignment and interfacial gap states. It is pertinent to note that there is no complete agreement on the exact origin of existing switching mechanisms in both cases (unipolar and bipolar RS). Some of the available conduction models, often used to analyze RS events, are based on Schottky emission (Bai et al. 2014), space-charge-limited current (Guo et al. 2015), Poole-Frenkel emission (S. M. Sze 1981), and formation and rupture of conductive nano-filaments (Dirkmann et al. 2018). Despite considerable effort, no generally acceptable transport mechanism for RS could be arrived at so far. This work, using charge transport measurements at ambient condition, will try to address some of these issues. We believe that the work we are proposing is unique in a few respects. First, we demonstrate stable and repetitive RS in a complex polyoxometalate (POM) molecular crystals – a not-so-conventional material for RRAM application. Being highly redox active and a large electron reservoir in itself, these POM clusters can possibly offer us to build multi-level and high-density memory. Second, we will use historic phenomenon of quantization of electrical conductance observed in a nanometer size (length scales of the order of Fermi wavelength) quasi-one dimensional transport channel (Wees et al. 1988) (Wharam et al. 1988) as a tool to probe the RS event in RRAM devices. Third, towards the end of the thesis we try to explore suitable substrate and contact materials for building flexible and wearable electronic circuitry.

1.11 Objectives of the thesis work:

1. To fabricate several batches of RRAM cells based on: (i) a binary transition metal oxide (Cu_xO with $1 \leq x \leq 2$) and (ii) sodium decavanadate polyoxometalate molecules, as switching layers. We will use chemical route to synthesize sodium decavanadate crystals and then deposit a thin film of it on indium-tin-oxide (ITO) coated glass slab using spin coating technique. For deposition of Cu_xO thin film on Pt coated Si-wafers, we will employ DC magnetron reactive sputtering.
2. To study the chemical, structural and morphological properties of the functional switching layers using Fourier-transform-infrared (FTIR) spectroscopy, atomic force microscopy (AFM), scanning electron microscopy (SEM), cyclic voltammetry (CV), x-ray photoelectron spectroscopy (XPS), etc.
3. To perform electrical transport measurements on the as-fabricated memory cells (at ambient condition) in order to find out switching mechanism as well as different device performance metrics (e.g., resistance ratio, endurance, retention) using computer-interfaced circuitry comprising of source-measure-unit and probe station.
4. To fabricate RRAM cells on flexible substrate and perform electrical transport measurements on them.

1.12 Organization of this thesis

The research presented in this dissertation is spanned across *six* chapters.

Chapter 1 gives a brief introduction to the existing memory technologies in general and RRAM in particular. Different aspects of RRAM have been discussed. Also, discussed in a nutshell are the advantages of using RRAM over FLASH, FERAM, PCRAM, etc. Extensive literature survey on different RRAM studies have also been included in this chapter. Finally, we provide with the scope and objectives of this thesis work.

Chapter 2 discusses the materials and experimental techniques used for the fabrication and characterization of the RRAM device.

Chapter 3 describes the RS characteristics of Cu_xO based RRAM. We show how some of the performance metrics have been improved from earlier published works. Also, shown are the quantized conductance steps in transport data in order to *indirectly* validate filamentary model in RRAM. We discuss the limitation of our data with possible ways to improve on it.

Chapter 4 demonstrates results on polyoxovanadate based RRAM cells. Polyoxovanadate belongs to the larger group of polyoxometalate (POM) family. The pros and cons of using POM as an active switching material has been elucidated therein. Also, we talk about scope for further improving on our results.

Chapter 5 introduces building of *flexible* resistive memory cells on indium-tin-oxide coated polyethylene-terephthalate (PET) substrate.

Chapter 6 summarizes the research findings in this thesis work. It also tries to open up doors for future research in this area and beyond.

CHAPTER 2

MATERIALS AND METHODS

Overview: This chapter provides a brief description of the materials used in this research and the experimental techniques employed for the structural and electrical characterization. Also, we discuss the deposition techniques used for growing switching dielectric layer and contacts.

2.1 Substrate materials (Bottom contact in RRAM)

In this thesis work, we used **three** different substrates:

- (i) For copper oxide based device, we used Pt/Ti/SiO₂/Si hard substrate. A 10 nm thick Ti thin film was grown using dc sputtering on commercially available Si substrate. On top of that a 80 nm thick Pt film was deposited using sputtering. Pt acted as bottom contact in the RRAM cells.
- (ii) For polyoxovanadate based RRAM, we used ITO coated glass substrate. This was purchased from Sigma Aldrich. ITO layer acted as the bottom contact.
- (iii) As for flexible memory, commercially available ITO coated polyethylene-terephthalate (PET) substrate was used. Here also, ITO served as bottom contact.

2.2 Active switching dielectric media

- (i) Copper oxide (Cu_xO with $1 \leq x \leq 2$)

Copper is a group-11 transition metal in periodic table. Its oxide formation is also easier than many other transition metal oxides. Apart from being an abundantly available metal, Cu is nontoxic, relatively inexpensive, and most importantly it offers a high degree of compatibility with the modern semiconductor process industry (Dong et al. 2007). Resistive memories based on Cu_xO can offer a promising alternative owing to its cost-effectiveness and facile fabrication. They also exhibit remarkably high ON/OFF ratio, stable and repetitive switching, long endurance and retention metrics, and more importantly the capability to accommodate a variety of top and bottom metal contacts (Ebrahim et al. 2012) (Deuermeier et al. 2019) (Yan et al. 2015) (Rehman et al. 2018) (Yang and Rhee

2007). Unlike many conventional binary oxides one can exploit variety of deposition techniques such as thermal oxidation (Dong et al. 2007), sputtering (Ebrahim et al. 2013) (Yang and Rhee 2007), solution processing (Rehman et al. 2018), atomic layer deposition (Lenef et al. 2021) and pulse laser deposition (Yang and Rhee 2007)[45] for obtaining smoother and sub-100 nm thickness Cu_xO thin films. In general, one can find two stable oxide phases of Cu – cupric oxide (CuO) and cuprous oxide (Cu_2O) – both being p-type semiconductor having bandgap (E_g) of 1.7 - 2.2 eV (Rehman et al. 2018). Therefore, the current-voltage characteristics in Cu_xO based devices are governed by the injection and transport of hole carriers. In general, both phases of Cu_xO are found while depositing its thin film. These above cited properties can be used to tailor the bandgap and carrier mobility of Cu_xO film, using which one can control its resistive switching behavior. Additionally, by adjusting oxygen partial pressure of the CuO and Cu_2O , the switching parameters can be effectively engineered.

(i) Polyoxometalate (POM) clusters

POMs are large group of molecular clusters with frameworks built from d-block transition metal oxo-anions linked by shared oxide ions, and were first explored by Jöns Jacob Berzelius in 1826 (Hill 1998). Since then there have been numerous discoveries of plethora of POMs with a wide range of molecular structures with versatile physical properties, electronic structures, and applications (Vasilopoulou et al. 2015) (Long et al. 2010) (Chen et al. 2019). Though resistive switching based memory has been reported in a wide range of materials as elucidated before, such extensive studies based on POM as active element still remain elusive. However, potential application of POM clusters as building block of molecular spin-qubit for quantum computing (Lehmann et al. 2007) (Shiddiq et al. 2016), spin field effect transistor (Cardona-Serra et al. 2017), organic optoelectronic device (Vasilopoulou et al. 2015), floating gate material in NVM (Vilà-Nadal et al. 2013), flash memory device (Busche et al. 2014), among others (AlDamen et al. 2009) (AlDamen et al. 2008) (Cardona-Serra et al. 2015), has been reported.

POMs are an important class of water-soluble, nanosized polynuclear clusters consisting of d-block transition metals and oxygen atoms with the basic building block $[\text{MO}_x]^{p-}$, where $M = \text{Mo}, \text{W}, \text{V}, \text{Nb}$. (Vilà-Nadal et al. 2013) (Busche et al. 2014) (Vasilopoulou et al. 2015). Normally POM clusters are polyanionic (implying that they are already in oxidized state) in nature, and therefore they can be complexed with additional cations as linkers (e.g., transition or alkali metal). POMs can form lacunary structures, whereby some of the cage atoms are removed to create vacancies that can be filled by linker atoms (Vilà-Nadal et al. 2013). Based on the chemical composition, POMs can be divided into two categories: (i) isopolyanion and (ii) heteropolyanion, as shown in Figure 2.1. These two anions may be represented by the general formulae of $[\text{M}_m\text{O}_y]^{p-}$ and $[\text{X}_x\text{M}_m\text{O}_y]^{q-}$, respectively. Here, M represents the addenda atom and X is the heteroatom/central atom (Kozhevnikov 2002). However, it is convenient to discuss the structural variation of the POMs starting from symmetric parent polyanions and others as their derivatives. There are three basic parent structures for POM molecules: tetrahedron, octahedron and icosahedron, with their central polyhedron as $[\text{MO}_x]$ ($x = 4, 6$ or 12). The structures mentioned above are known as Keggin $[\text{XM}_{12}\text{O}_{40}]^{x-8}$, Anderson-Evans $[\text{XM}_6\text{O}_{24}]$ and Dexter-Silverton polyanion $[\text{XM}_{12}\text{O}_{42}]^{x-12}$, respectively. In addition, there is one more lacunary derivative of the Keggin structure which is called the Wells-Dawson polyanions, $[\text{X}_2\text{M}_{18}\text{O}_{62}]^{2x-16}$.

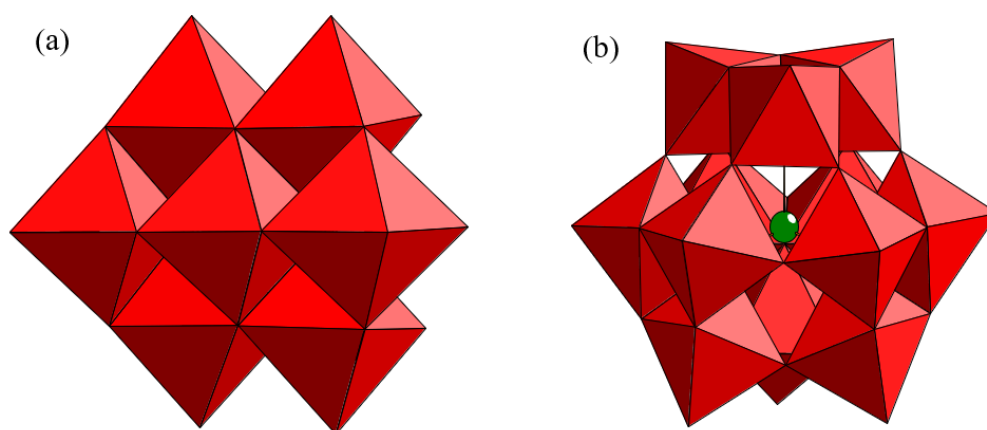


Figure 2.1 The schematic diagram of (a) isopolyanion, and (b) heteropolyanion (or Keggin structure)

In recent years, numerous theoretical as well as experimental studies have rendered detailed analysis about nature of POM compositions, their diverse structures and properties (Yang et al. 2021) (Vasilopoulou et al. 2015) (Long et al. 2010) (Jenkins et al. 2017) (Petel et al. 2018) (Chaumont and Wipff 2009). Being oxygen-rich clusters POMs act as natural electron reservoirs (Hou et al. 2019). Interestingly, POMs are also known as excellent electron acceptor that can reversibly store and release multiple electrons (Petel et al. 2018) (Chaumont and Wipff 2009) (Vilà-Nadal et al. 2013) (Busche et al. 2014). This implies that such clusters can easily undergo multiple reduction (or oxidation) that enables delocalization of large number of electrons throughout the metal-oxide cage (with only minor structural reorganization of the cluster) allowing them to play a vital role as excellent electron conductor in electronic nanoscale devices (Vilà-Nadal et al. 2013) (Busche et al. 2014). Such ability of multiple reductions can also facilitate POM as potential active material for multi-bit storage cell (Vilà-Nadal et al. 2013) (Busche et al. 2014). In addition, POMs are susceptible to low-pressure and high-temperature micro- and nano-fabrication processes (Busche et al. 2014) which can translate in better integration with commercial CMOS technology. Despite being highly (reversible) redox-active molecules and having other properties, sometimes even superior to conventional binary transition metal-oxides, POMs have not so far been visibly exploited for redox-based non-volatile memories in general, and RRAM in particular.

2.3 Top contact materials

In our RRAM devices, we employed tungsten probe tip (~ 25 μm diameter size), Cr (10 nm thick)/Au (80 nm thick), Cu (100 nm thick) and Al (180 nm thick) as top contacts. Except for the W probe tip, the other metal contacts were deposited on dielectric layer using either dc sputtering or thermal evaporation technique. Details of device and contact deposition are explained in Chapter 3, 4 and 5.

2.4 Device fabrication methods

In our work, the RRAM fabrication involves the below mentioned thin film deposition techniques.

(a) Spin coating

Spin coating is a low-cost thin film deposition technique. The substrate is held at a constant position with the help of a vacuum chuck. First, the desired material of correct weight percentage (to be deposited in form of a thin film) is evenly mixed with a suitable solvent to produce a solution. Then, drops of that solution is cast onto the substrate using a syringe or a pipette. Casting can be done in two ways: pouring the solution before spinning of the substrate starts (static spin coating), or after the start of substrate spinning (dynamic spin coating). The rotation speed of the substrate can be adjusted in such a way that the solution is spread uniformly over the substrate and finally yields a good quality uniform thin film. Finally, the substrate is given heat treatment in vacuum oven so the solvent dries up leaving behind a good quality uniform film behind. A schematic diagram of a spin coating setup is shown in Figure 2.2.

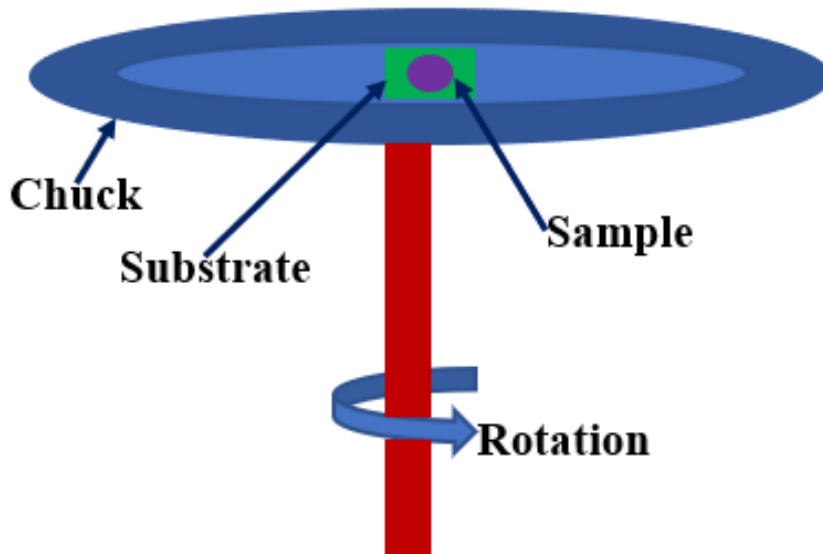


Figure 2.2. A schematic diagram of a spin coating unit.

(b) Thermal evaporation method

Thermal evaporation is a low-cost and simple physical vapor deposition method for growing thin film. Before we start the actual film deposition, a high vacuum is created inside the deposition chamber. The target material is kept in an evaporation source (coil or boat). On applying sufficient electrical energy to the source, the target material undergoes sublimation. They travel towards the substrate on which we wish to grow the sample. A sufficiently high vacuum is needed to maximize the mean free path of target atoms once they are evaporated. Finally, a thin film of the material is grown on the substrate. The thermal evaporation unit we used in our research is shown in Figure 2.3.

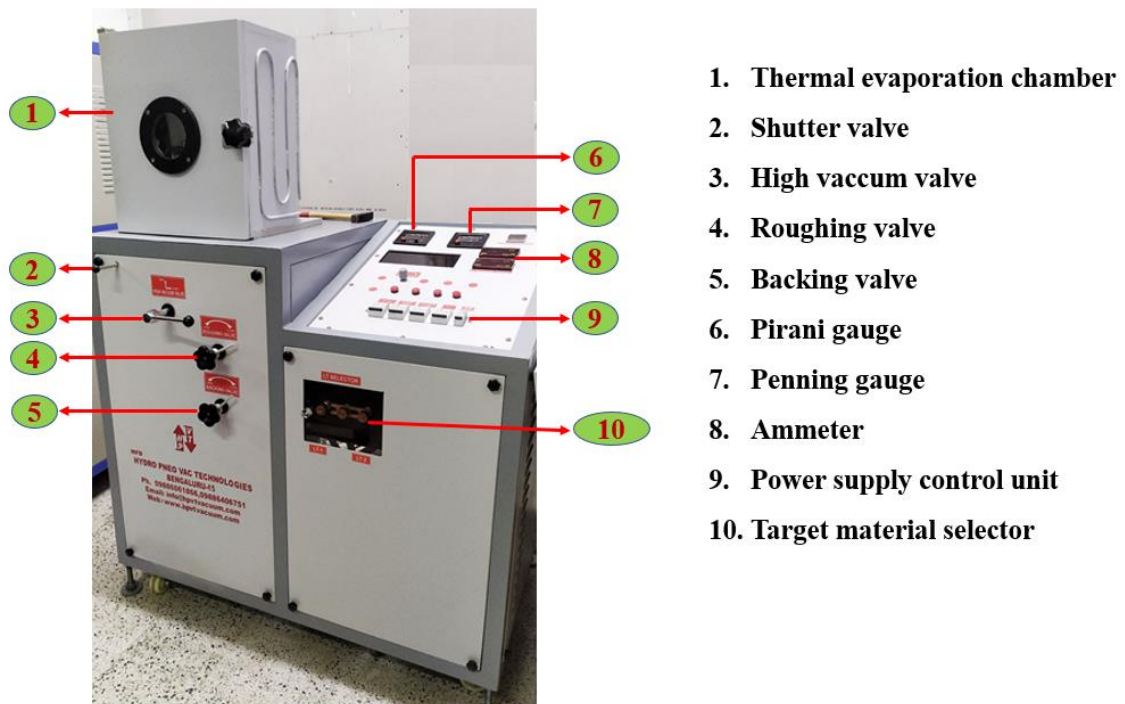
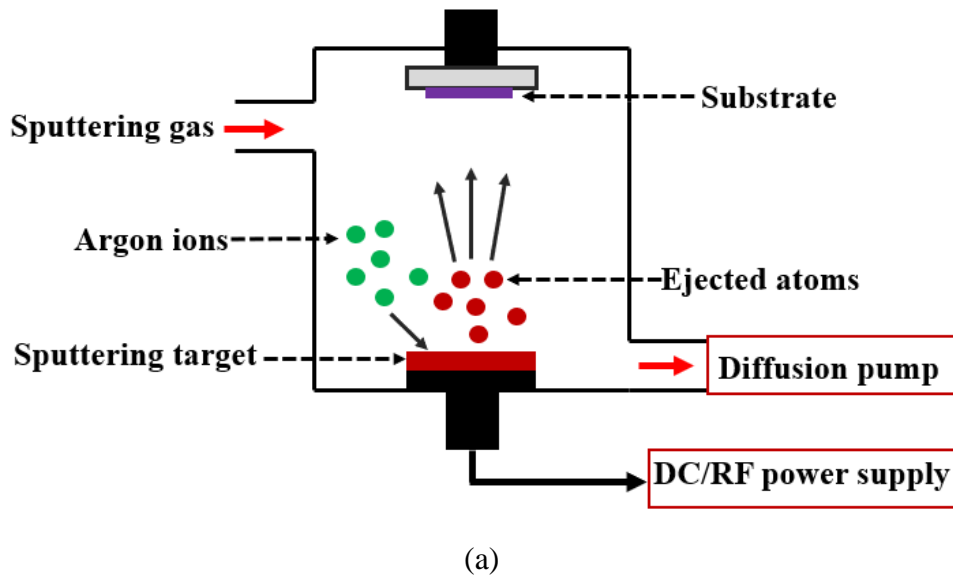
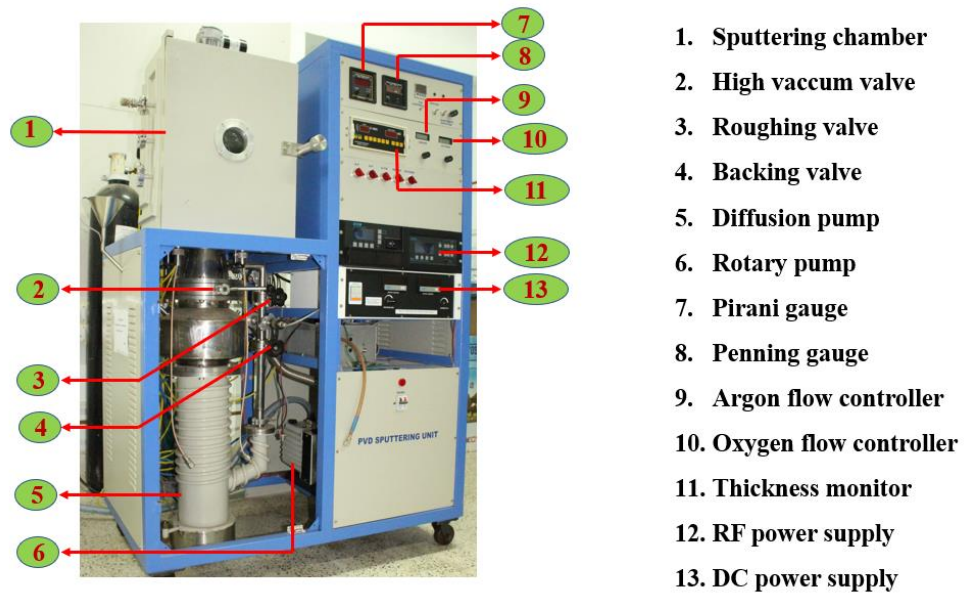


Figure 2.3 Thermal evaporation system used for the deposition of aluminum contacts.

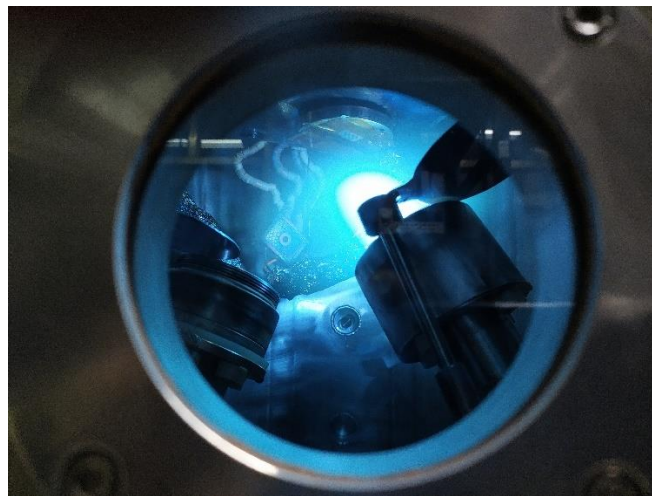
(c) Sputtering method

Sputtering is a physical vapor deposition (PVD) technique used for depositing thin films of target material (oxide or metal) onto a substrate (e.g., Si wafer). Once loaded the target and sample substrate, a high vacuum (pressure $\sim 10^{-6}$ mbar or below) is created inside the deposition chamber (Figure 2.4 (a) and (b)). A chemically inert gas, usually argon (Ar), is purged into that high-vacuum chamber in a controlled manner using a mass-flow controller. High electric voltage (DC or RF) is supplied to the cathode, whereon the target material is placed. Plasma of Ar is formed inside the chamber by losing an electron, which is then accelerated and made to hit the target. These high-energy Ar ions will dislodge some of the surface atoms from the target *via* the process of momentum transfer. These ejected atoms and argon ions together form plasma (Figure 2.4 (c)) and they move towards the substrate, and finally get deposited there. Suitable cleaning of the chamber and substrate is paramount in order to obtain a high vacuum and better adhesion of the target atoms onto the substrate.





(b)



(c)

Figure 2.4 (a) Schematic image of a sputtering system, (b) Sputtering system (VR Technologies Bangalore, India) used for the deposition of dielectric and metal thin films for this thesis work. Different parts of the system marked with numbers within circles. (c) Optical image of creation of plasma state during deposition.

(i) DC magnetron sputtering

A DC voltage, typically in the range of -2 V to -5 kV, is applied to the sputter target. The electrically neutral Ar atoms are ionized and then they hit the target. Due to high-energy impact ejection of atoms from the target surface happens and those atoms are driven to the substrate. The magnetic field generated by the magnetron traps the electrons near the target surface, and that improves the ionization of the sputtering gas, thereby increasing the thin film deposition rate. DC magnetron sputtering can also be used for depositing metal oxides. Here, a reactive gas such as oxygen is also purged into the chamber along with the sputtering gas (Ar). Oxygen reacts with the target metal atoms and forms the corresponding metal oxide at the substrate. This technique is called *magnetron reactive sputtering*. In this thesis work, we have used DC magnetron sputtering for depositing chromium/gold metal contacts as top electrode in sodium decavanadate based sample and DC magnetron reactive sputtering for depositing copper oxide (Cu_xO) thin film.

(ii) RF sputtering

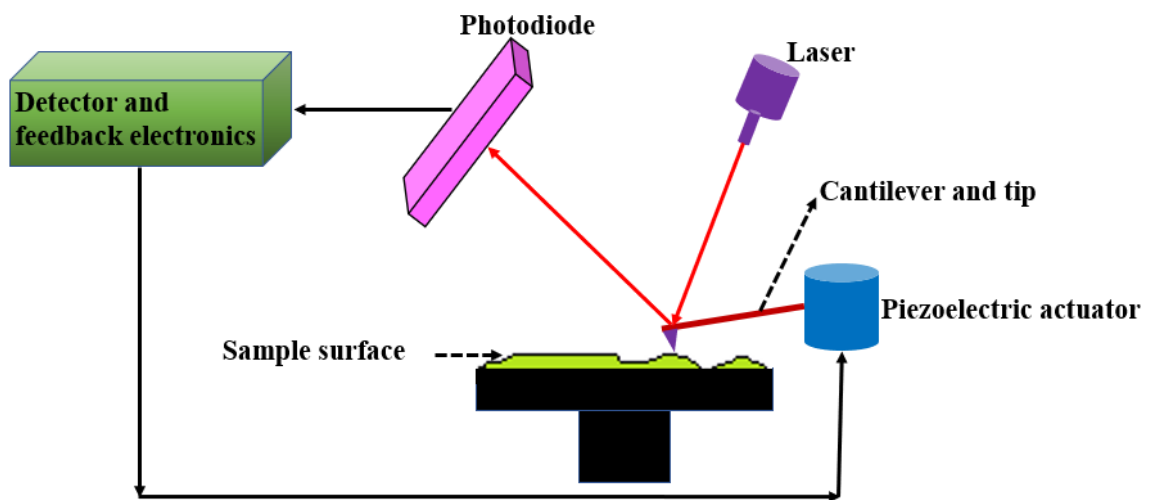
Radio-frequency (RF) sputtering is a thin film deposition technique that employs an alternating electrical potential at radio frequency in the power supply. RF sputtering is mainly used to deposit non-conducting targets such as metal oxides and oxide perovskites. A standard radio frequency of 13.56 MHz is used internationally in the RF power supply.

2.5 Structural characterization of RRAM devices

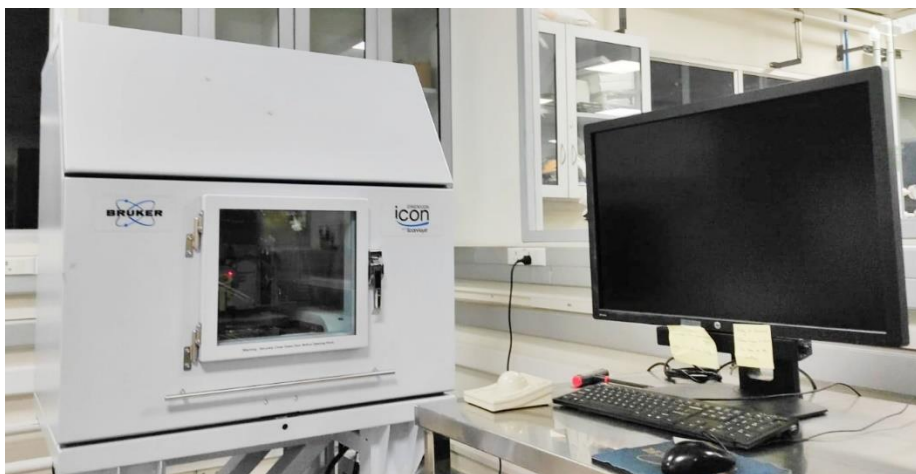
(a) Atomic force microscopy

Atomic force microscopy (AFM) is a powerful tool to 3D-image the topography of a surface on a sub-micron scale. It is one kind of scanning probe microscopy (SPM). A schematic diagram is shown in Figure 2.5(a) and the real setup is shown Figure 2.5(b). AFM involves the use of a shaped tip with an approximate radius of 10-20 nm. A feedback mechanism is placed to measure the interaction of the tip with the surface under

investigation when the tip is held a few nanometer above the surface. While raster-scanning all through the sample, the change in tip height is recorded to generate a topographic image of the sample surface. The highly polished AFM tip is attached to the end of a diving-board-shaped cantilever beam. The attractive and repulsive forces between the tip and the sample surface cause deflection of the cantilever beam. The cantilever is shone by a laser beam, which then reflects towards the photodiode. The magnitude of deflection of this reflected laser beam versus the AFM tip position constitutes the topographic image of the sample surface.



(a)



(b)

Figure 2.5 (a) Schematic diagram of an AFM showing its different components. (b) AFM setup (Bruker Dimension Icon AFM) used for studying surface morphology of our samples. (Image courtesy: CeNSE, IISc Bangalore).

The AFM can operate in three modes: contact, non-contact and tapping. In the contact mode the tip is in physical touch with the sample. This mode of operation is normally used for studying solid samples. In tapping mode, the cantilever (which is connected to AFM tip on one side and a small piezoelectric element on the other side) oscillates up and down near its resonance frequency (~ 500 to $50,000$ cycles/min). When the tip approaches the sample surface, the forces acting on the cantilever (Van der Waal forces, or dipole-dipole interactions, electrostatic forces, etc.) will bring down the amplitude of this oscillation. In the non-contact mode, the tip is not in physical touch of the sample surface. In this case, the cantilever oscillates at a frequency slightly higher than its resonance frequency. For our purpose, we used a 10 nm diameter tip and the contact mode of operation for scanning the samples.

(b) Scanning electron microscopy

The scanning electron microscope (SEM) uses high-energy electron beam as a source to image the sample surface. The beam of electrons that interacts with the sample reveals information, which includes morphology, crystalline structure and chemical composition. During the electron-sample interaction, secondary electrons are ejected from the sample which is then used to generate surface images of the sample. X-rays emitted from the sample are used to detect the chemical composition of the sample. This chemical analysis is called energy-dispersive-spectroscopy (EDS). In this thesis work, we have employed the SEM (Carl Zeiss Ultra 55 FESEM) to record the thickness of the thin film (using cross-sectional imaging) and also studied the chemical composition of the sample using EDS. The real setup is shown Figure 2.6.



Figure 2.6 Carl Zeiss Ultra 55 FESEM used for our study (Image courtesy: CeNSE, IISc Bangalore).

(c) X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a technique to determine the elements present in the sample under investigation and the nature of the chemical bonds that exist between these elements. When a beam of X-ray of energy $h\nu$ (h being Planck's constant, ν being frequency of incident X-ray photon) bombards the sample, the core electrons of the surface atoms get excited by absorbing sufficient energy from the incident X-ray beam. If the X-ray photon energy is large enough, these electrons may escape from the host material. The emitted electrons are called photoelectrons. An electron analyzer measures the kinetic energy (E_k) of these photoelectrons from which the binding energy (E_b) of the electrons is determined using Einstein's photoelectric equation:

$$E_b = h\nu - E_k - \phi, \dots \dots \dots (2.1)$$

where ϕ is the work function of the XPS spectrometer. Each elements produce a characteristic set of XPS peaks corresponding to the characteristic binding energy values. Upon analysis, each element that exists on the surface of the material being studied can be found. In this way, elemental composition, valence state, bonding environment, relative contents of different elements, etc. can be determined. The real setup of XPS instrument is shown Figure 2.7.

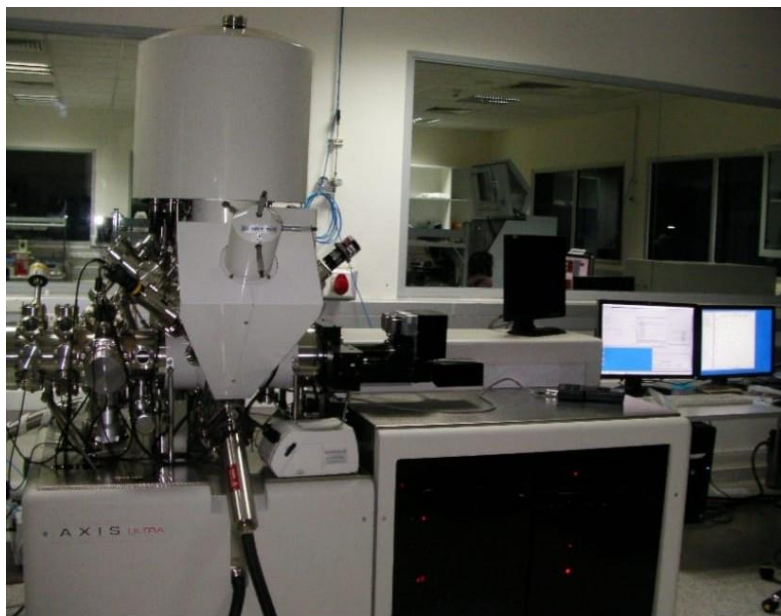


Figure 2.7 XPS setup (AXIS ULTRA) used in our investigation of RRAM samples (Image courtesy: CeNSE, IISc Bangalore).

(d) Fourier transform infrared spectroscopy

Fourier-transform-infrared (FTIR) spectroscopy is a technique used to identify the nature of chemical bonding of molecules in compounds. The FTIR method uses an infrared (IR) irradiation (wavenumber typically ranging from 4000 cm^{-1} to 400 cm^{-1}) as the source to examine the sample under investigation. The IR radiation that passes through the sample are absorbed and transformed to vibrational and rotational energy of atoms in the molecule. The detector in the instrument senses the vibrational frequency of the atomic particles and displays a transmittance and absorbance spectrum of functional groups present in the molecule. Each molecule or compound produces a unique FTIR spectrum as its molecular fingerprint, making FTIR a very efficient tool for identifying the type of chemical bonding and/or groups present in a molecular structure. The instrument used in our study is shown in Figure 2.8

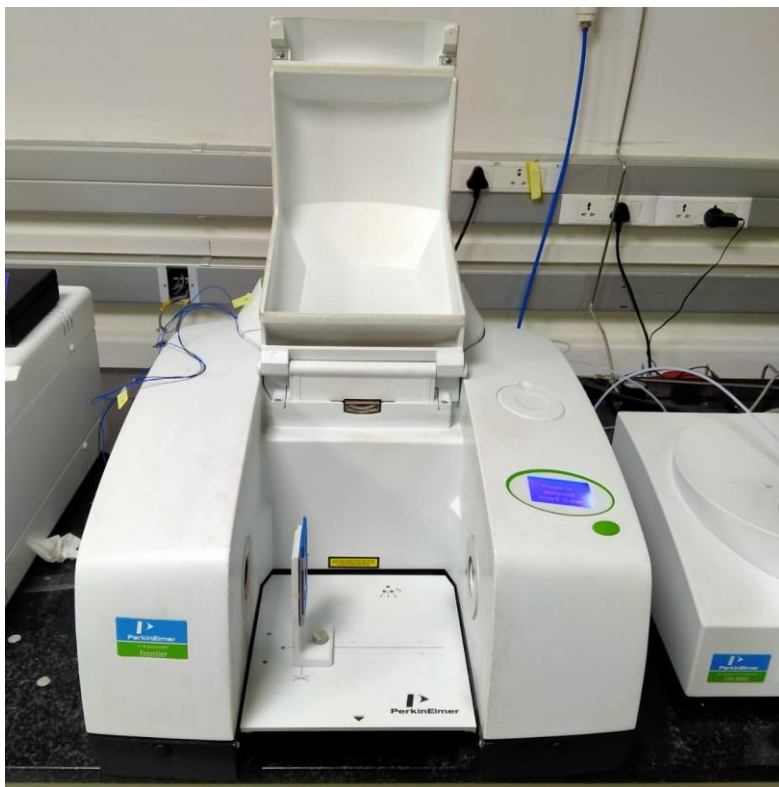


Figure 2.8 FTIR spectrometer used to study our samples. (Image courtesy: CeNSE, IISc Bangalore).

(e) Cyclic voltammetry

Cyclic voltammetry (CV) is an electrochemical characterization technique usually used to investigate the chemical kinetics, molecular electrochemistry, and redox (reduction and oxidation) response initiated by electron transfer due to the catalytic activity of the constituents. The voltammogram displays I - V characteristics demonstrating redox peaks at specific redox potentials. The experiments are performed by sourcing a potential sweep to an electrochemical workstation, and subsequently recording the electric current through the cell. The experimental setup of CV (as shown in Figure 2.9) generally consists of a three-electrodes: a reference electrode, a working electrode and a counter electrode. The peak positions in the voltammogram provide the multistage redox mechanism of the analyte, providing an insight into the electrochemistry of the compound.

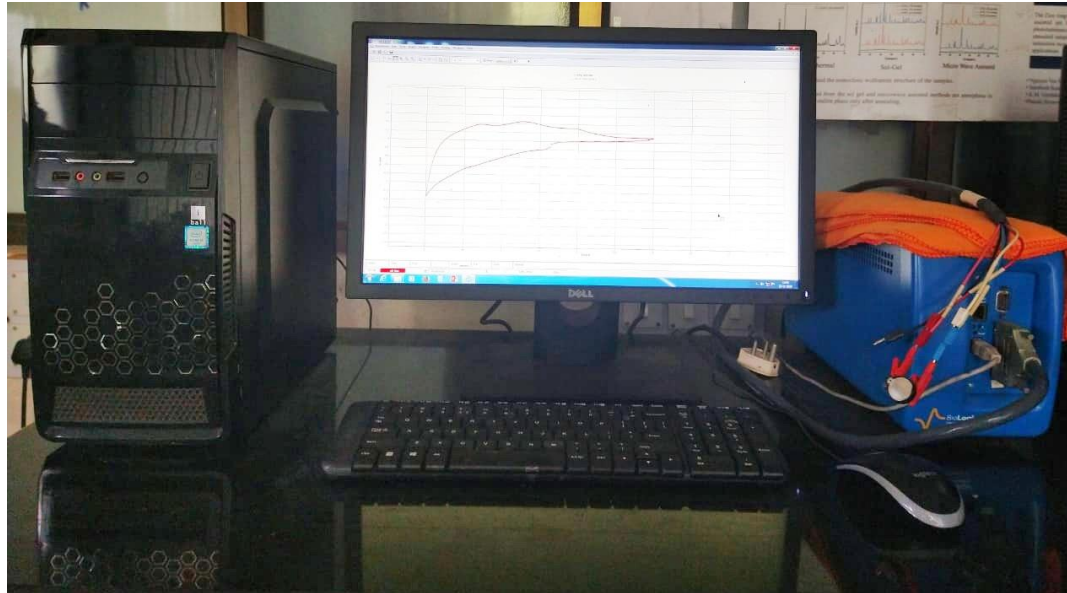


Figure 2.9 Cyclic voltammetry setup used to study the redox behavior of our POM samples. (Image courtesy: Physics Department, NIT Karnataka).

(f) Electrical characterization

In order to investigate the different RRAM device performance metrics (e.g., memory window, retention, endurance, etc.) we have to perform current-voltage (I - V) measurements. For this purpose, we used a Keithley 2614B Source/Measure Unit (SMU) which is interfaced with a computer *via* GPIB. The electrical measurement setup is shown in Figure 2.10.

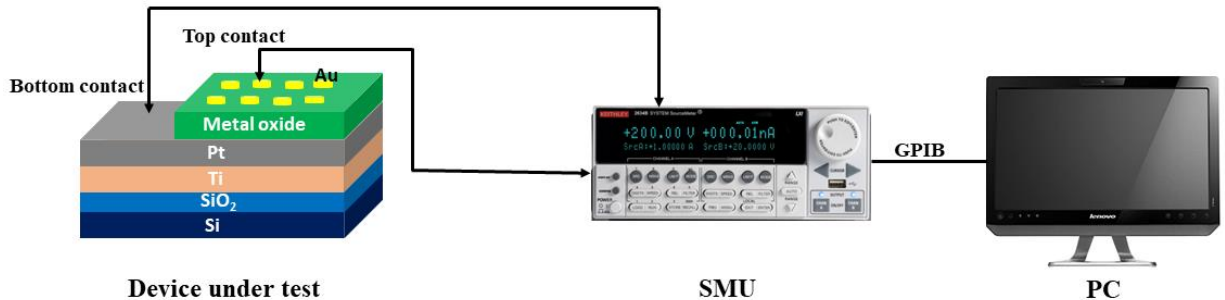


Figure 2.10. Electrical measurement setup used for the current-voltage (I - V) measurements.

The device under test was connected to the SMU using the DC probe station (as shown in Figure 2.11). The sample was placed on the metal chuck of the probe station, and the required electrical connections with the memory cell were made using tungsten probe tips (of 25 μm diameter) attached to the micromanipulator. These micromanipulators are connected to SMU through the BNC cables. The charge transport data is collected in form of I - V plots.

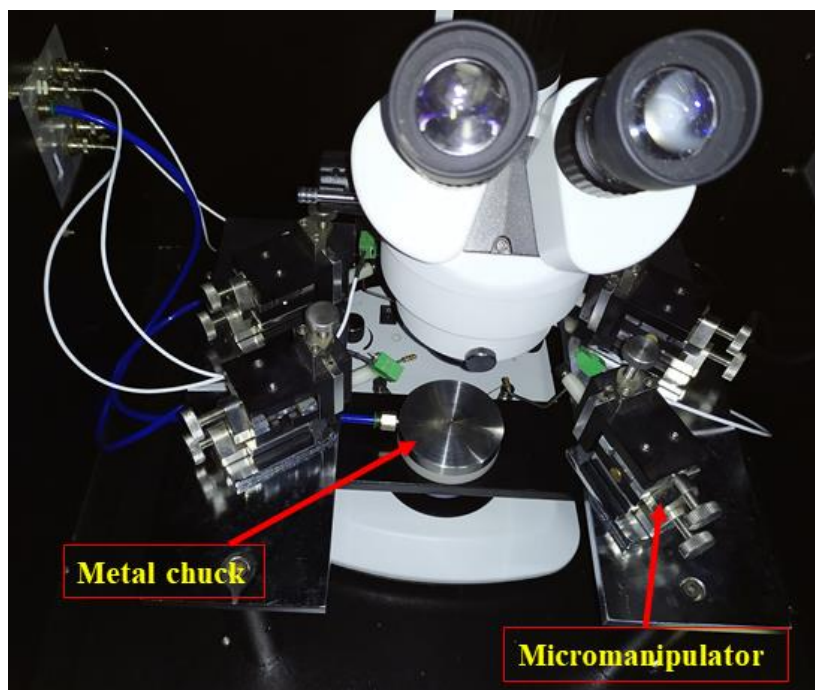


Figure 2.11 Optical image of DC probe station.

CHAPTER 3

UNDERSTANDING THE COEXISTENCE OF TWO BIPOLAR SWITCHING MODES WITH OPPOSITE POLARITY IN Cu_xO ($1 \leq x \leq 2$) BASED TWO TERMINAL DEVICES

Overview: In this work, we have fabricated and tested the resistive switching (RS) behavior of non-volatile nature in a number of devices with mainly two architectures: (1) W-tip/Cu_xO/Pt/Ti/SiO₂/Si and (2) Cu-contact-pad/Cu_xO/Pt/Ti/SiO₂/Si. The device type (1) showed coexistence of two bipolar resistive switching modes, commonly known as eight-wise (8w) and counter-eight-wise (c8w), in their current-voltage (I-V) characteristics. The formation and annihilation of metallic Cu nanofilaments was argued as the plausible reason behind the observed resistive switching events. The onset of quantized conductance steps in the typical conductance plots was exploited to provide an “indirect” proof for formation of metallic Cu-based filaments or channels during switching. On the contrary, in device type (2), we observed only “regular” bipolar switching.

3.1 Introduction

The reportedly increasing interest for realizing next generation non-volatile memories (NVMs) is perceived to have overcome some of the bottlenecks faced by the present CMOS based memory (Wong and Salahuddin 2015) (Banerjee 2020). There is an urgent need for an appropriate, non-charge-based memory technology to find a suitable alternative in order to go beyond von Neumann computing. Ferroelectric-random-access-memory (FeRAM) (Eshita et al. 2018), phase-change-random-access-memory (Xie et al. 2018) and resistive-random-access-memory (RRAM) (Shen et al. 2020) are the prominent emerging NVM technologies. Among them RRAM is considered to be very useful due to its remarkable features such as excellent scalability, low operational voltage (< 3 V), high endurance, simple structure, ease of fabrication and process compatibility with existing CMOS (Zahoor et al. 2020) (Wang and Yan 2019) (Espinal et al. 2018) (Lee and Lu 2017). As explained before, RRAM devices can modulate and retain their internal state variable(s) whenever needed (Prezioso et al. 2015) (Sheridan et al. 2017) (Zidan et al. 2018). Ability to form 3D stacking has made RRAMs an effective tool for extremely high-density data storage applications (Hou et al. 2019).

3.2 Experiments

In this work, we investigated the RS phenomena in RRAM cells fabricated using thin films of variants of oxide of copper (Cu_xO with $1 \leq x \leq 2$). We fabricated two types of devices with architectures: (i) W-tip/ Cu_xO /Pt/Ti/ SiO_2 /Si and (ii) sputter-deposited Cu-contact-pad/ Cu_xO /Pt/Ti/ SiO_2 /Si. Hereafter, we will use acronyms W tip- Cu_xO for device type (i), and Cu- Cu_xO for device type (ii). Why we chose copper centric device for our research has already been discussed in detail in Chapter 2.

The two different types of Cu_xO -based RRAM devices, as mentioned above, were fabricated using DC magnetron reactive sputtering technique. In the first set of devices, the functional oxide layer of Cu was sputtered on Pt coated SiO_2 /Si substrate wafer in presence of regulated oxygen pressure. Tungsten metal (W) probe tips of 25 μm diameter were used as the top electrode (TE). Platinum (Pt) acted as the bottom electrode (BE). Titanium (Ti) layer was used for good adhesion between the top Pt layer and the bottom SiO_2 /Si wafer substrate. The argon and oxygen flow rates inside the sputter chamber during oxide layer deposition were kept around 15 sccm and 10 sccm, respectively, which resulted in a chamber pressure of 4×10^{-2} mbar during deposition. The substrate temperature during sputter deposition was maintained at 200 °C. The fabrication process flow of Cu_xO based RRAM device is shown in Figure 3.1.

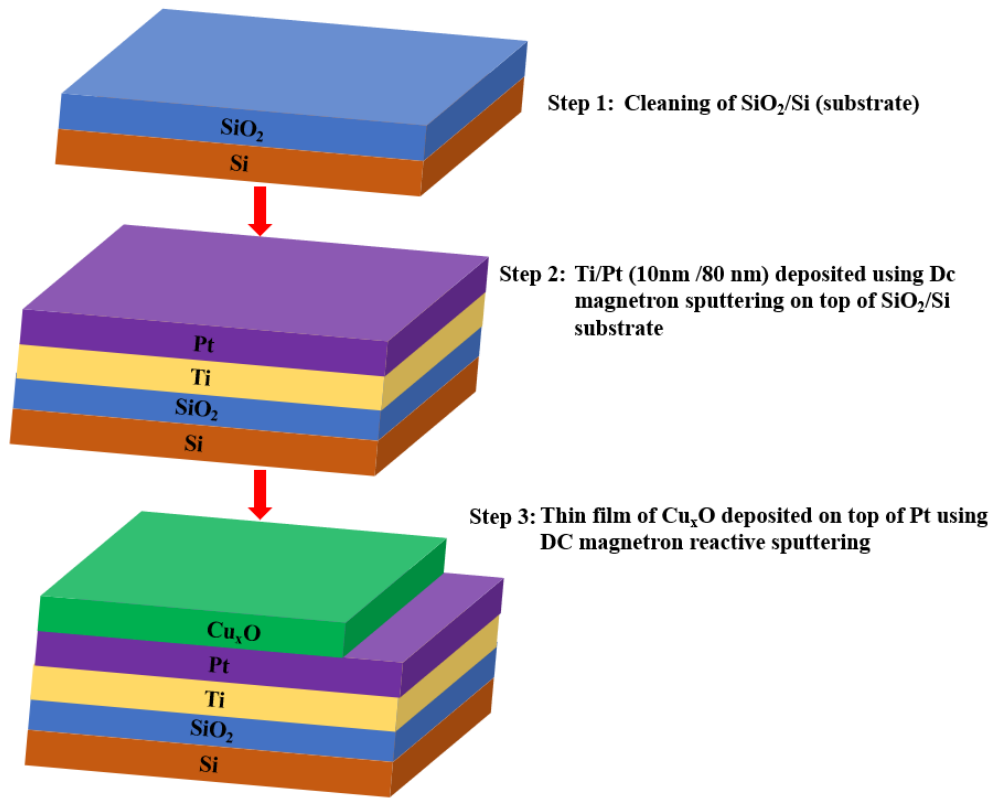


Figure 3.1 Fabrication process flow of Cu_xO based RRAM device.

The schematic of the W-tip/Cu_xO/Pt(80 nm)/Ti(10 nm)/SiO₂(300 nm)/Si device is shown in Figure 3.1(a) and its optical image in Figure 3.2(b). Secondly, we fabricated another set of devices with pure copper (Cu) metal as TE deposited on the same Cu_xO/Pt/Ti/SiO₂/Si heterostructure using the DC magnetron sputtering with shadow masks having patterned holes of 300 μm diameter, as shown in Figure 3.2(c) and 3.2(d). We performed charge based current-voltage (*I-V*) measurements on these memory cells using Keithley 2614B dual channel source/measure unit (SMU) in fully open-air conduction. The investigation on surface morphology, atomic composition and oxidation states of the sputter-deposited Cu_xO film were carried out using field-emission scanning electron microscopy (FESEM Gemini Ultra 55) and X-ray photoelectron spectroscopy (XPS Axis Ultra), respectively.

For W tip-Cu_xO cells, we observed two distinct bipolar resistive switching (BRS) modes that appeared in *opposite bias polarities*. Similar switching behavior was also observed in a number of cells made from variety of oxides in the past (Zhang et al. 2018) (Muenstermann et al. 2010) (Shibuya et al. 2010). In such situations, one can switch the device in both polarities in such a way that the same device can SET in positive voltage and RESET in negative voltage, and then SET in negative voltage and RESET in positive voltage. Strikingly, for Cu-Cu_xO devices, only *regular* BRS was observed, wherein SET happened only on positive polarity and RESET only on negative polarity of bias voltage. Details of both these types of switching events have been elucidated in the subsequent sections.

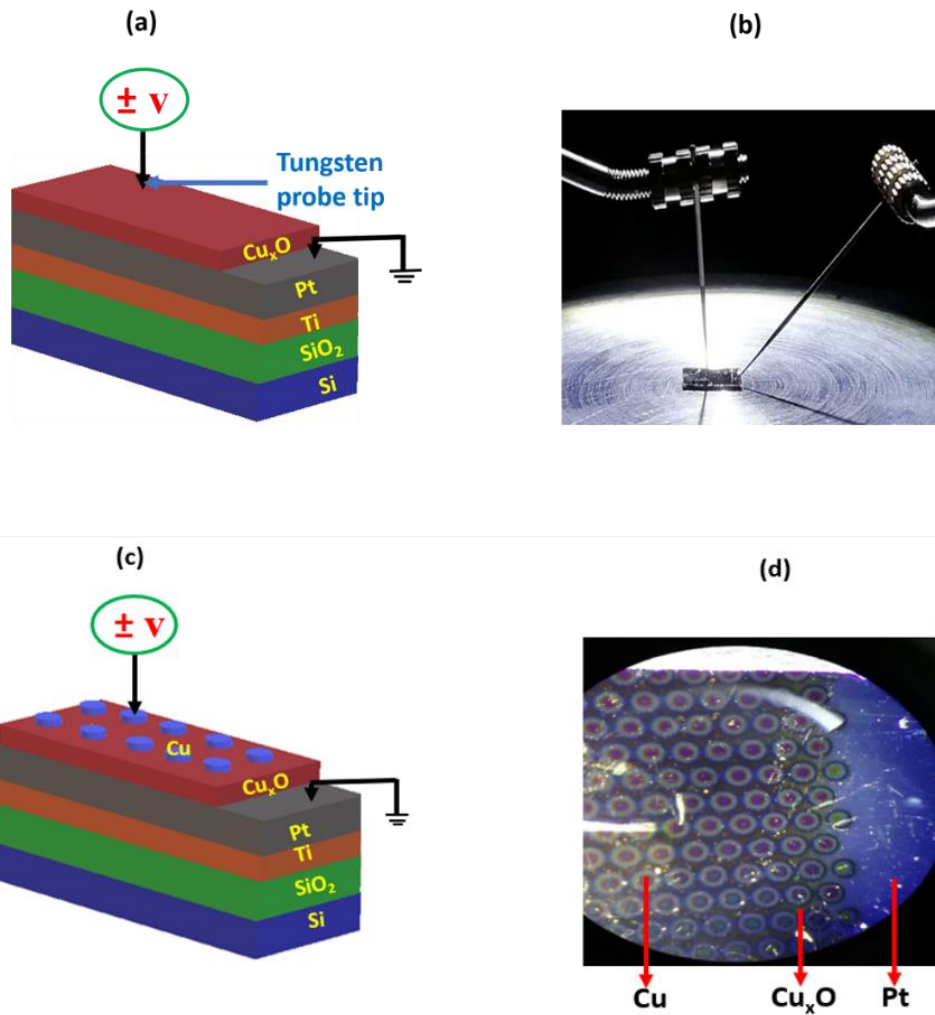
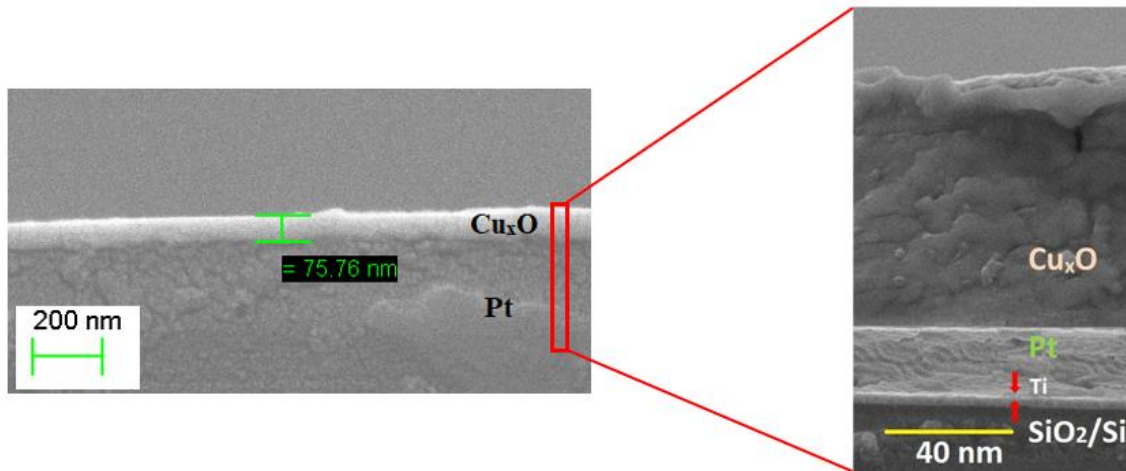


Figure 3.2 (a) Schematic representation of the biased W-tip/ Cu_xO device with Pt as BE and tungsten probe tip (of $25\ \mu\text{m}$ diameter) as TE (M-I-M configuration), (b) Optical image of probed W tip - Cu_xO device used for electrical characterization. (c) Schematic diagram of the biased Cu- Cu_xO device, (d) Optical image of Cu- Cu_xO devices wherein Cu metal pads were deposited on $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$ by DC magnetron sputtering using shadow mask technique. These Cu metal pads act as TE and Pt as BE.

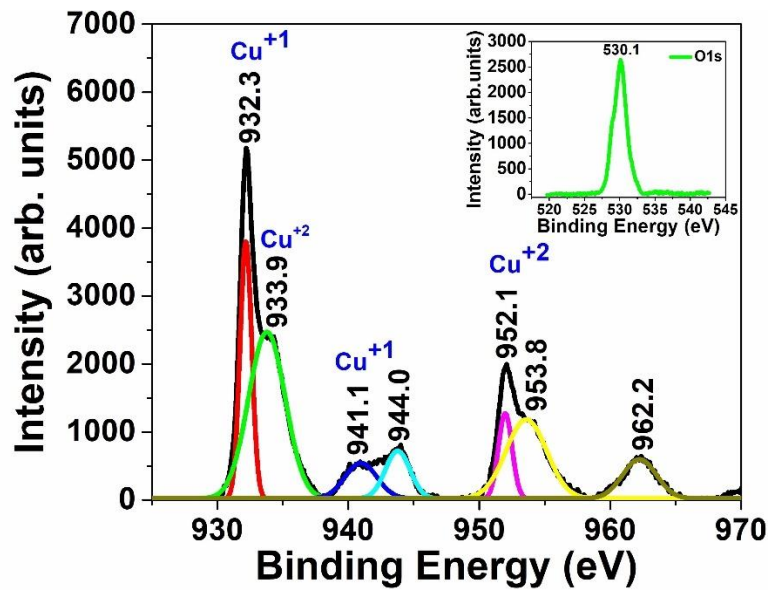
3.3 Results and discussion

3.3.1 Structural characterization

Figure 3.3(a) shows a cross-sectional scanning electron micrograph of the Cu_xO thin film deposited on Pt coated Si wafer. The thickness of the Cu_xO film was estimated to be around 75 nm. The XPS data, as shown in Figure 3.3(b), demonstrates binding energy peaks of Cu $2p_{3/2}$ and Cu $2p_{1/2}$ -- an indicative of the presence of Cu_2O and CuO phases, respectively (Lv and Tang 2011). R. Ebrahim *et al.* (Ebrahim et al. 2013) found one more peak for metallic Cu phase in addition to these two oxide phases. However, in our device, we did not observe the presence of metallic phase of Cu, and therefore, the initial LRS could not be found in our charge transport data. The Cu $2p_{3/2}$ peaks centered at binding energy values of 932.3, 933.9, 941.1, 944 eV indicate the presence of Cu_2O phase and the single peak at 933.9 eV showed the presence of CuO phase in the oxide matrix (Lv and Tang 2011) (Ebrahim et al. 2013) (Stadnichenko et al. 2008). The peaks at 941.1 and 944 eV are the satellite peaks. The onset of CuO phase in the Cu_xO thin film gradually shifts the position of Cu $2p_{3/2}$ peak towards higher binding energy values (932.3 to 933.9 eV). Additionally, the Cu $2p_{1/2}$ peaks at 952.1, 953.8 and 962.2 eV indicate the presence of CuO phase. The two Cu $2p_{3/2}$ peaks centered at 932.3 and 933.9 eV represent the Cu^{1+} and Cu^{2+} phases, respectively. The area under the peak centered at 932.3 eV is larger than that at 933.9 eV. This difference in area implies that the Cu_2O (Cu^{1+}) phase is more predominant over CuO (Cu^{2+}) phase (Lv and Tang 2011) (Ebrahim et al. 2013) (Stadnichenko et al. 2008).



(a)



(b)

Figure 3.3 (a) Cross-sectional SEM image of Cu_xO thin film grown on Pt coated Si substrate using DC magnetron reactive sputtering at 200°C . Thickness of the film is ~ 75 nm. (b) XPS spectra of the sputtered Cu_xO thin film showing the Cu^{+1} and the Cu^{+2} peaks. Inset image depicts O1s peak showing presence of oxide phases.

3.3.2 Electrical transport measurement

The I - V characteristics of the W tip - Cu_xO device were studied by sweeping the device through DC bias voltage applied between the top (W tip) and the bottom (Pt) electrodes. We observed very robust, repetitive and uniform switching between two distinct resistance (or current) levels in this metal-insulator-metal (M-I-M) configuration, as shown in Figure 3.4. All measurements were performed at room temperature and at ambient condition. During measurements, a compliance current (I_c) of 500 μA was prefixed in order to protect the device from permanent dielectric breakdown. The device remained in a high insulating state with an initial resistance of 66.5 $\text{M}\Omega$. An electroforming process was required to create defects in the oxide and push the device into the switching regime. This could SET the device to the switching mode from HRS to LRS, as can be seen in Figure 3.4 (a).

On sweeping the W tip - Cu_xO memory cell, using DC bias from 0 V to 5 V, we observed an abrupt change in current (transition from HRS to LRS) at a bias of 3.34 V, while keeping with $I_c = 500 \mu\text{A}$. This drives the cell into the *electroforming* process which happens across the bulk of the oxide matrix. Post this forming process a negative voltage sweep of 0 V to -2 V (with a compliance current of 10 mA) was sourced to the device, which RESET (transition from LRS to HRS) the device at voltage - 0.75V to a new HRS lesser than the resistance found before forming process. The device could now be cycled repeatedly between the HRS and the LRS. For all our W tip - Cu_xO memory cells, SET process occurred at positive polarity of bias voltage and RESET process at negative polarity (applied at the TE). This indicates the onset of *regular* BRS behavior. The semi logarithmic I - V graph of BRS characteristics observed in W tip - Cu_xO devices is shown in Figure 3.4 (b).

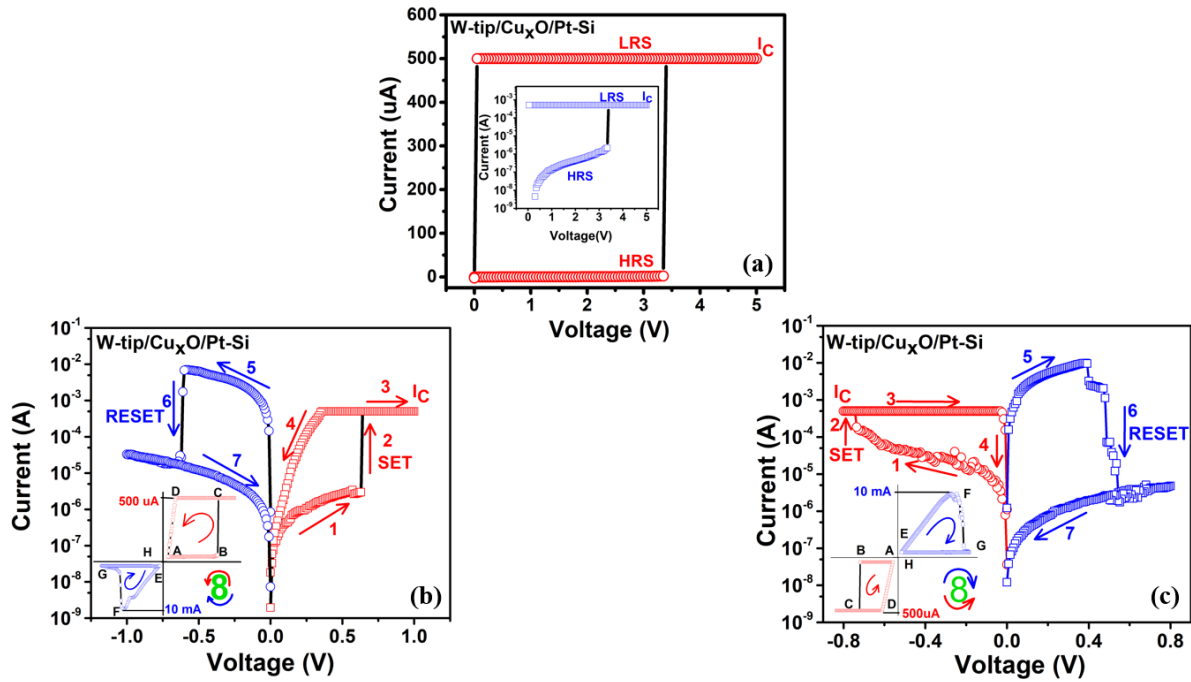


Figure 3.4 Results obtained from electrical characterization of W tip – Cu_xO devices. (a) Electroforming process with a compliance current of $500 \mu\text{A}$. Inset image shows corresponding semi-logarithmic plot (b) I - V plot (semi- logarithmic) of 8w BRS. The numbers 1 to 7 with the arrows represent one switching cycle with SET process under positive bias voltage and RESET process under negative bias voltage applied at the top W electrode. Inset image shows the corresponding normal I - V plot with SET and RESET in the upper (ABCD, in red) and lower (EFGH, in blue) halves, respectively, which resemble the drawing direction of handwritten ‘8’. (c) I - V plot (semi-logarithmic) of c8w BRS. The numbers 1 to 7 with the arrows represent one switching cycle with SET process under negative bias and RESET process under positive bias voltage applied at the top W electrode. Inset image shows the corresponding normal I - V plot with SET and RESET in the lower (ABCD, in red) and upper (EFGH, in blue) halves, respectively, which resemble the opposite drawing direction of handwritten ‘8’.

Once this RESET was attained, we gradually increased the positive bias at the top W tip (from 0 to 1 V, $I_c = 500 \mu\text{A}$) again, as shown in Figure 3.4 (b). We observed that the current was initially very low ($\sim 10^{-9}$ A), indicating the HRS of the device. However, it started increasing with increase in voltage which is shown by arrow-1, and at some threshold value of the bias the current shot up abruptly, driving the cell into the SET process, as indicated by arrow-2, in Figure 3.4 (b). Owing to the prefixed compliance current, even with further increase in bias voltage, the current remained constant thereon, as marked by arrow-3. Then the current decreased with decrease in voltage by maintaining the already obtained LRS (arrow-4). When the bias voltage polarity at TE was reversed, the device maintained its LRS (arrow-5) till the threshold voltage at which the device switched back from LRS to HRS (which we can call RESET process), as indicated by arrow-6. When the voltage decreased to zero the current also decreased by maintaining the cell in the same HRS, as can be seen with arrow-7. This one SET process and one RESET process constitute a full RS cycle for the RRAM device. It is noteworthy that apart from this regular BRS events, we also observed another peculiar switching behavior which we, hereafter, call *reversed* BRS – implying that we could observe an opposite hysteresis loop with SET process at negative bias polarity and RESET process at positive polarity (at TE). So, the device showed two distinct BRS modes in both positive as well as negative bias polarities. This switching pattern is similar to the ones reported in Ref. (Zhang et al. 2018) (Muenstermann et al. 2010) (Shibuya et al. 2010). Interestingly, Y. Sharma *et al.* reported a number of switching modes with both unipolar as well as bipolar nature in amorphous LaHoO₃ based memory cells (Sharma et al. 2015). Contrary to that, we observed only two distinct BRS modes that appeared in opposite polarity. The appearance of two BRS modes in both polarities and the absence of unipolar switching in our W tip-Cu_xO cells can, therefore, be termed as “two coexisting BRS modes” (Zhang et al. 2018).

In order to examine the above-mentioned RS behavior, a negative voltage sweep was sourced into the device. We observed a change in resistance from HRS to LRS (SET) at a bias of - 0.73 V. A positive voltage sweep could RESET the device at bias of 0.4 V. This reversed BRS behavior is shown in Figure 3.4 (c). The compliance current was kept the

same ($I_c = 500 \mu\text{A}$) in both the regular and reversed BRS. The switching process in both regular and reversed polarities happened in a range of $\pm 0.3\text{V}$ to $\pm 0.6\text{V}$ which confirms the coexistence of two BRS modes in opposite polarities. The RESET process was initiated by relatively a high current of 10 mA in both regular and reversed BRS. These switching modes are commonly called eight-wise (8w) and counter-eight-wise (c8w) BRS, respectively (Zhang et al. 2018) (Muenstermann et al. 2010) (Shibuya et al. 2010) (Shibuya et al. 2010). The I - V plot of regular BRS (SET under positive bias and RESET under negative bias applied at TE) resembles the drawing direction of handwritten ‘8’, as shown in the inset image of Figure 3.4 (b) with SET and RESET processes in upper (ABCD, in red) and lower (EFGH, in blue) halves, respectively. This is called 8w BRS. Similarly, the I - V plot of reversed BRS (SET under negative bias and RESET under positive bias applied at TE) shows the opposite drawing direction of handwritten ‘8’, as shown in the inset image of Figure 3.4 (c) with SET and RESET processes in lower (ABCD, in red) and upper (EFGH, in blue) halves, respectively. This switching scenario is known as c8w BRS. In a nutshell, controlled application of voltage at TE and appropriate compliance current resulted in two kinds of BRS events in W tip - Cu_xO devices. The I - V plots for 8w and c8w BRS are shown in Figure 3.4 (b) and 3.4 (c), respectively, wherein numbers “1” to “7” represent one full switching cycle. Inset shows the corresponding normal I - V plots. In both cases, once the switching happened the device maintained its states even after the removal of bias – implying non-volatility of the memory cells. In this way we could switch the device for a large number of cycles, and it showed repetitive and reliable RS behavior. Figure 3.5(a) depicts the first 110 switching cycles. We performed these charge transport measurements on nearly ten W tip- Cu_xO memory cells fabricated at different slots and observed similar switching behavior in all. We found that the switching voltage varied only in the small range of 0.33 V - 0.58 V in almost all cells, as can be seen in Figure 3.5(a). Obtaining such different switching windows is beneficial for them to be useful for practical device applications (Sterin et al. 2020). In regular BRS, we could observe the resistance change from $10.8 \text{ M}\Omega$ to 179Ω , which yields ON/OFF ratio $\sim 10^5$. This is several order magnitude higher than the value reported by R. Ebrahim *et al.* (Ebrahim et al. 2012). Figure

3.5(b) shows the distribution of resistances at HRS and LRS for first 110 cycles. Inset figure shows the variation in resistance at LRS (in a zoomed-in scale).

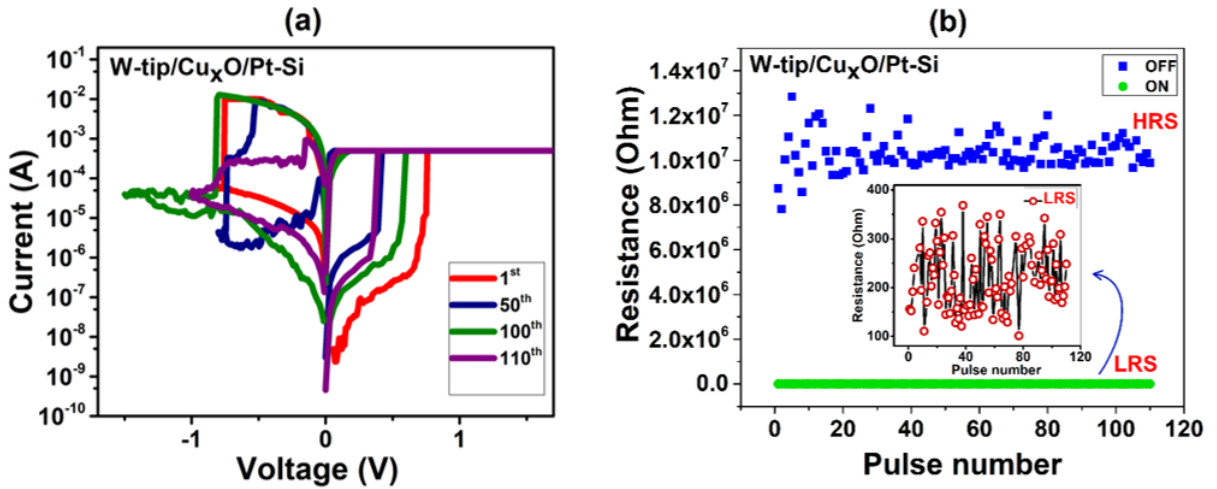


Figure 3.5 (a) *I-V* curves showing repetitive sweeping cycles of bipolar nature in W tip - Cu_xO devices for first 110 cycles. (b) Distribution of resistances at HRS and LRS for 110 cycles. Inset figure shows the variation in resistance at LRS.

Retention characteristics were studied by setting the device to LRS and applying a read voltage of 100 mV to keep the cell at that resistance state (binary ON) for 15×10^3 sec, followed by resetting the device to HRS and observed the resistance state (binary OFF) for same duration and with the same read voltage. The device was found to retain its two distinct resistance states for 15×10^3 sec without undergoing any noticeable change / drop in current. This is an indication that the Cu_xO based cells can be explored for fabricating nonvolatile memory for long-term data storage application. The retention characteristics of the device is shown in Figure 3.6 (a).

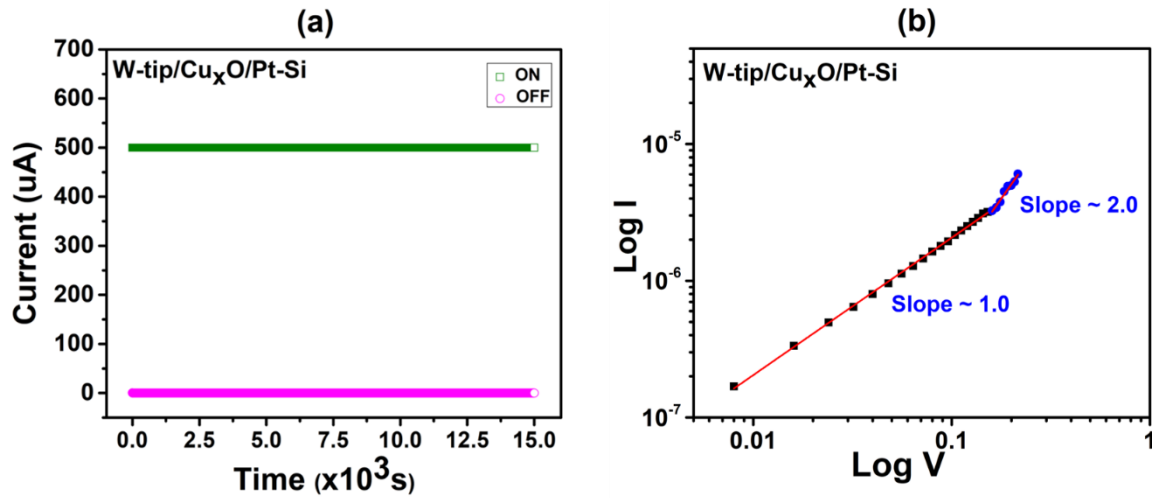


Figure 3.6 (a) Time retention characteristics of the resistance states of W tip - Cu_xO device for 15×10^3 sec read at 100 mV (b) Linear fit of $\text{Log } I$ vs $\text{Log } V$ curve for HRS with slope of 1 in the low voltage regime and 2 in the high voltage regime, confirming SCLC conduction.

With a view to analyzing the exact charge transport mechanism underlying our observed RS, we redrew I - V characteristics in Log-Log scale. As can be seen in the linear fit of the logarithmic I - V plot (shown in Figure 3.6 (b)), initially the current directly follows the voltage applied at the TE (Ohmic transport as given by $J \propto V$). Contrary to the linear behavior of current density in the low bias regime (< 0.152 V), we observed a sharp increase in current as we ramped up bias voltage further (> 0.152 V); the current follows $J \propto V^2$ law (Sterin et al. 2020). The slope of the $\text{Log } I$ - $\text{Log } V$ plot changes from 1 to 2 as the bias increases from very low to high values. This transport model carries a reminder of the space-charge-limited-current (SCLC) mechanism. In the regime of sufficiently low applied bias voltage (at the top W electrode tip), the number of thermally generated free charge carriers is abundantly higher in the oxide matrix than the injected carriers from the electrode. Here, the current directly depends on the applied bias and the conductivity of the bulk oxide film follows straight Ohm's law, and the slope of $\text{Log } I$ - $\text{Log } V$ plot is 1. Beyond a threshold voltage thermally generated carriers were dominated by the injected excess

carriers, resulting in a conduction process controlled mainly by shallow traps, as given in the equation below (Dong et al. 2007) (Waser et al. 2009):

$$J = \frac{9\varepsilon_r\varepsilon_0\mu V^2}{8L^3} \left(\frac{N_c}{N_t}\right) e^{\frac{-E}{kT}}, \dots\dots\dots(3.1)$$

where, ε_r is the static dielectric constant of the oxide material, ε_0 is the permittivity of free space, μ is the hole carrier mobility, V is the applied bias voltage, L is the film thickness, N_c is the effective density of states in the valence band, N_t is the number of shallow traps, E is the effective trapping potential and T is the working temperature. Further increase in current indicates the existence of deep traps which were distributed around trap level energies. The increase in the applied bias leads to the formation of a space-charge region by occupying the existing trap centers by the injected carriers. The conduction process then changes from trap-assisted to trap-filled event. With the further increase of voltage, the transport becomes completely trap-free (Chiu 2014) and subsequently the slope of the Log I - Log V plot reaches the value 2.

Many research reports – some directly and some indirectly – suggest the filament theory as the possible mechanism that drives the RRAM between two distinct electrical resistance states. The most prominent “direct” evidence for the filament formation includes *in-situ* transmission electron microscopy (Barman et al. 2016) and detection of local enhanced conductivity (Chae et al. 2008) (Son and Shin 2008). Another alternative way – though “indirect” – could be the observation of “quantized conductance” in the electrical conductance plot in *ballistic* transport regime. The quantization of electrical conductance in the units of $2e^2/h = (12.9 \text{ k}\Omega)^{-1}$ (where, e is the electronic charge and h the Planck's constant) is a signature of narrow and short (length scales comparable to conduction electrons' Fermi wavelength) one-dimensional quantum wires or transport channels (Das et al. 2019) (Das et al. 2017). Such systems (discovered in late 80s) are historically known as quantum point contacts (QPCs) (Wees et al. 1988) (Wharam et al. 1988). We can see the quantization of electrical conductance in two different types of such 1D structures –

top-gated (Wees et al. 1988) (Wharam et al. 1988) and side-gated (Das et al. 2019) (Das et al. 2017) QPC devices. Typical quantization of conductance in QPC is shown in Figure 3.7 (a), (b) and (c).

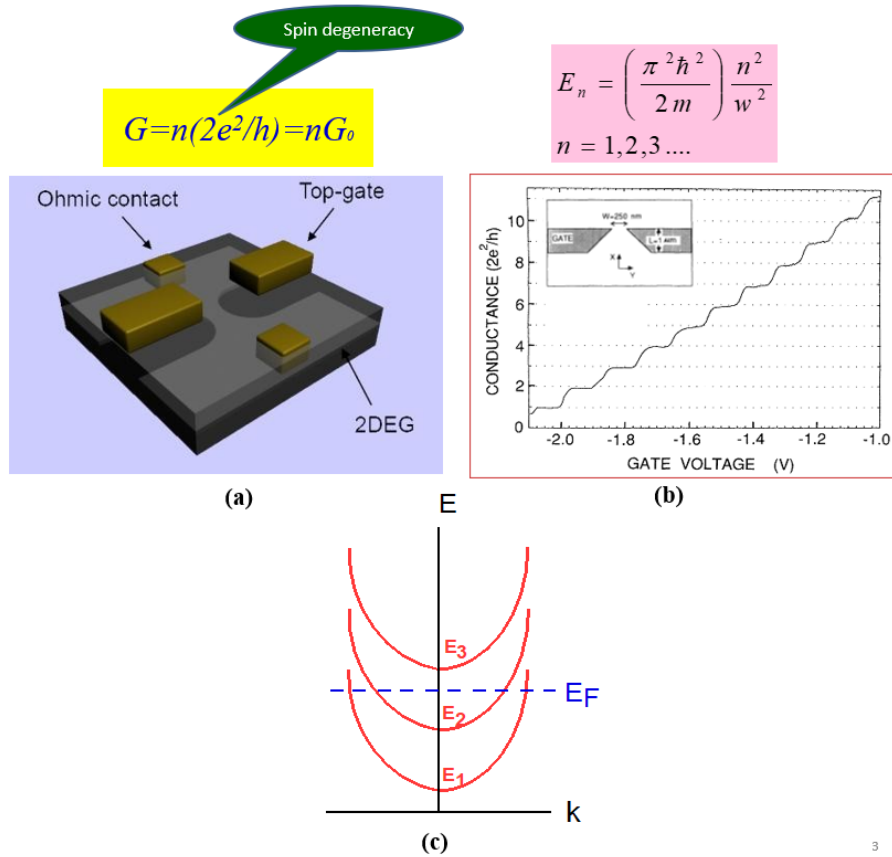


Figure 3.7 (a) The historic top-gated QPC structure on GaAs/AlGaAs 2DEG. The lithographically defined narrow channel on 2DEG underneath can be depleted to make it a quasi-1D channel by employing large negative bias on the top gates. (b) Conductance (recorded in units of $2e^2/h$) is seen as a function of bias voltage at 4.2 K temperature. Inset shows the schematic of the narrow channel with dimensions. Quantization of electrical conductance is observed in the transport data. (c) 1D sub bands in the QPC channel resemble the classic 1D potential box in quantum mechanics. The steps in conductance plot, which is a signature of 1D transport channels, are obtained as the Fermi level (E_F) sweeps through these sub bands when we change the bias potential at the two gate contacts.

The conductance quantization event is interesting not only because it offers rich physics of charge flow and resistive switching, but also it is capable of playing a major role in multilevel memories, quantum information processing and neuromorphic devices. In RRAM devices, the main transport mechanism is believed to be formation and rupture of nanoscale conductive filaments embedded in an insulating matrix (between two metal electrodes or electron reservoirs). Such nano-filaments in RRAMs resemble typical QPCs. One can now naturally expect quantum size effects — particularly the quantization of electrical conductance, for these filaments. In other words, RRAMs having resistance of the order of $12.9 \text{ k}\Omega$ or less will tend to have filaments or extended chains, as narrow as a single Cu ion or atom. From our charge transport data, the electrical conductance (G) was calculated using $G = I/V$, where I is the current through the device and V is the voltage applied to electrodes. Conductance was then recorded in units of $G_0 = 2e^2/h$, and plotted as a function of bias voltage V applied between TE and BE of our W-tip / Cu_xO based RRAM cells, as shown in Figure 3.6 (c). In the past, onset of such quantized plateaus, at conductance values of integer multiple of G_0 (Young and Sharma 2018) (Liu et al. 2013) (Wagenaar et al. 2012), half-integer multiple of $0.5G_0$ (Zhu et al. 2012), or sometimes even mix of both the levels (Zhu et al. 2012) (Gao et al. 2013) (Mehonic et al. 2013), have been reported for a number of RRAM systems. Furthermore, J. J. T Wagenaar et al. observed conductance steps around $0.1G_0$ and $0.3G_0$ in Ag_2S thin film based device (Wagenaar et al. 2012). In all of these findings, the observed conductance plateaus have been attributed to creation (during SET) and annihilation (during RESET) of conductive nanofilaments inside the switching layer. Very recently, C. Mahata et al. observed quantized steps in their transport data based on HfAlO_x memristor built for multi-level memory applications (Mahata et al. 2021). Their conductance steps were quite controllable, but at the expense of poor memory window. A typical G - V plot, as can be seen in Figure 3.8, of our W-tip / Cu_xO based devices shows plateaus around conductance values $1.2G_0$, $1.4G_0$ and $1.6G_0$.

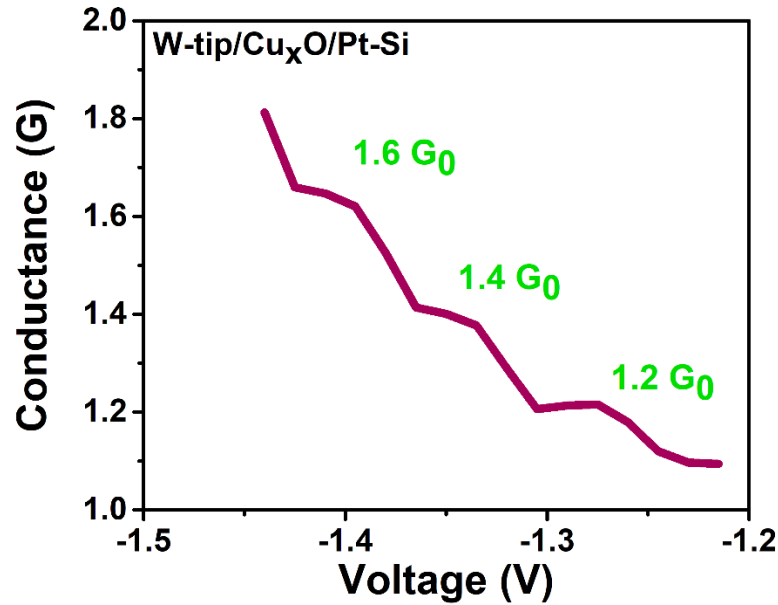
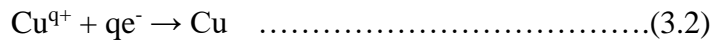


Figure 3.8 Conductance quantization steps in the conductance-voltage (G - V) plots implying presence of narrow filamentary conductive channels within the oxide matrix which are capable of facilitating repetitive sweeps between HRS and LRS.

It is noteworthy that we did not observe plateaus either at normal integer or at half-integer value of G_0 in all of our conductance plots. There is also a problem with the reproducibility of these conductance steps. The reason behind this could be the difficulty in controlling the width of the narrow bridge-like atomic constriction (unlike in a well-defined conventional QPC) between the two electron reservoirs, or the possibility of multiple such channels contributing to total conductance of the device at the same time. Therefore, before making the quantization of conductance a useful tool for building multi-level memories, we believe that further work on the device architecture is necessary. This will eventually enable us to use them in future nanodevices in new types of computer architecture.

Taking the onset of quantized conductance steps in our transport data as basis, we explain the RS processes in our Cu_xO based RRAMs using the concept of formation and rupture (or dissolution) of metallic CFs connecting the top (W tip) and bottom (Pt)

electrodes through the dielectric matrix. A. Mehonic *et al.* (Mehonic et al. 2013) argued that the impossibility of maintaining large difference in chemical potentials ($\Delta\mu$) between the two electron reservoirs (TE and BE) can be treated as a characteristic of metallic filaments-based ECM memory cells. Their findings serve as an incentive for us to build our argument around metallic (Cu) filaments formed and ruptured during the RS event (the chemical potential values of W and Pt are very close – 9.75 eV and 9.74 eV, respectively). The electrochemical formation of Cu metal filaments in the active switching layer during SET process and its dissolution during RESET process can be explained through 8w BRS, as elucidated above. The processes underlying the switching in 8w BRS are shown in Figure 3.9 (a). Here, step (1) shows the initial HRS of the device. The positive voltage applied to the TE pushes the Cu^{q+} ions ($1 \leq q \leq 2$) of oxide matrix towards the BE (cathode) and starts forming the Cu nanofilaments through the electrochemical reduction process, as in the following:



This causes accumulation of Cu atoms at the bottom Pt electrode which will subsequently facilitate gradual formation of CFs towards the top (as shown schematically in Figure 3.9(a), step (2)). Further increase in positive bias will finally result in formation of the complete channel connecting the two electrodes (step (3) in Figure 3.9(a)). This Cu nano-channel reduces the oxide resistance locally and SET the device from HRS to LRS. This is device ON state. The negative voltage with relatively high compliance current (10 mA) applied to the TE initiates the joule heating and also the electrochemical oxidation process, as shown in the following:



This dissolves the previously formed Cu nanofilaments from the BE. These Cu ions will drift away from the filament causing its rupture, as we can see in step (4) of Figure 3.9 (a). This will RESET the device from LRS to HRS. This is device OFF state. It is important to

note that in this switching cycle (which was named 8w BRS beforehand), both the formation and rupture of CFs started from the BE.

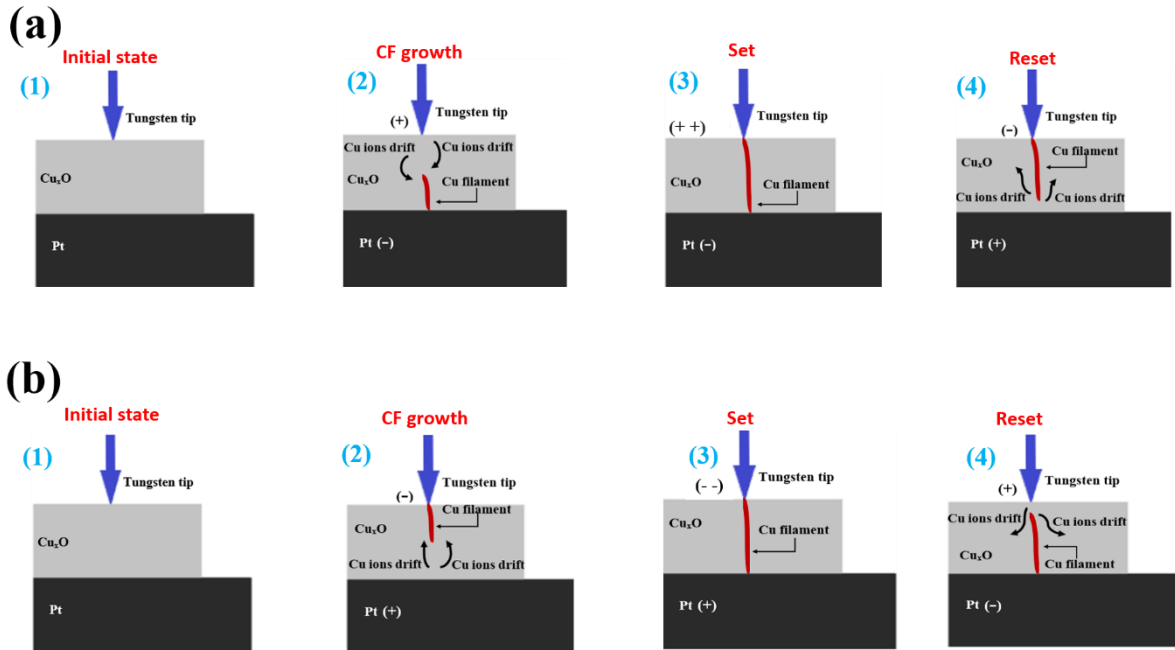


Figure 3.9 Resistive switching mechanism for (a) 8w BRS observed in W tip – Cu_xO device. Step (1)-Initial HRS, step (2)-Application of positive voltage to TE and negative voltage to BE initiates growth of conductive filament (or channel) from the BE. The filament is formed of Cu atoms which are accumulated at BE *via* reduction of Cu ions from the Cu_xO matrix. Step (3)-With increased voltage the filament starts growing and finally connects the TE and BE (SET process). Step (4)-On gradual reversal of bias polarity Cu atoms of filament near the BE get oxidized to form ions and move away from the filament which then results in rupture of the filament (RESET). (b) c8w BRS observed in W tip – Cu_xO device. Step (1)-Initial HRS, step (2)- Application of negative voltage to TE and positive voltage to BE initiates filament growth from the TE. Here, the Cu filament is formed *via* congregation of Cu atoms at TE by reduction of Cu ions from the Cu_xO matrix. Step (3)- With increased voltage the conductive filament starts growing and connects the TE to the BE (SET process). Step 4-Under reversed voltage Cu atoms in the filament near

TE get oxidized to form ions and move away from the filament which results in rupture of the filament (RESET).

During the reversed c8w BRS event, exactly the opposite of what is explained in Figure 3.9(a) happens. Step (1) of Figure 3.9 (b) shows the HRS. When a negative bias was applied to the top W probe and positive to bottom Pt electrode, Cu ions within the Cu_xO matrix would move towards the TE whereon it undergoes reduction. Thus, filaments of Cu atoms will start growing, as shown in step (2) of Figure 3.9 (b). With further increase in bias this filament connects the TE with the BE; the device will switch from HRS to LRS (step (3) of Figure 3.9(b)). On reversal of the bias polarity, the Cu atoms of the filament undergo oxidation to form ions. These copper ions will move away from the filament causing its rupture. During this reversed c8w BRS, both the growth initiation and rupture of the filament began at the TE. Thus, the regular 8w and reversed c8w BRS observed in our Cu_xO thin film based RRAMs can be explained on the basis of formation and dissolution of metallic nanofilaments made of Cu atoms.

Below we present a model to roughly estimate the size of these Cu filaments. Let us consider that the shape of the nanofilaments formed within the Cu_xO solid electrolyte is cylindrical. The energy needed to form the Cu filament, experimentally, is given as,

$$E_{experimental} = \sum_{V=0}^{V_{SET}} (\Delta V \cdot \Delta I) t_d, \dots\dots\dots(3.4)$$

where, V_{SET} is the SET voltage (0.38 V), ΔV is the step voltage (30 mV), ΔI is the current difference ($\Delta I = I_{max} - I_{min}$), I_{max} is the current at LRS (filament formation current), I_{min} is the leakage current at the HRS (as shown in Figure 3.10), t_d is the time between two data points (100 μs).

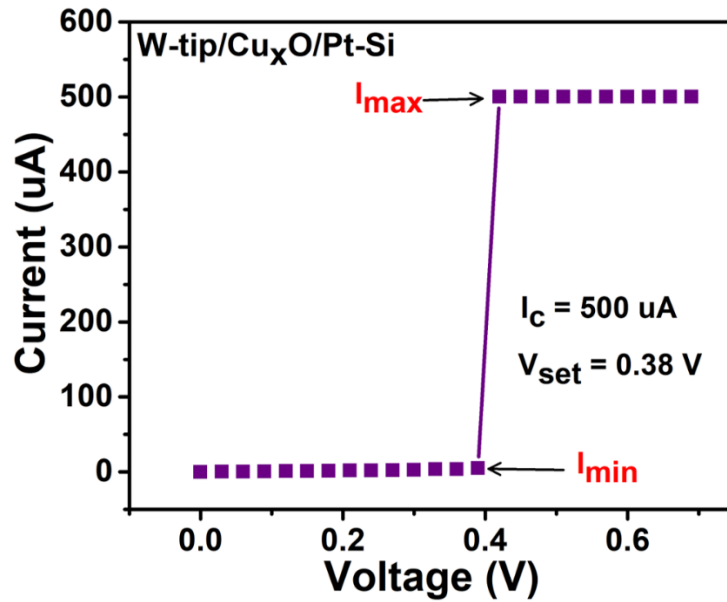


Figure 3.10 Typical current-voltage (*I-V*) characteristics in the switching regime.

The theoretical expression which represents the energy to form the filament is given as (S. M. Sze 1981),

$$E_{Theoretical} = J\phi V_{SET}t_d \dots \dots \dots (3.5)$$

$$J = ne\mu_{Cu} \frac{V_{SET}}{L} \dots \dots \dots (3.6)$$

$$\phi = \frac{\pi D^2}{4}, \dots \dots \dots (3.7)$$

where, *J* is the current density, ϕ is the cross-sectional area of the filament, *n* is the electron density in the bulk, *e* is the electronic charge, μ_{Cu} is the field effect mobility ($0.05 \times 10^{-4} \text{ m}^2/\text{Vs}^{35}$), *L* is the length of the filament ($\sim 75 \text{ nm}$).

The filament diameter can be calculated by using the equation below,

$$D = \sqrt{\frac{4L \sum_{V=0}^{V_{SET}} (\Delta V \cdot \Delta I)}{ne\pi\mu_{Cu}V_{SET}^2}} \dots\dots\dots (3.8)$$

We can obtain the resistivity of the cylindrically shaped Cu filament using the equation,

$$\rho_{Filament} = \frac{R_{LRS}\varphi}{L} \dots\dots\dots (3.9)$$

The cylindrical diameter of the Cu nanofilament was calculated to be around 115 nm with a resistivity of 1.4 $\mu\Omega$ cm, which is in corroboration with the reported literature (Lee et al. 2011). These estimated values suggest that the conductive channels were formed (during the SET process) and ruptured (during the RESET process) during RS due to oxidation and reduction of Cu ions. This is yet another indirect proof in support of metallic filamentary model for our W tip- Cu_xO cells.

It is important to note that our observed two *coexisting* BRS modes is somewhat similar to the *complementary* RS reported in the past for a number of memory cells (Yang et al. 2012) (Chen et al. 2013) (Bae et al. 2012). The complementary RS is envisaged as an effective route to suppress the unintended sneak (or leakage) current in a 3-dimentional crossbar array of memories that mainly arises due to parasitic paths around neighboring cells (Chen et al. 2013). The only difference between the two is that while observing the two distinct coexisting BRS modes the SET and RESET happened to occur in opposite polarities, whereas in complimentary RS it happens in the same polarity of applied bias. Additionally, the complementary RS has been usually demonstrated in a slightly complicated device structure comprising of two anti-serially stacked bipolar resistive switches (Yang et al. 2012) (Chen et al. 2013) (Bae et al. 2012). In contrast, we have observed the two coexisting BRS modes in a fairly simple metal-insulator-metal architecture. Therefore, it would be interesting to investigate if our observed coexisting BRS modes presented in this work could also be exploited in order to get rid of the sneak current problem in high density crossbar memory.

Next, let us discuss the RS observed in the cells having structure Cu contact pad/ $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$ devices. For brevity, we named it Cu- Cu_xO device, as already described in Figure 3.2(c) and 3.2(d). In this case, Cu metal acts as the TE and Pt acts as BE.

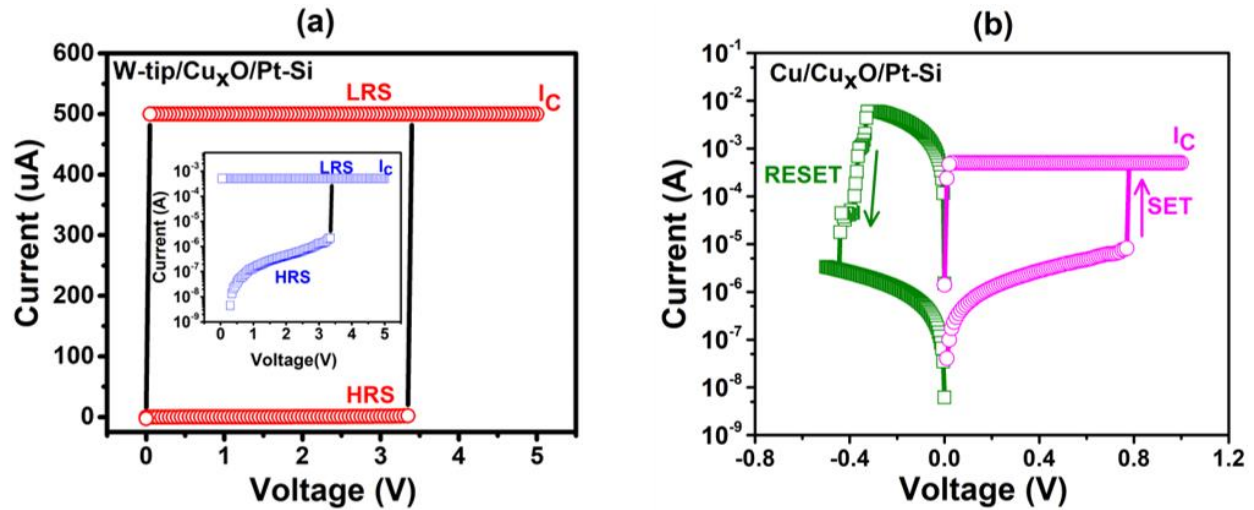


Figure 3.11 Current-voltage data obtained from electrical characterization of Cu – Cu_xO devices. (a) Electroforming process with compliance current 500 μA . Inset figure represents the semi-logarithmic plot (b) I - V plot (semi- logarithmic) of bipolar resistive switching. SET and RESET processes occurred for opposite polarity of voltages, implying that the device exhibits bipolar resistive switching.

We observed that the I - V characteristics of Cu- Cu_xO devices were different from those of earlier W tip - Cu_xO cells. Here, the device showed only “regular” 8w non-volatile BRS. The device which was initially at HRS changed its state to LRS under a positive voltage applied to the top Cu electrode. The compliance current was set at 500 μA . The forming voltage was found to be 4.8 V, which is slightly higher than the former device (with W-tip as TE). It could be owing to the interface effect which gave rise to more space-charge, and

finally resulting in a large Schottky barrier at metal-insulator interface (Scott 2014). The electroforming process is shown in Figure 3.11 (a) and its semi-logarithmic counterpart is put as inset image therein. RESET occurred at negative polarity of bias (-0.31V) applied to the top Cu electrode. The device showed stable regular BRS with SET and RESET voltages less than ± 1 V. The semi-logarithmic I - V graph in Figure 3.11(b) shows 8w bipolar switching in Cu-Cu_xO devices. It is worth taking note of the fact that we observed two coexisting BRS modes (8w and c8w) in opposite bias polarities in the W tip-Cu_xO, and normal regular BRS (8w) in the Cu-Cu_xO cells. It is because, in the former, the switching appears to be a bulk phenomenon and, in the latter, it is an interface event (Scott 2014) (as Cu contact pads were sputtered on the oxide layer). Also, in Cu-Cu_xO cells, there is a likelihood that the sputtering can locally change the stoichiometry of the Cu_xO matrix and we conjecture that the switching could be based on orientation of oxygen vacancy sites – a characteristic of EVM memory. Further study on Cu-Cu_xO cells is underway in our group and will be presented as a separate work. It would also be interesting to observe the nature of the switching with application of varied set of top and bottom electrodes at different device operation conditions.

3.4 Conclusion

In summary, the RRAM based on Cu_xO thin film deposited using DC magnetron reactive sputtering was fabricated and tested using (i) 25 micron diameter size W tip, and (ii) Cu metal contact pads as TEs. The Pt coated Ti/SiO₂/Si wafers acted as the BE for the both structures. Coexistence of two BRS modes at fairly low switching voltage for more than 110 cycles was observed in the W tip-Cu_xO cells. The resistance ratio was significantly higher ($\sim 10^5$) compared with that published elsewhere (Ebrahim et al. 2012). To the best of our knowledge, we also presented the first ever retention metric on Cu_xO based RRAMs ($\sim 15 \times 10^3$ sec). From the XPS and I - V analysis, we conclude that the RS occurred under electric stimuli due to the reduction and oxidation of Cu ions which eventually helped us build the filamentary model for RRAM operation. The same was further confirmed with the help of resistivity calculation of the Cu nanofilaments. Creation

and annihilation of nanometer-size conductive paths or filaments within the oxide layer, which played a pivotal role in observing RS, was accessed with the help of quantization of conductance phenomenon. The underlying transport mechanism was attributed to SCLC. On the other hand, the Cu-Cu_xO devices exhibited only regular 8w non-volatile BRS events. The switching occurred at a low operating voltage (<1 V). The high retention, low switching voltage and consistent switching cycles demonstrate Cu_xO based resistive memory as a potential candidate for stable, low power, highly scalable and long-term data storage applications.

CHAPTER 4

REDOX-ACTIVE VANADIUM-BASED POLYOXOMETALATE AS AN ACTIVE ELEMENT IN RESISTIVE SWITCHING BASED NONVOLATILE MOLECULAR MEMORY

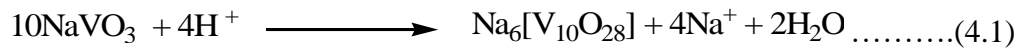
Overview: In this chapter, a new uniform, repetitive and stable resistive switching (RS) phenomenon is demonstrated based on very low- cost two-terminal metal-insulator-metal stack fabricated using a highly redox-active vanadium based polyoxometalate (POM) molecular clusters, $[V_{10}O_{28}]^{6-}$ – belonging to polyoxovanadate (POV) family. We attribute the switching event to the cycling between formation and rupture of tiny conductive nanofilaments formed due to trapping and de-trapping of positively charged ionized oxygen vacancy sites present in the active switching layer of $[V_{10}O_{28}]^{6-}$. POMs, in their rich abundance, are highly stable early transition metal oxide nanosized clusters, capable of storing as well as releasing a large number of electrons. In addition, they can undergo fast and reversible redox reactions (both in solid and liquid electrolyte media) in “stepwise” manner – a property that makes them a promising candidate for ultra-fast and multi-level non-volatile molecular memory for high-density data storage.

4.1 Introduction

In Chapter 2, we discussed at length the immediate need of exploring redox active molecular clusters for building high-speed and high-density memory. With that goal, we have explored the role of a vanadium (V) based polyoxometalate (POM) nanocluster, called *sodium decavanadate* (having chemical formula, $Na_6V_{10}O_{28}$) that belongs to *polyoxovanadate* (POV) family, as active material in our RRAM devices. Hereafter, we refer to this functional material using the acronym “SDV”. POMs are large group of molecular clusters with frameworks built from d-block transition metal oxo-anions linked by shared oxide ions, and were first explored by Jöns Jacob Berzelius in 1826 (Hill 1998) (Gouzerh et al. 2006). Since then there have been numerous discoveries of plethora of POMs with a wide range of molecular structures with versatile physical properties, electronic structures, and applications (Stuckart 2019) (Parac-vogt 2020) (Hampson et al. 2019). Though RS based memory has been reported in a wide range of materials as elucidated before, such extensive studies based on POM as active element still remain elusive.

4.2 Sodium decavanadate

SDV molecules ($\text{Na}_6\text{V}_{10}\text{O}_{28}$) were used as an active element to observe resistive switching in our RRAM device. SDV was prepared following the standard procedure described elsewhere (Hartung et al. 2015). SDV belongs to the isopoly (only metal-oxygen cluster) polyoxometalate group, wherein all vanadium atoms are connected through bridging oxygen atoms making it vanadium-oxygen cluster or polyoxovanadate (POV). Figure 4.1(a) and (b) shows a ball and stick representation and polyhedral structure of SDV nano-cluster, respectively. Presence of vanadium atoms in their highest possible oxidation state of 5+ (vanadium being a group-V transition element in the periodic table) makes the size of its cation small, and therefore, it attracts more oxygen in acidic medium, eventually producing $[\text{V}_{10}\text{O}_{28}]^{6-}$ cluster through self-assembly process, as shown in the scheme below:



In SDV, each vanadium atom is octahedrally connected *via* six oxygen atoms throughout the cluster (see Figure 4.1a).

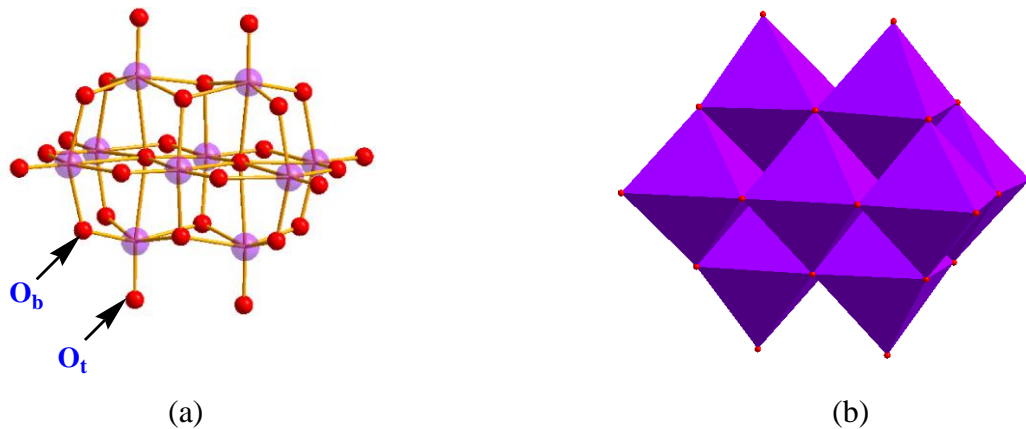


Figure 4.1 (a) Ball and stick representation of $[\text{V}_{10}\text{O}_{28}]^{6-}$, color code: red=O, purple=V, O_t = terminal, O_b = bridging oxygen (b) Polyhedral structure of $[\text{V}_{10}\text{O}_{28}]^{6-}$.

4.3 Device fabrication

The SDV crystals were dissolved in deionized water to form a solution with concentration 10 mg mL^{-1} . Drop of the as-prepared fresh solution was spin-casted on conducting indium-tin-oxide (ITO) coated glass substrate with an initial speed of 500 rpm for 40 sec followed by 1400 rpm for 50 sec. Later the substrate was kept in oven for drying at $70 \text{ }^\circ\text{C}$ for 15 min. The ITO substrate with surface resistivity of $8\text{-}12 \text{ Ohm Sq}^{-1}$ was acquired commercially from Sigma Aldrich. Prior to the spin-casting, the ITO substrate was cleaned in ultrasonic bath followed by acetone, isopropyl alcohol and deionized water treatment, each for 15 min, and finally ultraviolet/ozone treatment for the same duration. Subsequently, Cr(10 nm)/Au(80 nm) contact pads were deposited on top of Glass/ITO/SDV structure using DC sputtering technique through a shadow mask having patterned holes of about 300 micron diameter. Here, 10 nm thick Cr acts as an interfacial layer between Au pad and (semi)insulating SDV layer which facilitates better adhesion (between Au and SDV) as well as lowering of Schottky barrier height at metal-insulator interface. The ITO acts as bottom electrode and the Au as the top electrode in all our RRAM devices. Figure 4.2 shows the fabrication process flow of SDV based RRAM device.

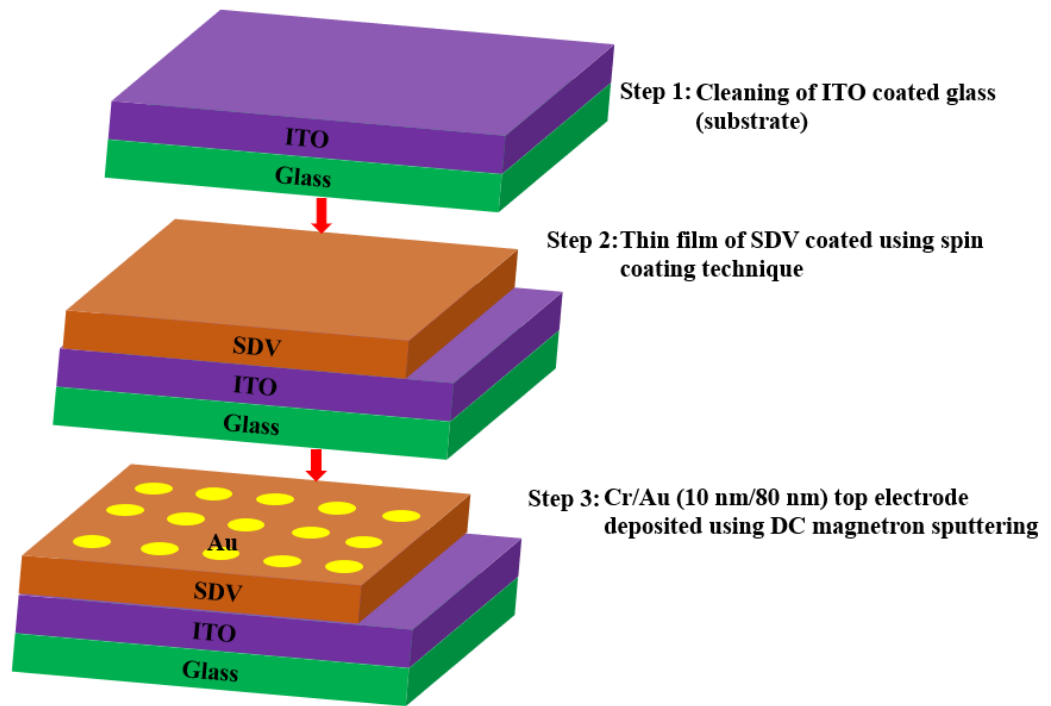


Figure 4.2 Fabrication process flow of SDV based RRAM device.

Figure 4.3(a) illustrates a 3-dimensional schematic representation of our Glass/ITO(150 nm)/SDV/Cr(10 nm)/Au(80nm) memory cell. Using field-emission scanning electron microscopy (Carl Zeiss Ultra 55 FESEM) and atomic force microscopy (Bruker Dimension Icon AFM), the thickness of the functional SDV thin film was found to be around 90 nm, as shown in Figure 4.3 (b) and (c), respectively.

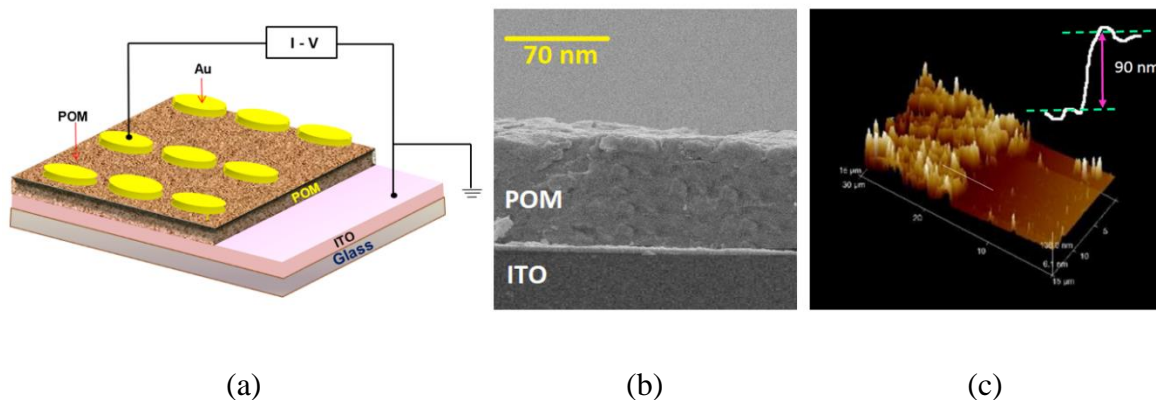


Figure 4.3 (a) Schematic representation of the RRAM device that exhibits different layers involved. Typical current-voltage measurements are performed treating Au as top contact and ITO as bottom contact, (b) Cross-sectional view of a scanning electron micrograph showing thickness of the spin-casted POM layer on top of ITO, (c) 3-dimensional atomic force micrograph of the POM layer yielding its thickness around 90 nm.

4.4 Results and Discussion

The integrity of the as-prepared SDV was verified using standard Fourier transform infra-red (FTIR) spectroscopy, UV-visible spectroscopy and energy dispersive X-ray (EDX) analysis – details of which can be found in Figure 4.4 (a), (b) and (c), respectively.

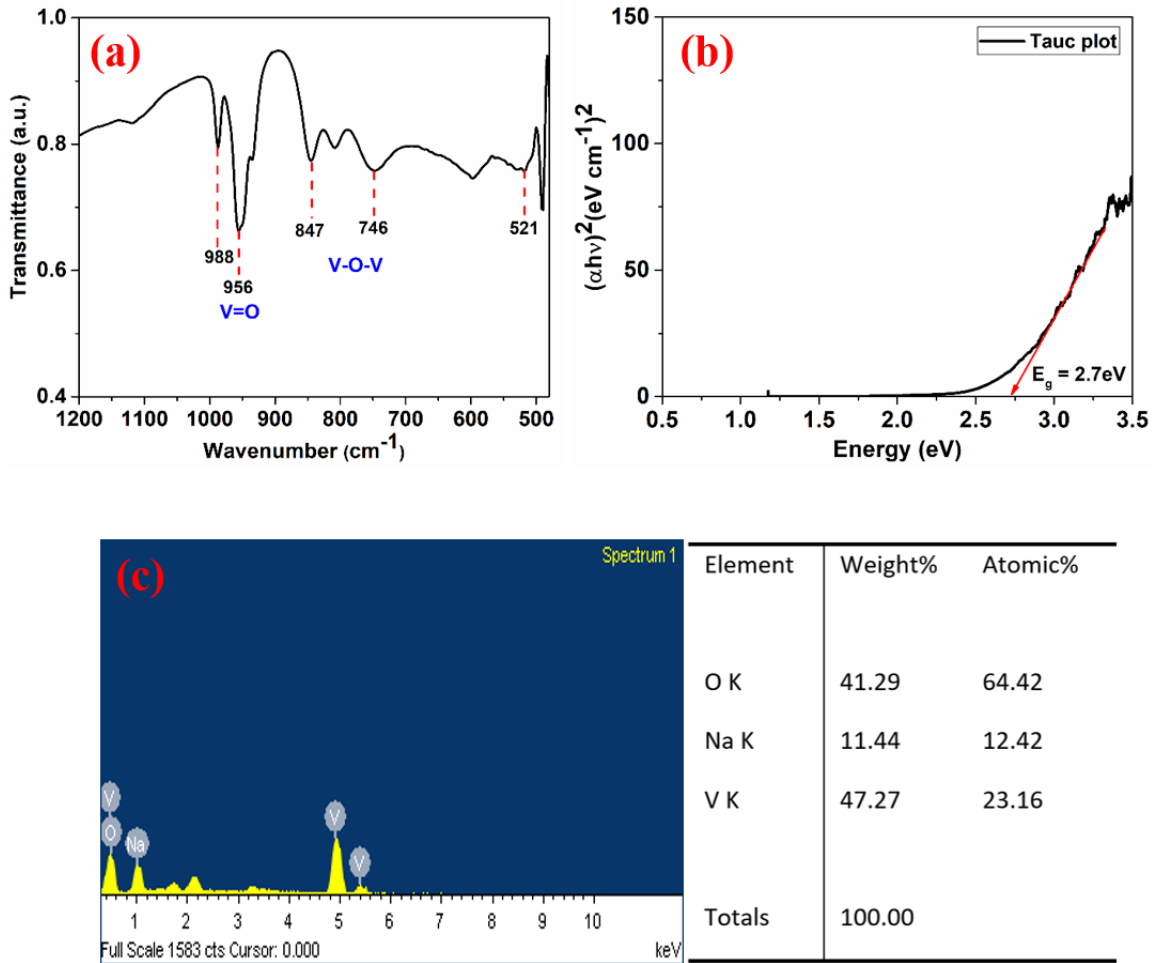


Figure 4.4 (a) FTIR spectra of Sodium decavanadate (SDV). The vibrational bands at 988 cm^{-1} and 956 cm^{-1} are attributed to V=O bond. The bands at 847 cm^{-1} , 746 cm^{-1} and 521 cm^{-1} indicates the V-O-V bond in the SDV, (b) UV-Visible spectroscopy of Sodium decavanadate (SDV), (c) Energy-dispersive X-ray spectroscopy of Sodium decavanadate (SDV).

For charge transport measurements, a Keithley 2614B source/measure unit (SMU) was used to investigate typical current-voltage (I - V) characteristics of MIM devices with Glass/ITO/SDV/Cr/Au stack. During all measurements we treated Au as the top contact and ITO as bottom contact. All I - V measurements were performed at room temperature and ambient condition. Figure 4.5(a) depicts a semi-logarithmic plot of current-voltage

characteristics of the device. Initially, the as-fabricated device was in insulating state with resistance of $10\text{ M}\Omega$ (read at 0.1 V) until the applied voltage reached $+3\text{ V}$. On reaching this voltage, an abrupt increase in current took place and the resistance dropped to a low value of $640\ \Omega$ (read at 0.1 V). The cell then enters LRS or ON-state (driving the device to a soft dielectric breakdown): the process is known as the *initial electroforming* or *forming process*. During the forming process, the compliance current (I_{cc}) was maintained at 2 mA to avoid permanent dielectric breakdown of the device due to high current flow in LRS. The LRS of the device, once obtained, persisted even when the applied voltage was gradually decreased to zero. As the voltage was again swept from 0 to $+1\text{ V}$ in small steps, a sudden drop in current (from 2 mA to $80\ \mu\text{A}$) was observed at voltage of 0.8 V resulting in abrupt increase in the resistance of the device. At this point, the device switched from LRS to HRS, referred to as the RESET process. The device can now be retained in the HRS even after removal of the applied bias and can again be switched back to LRS (SET process) after application of a voltage (generally smaller than that required to trigger initial forming process). Thus, the forming process drives the device into resistive switching regime (with device resistance between $10\text{ k}\Omega$ and $550\ \Omega$ for HRS and LRS, respectively). After the forming process, the device can alternately be switched between binary OFF and ON states. Once the device enters the switching regime, bias was swept between 0 to 1.5 V . The SET process was observed to occur at 1.2 V (red plot in Figure 4.5(a)) and the RESET process at 0.8 V (blue plot in Figure 4.5(b)). Both the resistance states, LRS and HRS, once reached can be maintained even after withdrawal of the bias, indicating non-volatile nature of the RRAM device.

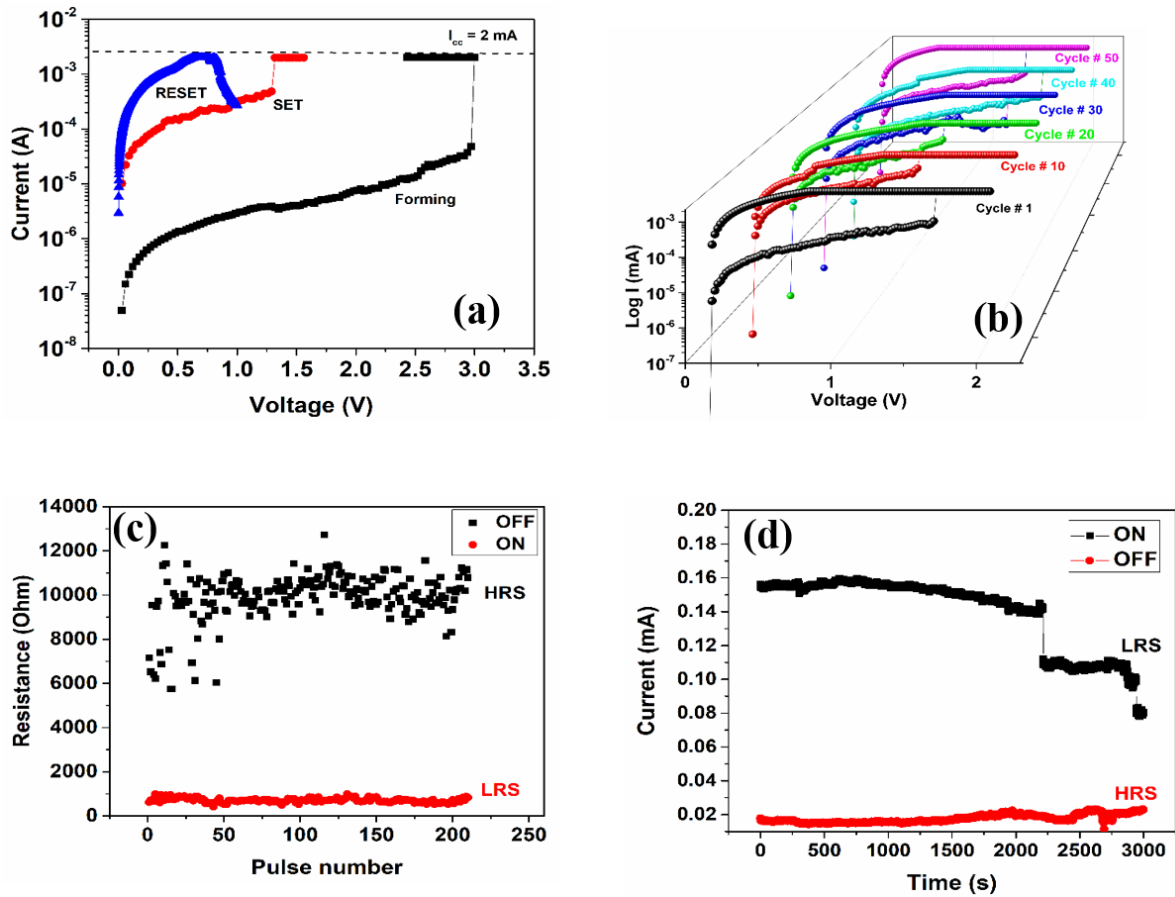


Figure 4.5 (a) Semi-log plot of current-voltage characteristic showing forming process prior to resistive switching on our SDV based RRAMs. Post forming SET and RESET states are also shown. (b) Repeatability test for the first 50 switching cycles. (c) and (d) Endurance and retention ability tests of the RRAM device, respectively.

Ten memory cells were tested and all showed uniform, repetitive, and reversible resistive switching behavior occurring at fairly low voltage (less than +2 V), suggesting their potential use for low power applications. Figure 4.5(b) shows consistent repeatability over 50 cycles with higher degree of accuracy. After repeating the switching events over a large number of cycles, the SET voltage was found to occur in the range of 1.2 V to 1.8 V (See Figure 4.5(b)). Existence of such window of operational voltages between the two binary states is an essential feature in order to have distinguishability between ON and OFF

states for practical application of POM based cells as NVM. Overall, we observed an unipolar resistive switching in our Glass/ITO/SDV/Cr/Au RRAM cell with an ON/OFF ratio of 25. The device could be maintained at distinct LRS and HRS for more than 210 cycles, as shown in the endurance plot in Figure 4.5(c). To assess the retention ability, the device was held at HRS and LRS states under read voltage of 0.1 V, as shown in Figure 4.5(d). No significant degradation of device ON and OFF states was observed for more than 2200 sec at room temperature. The device then slowly started losing its distinguishability between the two binary states, which can be attributed to gradual Joule heating process that might cause partial breakage of conductive channels formed between the contacts. There is room to improve device performance metrics (e.g., ON/OFF ratio, retention, endurance, etc.) by using proper blend of POM with binary oxide (that enhances capacitive behaviour of the cell with controlled defects in the active layer) and also novel hybrid device design.

To test the longevity feature of our RRAM device, an environment stability check was performed at regular interval of 4 weeks for straight 12 months. Figure 4.6 shows a representative I - V plot showing slight increase of SET voltage after 12 months. Except for this nominal increase in SET voltage, all other device performance parameters remained unchanged at room temperature and ambient condition even after 12 months. Our devices showed much higher longevity than that reported by A. Moudgil et al. using novel and unconventional material-based memories, such as protein (Moudgil et al. 2018).

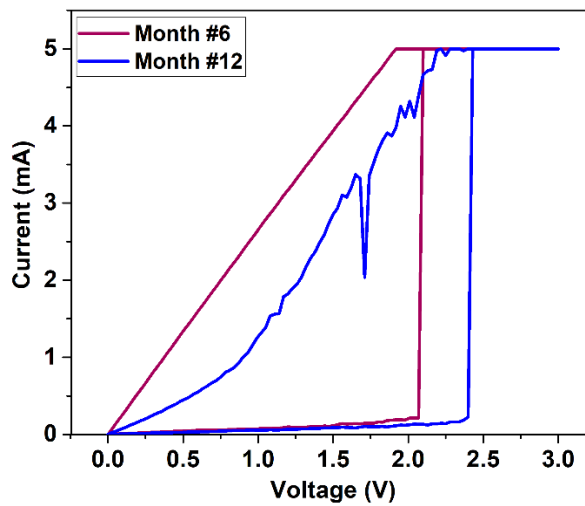
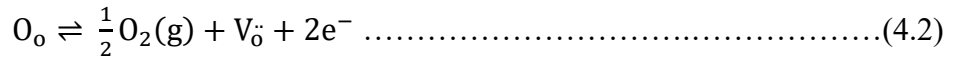


Figure 4.6 Current-Voltage (I - V) measurement recorded after 6 and 12 months.

As described in the introduction, such reversible resistive switching (RS) behavior of RRAMs (SET \rightarrow RESET \rightarrow SET) can be ascribed to formation and rupture of conductive filaments (CFs) formed inside the semi-insulating matrix sandwiched between a top electrode (TE) and a bottom electrode (BE). Such tiny CFs can form due to migration of either cationic metal ions (M^+) or anionic oxygen ions (O_2^-) from one electrode to the another. In our RRAM device, it is argued below that pre-existence of positively charged oxygen vacancy sites (which is an outcome of presence of O_2^- ions) within POV matrix triggered formation of nanoscale conductive paths between the two electrodes.

One of the striking features of POM clusters is, unlike in conventional binary transition metal oxides (e.g., TiO_2 , HfO_2 , etc.), the charge storage within POM molecules is highly delocalized throughout its metal-oxide cage. In addition, the POM molecules are highly rich in oxygen and therefore, often referred as reservoir of electrons (Vilà-Nadal et al. 2013). They are easily reducible chemical species both in solid and liquid electrolyte media. Laia Vilà-Nadal *et al.* have demonstrated that POMs can undergo reduction (or oxidation) in multiple steps under influence of electric stimuli (e.g., an applied electric field) by accepting (or releasing) electrons, and subsequently delocalizing that charge cloud

around the metal-oxide cage, without causing significant structural change or damage to its overall molecular arrangement (Vilà-Nadal et al. 2013). They also showed that this process is reversible and the molecule can be brought back to its original redox-state by applying a field in the opposite direction or by gradually withdrawing it. Standard electrochemical cyclic voltammetry provides an unambiguous proof for highly active redox behavior of all types of POMs. M. Vasilopoulou *et al.* demonstrated that such charge transfer mechanism due to redox reaction in a solid-state cell takes place at the vicinity of POM-metal contact interface (Vasilopoulou et al. 2015). Their finding is the key exploration for the observed resistive switching in our POV ($[V_{10}O_{28}]^{6-}$) based RRAM cells in terms of (redox reaction driven) onset and dissolution of CFs formed due to oxygen vacancy (OV) migration between the two electrodes. It has been shown that the OVs are, in general, likely to be more mobile than the metal cations in solid electrolyte medium of transition metal oxide under electric stimuli (Zheng et al. 2018) (Kang et al. 2017). In POM clusters, the bridging oxygen species between transition metal atoms (in our case, vanadium atoms in $[V_{10}O_{28}]^{6-}$ cage) get depleted when reduction happens, which subsequently leads to onset of OV sites around the POM molecules (Vasilopoulou et al. 2015) (Zheng et al. 2018). Depletion of oxygen species (or formation of OV sites) affects the change in valance state of the transition metal cations within POM clusters, which eventually gives rise to noticeable change in conductivity (Gam Derouich et al. 2014). Furthermore, B. E. Petel *et al.* also carried out extensive investigation of a vanadium-based POM to study presence of OV sites within the molecular cluster (Petel et al. 2018). They too argued that such vacancy sites are formed naturally at the surface of the POM clusters as a result of removal of neutral oxygen atoms from it. The structure then gets reduced through delocalization of electronic charge density. The partially filled *d*-orbitals of vanadium (V) atoms in POM molecules can accommodate added electron charge cloud causing its reduction, which subsequently triggers removal of surface oxygen ions (O_2^-). Absence of surface O_2^- ions is responsible for the onset of cationic oxygen-atom vacancy sites or simply oxygen vacancies on the surface of POM molecules according to the following oxygen exchange reaction:



where O_o and V_o^{\bullet} , following the notation of Kröger and Vink (Kröger et al. 1958), represent oxygen ions on regular lattices sites and OV_s, respectively. These OV_s act as trap sites for electrons. Furthermore, Han-Yi Chen *et al.* experimented on electron transfer mechanism within $Na_6V_{10}O_{28}$ molecules during redox reaction, and showed that under proper electric stimuli ten vanadium (V) atoms with their highest oxidation state V^{5+} could easily be reduced to V^{4+} (by adding ten electrons to the structure) (Chen et al. 2015). However, they ruled out any further reduction to lower oxidation states such as V^{3+} or V^{2+} . This phenomenon is confirmed by the observation of only one peak for reduction and another peak for oxidation in their cyclic-voltammetry plot. We have observed similar results, as shown in Figure 4.7. Recently, P. F. Avila *et al.* performed extensive density functional theory (DFT) calculation and concluded the highest possible oxidation state of all 10 V atoms in decavandate clusters as 5+ (Avila et al. 2019). The work of B. E. Petel *et al.* provides enough evidence in support of natural presence of OV_s in neutral and stable POM clusters (Petel et al. 2018). Proper external electric stimuli (in case of RRAMs, it is the bias voltage applied between top and bottom contacts) can further multiply the number of OV_s within the POM matrix facilitating fast and reversible redox reaction. The results described above are indicative that the resistive switching in our study is primarily driven by OV_s, and not metal cations.

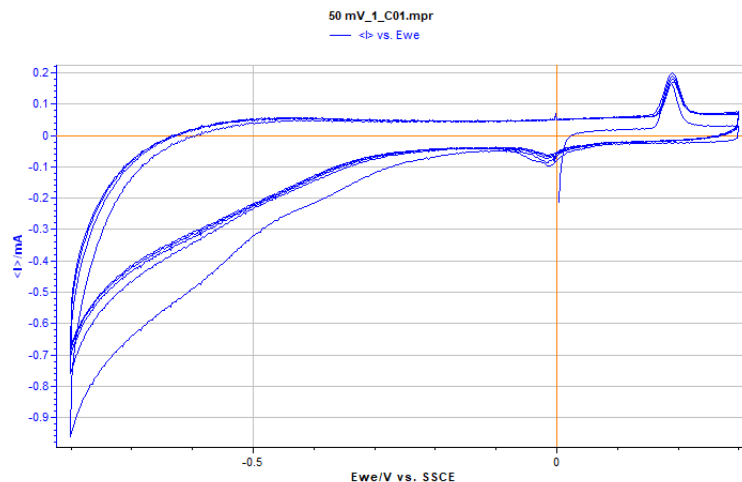


Figure 4.7 Cyclic voltammogram of Sodium decavanadate (SDV).

To further access the importance of OV as well as to know the possible oxidation states of the V atoms (present in $\text{Na}_6\text{V}_{10}\text{O}_{28}$), we performed X-ray photoelectron spectroscopy (XPS) analysis in ambient condition, as shown in Figure 4.8. The binding energy values of V $2p_{3/2}$ and V $2p_{1/2}$ levels were found at 517.2 and 524.5 eV, respectively, which are attributed to V^{5+} oxidation state (Hartung et al. 2015) (Chen et al. 2017) (Chen et al. 2014) (Silversmit et al. 2004). In general, the peak for V^{4+} oxidation state appears corresponding to binding energy of 516.2 eV; however, the same was not observed in our XPS spectra (Chen et al. 2015)– very likely due to instantaneous re-oxidation of vanadium atoms from V^{4+} to V^{5+} caused by presence of ambient air (Chen et al. 2017). Furthermore, the absence of peaks for V^{3+} and V^{2+} oxidation states in our XPS spectra corroborates findings of Han-Yi Chen *et al.* (Chen et al. 2017), as described earlier. Curve fitting of O1s XPS spectra reveals presence of lattice oxygen and oxygen vacancies in SDV. The peaks for O 1s appear at three regimes – low, middle and high binding energies, at 530.2, 531.7, 532.4 eV, respectively (Bharti et al. 2016). The peak at 530.2 eV is ascribed to the lattice oxygen ions (Silversmit et al. 2004) and that at 531.7 eV, which is very close to reported value (Bharti et al. 2007), appears due to presence of cationic OVs at the surface of SDV

molecular clusters. The XPS peak at the binding energy value of 532.4 eV corresponds to chemisorbed oxygen on the surface of the nano-clusters (Bharti et al. 2016).

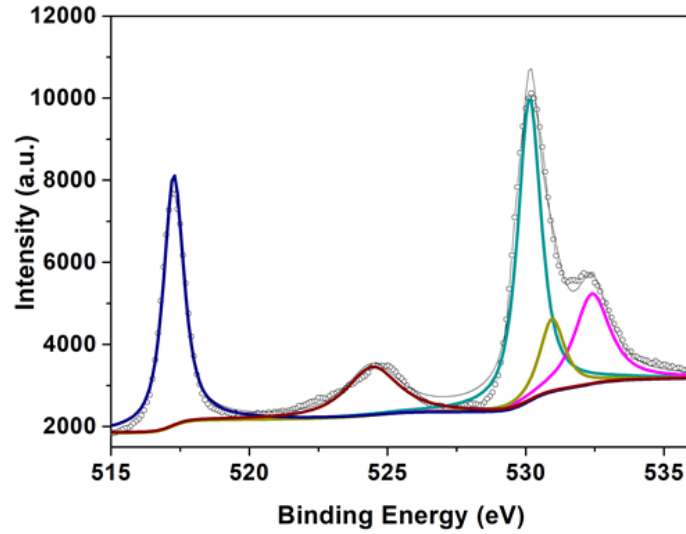


Figure 4.8 XPS spectra of polyoxovanadate ($\text{Na}_6\text{V}_{10}\text{O}_{28}$) cluster.

The migration of OV_s via energetically favorable sites present inside POM matrix facilitates “tunneling” of electrons from one electrode to the other which eventually results in a change in resistance state of the RRAM device. The following model is proposed to describe this phenomenon. In the beginning, positive bias at top metal contact produces a lot of anionic oxygen ions (O_2^-) near POM-top metal interface. As this bias increases, these O_2^- ions get activated to migrate because of lowered potential barrier, as illustrated in Figure 4.9. With the increase in positive bias the OV_s thus formed near top surface migrate towards the cathode and assemble thereon. They finally create tiny conductive filaments (CFs) or paths connecting anode (top electrode) with cathode (bottom electrode). These CFs may be broad but their bottlenecks are near the top electrode. Initially, the oxide cluster of vanadium remains at an equilibrium state with lattice oxygen atoms in gas phase. At that stage, the chemical potential of lattice oxygen μ_o can be written as (Wang et al. 1998),

$$\mu_o = \mu_o^0 + RT\ln(p/p^0) \dots\dots\dots(4.3),$$

where, μ_o^0 is standard chemical potential of oxygen, R gas constant, p oxygen partial pressure, and p^0 standard pressure of 1 atm.

On application of electric stimuli, the equilibrium is determined by both chemical potential of oxygen as well as the applied electric potential. Thus, the electrochemical potential gets modified as follows (Ashcroft and Mermin 1976),

$$\tilde{\mu}_o = \mu_o^0 + RT\ln(p/p^0) + ZF\varphi \dots\dots\dots(4.4)$$

where, Z is 1 for an electron and 2 for an oxygen anion, F the Faraday constant, and φ the electrostatic potential. The electrochemical potential governs the process of oxygen anion (O_2^-) migration between electrodes. In this process, one electrode supplies electrons to the oxide matrix, which reduces V^{5+} to V^{4+} . Simultaneously, one electron is extracted from O_2^- to oxidize it to an O atom at the other electrode.

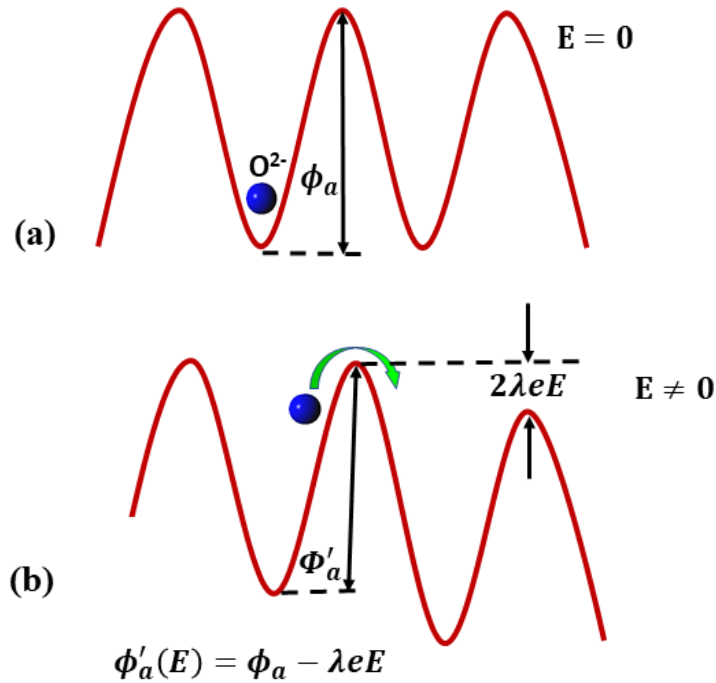


Figure 4.9 Schematic of the model describing the electric field effect. Top image (a) depicts energy barriers offered to oxygen anions in POM cluster with no electric field. Bottom image (b) depicts the same with electric field turned on. In both figures, the blue ball describes oxygen anion. Application of an electric field lowers the barrier height enabling the anions move towards anode. ϕ_a is the activation energy, ϕ'_a is the bias-dependent activation energy and λ is the jump length for the oxygen anions (O_2^-) present in POM clusters. E denotes strength of the electric field due to application of bias.

As the CFs are metallic in character, they carry considerably high current in the LRS. With the high bias voltage at LRS, this current rapidly increases. Such high current through the filaments results in Joule heating within the oxide matrix, which eventually causes rupture of the CFs formed during switching process (Bharti et al. 2014). The device then reverts to HRS. Figure 4.10 explains schematically the formation and rupture of CFs within oxide layer during SET and RESET.

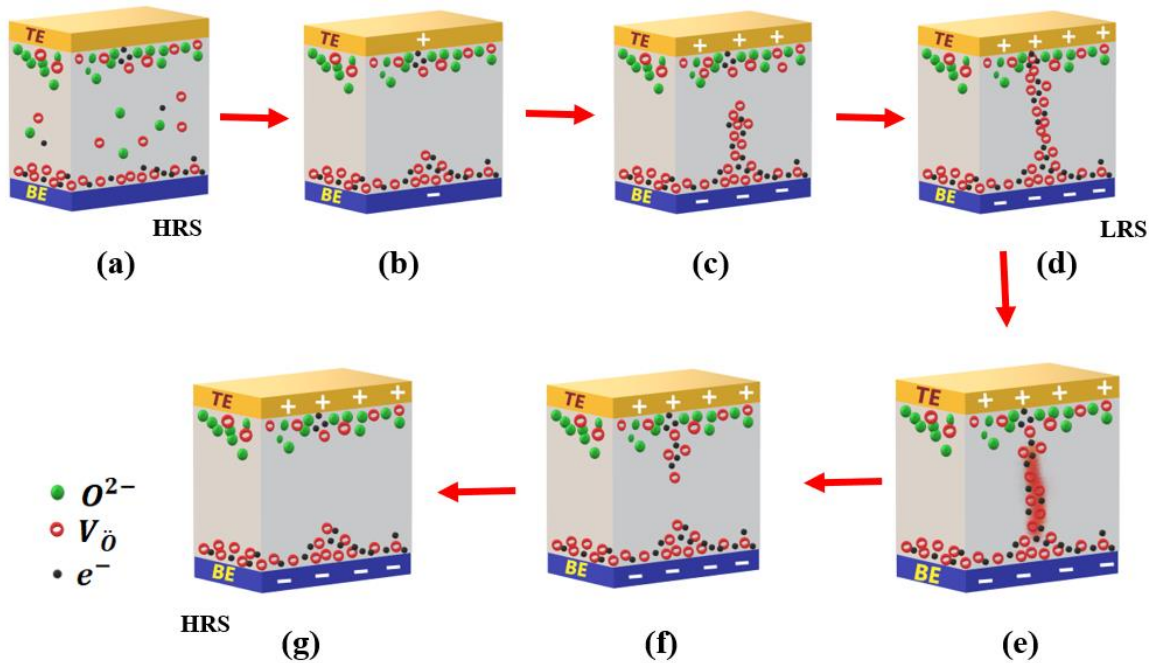


Figure 4.10 Illustrative diagrams showing formation and rupture of CFs due to OV migration. Figure (a) is the initial HRS when no bias is applied, and Figures (b) and (c) show gradual formation of CFs as the OVs move towards cathode and accumulate there with increase in bias. Figure (d) demonstrates a full-grown CF between the top electrode (TE) and the bottom electrode (BE), when the bias reaches SET voltage. Device is in LRS and the process is known as SET process, Figures (e) to (g) show rupture of the filament paths due to Joule heating, driving the device back to again HRS. This is the RESET process.

The exact conduction mechanism behind resistive switching event in Glass/ITO/SDV/Cr/Au RRAM cell was found out investigating the linear fit in a Log-Log plot of the current-voltage (I - V) characteristics, as illustrated in Figure 4.11. As can be seen in the linear fitting of logarithmic I - V plot (see Figure 4.11), there are three distinct regimes – one in LRS and two in HRS. Unlike ohmic behavior in the LRS (slope ~ 1), the HRS shows rather complicated features with two distinct parts. Detail analysis of the charge

transport characteristics in HRS, as elucidated below, seemed to have confirmed trap-controlled space-charge-limited-current (SCLC) model (Moudgil et al. 2018) (Sharma et al. 2014) for observed conduction event. In HRS regime, initially when the applied voltage is low (< 0.86 V), there are more thermally generated free charge carriers in the bulk oxide than injected carriers from the electrode. Since, the current depends on the applied bias and the conductivity of the bulk oxide film, the I - V curve shows ohmic conduction, and therefore, the slope of $\text{Log } I$ vs $\text{Log } V$ is 1. The current density (J) for the ohmic conduction is in agreement with the equation (Moudgil et al. 2018):

$$J_{ohm} = qn\varepsilon\mu \frac{V}{d} \dots\dots\dots(4.5),$$

where, q is electronic charge, n is concentration of free charge carriers, ε is dielectric constant of the oxide, μ is carrier mobility, V is applied voltage, and d is the thickness of the oxide film. As the bias is increased from 0.86 V to 1.28 V, the number of carriers injected into the bulk film will increase rapidly. The trap sites present in the oxide film will capture some of those carriers, while the rest will contribute to the total conduction. The oxide can not accommodate the excess carriers and therefore space-charge is generated at the electrode-oxide interface (Kim et al. 2014). This is called trap-controlled SCLC mechanism and the corresponding current density is described by the equation (Moudgil et al. 2018):

$$J_{with\ traps} = \frac{9n\mu\varepsilon V^2}{8n_t d^3} \dots\dots\dots(4.6),$$

where, n_t is the free carrier concentration of trapped charge. Further increase in bias will fill all the available trap sites and the current density will then obey Child's law ($J \propto V^2$) (Moudgil et al. 2018):

$$J_{trap-filled} = \frac{9}{8} n\varepsilon\mu \left[\frac{V^2}{d^3} \right] \dots\dots\dots (4.7).$$

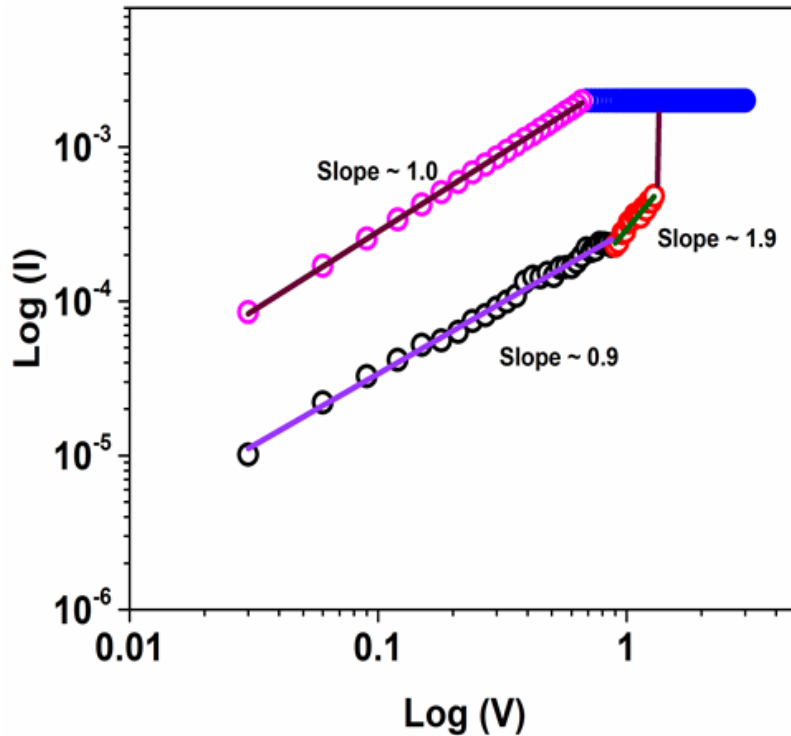


Figure 4.11 Linear to $\text{Log } I - \text{Log } V$ plot in LRS (top blue part) and HRS (bottom purple and red part) showing ohmic and SCLC conduction mechanisms, respectively. Different colors of the straight lines mean different regimes of operation and different slopes.

4.5 Conclusion

In summary, unipolar resistive switching behavior was observed in highly redox active polyoxovanadate ($[\text{V}_{10}\text{O}_{28}]^{6-}$) based RRAM cell under fully open-air condition. The switching was found to be stable, uniform, repetitive and non-volatile in nature. The formation and rupture of conductive nanofilaments due to electromigration of cationic oxygen vacancies via bulk oxide caused the resistive switching event between two binary states – HRS and LRS. Our device exhibited considerably high endurance, retention and resistance ratio. The switching was found to be stable even after 12 months. Ohmic and trap-assisted SCLC conduction mechanisms were exploited to describe the switching behavior in LRS and HRS, respectively. As POMs are large reservoirs of electrons and can

undergo multiple-stage redox reaction they hold great promise for realization of multi-level and high-density molecular memories. We believe that suitable blending of POMs with conventional metal-oxides in hybrid device design may yield improved device performance metrics.

CHAPTER 5

FABRICATION AND INITIAL CHARACTERIZATION OF Cu_xO ($1 \leq x \leq 2$) BASED FLEXIBLE RRAM FOR WEARABLE ELECTRONICS

Overview: This chapter depicts very briefly the work we initiated on flexible RRAM. We employed ITO-coated flexible polyethylene terephthalate (PET) substrate and sputter-deposited copper oxide thin film. On top of the oxide film aluminum contact pads were deposited using thermal evaporation. The preliminary charge transport data of the as-fabricated memory cell is presented. We also discuss the future course of action.

5.1 Introduction

Another important aspect is the integration of RRAM into emerging flexible and wearable electronics. For that to happen suitable ways must be found to replace conventional rigid substrate (for example, Pt coated Si) by some other substrate material which is bendable, foldable and stretchable. In addition, we should try to explore contact (electrode) materials compatible with such flexible substrates. A few potential low-cost electrode materials are solution-processed hybrid materials such as polymer on plastic (Baek and Cho 2018), graphene-oxide (GO) (Zhao et al. 2018), silver nanowire (Yeom et al. 2017), stainless steel (Yan et al. 2018), etc. For substrates, polyethylene-terephthalate (PET) (Zhao et al. 2018), polyethylene-naphthalate (PEN) (Zhang et al. 2019), paper (Minnai et al. 2018) and plastic (Vartak et al. 2018) have been reported as yet. However, its flipside should also be accounted for – for example, the flexible substrates in general possess rough surface area and they are averse to high temperature process flow compared with that of conventional rigid substrates such as Si. The rough surface induces the degradation of device performance, current leakage, and even electrical shorting. Therefore, we need some planarizing layers between the substrate and switching layer so as to keep the device performance degradation at bay. The current fabrication methods, such as sputtering, thermal evaporation, atomic layer deposition and pulsed laser deposition, have low yield and limitations on low-cost mass production of such flexible devices. On the other hand, the major obstacles for solution-processed fabrication techniques such as inkjet printing (Liu et al. 2019), solvothermal method (Bao et al. 2018), and spray coating are solvent compatibility issues and high annealing temperatures, which

induce the dilation of the flexible plastic substrate. However, delicate selection of materials and fabrication techniques will facilitate the development of practical flexible non-volatile memories in the near future. Surprisingly, a good amount of studies on different aspects of flexible memory is still elusive in literature. Therefore, concerted research effort is due to explore the feasibility of use of these kinds of materials as electrodes/substrates in order for efficient integration of RRAMs into flexible device architecture.

5.2 Device description and preliminary results

In this section, we have investigated the RS characteristics of Cu_xO -based RRAM fabricated on ITO-coated PET substrate. The Cu_xO layer predominantly contains both CuO and Cu_2O phases. A thin film of Cu_xO was deposited on top of ITO-coated PET substrate using DC magnetron reactive sputtering. The top aluminum (Al) contacts were deposited using thermal evaporation technique ($\text{Al}/\text{Cu}_x\text{O}/\text{ITO}/\text{PET}$). The schematic of the $\text{Al}/\text{Cu}_x\text{O}/\text{ITO}/\text{PET}$ device is shown in Figure 5.1 and its optical image in Figure 5.2(a) and (b).

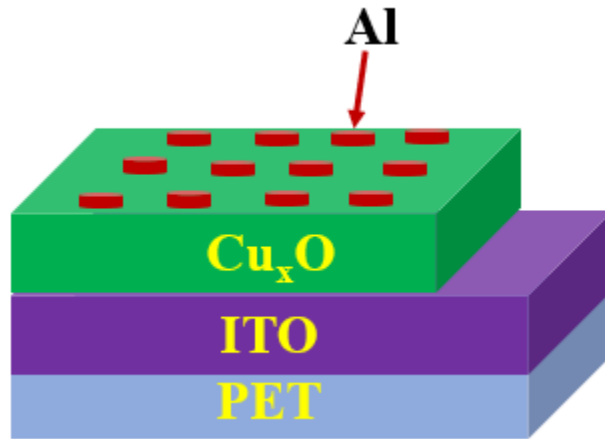


Figure 5.1 Schematic representation of the $\text{Al}/\text{Cu}_x\text{O}/\text{ITO}/\text{PET}$ device.

To study the switching characteristics, the voltage was swept from 0 V to 3 V using a compliance current of 100 μA . We observed a sharp increase in current at voltage of 2 V with a resistance change from 108 M Ω (HRS) to 990 Ω (LRS), as shown in Figure 5.2 (c) (Electroforming process drawn in red plot). The RESET process occurred at a voltage of 0.9 V with a compliance current of 10 mA (black plot in Figure 5.2(c)). To study the SET process, voltage was swept from 0 V to 2 V and the resistance changed from 25 M Ω to 670 Ω at a voltage of 1.3 V (blue plot in Figure 5.2(c)).

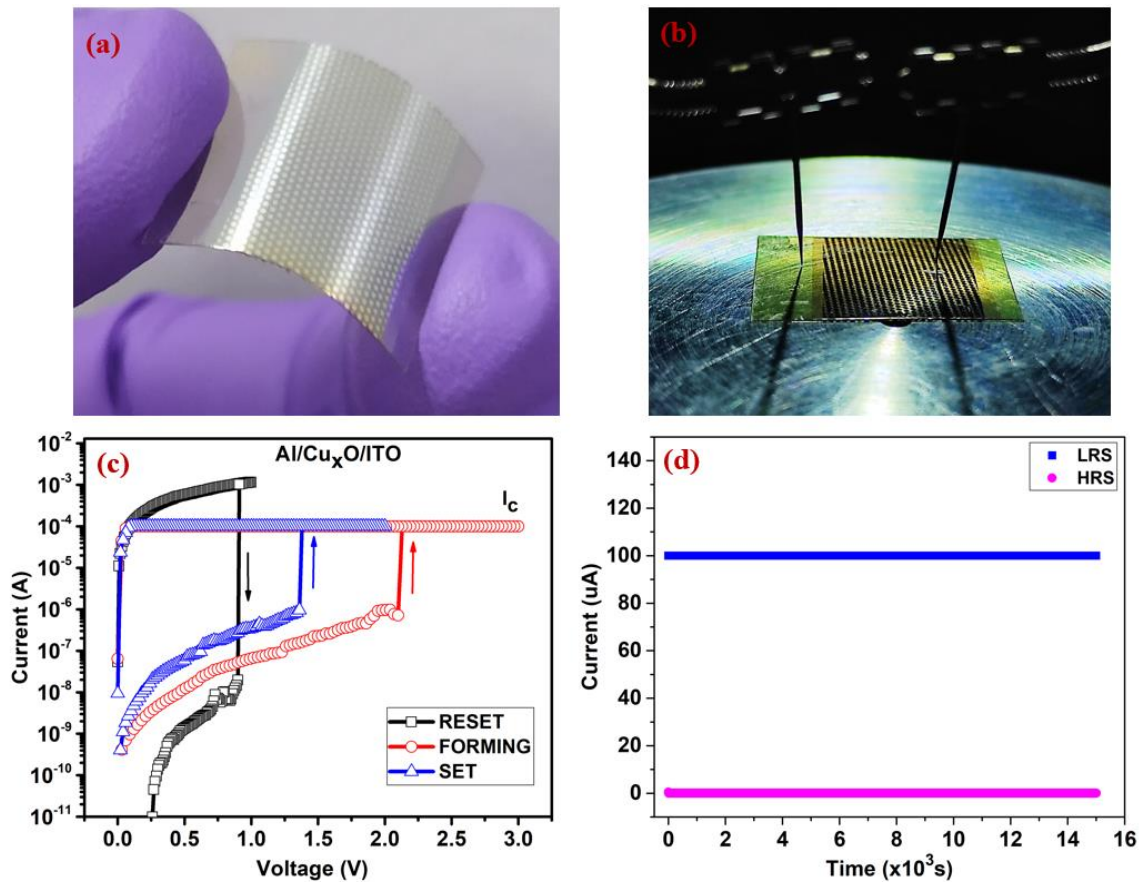


Figure 5.2 (a) An optical image of the flexible device fabricated on PET substrate, (b) Optical image of probed Al/Cu_xO/ITO/PET device used for electrical characterization, (c) Red, blue and black plots indicate the electroforming, SET and RESET, respectively, (d) retention ability tests of the flexible RRAM device.

The device shows excellent resistance ratio of the order of $\sim 10^4$. Retention studies were carried out by setting the device to LRS and applying a read voltage of 100 mV for 14×10^3 sec, followed by resetting the device to HRS. The device was found to retain its two distinct states for 14×10^3 sec without undergoing any noticeable change / drop in current. Further work regarding study of substance-property relationship is necessary to enhance device performance.

5.3 Conclusion

In summary, the Cu_xO thin film was deposited on a flexible substrate (ITO coated PET) using DC magnetron reactive sputtering. We observed unipolar resistive switching at a fairly low voltage. The device exhibits a resistance ratio of $\sim 10^4$. The ability of the device to retain the data was confirmed using retention measurements for $\sim 14 \times 10^3$ sec. Further work on this is underway in our group.

CHAPTER 6

SUMMARY AND FUTURE DIRECTION

6.1 Summary

In a nutshell, we summarize the work presented in this dissertation as in the following.

1. We fabricated RRAM devices based on Cu_xO thin film deposited using DC magnetron reactive sputtering and also tested using 25 micron diameter size W tip as TE. The Pt coated Ti/SiO₂/Si wafers acted as the BE. Coexistence of two BRS modes at fairly low switching voltage for more than 110 cycles was observed in the W tip-Cu_xO cells. The memory window was significantly higher ($\sim 10^5$) compared with that published elsewhere (Ebrahim et al. 2012). To the best of our knowledge, we also presented the first ever retention metric on Cu_xO based RRAMs ($\sim 15 \times 10^3$ sec), which is comparable with that published on conventional TMO based RRAM. From the XPS and *I-V* analysis, we conclude that the RS occurred under electric stimuli due to the reduction and oxidation of Cu ions which eventually helped us build the filamentary model for RRAM operation. The same was further confirmed with the help of resistivity calculation of the Cu nanofilaments. Creation and annihilation of nanometer-size conductive paths or filaments within the oxide layer, which played a pivotal role in observing RS, was accessed with the help of quantization of conductance phenomenon. The underlying transport mechanism was attributed to SCLC.
2. We observed unipolar RS behavior in highly redox active POV, ($[\text{V}_{10}\text{O}_{28}]^{6-}$) based RRAM cells under fully open-air condition. The switching was found to be stable, uniform, repetitive, and nonvolatile in nature. The formation and rupture of conductive nanofilaments due to electromigration of cationic OV_s via bulk oxide caused the RS event between two binary states—HRS and LRS. Despite the fact that POV is not so a conventional material for use in memory cells so far, our device exhibited considerably high endurance, retention, and resistance ratio. Ohmic and trap-assisted SCLC conduction mechanisms were exploited to describe the switching behavior in LRS and HRS, respectively.

3. We initiated preliminary work on fabrication and characterization of flexible memory device. Active switching thin film of Cu_xO was deposited on a flexible substrate (ITO coated PET) using DC magnetron reactive sputtering. With thermally deposited Cu top contacts, we observed unipolar resistive switching at a fairly low voltage. The device exhibits resistance ratio of $\sim 10^4$. The ability of the device to retain the data was confirmed using retention measurements for $\sim 14 \times 10^3$ sec. Further work to obtain an in-depth understanding of structure-property relationship is underway in our group.

6.2 Future direction

We keep the following points as open-ended questions for future research endeavor.

1. Alongside conventional transition metal oxides and perovskites one must try to explore other novel materials and also new device architectures for practical integration of RRAMs into CMOS circuitry. To make RRAM more reliable as next generation memory, thorough understanding on metal-insulator interface property under high electric field condition is paramount. Quantitative and qualitative studies on kinetics of the defects present at the metal-dielectric interface are very important. Low temperature transport study can help us achieve this goal. It is also important to investigate if multiple layers of dielectric media in RRAM can provide superior performance than the ones with just one single active layer. This will open up avenues for investigation on heterostructure based memory cells.
2. Switching properties are heavily dependent on the work function of the contact metals. Therefore, one can explore in that direction with variety of choices for top and bottom contacts.
3. Obtaining miniaturized reliable molecular memory is still a challenge. One can explore wide variety of polyoxometalate clusters and their likes with proper blending with polymers. Different versatile properties of polyoxometalates

molecules (e.g., high redox activity, large electron storage, etc.) can possibly enable us to build low-cost, high-speed and high-density molecular memory.

4. In this work, we have demonstrated how the quantization of electrical conductance can be used as an alternate tool, though “indirect”, to prove nanofilament formation within dielectric media. The same is also useful in fabricating multi-bit memory. Such effort will become reality only when we have better control on the onset of those quantized steps. Much work is necessary in that direction – both at high and low temperature (down to liquid helium temperature) regimes.
5. Extensive work is needed to optimize different factors relating to *flexible* RRAM (e.g., type of substrate and contact materials which can withstand high-temperature processing steps, suitability of active dielectric thin film, deposition technique, etc.) for it to eventually translate to real working device.
6. Mott insulators can undergo an electronic phase transition from a Mott insulating phase to a metallic-like state when subjected to electric stimuli. This transition is part of a new class of RS process that is most likely related to Mott physics. RS observed in such materials is perceived to have the potential to create a new class of RRAM
7. The rapid advancement in 2D material based nanodevice has driven scientific community to more experimental investigation, including the study of the RS effect in them. A few 2D materials have shown stable resistance switching such as graphene and molybdenum disulfide (MoS₂). A very little work on another widely explored 2D material hexagonal boron nitride (hBN) has been done. We believe that for resistive switching applications, 2D materials still have a lot of room to explore

List of publications

Journal publication from this thesis work

1. **Sterin N. S.**, N. Basu, M. Cahay, M. N. Satyanarayan, S. S. Mal, and P. P. Das (2020). “Redox-Active Vanadium-Based Polyoxometalate as an Active Element in Resistive Switching Based Nonvolatile Molecular Memory.” *Phys. Status Solidi A*, 217(18), 1–9. (DOI: 10.1002/pssa.202000306)
(This article featured as the cover-page article)
2. **Sterin N. S.**, Nivedya T., S. S. Mal, P. P. Das. (2021). “Understanding the coexistence of two bipolar resistive switching modes with opposite polarity in Cu_xO ($1 \leq x \leq 2$) based two terminal devices.”, “*Journal of Materials Science:Materials in Electronics*”,pp.1-15.

Journal publication from other projects

1. P. P. Das, A. Jones, M., Cahay, S. Kalita, S. S. Mal, **N. S. Sterin**, T. R. Yadunath, M. Advaita, S. T. Herbert. (2017). “Dependence of the $0.5 \times (2e^2/h)$ conductance plateau on the aspect ratio of InAs quantum point contacts with in-plane side gates.” *Journal of Applied Physics*, 121(8), p.083901.
2. Nimith K.M., **Sterin N. S.**, P.P. Das, G. Umesh, M. N. Satyanarayan, (2019). “Capacitance and impedance spectroscopy studies of polymer light emitting diodes based on MEH-PPV: BT blends.” *Synthetic Metals*, 250, pp.99-103.
3. N. Basu, **Sterin N. S.**, S. R. Mamidala, A. Shenoy, N. Bhat, (2019). “Optimization of Platinum dioxide properties by plasma oxidation of sputtered PtOx.” *Materialia*, 8, p.100477.

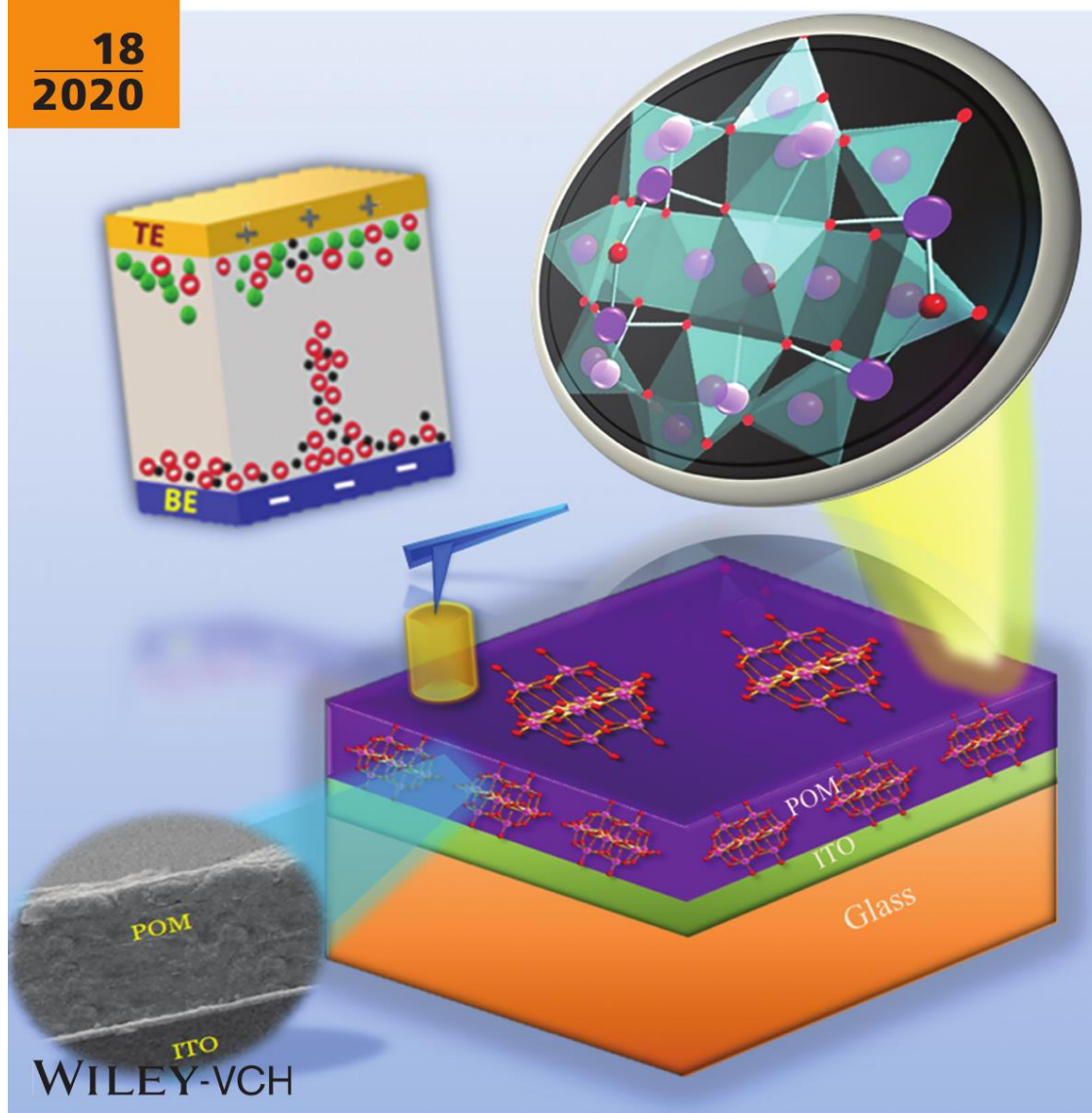
Conference publication

1. Nivedya T., **N. S. Sterin.**, B. R. Biradar, S.S. Mal., P. P. Das, “Coexistence of two bipolar resistive switching modes with opposite polarity in Cu_xO ($1 \leq x \leq 2$) based RRAM devices”. XXI International Workshop on Physics of Semiconductor Devices (IWPSD – 2021), IIT Delhi, India, Dec 14 – 17, 2021.
2. **Sterin N. S.**, Nivedya T., Maity Sukanya., B. R. Biradar, S. S. Mal, P. P. Das, “Resistive Switching in Redox Active Vanadium Based Polyoxometalate ($\text{Na}_6\text{V}_{10}\text{O}_{28}$) for RRAM Devices”. International Conference on Functional Materials and Applied Physics (FMAP-2021), S. V. National Institute of Technology, Surat-395 007. Gujarat, India. May 14-15, 2021.
3. **Sterin N. S.**, S. S. Mal, P. P. Das, (2018). “Resistive switching in $\text{Na}_6\text{V}_{10}\text{O}_{28}$ polyoxometalate thin film based two terminal device”. International Conference on Recent Advances in Materials Science and Biophysics, Mangalore University, January 23-25, 2018.
4. P. P. Das, A. Jones, M. Cahay, **Sterin N. S.**, S. Kalita, . R. Yadunath, M. Advaita, S. T. Herbert, “Towards the realization of an all-electric semiconductor Datta-Das spin field effect transistor”, Proceeding of The XIX International Workshop on The Physics of Semiconductor Devices (IWPSD 2017), IIT Delhi, India, Dec 11-15, 2017.
5. Chetan K., **Sterin N. S.**, M. N. Satyanarayan, Shee D., P. P. Das, S. S. Mal, “Synthesis and Characterisation of Graphene Oxide–Polyoxometalate Composite Materials for Device Applications”, Oral presentation at 4th National Conference on Condensed Matter Physics and Applications, MIT Manipal, India, May 23-24, 2016.

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