EFFICIENT CONTROL OF POWER CONVERTER INTERFACES FOR SOLAR GRID TIE INVERTERS

Thesis

Submitted in partial fulfillment of the requirement for the award of degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby declare that the Research Thesis entitled "Efficient Control of Power Conversion Interfaces for Solar Grid-Tie Inverter" which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

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This is to certify that the Research Thesis entitled "Efficient Control of Power Conversion Interfaces for Solar Grid-Tie Inverter" submitted by Roopa Viswadev Damodaran (Register Number: 177EE012) as the record of the research work carried out by her, *is accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

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(Chairperson D.R.P.C/ H.O.D., EEE)

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Abstract

Amongst the available renewable sources, solar photovoltaic (PV) energy sources is becoming dominant due to its long operational life, lesser emission and decreasing installation and maintenance costs. The grid integration of PV sources eliminates the requirement of additional storage and provides support for the peak loads. With the increasing number of PV sources integrated to the grid, the standards for grid integration are continuously revised in order to ensure that only stable, safe, efficient and reliable systems are integrated with the grid. The present standards recommend the sources to stay connected to provide support to the grid especially during voltage sags. Due to this reason, developing improved topologies and control strategies for power conversion interfaces (PCI) that can perform satisfactorily under varying grid conditions.

Several control techniques for PCIs exist in literature based on the pulse width modulation (PWM). Amongst these, the hysteresis control (HC) exhibits superior performance when compared to other conventional PWM techniques. The HC is one of the most simple modulation techniques especially for grid tie inverters (GTIs). It regulates the ripple current output of GTI within fixed hysteresis limits. This results in a varying switching frequency which is not implicitly known prior to control implementation. Hence, HC of conventional PCI for GTI is hindered by its varying switching frequency, requirement of high precision AC current sensor and undecided switching intervals. Due to these reasons, HC is also not often used in novel PCI topologies, despite all its advantages. In this thesis, the above mentioned shortcomings are discussed along with their solutions so as to improve the HC. These contributions can provide assistance to researchers and engineers in design and implementation of applications such as GTIs using HC.

The output filter design, switching device selection, switching and conduction loss calculations of GTIs are predominantly dependent on the switching frequency. Hence, estimating the minimum and maximum switching frequencies is essential for a reliable system design. The existing estimations for HC assume linear ripple current. Since the frequency variation is large in HC, this assumption is invalid for the range of low frequencies. Inaccurate estimation of switching frequency can have considerable effect on system design. In this thesis, a more precise and generalized expression to estimate the switching frequency of multilevel GTI is obtained by time-domain analysis. The accurate estimation results in the improvement of system design which is demonstrated with an example of a second order filter.

The effect of changes in system parameters on the switching frequency is also analysed to determine the operating point for an accurate system design.

One other limitation of HC is the requirement of high precision AC current sensors. Though no current sensorless HC can be found in the literature, the current emulation technique of eliminating current sensor may be modified and implemented for HC. However, the computational requirement for such a control is high. To this end, an AC current sensoreless HCC for two-level GTI is developed by formulating the switching intervals as a function of known system variables. All real time conditions such as non-linearity of ripple current, dynamic changes in operating conditions and effects of digital sampling are considered while developing the algorithm of the proposed AC current sensorless HC.

Due to the uncertain switching intervals of HC, its use in the relatively novel PCIs are not vastly explored. Hence in this work, the closed loop controls for Z-source inverter (ZSI) and microinverter (μI) using HC are presented. A single stage PCI with independent input and output side controls can be achieved using ZSI. The shoot through interval is an important parameter which decides the boost ratio of ZSI. For ZSI with HC, determining the shoot through interval is difficult due to the undecided switching intervals. Hence, in this thesis, a detailed analysis of ZSI as a single-stage PCI is discussed. A closed loop control using HC with shoot through error estimation is developed based on this analysis.

AC modules and the associated PIC, commonly referred to as μIs have been gaining attention due to the advantage of eliminating partial shading in series connected PV modules. The prime features of a μI are high efficiency, high gain ratio with less number of switching components and preferably without using coupling inductors or transformers, simple control and reduced THD. Keeping these in mind, an efficient μI with pseudo DC-link (pDC-l) for grid integration of AC module is proposed as a part of this work. A high gain buck-boost Z-source converter (ZSC) is used to obtain a pDC-l from a single PV module. An unfolding circuit follows the ZSC. It operates at fundamental frequency which reduces the switching losses without affecting the THD. A simple closed loop control using voltage HC is developed to obtain a pseudo DC-link voltage. A current HC ensures power balance by controlling the current to the inverter bridge.

Simulations and experimental validations are carried out to verify the theoretical analysis and ensure the proposed controls achieve the standards of grid integration of PV systems. The simulation studies are carried out in MATLAB while ensuring the real time operating conditions.

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Symbols and Nomenclature

ϵ	Shoot-through hysteresis limit
Δi_{r}	Change in ripple current i_{r}
Δt	Switching interval
Δt_{L}	Switching interval when linear current is assumed
Δt_{k}	Switching interval at k^{th} switching
$\Delta t_{\mathrm{k-1}}$	Switching interval at $k-1^{\mathrm{th}}$ switching
θ	phase shift due to filter
ω	Fundamental switching frequency in rad/s
A	Total gain ratio
B	Boost ratio of Z-source network
$B_{\mathrm{k-max}}$	Maximum constant boost ratio
B_{max}	Maximum boost ratio
C_{f}	Filter Capacitor
C_{z}	Z-source Capacitor
d_1	Duty ratio of S_1 in Z-source capacitor
d_2	Duty ratio of S_2 in Z-source capacitor
f_{avg}	Average switching frequency in Hz
f_{g}	Fundamental frequency in Hz
f_{max}	Maximum switching frequency in Hz
f_{min}	Minimum switching frequency in Hz
f_{sw}	Switching frequency in Hz
$f_{\mathrm{sw-L}}$	Switching frequency in Hz assuming linear ripple current
G	Solar irradiation
h	Hysteresis band
i_{g}	Grid current
i_{i}	Actual instantaneous inverter output current
i_{i}^*	Reference instantaneous inverter output current
$i_{\mathrm{L_z}}$	Z-source inductor current
I_{PV}	PV output current
i_{r}	Ripple current at inverter output
k	Present switching level of inverter output voltage
L_{g}	Grid side filter inductance
L_{i}	Inverter side filter inductance

L_{z}	Z-source network inductance
M	Modulation index
m	Modulating signal
$\dot{m}$	Time rate of change of modulating signal
n	Number of switching levels in inverter output voltage
P	Total power output
p	Set containing all levels of inverter output voltage
p_{n}	Maximum of the set p
T	Switching period
t_{AS}	Switching Interval for active state
t_{ST}	Switching Interval for shoot-through state
t_{sw}	Switching instant
t_{ZS}	Switching interval for zero state
u	Switching state
u_{ST}	Shoot-through switching state
$V_{\mathrm{C_z}}$	Z-source capacitor voltage
$V^*_{\mathrm{C_z}}$	Z-source capacitor reference voltage
V_{dc}	Inverter input DC link voltage
v_{g}	Instantaneous grid voltage
v_{i}	Instantaneous inverter output voltage
v^*_{i}	Instantaneous inverter output voltage reference
V_{PV}	PV output voltage
v_{z}	Instantaneous Z-source network output voltage
$\hat{v_{\mathrm{z}}}$	Peak Z-source network output voltage

Acronyms and Abbreviations

μI	Micro Inverter
AC	Analog Current
ADC	Analog to Digital Converter
AS	Active State
CCM	Continuous Conduction Mode
CET	Current Emulation Technique
CS	Current Sensor
CSLHC	Current Sensorless Hysteresis Control
CSI	Current Source Inverter
DB	Dead-beat
DC	Direct Current
DCM	Discontinuous Conduction Mode
DGS	Distributed Generation Systems
DHC	Digital Hysteresis Control
GTI	Grid-tie Inverter
HB	Hysteresis band
HC	Hysteresis Control
LPF	Low Pass Filter
MGTI	Multilevel Grid-tie Inverter
MPP	Maximum Power Point
PCI	Power Conversion Interface
pDC-l	Pseudo DC-link
PI	Proportional Integral
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
STS	Shoot-through State
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
ZS	Zero State
ZSC	Z-Source Converter
ZSI	Z-Source Inverter

Chapter 1

Introduction

Contents

1.1 Background

The energy demand across the globe has been considerably increasing for industrial as well as household requirements. A large share of this demand was met by conventional sources, mainly fossil fuels resources. However the finite reserve of these conventional energy sources, their increasing costs and detrimental effects on environment has led to the increased use of alternative energy sources such as

hydro, wind and solar photovoltaic (PV) [Bhattacharyya, 2006, IRE, 2019b, IRE, 2019a]. Amongst the renewable sources of energy, solar PV sources have advantages of negligible pollution during the power generation, very low maintenance costs and less wear and tear due to absence of moving parts. Based on the type of interconnection with the loads and other power sources, the PV based energy systems can be briefly classified as standalone, hybrid and grid connected systems. The stand alone and hybrid systems require energy storage so as to ensure availability of power during low or no irradiation like cloudy or night hours. To utilize the total capacity the distributed generation systems (DGS) with PV sources are interconnected to the utility grid [Kaundinya et al., 2009]. The grid is often considered as an infinite source or sink, and thereby enables injection of power input whenever possible while ensuring power availability to connected loads at all times. However the grid is often not as stable and rugged as expected. The grid conditions vary considerably, but with an allowable range, due to several factors. This coupled with the unpredictable nature of PV input power provides challenges in the development of controls capable of ensuring grid requirements under all conditions.

The PV source produces DC power which is converted to AC power synchronized in terms of magnitude, phase and frequency of the single/three phase utility grid by a power conversion interface (PCI) of grid tie inverter (GTI). A basic block diagram of a PCI is shown in Fig. 1.1. The PCI comprises of one or more power electronic converters that ensure the power from the PV source is efficiently pushed to the grid while ensuring all safety regulations and stability requirements. One converter of the PCI is definitely an inverter that ensures the DC power is converted to AC power for the grid. In cases where the DC voltage of the PV source is not sufficient to meet the grid voltage requirement, a suitable DC-DC converter is cascaded to the input of the inverter. Similarly, multiple configuration for the PCI exists in the literature and several controls can also be found [Tekumalla et al., 2019, Zeb et al., 2018, Athari et al., 2017, Singh et al., 2018]. Most of these are application or rating specific.

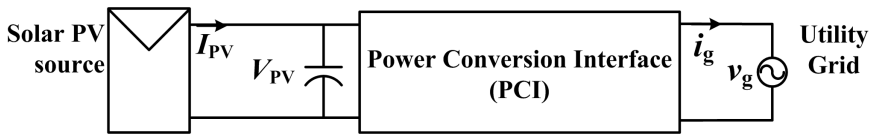


Figure 1.1: Basic block diagram of PCI for PV-grid integration

Considerable increase in the number of DGSs interconnected with grid is expected in the near future, thereby demanding improved and stable system perfor-

mances under varying grid conditions. Challenges for PV systems are considerable, as they are often connected to either low or medium voltage networks unlike the conventional power plants or large wind farms. The high penetration level of PV systems imposes new challenges for the distributed system, leading to modifications in grid standards. For example, large number of DGSs disconnecting together from the distribution grid during any grid voltage fluctuation would only result in worsening the grid condition, and is hence undesirable in a grid with high density of DGS integration. Present standards recommend DGSs to stay connected with the grid so as to provide support to the grid voltage especially during voltage sags. Careful design of the system as well as the controls are very much essential so that the grid requirements as per standards are met. For this a proper understanding of the standards of grid integration is desired.

1.2 Standards for grid integration of PV systems

Standards of grid integration are the essential guidelines for design, control and operation of grid-connected renewable energy systems [Dugan et al., 2006]. The grid standards initially addressed elementary demands for PV systems, due to their low penetration level. The high penetration level of multiple PV systems at a PCC imposed new challenges for the distributed system. This led to modifications in grid standards. The power inputs to the utility grid are widely transforming to distributed in nature. Owing to this, the present standards recommend DGSs to stay connected with the grid so as to provide support to the grid voltage especially during voltage sags. One such standard is the IEC 61727 which specifies the main requirements for a grid interface which ensures both functionality and safety for PV interconnections of less than 10 kW to low voltage grid.

Another standard for grid integration is IEEE 1547. An overview of IEEE 1547 standards is given in [Basso and DeBlasio, 2004] which establishes technical requirements for DGS that helps utilities tap surplus electricity from alternative sources. IEEE standard 1547 (2003) was the first in the series of standards developed concerning DGS interconnection. It includes general requirements, responses to abnormal conditions, power quality, islanding, and test specifications and requirements for design, production, installation evaluation, commissioning, and periodic tests. It was revised to IEEE 1547.3 in 2007 to include requirements for DGS such that they do not unintentionally provide power to the utility grid when it is disconnected from the transmission system. The IEEE Standard 1547.4 (2011) addresses the capability to separate from and reconnect to part of the grid

during faults. In IEEE Standard 1547a (2014), the allowable advanced functionality that will provide a more robust grid is addressed. According to this, the DGS is permitted to stay connected for a wider range of abnormal grid voltage and frequency conditions.

Table 1.1: Harmonic current distortion limits (in %) based on the ratio of maximum short circuit current to maximum load current ($\frac{\hat{I_{sc}}}{\hat{I_g}}$) as per IEEE Std 519

$\frac{\hat{I_{sc}}}{\hat{I_g}}$	Harmonic order					
	< 11	$11 - 15$	$17 - 21$	$23 - 33$	≥ 35	TDD
< 10	4.0	2.0	1.5	0.6	0.3	5.0
$10 - 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 - 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 - 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

One other important standard is the IEEE 519 which provides the recommended practice and requirements for harmonic control in electrical power systems. IEEE 519-1981 focuses on the recommended practices for line notch limits, voltage distortion limits, telephone influence limits and flicker limits. The terms total harmonic distortion (THD) and total demand distortion (TDD) were introduced in IEEE 519-1992. IEEE 519-2014 lists the harmonic measurements and recommended harmonic limits for current distortion listed in Table 1.1.

In addition to meeting the standards, the DGSs connected to the grid should also consider the possible non-ideal operating conditions and limitations.

1.3 Non-ideal Operating Conditions

In real systems, PCIs for GTI may have to operate under several non-ideal conditions which can arise due to presence of grid, the connecting filter structure, sensors and also due to limitations in controller implementation. The controls or topologies used must support their operation under these non-ideal conditions. A list of such conditions within the scope of this work are presented below.

Non-ideal Utility Grid

The early works on topologies and controls of PCIs for GTIs consider grid as an ideal stiff source with constant voltage and frequency. Any effect on the system due to this consideration was assumed to be negligible. However, in practice, the

behavior of an electric power grid may deviate from the assumed ideal characteristics due to its finite capacity, impedance offered by transmission and distribution system, sudden changes in the loads and faults in system. Such sudden changes due to these non-ideal conditions lead to increased losses, instability, waveform distortion and disconnection from grid. However based on the revised standards, DGS should remain connected to grid through PCI and operate accordingly under these non-ideal conditions.

Non-ideal conditions due to sensors

The sensor circuits used for voltage and current sensing can introduce offset into the controller, due to ageing and temperature related issues. This in turn can inject DC current into the grid or create imbalance in the DC bus of PCI. In addition, certain controls such as hysteresis controls (HC), require precise sensing of current. This require high precision current sensors which contribute to the increased cost and size of the system.

Non-idealities in PCI

The limitations in realising the hardware structure of a PCI give rise to non-ideal conditions such as switching ripple, low order harmonics due to dead band, on state drop of semiconductor switch and mismatch between DC bus capacitors. Increased THD and imbalance in DC bus are few of the resulting problems.

Digital controller limitations

Digital controllers are considered a low cost alternative to analog controllers which are prone to errors due to ageing and environmental factors. However, they introduce inevitable time delays due to sampling and computation. These delays increase with the complexity of control. Hence optimization of code and implementation of simple control structures are inevitable. Furthermore, the effects of these delays maybe reduced by suitable analysis and control.

1.4 Classification of Power Conversion Interfaces

The PCIs play a major role in determining the efficiency, stability and power quality of PV systems integrated with the grid. Conventional topologies for PCIs may be briefly classified based on the power conversion stages as single stage PCI and

two stage PCI. ([Kjaer et al., 2005]). The single stage conversion maybe considered more desirable over the two stage conversion due to its improved efficiency owing to the reduced number of active and passive components [Wu et al., 2011]. It consists of an inverter, single or three phase, and require the input PV voltage to remain greater than a minimum under all conditions.

A two stage system includes a converter, with gain value greater than 1, between the PV source and the inverter. This reduces the number of series connected PV modules compared to the single stage system. It reduces the effects of shading at the expense of increased components and reduced efficiency. On the other hand, single stage systems with inverter configurations capable of providing gain ratios greater than 1 can improve the system efficiency.

One other increasingly popular concept is that of the AC module. It employs high efficient high gain PCIs to convert the low voltage output from a single PV module to AC voltage of required magnitude and frequency. AC modules considerably reduce the effect of partial shading in series connected modules.

The control of these PCIs play a great role in ensuring grid standard requirements while maintaining high efficiency operation [Blaabjerg, 2018].

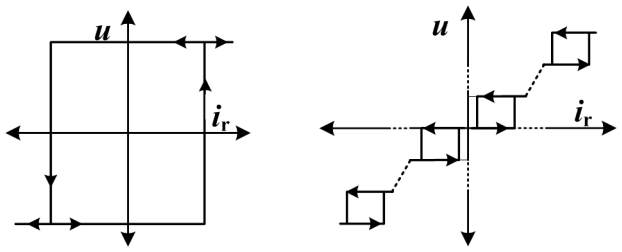
1.5 Conventional PCI Controls

Grid connected applications employ current controlled inverters that implement an inner control loop to control the inverter output current and hence vary the real and reactive power to desired values. Several current controlled architectures with their advantages and disadvantages are presented by [Parvez et al., 2016]. The controls can be widely classified as linear and non-linear. The proportional integral (PI), proportional resonant (PR) and repetitive current (RC) controllers come under linear controls while dead-beat (DB), predictive and hysteresis controllers can be listed under non-linear control techniques as shown in Table 1.2.

The controls of PCIs are expected to operate under varying input and grid conditions while maintaining the grid standards. The controls should not contribute to increased complexity. Hence, rapid and stable response with simple and reliable control is hence vital for PCI for solar PV based GTIs. We observe from Table 1.2 that HC is an ideal control strategy.

Table 1.2: Conventional Control Techniques [Parvez et al., 2016]

Frame	Control	Advantages	Limitations
dq-frame	PI	Simple control and hardware implementation, good dynamic response	Poor harmonics compensation
$\alpha\beta$-frame	PR	improved dynamic response, good harmonic compensation	Complex hardware implementation
	RC	High order harmonics compensation	Slow dynamic response
abc-frame	DB	Improved dynamic response, ease of control implementation	Requires high frequency DSP for hardware implementation
	Predictive	Optimized switching frequency, good dynamic response	Complex implementation, high sampling rate
	Hysteresis	High dynamic response, simple control structure	varying switching frequency



(a) Two-level HC (b) Multilevel HC

Figure 1.2: Current limits and switching levels of Current HC

1.5.1 Hysteresis control of PCIs

The HC operates by limiting the voltage or current within specified limits. For example, in current HC for GTI, the actual current output of the inverter is sensed and compared with a reference current. The difference is termed as ripple or error current. The ripple current is maintained within predetermined limits by varying the switching pulses of the inverter as required. The representation of two level and multilevel HCs with switching level u and ripple current i_{r} are presented in Fig.1.2.

As discussed, HC can provide improved dynamic response with stable steady state response with a simple control architecture. However the use of hysteresis control is limited often due to the varying switching frequency operation. This is specifically important when HC is used to control the grid current in a GTI. In GTI controls, the switching frequency is a determining factor in choosing the switching devices, filter design as well as pre-calculating the switching and conduction losses.

Hence estimating the switching intervals and the switching frequency for a HC of GTI is of major interest. Furthermore the current sensors play a very important role in HC. The sensors used to obtain the inverter output current forms a part of inner loop in a GTI control. For HC, the changes in current as low as the hysteresis limits are required to be accurately estimated. This implies that the inverter output current ripple requires to be precisely sensed. Therefore high precision current sensors are an inevitable for HC.

Several contributions in the existing literature discusses the shortcommings of HC and their possible solutions in order to meet the specifications required by the grid standards while considering the non-ideal conditions of operation. Hence a detailed literature review is presented.

1.6 Literature Review

An extensive literature search for the grid integrated PV sources was performed. The literature review encompasses the existing PV grid interfaces and their controls with focus on identifying the improvements made in the conventional topologies and/or controls. The advantages as well as limitations of these improved techniques were identified during the review. The literature survey was performed in each of the following areas:

- Switching frequency estimation of HC
- Current Sensorless control for HC
- HC for novel PCI configurations
  - Z-Source Inverter for Single stage PCI
  - Micro-inverters for AC modules

The literature reviews are presented in detail in the following sections.

1.6.1 Switching frequency estimation of HC

Unlike other modulation techniques for GTIs, the switching frequency of HC is not fixed by control. It varies along the fundamental cycle due to the fixed limits of the ripple current. This variable frequency of HC inhibits its use in multilevel GTI (MGTI) applications due to the difficulties in the system and control designing.

Few switching frequency derivations of MGTIs employing HC are available in the literature. They are based on either frequency domain [Albanna and Hatziadoniu, 2009, Albanna and Hatziadoniu, 2010, Gupta, 2012] or time domain analysis [Kumar and Gupta, 2017, Gautam and Gupta, 2014, Wu et al., 2013b]. Time domain analysis is often preferred since a direct relation, of instantaneous frequency and system parameters, such as DC input voltage, grid voltage, ripple current and filter specifications, is obtained. The switching frequency formulations found in literature are mostly for 2- and 3 level inverters [Albanna and Hatziadoniu, 2010, Gupta, 2012, Kumar and Gupta, 2017]. A generalized switching frequency formulation for cascaded multilevel current controlled inverters is presented in [Gautam and Gupta, 2014].

All the existing formulations in [Albanna and Hatziadoniu, 2010, Gupta, 2012, Kumar and Gupta, 2017, Gautam and Gupta, 2014] are derived assuming that the ripple current of MGTI output is presumed to vary linearly within specified hysteresis limits by considering high switching frequencies only. But the switching frequency of HC oscillates between a minimum and maximum range in a fundamental cycle and the existing formulations do not provide an accurate estimation during the low frequency range. In [Gautam and Gupta, 2014], low switching frequency operation of cascaded multilevel inverters with inductive load is considered. Yet, a linear rate of change in ripple current is assumed. In multilevel inverters, there exist time duration during which the slope of ripple current is highly nonlinear. This is owing to its slope reversal detailed in [Wu et al., 2013a, Wu et al., 2015]. Using the existing formulation of [Gautam and Gupta, 2014], the calculated switching frequency at these instants is zero which is an improbable value for switching frequency.

The above mentioned shortcomings of the existing frequency analysis can result in inaccurate design of MGTIs causing distortions in the grid current.

1.6.2 High precision sensors in HC

In conventional fixed band HC, the inverter output current is modulated by limiting the error current within a predefined hysteresis band (HB). Hence a high precession current sensor (CS) is required to sense changes as small as HB at varying switching frequency. Several fixed frequency HCs exist [Ho et al., 2009, Wang et al., 2018,Ebrahimi and Khajehoddin, 2016], but these controls increase the complexity and compromise the dynamic response while retaining the requirement of CS. These sensors contribute to overall cost and size and introduce measurement

noises and delays. One solution to the aforementioned problem is to employ an AC current sensorless hysteresis control.

Though several sensorless controls exist in literature [Su et al., 2019, Zhang et al., 2015, Jiang et al., 2017], they mostly focus on eliminating voltage sensors. But unlike voltage sensors, current sensing techniques induce losses and noise in the power circuit and are often invasive. Though non-invasive techniques exist, they increase the cost and size of the system. Hence there is a need for further investigation on sensorless current control strategies. Few current sensorless controls exist in literature, amongst which current emulation technique (CET) is most common [Su et al., 2019,Zhang et al., 2015]. It uses system parameters and switching states to emulate the required current. However computations are required at each sample leading to delays and cumulative errors. Methods existing in literature to eliminate such miscalculations for other controls [Zhang et al., 2015] may be adapted for HC, but they tend to further increase the computational burden. Moreover the generation of hysteresis band and its comparison with error current are required if the existing current sensorless techniques are used to develop AC current sensorless hysteresis control.

1.6.3 HC of novel PCIs

As discussed earlier, HC does provide a superior control and is compliant with the requirements of GTIs. However, unlike other pulse width modulation (PWM) techniques that often use carriers and modulating signals, the switching intervals in HC solely depends on the current limits. Hence, the exact switching intervals is undetermined due to which HC is not commonly used for the control of many novel topologies such as Z-source inverters (ZSI) and micro-inverters (μIs).

ZSI for Single stage PCI

The commonly used transformer-less two stage PV to grid power conversion interface (PCI) is often preferred over single stage interface in low power applications. This is because the two stage interface offers independent input and output controls, stability in case of systems with wide fluctuation in input voltage. The two stage system also requires less number of PV modules in series. However it decreases the overall conversion efficiency and reliability while increasing the cost of the PCI. Furthermore, both the single stage as well as the two stage PCIs include a traditional voltage source inverter (VSI) or current source inverter (CSI). The intentional or unintentional switching on of upper and lower devices of the same

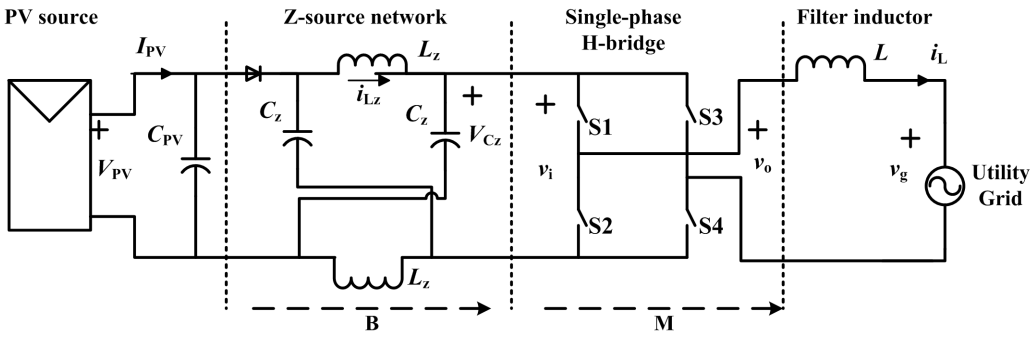


Figure 1.3: Block diagram of ZSI for PV grid integration

leg in traditional inverters will cause a shoot-through condition where the source terminals are shorted. This may be avoided by introducing dead-times between switching pulses but will in turn cause the output waveform to be distorted.

A single stage system with the possibility of independent control can be obtained with the ZSI as a solution to the two aforementioned problems([Cao et al., 2011, Zhang and Ge, 2010]). The ZSI is proposed in [Peng, 2003] and a block diagram of the same is shown in Fig.1.3. It provides a unique feature of boosting the input voltage by utilizing the shoot-through condition. It enables independent control of input and output side in a single stage interface. The Z-source network is symmetric with two pairs of identical capacitors and inductors. The capacitors and inductors of the network are capable of storing energy so as to provide the required boost in voltage. Such a network can thereby replace the DC-DC conversion stage for a more efficient single stage PCI for a PV-grid interface ([Galigekere and Kazimierczuk, 2012]). It also avoids harmonics caused by dead zones in VSI which is clearly depicted by [Huang et al., 2006] and [Gajanayake et al., 2007].

Several open loop as well as closed loop controls for ZSI in literature are often based on traditional or modified sinusoidal or space-vector pulse width modulation (PWM) techniques [Shen et al., 2006, Zhou et al., 2016, Jain et al., 2018]. Few controls for implementation of HC for ZSI can also be found in literature([Zare and Firouzjaee, 2007, Singh et al., 2016, Ke et al., 2011, Husev et al., 2014]). An analysis of symmetrical and asymmetrical Z-source network for hysteresis current controlled single-phase ZSI is presented in [Zare and Firouzjaee, 2007] where the previous switching cycle is used to estimate the shoot-through time. A hysteresis controlled active power filter to suppress the low frequency harmonics in Z-source networks is proposed in [Singh et al., 2016]. In [Ke et al., 2011], a constant frequency hysteresis control for a single phase ZSI used for PV-grid interface is realized by varying the hysteresis band based on the system parameters and using

truth-table to determine shoot-through states.

A general HC algorithm for single phase or three phase ZSI and quasi ZSI are proposed in [Husev et al., 2014] with a case study of single phase three-level neutral point clamped quasi-ZSI implemented for PV-grid integration. The current reference is calculated from the available power and grid voltage magnitude. The shoot-through limit is determined from the proportional-integral (PI) controller that is used to maintain Z-source capacitor voltage at required reference value. In many of the existing controls, the results show distortions in current waveform during initial dynamics. Furthermore, the effect of variations in grid voltage has not been analysed. Due to the difficulty in determining the shoot-through states, the development of a stable closed loop control for hysteresis controlled ZSI has not been as widely explored as other PWM control techniques for ZSI. The existing controls result in distortions in current waveform during initial dynamics. Furthermore, the effect of variations in grid voltage has not been analysed.

Micro-inverters for AC modules

For grid connected PV systems, the voltage at the input of the inverter is expected to be greater than peak of the grid voltage. This would require several series connected PV modules in order to achieve the required voltage at the DC bus. The power conversion stage between the PV input and grid would operate at the maximum power point (MPP) of the whole PV system. This, under mismatch in operating conditions of the PV modules in series, would lead to loss of available power, thereby reducing efficiency of the system. One possible solution for this is to have individual converters for each module. Such PCIs are known as micro-inverters (μIs). PV modules with μIs produce AC output voltage of required voltage and frequency and is known as AC modules [Pal et al., 2016, De Rooij et al., 2013, Çelik et al., 2018].

For applications involving grid integration of AC modules, the alternating output to PV module voltage ratios are often high. This would require μIs capable of providing a large overall voltage gain. It is well known that though conventional boost converter is theoretically expected to give high gains, it is practically limited by parasitic resistances, stresses on switching devices, stability and efficiency considerations [Li and He, 2011]. Hence high gain converters are an inevitable part of AC modules.

A comprehensive review with classification of high step-up DC-DC converters based on their applications is presented in [Tomaszuk and Krupa, 2011, Forouzesh

et al., 2017, Hsu, 1994]. Transformer-less or non-isolated converters are often preferred for low power systems due to reduced cost, size and improved efficiency [Li and He, 2011,Forouzesh et al., 2017,Liang et al., 2012,Axelrod et al., 2008,Shen et al., 2016, Shen et al., 2017]. The non-isolated high gain DC-DC converters can be broadly classified based on the voltage boosting technique as interleaved boost, switched capacitor and/or inductor, voltage multiplier, coupled inductor based and Z-source based converters (ZSC) [Zhang et al., 2017, Shen et al., 2016]. Among these converters, high-gain ZSC have advantages over the other voltage boosting techniques in terms of reduced number of components, higher efficiency and simplicity of control [Siwakoti et al., 2015, Tayebi and Batarseh, 2018].

The high-gain converter in a μI for AC module is followed by an inverter which is generally single-phase due to the low power rating of the system. The existing low power GTIs are either two or three level inverters which require large filter components to limit the total harmonic distortion (THD) of the grid current within grid requirements [Association et al., 2003, Group et al., 2014]. The filter inductance and capacitance requirements can be reduced without affecting the harmonics content by employing multi-level inverters [Rahim et al., 2011]. However the existing multi-level inverter topologies achieve increased number of levels with an increased number of switches and passive components. This decreases the overall efficiency and increases the complexity of the system and control. Choice of inverter is hence a trade-off between filter requirement and system efficiency which suggests that use of multi-level inverters is not advisable for low power applications, such as in AC modules. However, the psuedo DC-link (pDC-l) inverters can help overcome this limitation [Meneses et al., 2013].

The pDC-l inverter is based the concept that an alternating output voltage can be obtained from a single-phase H-bridge inverter operating at fundamental frequency if its input DC-link voltage varies as a rectified sinusoid. This concept can be first found in literature in [Jalade et al., 1981] with further analysis in [Capel et al., 1982]. It has advantages over all other multi-level inverter configurations in terms of improved waveform with very low THD without additional switching or passive components. Moreover, the inverter operating at fundamental frequency switches only at zero voltage resulting in negligible switching losses and dead-time effects. Several improvements have been proposed over the years for this method which is commonly termed in literature as 'unfolding circuit'or 'pseudo DC-link inverter' [Yang and Sen, 1998, Yang. and Sen, 2000, Reddy et al., 2015, Rodriguez and Amaratunga, 2008, Caceres and Barbi, 1999, Liang et al., 2004, Ahmed et al., 2013, Thang et al., 2014, Husev et al., 2018].

In [Yang and Sen, 1998], the duty ratio of a conventional buck converter is controlled to obtain a fully rectified sinusoidal output. It is cascaded with a single-phase H-bridge inverter operating at fundamental frequency to feed resistive loads. A bidirectional circuit is proposed in [Yang. and Sen, 2000] that can support both resistive and inductive loads. In [Reddy et al., 2015], an n-level sinusoidal output is obtained by implementing an embedded control for a buck converter followed by a single-phase H-bridge inverter operating at fundamental frequency. The input DC voltage should be greater than the expected peak output voltage when a buck converter is used. This is a shortcoming when used for PV applications as the series connection of a large number of modules increases the probability of power loss under module mismatching conditions.

In [Rodriguez and Amaratunga, 2008], module level conversion is made possible at the expense of increased number of power conversion stages. A full bridge inverter with a high frequency transformer and bridge rectifier is used to amplify PV voltage and feed a buck converter followed by H-bridge inverter. A boost inverter topology with gain characteristics represented by $G = \frac{2d-1}{d(1-d)}$ is proposed in [Caceres and Barbi, 1999]. The duty ratio is varied around 0.5 to obtain an AC output voltage. In [Liang et al., 2004], the boost inverter topology was improved by operating only one of the converters in a half cycle thereby improving the efficiency yet providing similar results as in [Caceres and Barbi, 1999]. Though both buck and boost operations are possible in boost inverters, the complementary switching requirement results in increased complexity of control. In [Ahmed et al., 2013], a two-stage micro-inverter for single-phase grid integration of PV at module level is proposed. A switched inductor boost converter is used to obtain an improved gain in comparison with conventional boost converter, and is followed by a current-shaping circuit.

Interleaved fly-back converter cascaded with an unfolding H-bridge based are considered as a classical architecture of pseudo DC link micro-inverters. In [Thang et al., 2014], a grid connected PV system at module level with pseudo DC link is achieved using distributed fly-back converters operating in continuous conduction mode (CCM). Though the CCM operation overcomes the drawbacks of discontinuous conduction mode (DCM) such as high current stresses and lower efficiencies, it requires high frequency sensors and complex control [Christidis et al., 2016]. In [Husev et al., 2018], a novel family of single stage buck boost inverter is introduced with detailed analysis and comparison with similar existing topologies. The tapped inductor and single-inductor twisted unfolding circuits utilize coupled inductors to achieve high gains. The gain factor is similar to that of a conventional

buck-boost converter.

From the literature review, it is noticed that though several high gain ZSC are available in literature, their suitability for AC module applications when cascaded with pDC-l inverters have not been reported. Furthermore, the control of μIs are expected to ensure simple but high efficiency operation. As discussed, HC is known to provide superior control with reduced complexity. However, the control of μI topologies using HC are non-existent in the available literature.

1.7 Motivation

Based on literature review, the following research gaps were identified in the area of PCIs for PV-grid integration:

- The varying switching frequency provides several challenges when used for control of grid connected inverter.
  - The existing switching frequency formulation has several shortcomings. Hence a precise and generalized estimation of the switching frequency of multilevel inverters is required.
  - The effects of varying operating conditions on frequency is assumed to be considerable. However no analysis exists in the available literature.
- The HC also suffers from the limitation of high precision current sensors and digital sampling.
  - An AC current sensorless HC is a solution to the problem of high precision current sensor. However the existing sensorless controls when modified to suit the specific application can result in increased computational requirement.
  - The effect of dynamic changes and digital sampling in case of an AC current sensorless HC requires further analysis.
- Independent input and output control can be achieved in single stage inverters by employing Z-source inverters. Existing open and closed loop controls are based on conventional or modified PWM techniques.
  - HC and its advantages are not yet analysed for ZSI in detail.
  - Closed loop controls for ZSI using HC is not widely explored in the available literature.

- Topologies for AC modules and their controls are an emerging area of interest for researchers. AC modules are expected to operate at very high efficiency due to their low power rating and the choice of converter topology and control can affect the overall efficiency.
  - The use of Z-source converters and pseudo DC link concept for the specific application has not been explored in detail.
  - A closed loop control of AC modules with HC is not available in the existing literature.

1.8 Objectives

Based on the research gaps observed in the available literature, the following were identified as research objectives:

1. To precisely estimate the switching frequency of a hysteresis current controlled multilevel GTIs.
2. To develop a AC current sensor less control based on switching instant analysis considering the effects of real-time operating conditions.
3. To develop an independent input and output control using HC for single stage string inverters implemented by ZSI.
4. To develop an efficient closed loop control with HC for AC modules consisting of high gain converter cascaded by pDC-l inverter.

1.9 Organization of Thesis

There are six chapters in this thesis report. The chapter 1 presented a brief introduction to the state-of-the-art of grid tie inverters, their requirements and non-ideal operating conditions. A review of the existing topologies and controls for power conversion interfaces is presented. The HC for PCI and its advantages are also discussed. The shortcomings of HC that hinder its use in many applications are identified. Further a detailed literature review based on these shortcomings and existing solutions are presented. Based on the review, research gaps are identified as the motivation to this work and the objectives of the thesis are formulated. Each of the following chapters present the work done towards achieving these objectives.

Chapter 2: A generalized formulation for switching frequency variation in HC of multi-level inverters is presented. The improvement in system design is verified by an example of filter design. The effect of system parameters and operating conditions on the switching frequency is analysed.

Chapter 3: As a solution to the high precision current sensor requirement in HC, an AC current sensorless hysteresis current control for two level GTI is developed and presented. The effects of non-linearity in ripple current, dynamic variations and digital sampling are analysed. The control is modified to minimize these effects.

Chapter 4: A closed loop HC for a single stage string inverter using an ZSI is presented. The switching interval analysis and the maximum boost ratio using the proposed control are discussed.

Chapter 5: A closed loop control is developed for a pDC-l μI with high gain ZSC. The operating modes of the considered ZSC when cascaded with pDC-l inverter is discussed in detail.

Chapter 6: This chapter summarizes the thesis with major contributions and discussions on possible future research.

Chapter 2

Switching Frequency Formulation of Hysteresis Control

Contents

2.1 Introduction

The grid tie inverter (GTI) is an essential stage in power conversion interfaces, amongst which multilevel GTIs (MGTIs) are more prevalent lately due to reduced switching losses, harmonics and filter size. A large range of operating conditions are possible in MGTIs, due to sudden changes in the input and grid. Hence simple and stable inverter controls with robust steady state operation and rapid dynamic response are vital [Group et al., 2014, Association et al., 2003]. From the discussion in section 1.5.1, hysteresis control (HC) is an ideal choice due to its rugged and accurate control with fast dynamic response. Though the simple and direct modulation is enabled, its variable frequency of HC inhibits its use in MGTI applications due to the difficulties in the system and control designing. Therefore formulating the switching frequency of HC can aid in low-pass filter (LPF) design [Beres et al., 2016, Wu et al., 2017a, Jayalath and Hanif, 2017, Solatialkaran et al., 2018], switching device selection and loss estimation [Anderson et al., 2017, Bazzi et al., 2012, Sadigh et al., 2016, Delaram et al., 2018].

In the available literature, the switching frequency estimations for low frequency operation and at those instants of slope reversal of current in MGTI are overlooked. This causes erroneous calculations resulting in imprecise system design. Hence the major contributions of this chapter are summarized as follows.

- A precise and generalized expression for switching frequency is derived for single-phase MGTI employing HC considering non-linear ripple current.
- To demonstrate the improvement using the proposed formulation, an example of a second order filter design is discussed. The limitations of the existing equation due to the assumption of linear ripple current is emphasized.
- The effects of change in hysteresis band, input voltage and phase shift on the switching frequency are analysed. The operating point at which the switching frequency is to be estimated for an accurate system design is determined.

2.2 HC of MGTI and Analysis of Ripple Current

Consider a single-phase MGTI of any existing topology with n-level output voltage v_{i}, connected to the grid with voltage $v_{\mathrm{g}} = V_{\mathrm{g}} \sin(\omega t)$ via a LPF as shown in Fig. 2.1. Let the inverter side filter inductance be L_{i} and the current through it

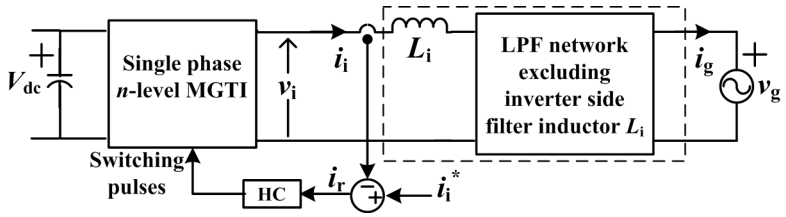


Figure 2.1: Single-phase MGTI with HC connected to the grid via LPF

be i_i. For DC input voltage V_dc, the n levels of v_i can be defined as $\frac{p}{p_\mathrm{n}}V_\mathrm{dc}$, where $p_\mathrm{n} = \frac{n-1}{2}$ and $p = \{-p_\mathrm{n}, ..0, ..p_\mathrm{n}\}$. For example, in a 3-level inverter, $p_\mathrm{n} = 1$ and $p = \{-1, 0, 1\}$ and the three levels are $\{-V_\mathrm{dc}, 0, V_\mathrm{dc}\}$. For all MGTI controls including HC, the actual inverter output current i_i is required to be controlled to a reference current i_i^*. Let $v_\mathrm{i}^* = V_\mathrm{i}^* \sin(\omega t + \theta)$ be the reference inverter output voltage corresponding to the reference current i_i^*, where V_i^* is the peak reference voltage and θ is the phase shift w.r.t. the grid voltage v_g. To generalize the analysis for all LPF configurations, V_i^* and θ are considered as functions of v_g, i_i^* and filter parameters. The modulating signal $m = M \sin(\omega t + \theta)$ is

$$m = \frac{v_\mathrm{i}^*}{V_\mathrm{dc}} = \frac{V_\mathrm{i}^*}{V_\mathrm{dc}} \sin(\omega t + \theta) \tag{2.1}$$

In HC, the inverter output current i_i is controlled by comparing it with a reference i_i^* to generate the ripple current $i_\mathrm{r} = i_\mathrm{i}^* - i_\mathrm{i}$. The ripple current is then maintained within predefined hysteresis limits by switching the inverter accordingly. From the dynamic equations for i_i^* and i_i in (2.2) and (2.3), the rate of change of i_r can be expressed as in (2.4).

$$\frac{\mathrm{d}i_\mathrm{i}^*}{\mathrm{d}t} = \frac{1}{L_\mathrm{i}} (v_\mathrm{i}^* - v_\mathrm{g}) \tag{2.2}$$

$$\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t} = \frac{1}{L_\mathrm{i}} (v_\mathrm{i} - v_\mathrm{g}) \tag{2.3}$$

$$\frac{\mathrm{d}i_\mathrm{r}}{\mathrm{d}t} = \frac{\mathrm{d}i_\mathrm{i}^*}{\mathrm{d}t} - \frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t} = \frac{1}{L_\mathrm{i}} (v_\mathrm{i}^* - v_\mathrm{i}) \tag{2.4}$$

Substituting v_i^* from (2.1), we obtain the rate of change of ripple current as

$$\frac{\mathrm{d}i_\mathrm{r}}{\mathrm{d}t} = \frac{V_\mathrm{dc}}{L_\mathrm{i}} \left(m - \frac{v_\mathrm{i}}{V_\mathrm{dc}} \right). \tag{2.5}$$

For the HC employed, let h be the hysteresis width and 2δ be the dead zone between hysteresis bands to avoid their overlapping. With reference to Fig. 2.2, let k be the present switching level where $k \in p$, $k \neq -p_\mathrm{n}$. For a constant DC input voltage V_dc, the ratio $\frac{v_\mathrm{i}}{V_\mathrm{dc}}$ would switch between $\frac{k}{p_\mathrm{n}}$ and $\frac{k-1}{p_\mathrm{n}}$ while i_r remains

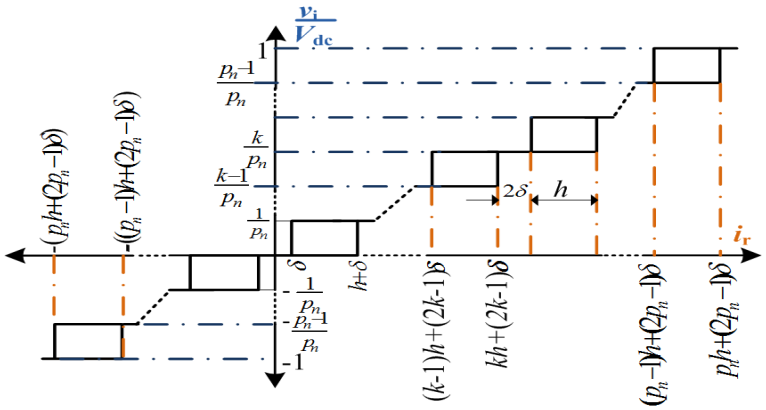


Figure 2.2: Hysteresis limits corresponding to ripple current i_{r} and the ratio $\frac{v_{\mathrm{i}}}{V_{\mathrm{dc}}}$

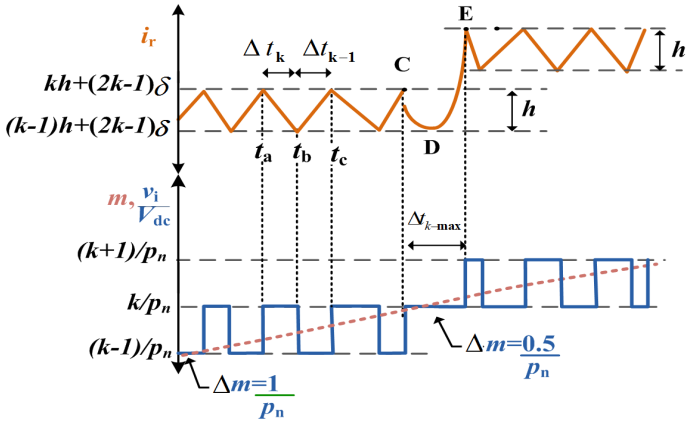


Figure 2.3: Ripple current i_{r}, modulating signal $m = \frac{v_{\mathrm{i}}^*}{V_{\mathrm{dc}}}$ and the ratio $\frac{v_{\mathrm{i}}}{V_{\mathrm{dc}}}$

limited within the band $kh+(2k-1)\delta$ and $(k-1)h+(2k-1)\delta$. The ripple current i_{r}, modulating signal $m = \frac{v_{\mathrm{i}}^*}{V_{\mathrm{dc}}}$, and the ratio $\frac{v_{\mathrm{i}}}{V_{\mathrm{dc}}}$ can be observed in Fig. 2.3.

Consider the interval $t_{\mathrm{a}} \leq t < t_{\mathrm{c}}$ in (2.5), the slope of ripple current $\dfrac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t}$ is

$$\frac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t} = \frac{V_{\mathrm{dc}}}{L_{\mathrm{i}}} \begin{cases} m - \frac{k}{p_{\mathrm{n}}} \; ; & t_{\mathrm{a}} \leq t < t_{\mathrm{b}} \\ m - \frac{k-1}{p_{\mathrm{n}}} \; ; & t_{\mathrm{b}} \leq t < t_{\mathrm{c}} \end{cases} \tag{2.6}$$

The switching intervals are $\Delta t_{\mathrm{k}} = t_{\mathrm{b}} - t_{\mathrm{a}}$ and $\Delta t_{\mathrm{k-1}} = t_{\mathrm{c}} - t_{\mathrm{b}}$. From the rate of change of ripple current in (2.6), we derive the expressions of switching intervals.

2.3 A Discussion on the Existing Switching Frequency Formulation

In the existing literature, (2.6) is linearised and the slope of ripple current $\dfrac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t}$ is approximated to $\frac{\Delta i_{\mathrm{r}}}{\Delta t}$. Let the switching intervals be $\Delta t_{\mathrm{k_L}}$ and $\Delta t_{\mathrm{k-1_L}}$ when linear ripple current is assumed as shown in Fig. 2.4. The change in ripple current

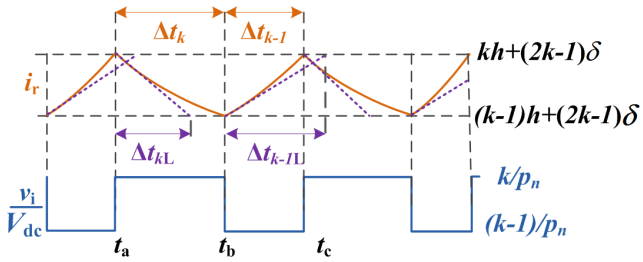


Figure 2.4: Ripple current i_{r} to analyze switching instants

during these intervals are $-h$ and h respectively. Hence $\frac{\Delta i_{\mathrm{r}}}{\Delta t}$ is expressed as

$$\frac{\Delta i_{\mathrm{r}}}{\Delta t} = \begin{cases} \frac{-h}{\Delta t_{\mathrm{k_L}}} & ; \quad t_{\mathrm{a}} \leq t < t_{\mathrm{b}} \\ \frac{h}{\Delta t_{\mathrm{k-1_L}}} & ; \quad t_{\mathrm{b}} \leq t < t_{\mathrm{c}} \end{cases} \tag{2.7}$$

From (2.6) and (2.7), the change in current during the switching intervals are

$$-h = \frac{V_{\mathrm{dc}}}{L_{\mathrm{i}}} \left(m - \frac{k}{p_{\mathrm{n}}} \right) \Delta t_{\mathrm{k_L}} \text{and} \tag{2.8}$$

$$h = \frac{V_{\mathrm{dc}}}{L_{\mathrm{i}}} \left(m - \frac{k-1}{p_{\mathrm{n}}} \right) \Delta t_{\mathrm{k-1_L}} \tag{2.9}$$

Hence $\Delta t_{\mathrm{k_L}} = \frac{L_{\mathrm{i}} h}{V_{\mathrm{dc}}} \frac{1}{\Delta m}$ and $\Delta t_{\mathrm{k-1_L}} = \frac{L_{\mathrm{i}} h}{V_{\mathrm{dc}}} \frac{1}{\frac{1}{p_{\mathrm{n}}} - \Delta m}$, where $\Delta m = \frac{k}{p_{\mathrm{n}}} - m$. The switching frequency $f_{\mathrm{sw-L}}$ assuming linear ripple current is obtained as in (2.10).

$$f_{\mathrm{sw-L}} = \frac{V_{\mathrm{dc}}}{L_{\mathrm{i}} h} \Delta m p_{\mathrm{n}} \left(\frac{1}{p_{\mathrm{n}}} - \Delta m \right) \tag{2.10}$$

This expression for frequency is analogous to those in existing literature ([Albanna and Hatziadoniu, 2010,Gupta, 2012,Kumar and Gupta, 2017,Gautam and Gupta, 2014]). The maximum switching frequency occurs at $\Delta m = \frac{0.5}{p_{\mathrm{n}}}$ and expressed as

$$f_{\mathrm{max-L}} = \frac{V_{\mathrm{dc}}}{4 L_{\mathrm{i}} h p_{\mathrm{n}}} \tag{2.11}$$

In the existing literature of [Gautam and Gupta, 2014], the frequency is considered minimum $\Delta m = 1 - M$ and is expressed as in (2.12).

$$f_{\mathrm{min-L}} = \frac{p_{\mathrm{n}} V_{\mathrm{dc}}}{L_{\mathrm{i}} h} (1 - M) \left(\frac{1}{p_{\mathrm{n}}} - 1 + M \right) \tag{2.12}$$

2.3.1 Limitations of the existing formulation

As we observe from Fig.2.4, when the variation in ripple current i_{r} is assumed to be linear, the switching intervals are not accurate. In other words, we obtain the

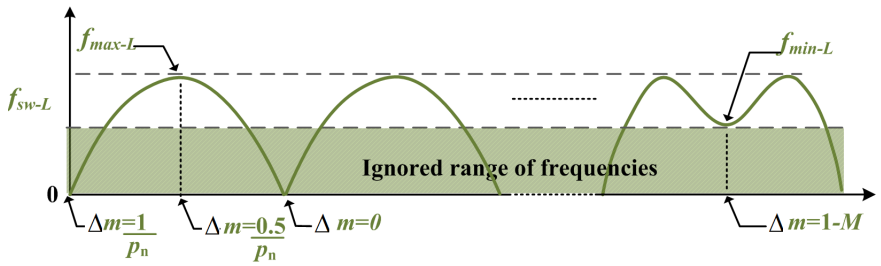


Figure 2.5: Switching frequency variations as per existing literature

approximate intervals $\Delta t_{\mathrm{k_L}}$ and $\Delta t_{\mathrm{k-1_L}}$ instead of the actual switching intervals Δt_{k} and $\Delta t_{\mathrm{k-1}}$. This can result in an error in the estimation of switching frequency variation, especially during low frequencies.

To analyse this further, we plot the switching frequency variation depicted by the existing equation presented in (2.10) as shown in Fig.2.5. On analysing the equation, we can notice that $f_{\mathrm{sw-L}} = 0$ at two instants during a switching level k, viz. when $\Delta m = 0$ and $\Delta m = \frac{1}{p_{\mathrm{n}}}$. However, practically the switching frequency of an inverter is never zero and is expected to be greater than 10 times the grid frequency in GTI applications [Wu et al., 2017a]. Therefore it is certain that (2.10) does not accurately estimate the switching frequency.

All frequencies less than $f_{\mathrm{min-L}}$, specifically the instants at which $f_{\mathrm{sw-L}} = 0$, are ignored in the existing literature [Gautam and Gupta, 2014]. However the frequencies around these unaccounted intervals are often less than $f_{\mathrm{min-L}}$ as shown in Fig. 2.5. The minimum switching frequency is an important parameter for system design including design of LPF. Therefore such errors result in inaccurate design leading to problems such as resonance in second order filters. Furthermore, as the switching period increases, the switching frequency calculated using (2.10) can be incorrect for a wider range. It is observed from Fig. 2.3 that the reason for this error is owing to the invalid assumption of linear ripple current specifically during the intervals when the ripple current reverses following the path CDE. Therefore in this work, the non-linearity in ripple current is considered while formulating an improved expression for switching frequency.

2.4 Generalized Switching Frequency Considering Non-linear Nature of Ripple Current

To consider the non-linear nature of ripple current in this work, the slope of ripple current in (2.6) is integrated within the limits of corresponding switching intervals.

During the interval $t_a \leq t < t_b$, $\int_{t_a}^{t_b} \frac{di_r}{dt} dt = \frac{V_{dc}}{L_i} \int_{t_a}^{t_b} \left(m - \frac{k}{p_n}\right) dt$

$$\implies \left[i_r(t)\right]_{t_a}^{t_b} = \frac{V_{dc}}{L_i} \left[\frac{-M\cos(\omega t + \theta)}{\omega} - \frac{k}{p_n} t\right]_{t_a}^{t_b}$$

Simplifying the above expression using trigonometric identities, we obtain (2.13), where $\dot{m} = \frac{dm}{dt} = \omega M \cos(\omega t + \theta)$.

$$-h = \frac{V_{dc}}{L_i} \left[\frac{m \sin(\omega \Delta t_k)}{\omega} + \frac{\dot{m}\,(1 - \cos(\omega \Delta t_k))}{\omega^2} - \frac{k}{p_n} \Delta t_k\right] \tag{2.13}$$

For small values of Δt_k(<1ms), (2.13) can be simplified using second order approximation of Maclaurin series (Taylor series expansion centered at zero) for sine and cosine functions as in (2.14). This is also known as small angle approximation.

$$\cos(\omega \Delta t_k) = 1 - 0.5(\omega \Delta t_k)^2 \quad , \quad \sin(\omega \Delta t_k) = \omega \Delta t_k \tag{2.14}$$

Substituting (2.14) in (2.13), the change in current , considering a non-linear rate of change of ripple current during $t_a \leq t < t_b$, is obtained as in (2.15). Similarly, during $t_b \leq t < t_b$, the change in ripple current can be expressed as (2.16).

$$-h = \frac{V_{dc}}{L_i} \left[\left(m - \frac{k}{p_n}\right) \Delta t_k + 0.5 \dot{m} \Delta t_k^2\right] \tag{2.15}$$

$$h = \frac{V_{dc}}{L_i} \left[\left(m - \frac{k-1}{p_n}\right) \Delta t_{k-1} + 0.5 \dot{m} \Delta t_{k-1}^2\right] \tag{2.16}$$

On comparing (2.8) and (2.9) with (2.15) and (2.16) respectively, it is observed that the additional term $0.5\dot{m}\Delta t_k^2$ is accountable for considering the non-linearity of i_r. This additional term takes into account of the rate of change of m within the switching interval which is the cause of non-linearity in i_r. Substituting $\Delta m = \frac{k}{p_n} - m$ and $C = \frac{L_i h}{V_{dc}}$, (2.15) and (2.16) are simplified as

$$0.5 \dot{m} \Delta t_k^2 - \Delta m \Delta t_k + C = 0 \text{ and} \tag{2.17}$$

$$0.5 \dot{m} \Delta t_{k-1}^2 + \left(\tfrac{1}{p_n} - \Delta m\right) \Delta t_{k-1} - C = 0 \tag{2.18}$$

To obtain Δt_k and Δt_{k-1}, the quadratic equations in (2.17) and(2.18) are solved. In general, quadratic equations of the form $ax^2 + bx^+c = 0$ ($a \neq 0$) can have two solutions, one solution or no solution based on the values of a, b and c. When the equation has two solutions, viz. $\frac{1}{2}(-b \pm \sqrt{b^2 - 4ac})$, the appropriate

solution is chosen based on other known conditions or constraints. On analysis, it is observed that the choice of solution of (2.17) and (2.18) depends on the sign of $\dot{m}$. Hence, Δt_{k} and $\Delta t_{\mathrm{k}-1}$ can be simplified as (2.19) and (2.20) respectively . The switching frequency is obtained as in (2.21).

$$\Delta t_{\mathrm{k}} = \begin{cases} \Delta t_{\mathrm{k_L}} & ; |\dot{m}| = 0 \\ \dfrac{-\Delta m + \sqrt{\Delta m^2 + 2C|\dot{m}|}}{|\dot{m}|} & ; |\dot{m}| \neq 0 \end{cases} \tag{2.19}$$

$$\Delta t_{\mathrm{k}-1} = \begin{cases} \Delta t_{\mathrm{k}-1_{\mathrm{L}}} & ; |\dot{m}| = 0 \\ \dfrac{-\left(\frac{1}{p_{\mathrm{n}}} - \Delta m\right) + \sqrt{\left(\frac{1}{p_{\mathrm{n}}} - \Delta m\right)^2 + 2C|\dot{m}|}}{|\dot{m}|} & ; |\dot{m}| \neq 0 \end{cases} \tag{2.20}$$

$$f_{\mathrm{sw}} = \begin{cases} f_{\mathrm{sw-L}} & ; |\dot{m}| = 0 \\ \dfrac{|\dot{m}|}{-\frac{1}{p_{\mathrm{n}}} + \sqrt{\Delta m^2 + 2C|\dot{m}|} + \sqrt{\left(\frac{1}{p_{\mathrm{n}}} - \Delta m\right)^2 + 2C|\dot{m}|}} & ; |\dot{m}| \neq 0 \end{cases} \tag{2.21}$$

From Fig. 2.5, the maximum frequency occurs when m takes a value exactly half between the two consecutive switching levels, i.e. $m = 0.5\left(\frac{k}{p_{\mathrm{n}}} + \frac{k-1}{p_{\mathrm{n}}}\right)$ and hence $\Delta m = \frac{0.5}{p_{\mathrm{n}}}$. The expression for maximum frequency can be derived by substituting for Δm in (2.21) and simplifying as in (2.22).

$$f_{\mathrm{max-NL}} = \frac{|\dot{m}|p_{\mathrm{n}}}{2\sqrt{0.25 - 2Cp_{\mathrm{n}}^2|\dot{m}|} - 1} = f_{\mathrm{max-L}}\left(\sqrt{0.25 - 2Cp_{\mathrm{n}}^2|\dot{m}|} + 0.5\right) \tag{2.22}$$

At high switching frequencies, the rate of change of modulating signal within the switching period $\dot{m} \to 0$. On substituting $\dot{m} = 0$, the maximum frequency $f_{\mathrm{max-NL}}$ in (2.22) can be approximated to $f_{\mathrm{max-L}}$ in (2.11). Therefore maximum frequency is hereafter denoted by f_{max} calculated using (2.11).

The approximation of $\dot{m} \to 0$ is invalid while estimating the minimum frequency as the range of frequency variation for HC is considerably large. From Fig. 2.5, the minimum frequency is observed to occur when $\Delta m = 0$ (or $\frac{1}{p_{\mathrm{n}}} - \Delta m = 0$). Substituting this in (2.21), we obtain the expression for $f_{\mathrm{min-NL}}$ as

$$f_{\mathrm{min-NL}} = \frac{|\dot{m}|p_{\mathrm{n}}}{-1 + \sqrt{2Cp_{\mathrm{n}}^2|\dot{m}|} + \sqrt{1 + 2Cp_{\mathrm{n}}^2|\dot{m}|}}. \tag{2.23}$$

The improvement in accuracy of frequency estimation by the proposed method is demonstrated by comparing the frequencies of 3, 5 and 7 level inverters deter-

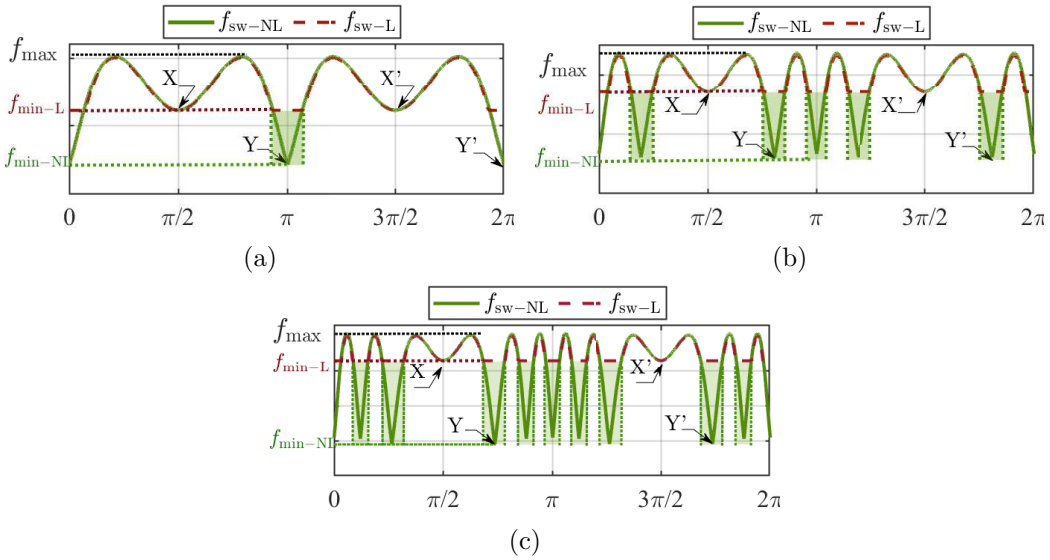


Figure 2.6: Switching frequencies $f_{\mathrm{sw-L}}$(2.10) and $f_{\mathrm{sw-NL}}$(2.21) of (a) 3 level, (b) 5 level and (c) 7 level inverters

mined using the existing and proposed equations, i.e. (2.10) and (2.21) respectively, as shown in Fig.2.6. As per the existing literature [Gautam and Gupta, 2014], the minimum frequency $f_{\mathrm{min-L}}$ is assumed to be at X. This implies that frequencies less than $f_{\mathrm{min-L}}$ are ignored as shown in Fig.2.6. However if the switching frequency is calculated considering the non-linearity of error current using the proposed formulation (2.21), it is noticed that the minimum frequency $f_{\mathrm{min-NL}}$ occurs at Y. Furthermore $f_{\mathrm{min-NL}} < f_{\mathrm{min-L}}$ for 3, 5 and 7 level inverters. This can have a considerable effect while deciding the minimum frequency for filter design and calculating switching and conduction losses. The actual minimum frequency $f_{\mathrm{min-NL}}$ maybe less than $10f_{\mathrm{g}}$ if the hysteresis band h and inverter side inductor L_{i} are chosen based on $f_{\mathrm{min-L}}$. This can induce low frequency harmonic distortions in the grid current [Beres et al., 2016] and is avoided if the proposed equation (2.21) is used to estimate switching frequency.

2.5 Filter design example demonstrating requirement of accurate formulation

The proposed formulation is observed to accurately calculate the switching frequency specifically around the instants of current reversal (shaded regions in Fig. 2.6). However, the need for such an accurate estimation of frequency is justified with an example of second order filter design. Among the various configurations of LPFs [Beres et al., 2016], the LCL filter provides better response

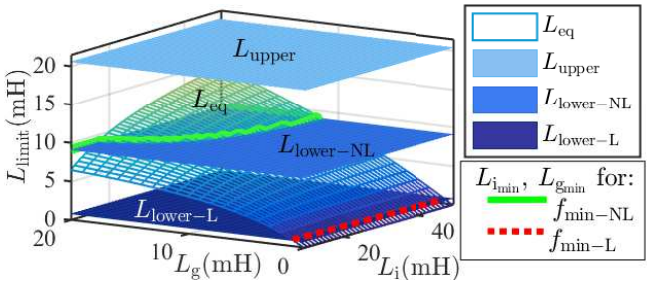


Figure 2.7: L_{eq} mapped as a function of L_1 and L_2

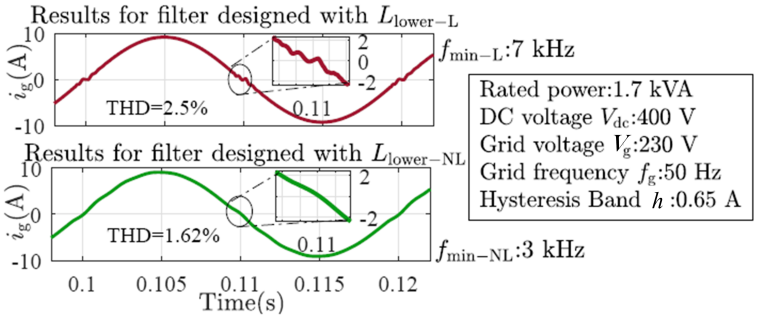


Figure 2.8: Grid Current i_{g} for filter designed based on frequency calculated using (2.10) as per [Gautam and Gupta, 2014] and using the proposed formulation (2.21)

with reduced filter size and reduces the effect of grid impedance. Due to resonance in its second order network, an LCL filter configuration can clearly demonstrate the effect of error in switching frequency calculations [Wu et al., 2017b]. Let L_{i} and L_{g} be the inverter side and grid side filter inductances and Cf be the filter capacitance. As per the known design procedure [Delaram et al., 2018], L_{i}, C_{f} and L_{g} should satisfy the following inequalities.

$$L_i \geq \frac{V_{\text{dc}}}{4hp_{\text{n}}f_{\text{max-NL}}} \text{ and } C_{\text{f}} \leq \frac{5\%S_{\text{rated}}}{\omega V_{\text{g}}^2} \tag{2.24}$$

$$10f_{\text{g}} \leq \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i L_g C_{\text{f}}}} \leq 0.5f_{\text{min}} \tag{2.25}$$

If $L_{\text{eq}} = \frac{L_i L_g}{L_i + L_g}$, (2.25) is simplified to (2.26).

$$\left[(\pi f_{\text{min}})^2 C_{\text{f}}\right]^{-1} \leq L_{\text{eq}} \leq \left[(20\pi f_{\text{g}})^2 C_{\text{f}}\right]^{-1}. \tag{2.26}$$

The upper limit on L_{eq}, $L_{\text{upper}} = [(20\pi f_{\text{min}})^2 C_{\text{f}}]^{-1}$, depends on the grid frequency f_{g} while the lower limit on L_{eq} is dictated by the minimum switching frequency f_{min}. The lower limits calculated with $f_{\text{min-L}}$ and $f_{\text{min-NL}}$ are termed as $L_{\text{lower-L}} = [(\pi f_{\text{min}})^2 C_{\text{f}}]^{-1}$ respectively. For ease of design, L_{eq}, L_{upper}, $L_{\text{lower-L}}$

and $L_{\text{lower}-\text{NL}}$ are mapped as functions of L_{i} and L_{g} as shown in Fig.2.7. The values of L_{i} and L_{g} should be chosen such that L_{eq} lie within the limits L_{lower} and L_{upper}. When the minimum frequency is assumed as $f_{\text{min}-\text{L}}$ as per the existing formulation [Gautam and Gupta, 2014], $L_{\text{lower}} = L_{\text{lower}-\text{L}}$. The minimum values of L_{i} and L_{g}, i.e. $[L_{\text{i}_{\text{min}}}, L_{\text{g}_{\text{min}}}]$ lie on the points of intersection of L_{eq} and $L_{\text{lower}-\text{NL}}$. Clearly $[L_{\text{i}_{\text{min}}}, L_{\text{g}_{\text{min}}}]$ considering $f_{\text{min}-\text{NL}}$ is greater than those assuming $f_{\text{min}-\text{L}}$.

To analyse the effect of choice L_{i} and L_{g}, the grid current i_{g} obtained with filters designed considering the minimum frequency equal to $f_{\text{min}-\text{L}}$ and $f_{\text{min}-\text{NL}}$ are compared as shown in Fig. 2.8. If the filter is designed assuming $f_{\text{min}} = f_{\text{min}-\text{L}}$, the grid current i_{g} show distortions when the switching frequency is less than $f_{\text{min}-\text{L}}$. This occurs particularly around the zero-crossings in a 3 level inverter which contribute to increased lower order harmonics. Furthermore, these low order harmonics affect the current waveform at instants other than zero-crossings in case of higher level inverters as seen in Fig. 2.6. With reference to Fig. 2.8, notice that these distortions are considering $f_{\text{min}} = f_{\text{min}-\text{NL}}$. The current waveform and THD are observed to have clearly improved. This supports the requirement of the proposed formulation despite the marginal increase in computation.

2.6 Effect of Variation of System Parameters and Operating Conditions on Switching Frequency

Table 2.1: Base System Ratings

Parameter	Numerical Value
Rated power S_{rated}	1.5 kVA
DC link voltage V_{dc}	400 V
Grid voltage V_{g}(rms)	230 V, 50 Hz
Rated grid current I_{g}(rms)	6.52 A
Filter parameters L_{i}, L_{g}, C_{f}	9.7 mH, 1 mH, 4.7 μH
Hysteresis and Dead Bands h, δ	0.65 A, 0.065 A

Generally, MGTIs are designed at rated operating conditions. However on analysing 2.21 it is observed that for MGTIs employing HC, the switching frequency f_{sw} and hence $f\text{min}$ and $f_{\text{max}-\text{NL}}$ are dependent on several system parameters and operating conditions such as hysteresis band h, DC link voltage V_{dc} and the number of levels n. Hence, it is essential to examine the effect of change in switching frequency due to operating conditions on the performance of a system. The system parameters used for the calculations are as listed in Table 2.1.

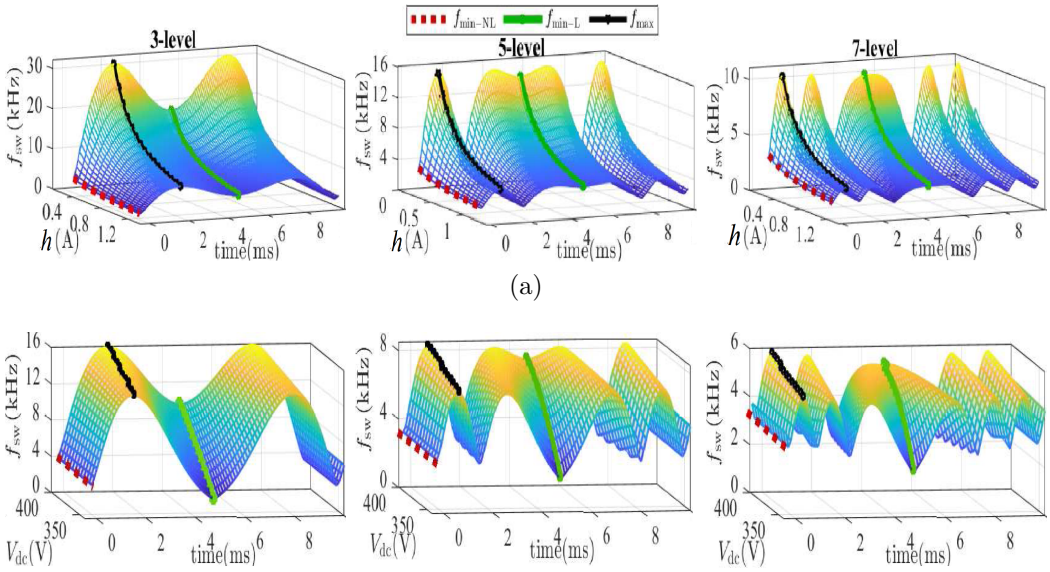


Figure 2.9: Computed values of $f_{\mathrm{sw-NL}}$ of 3, 5 and 7 level inverters with $f_{\mathrm{max-NL}}$, $f_{\mathrm{min-L}}$ and $f_{\mathrm{min-NL}}$ for change in (a) h and (b) V_{dc}

2.6.1 Effect of change in ripple current h

With reference to Fig. 2.9a, the computed switching frequency f_{sw} is observed to be inversely proportional to hysteresis limit h for 3, 5 and 7 level inverters. However the profile of switching frequency variation remains the same and $f_{\mathrm{min-NL}}$ is less than $f_{\mathrm{min-L}}$ throughout the considered range of variation of h. The difference between the minimum frequencies computed using the existing and proposed formulations, $f_{\mathrm{min-L}}$ and $f_{\mathrm{min-NL}}$, are observed to be significant predominantly for small values of h. The decrease in the minimum frequency $f_{\mathrm{min-NL}}$ due to change in h is observed to be gradual. However the change in $f_{\mathrm{max-NL}}$ is considerable. Generally MGTIs employing HC have a constant hysteresis band irrespective of other system variations. In case of a varying hysteresis band control, the system design should be performed with f_{max} calculated at the maximum value of h.

2.6.2 Effect of change in DC voltage V_{dc}

Fig. 2.9b shows the effect of variation in V_{dc}, from 400 V to 340 V on the switching frequency for a period of half the fundamental cycle. For 3, 5 and 7 level inverters, the maximum switching frequency, f_{max} gradually decreases in proportion with the input voltage. The minimum frequency calculated using the proposed formulation $f_{\mathrm{min-NL}}$ also has gradual change due to V_{dc}. However a steep decrease in frequency $f_{\mathrm{min-L}}$ is observed with decrease in V_{dc}. Due to this, the profile of frequency

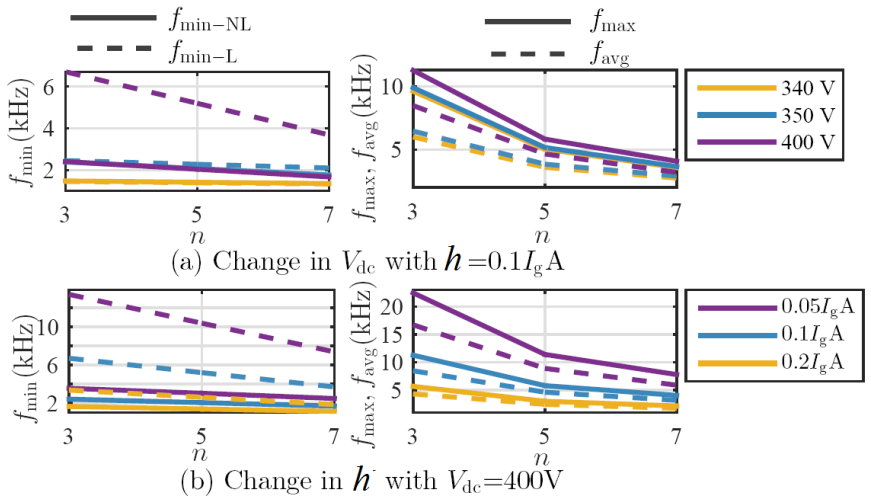


Figure 2.10: Calculated minimum, maximum and average switching frequencies for changes in V_{dc} and h

plot is observed to alter. The value of $f_{\text{min-NL}}$ is considerably less than $f_{\text{min-L}}$ for V_{dc} greater than 340 V. For MGTI applications, the DC link voltage is often maintained constant at values greater than 340 V. Hence the proposed equation for $f_{\text{min-NL}}$ gives a more accurate estimation of the minimum frequency. The system parameters can be designed at rated operating conditions for MGTI systems with possibility of variations in DC-link voltage such as PV sources.

2.6.3 Effect of change in number of levels n

The calculated minimum frequencies $f_{\text{min-L}}$ and $f_{\text{min-NL}}$, maximum frequency f_{max} and average frequency f_{avg} for 3, 5 and 7 level inverters are shown in Fig. 2.10. For all the considered cases, the minimum frequency calculated as per the proposed formulation is less that that in the existing literature, i.e. $f_{\text{min-NL}} < f_{\text{min-L}}$. The frequencies $f_{\text{min-L}}$, f_{avg} and f_{max} are observed to decrease with an increase in the number of levels n. However the change in $f_{\text{min-NL}}$ is negligibly small. Also notice that as the number of levels increase, the differences between minimum, average and maximum frequencies decrease. Thus the range of frequency variation is narrow for inverters with 7 or higher number of levels. Hence the switching frequency can be assumed approximately constant for HC of MGTIs with $n \geq 7$.

2.7 Results and Discussion

To verify the proposed formulation of switching frequency, simulations are performed in MATLAB/Simulink platform for a single-phase 3, 5 and 7 level MGTI with HC. The experimental results are obtained by implementing HC for a single-phase inverter using the dSPACE Microlab 1202 as shown in Fig. 2.11. The system

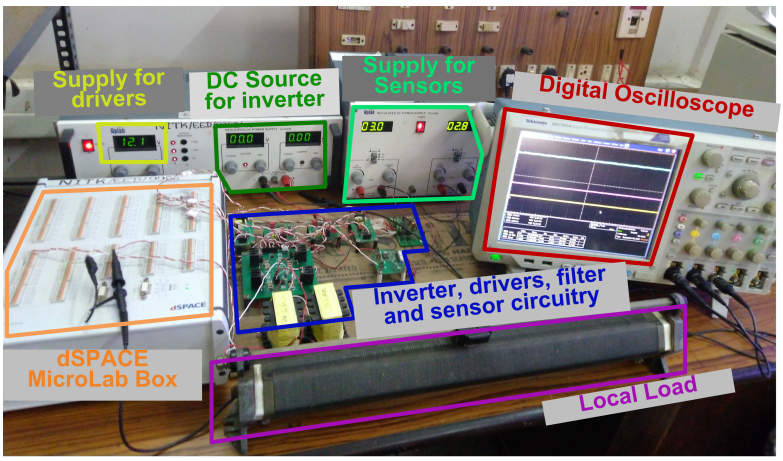


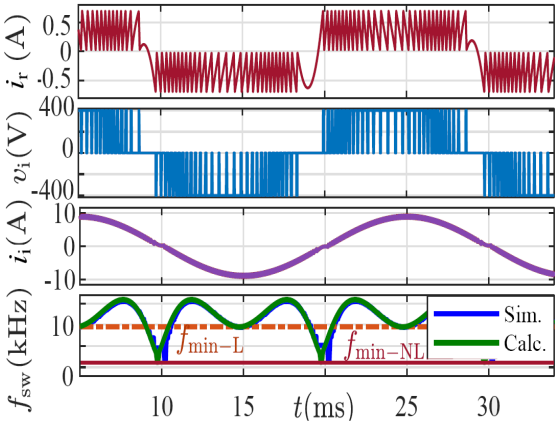
Figure 2.11: Setup used to obtain the experimental results

specifications including the filter design used for simulation and experiment are listed in Table I.

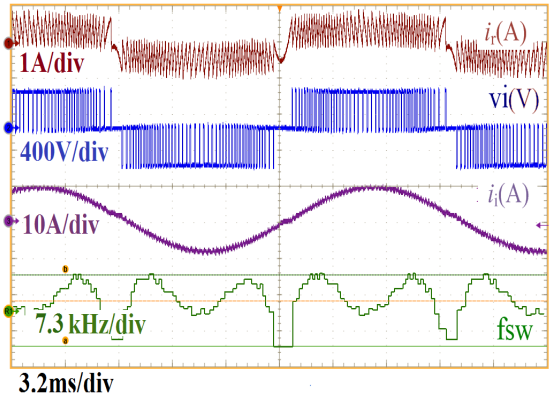
The operating conditions of MGTI change due to fluctuations in input and grid. The range of such variations are often limited by associated controls to ensure safe and stable operation. In the case of occurrence of large fluctuations beyond the grid standards, MGTI is disconnected from the grid [Group et al., 2014, Association et al., 2003]. Hence MGTI systems are designed at rated operating conditions. This is also supported by the fact that system parameter design based on worst possible operating conditions that exists only for very short duration of time can lead to over-sizing of the system. Nevertheless, to validate the proposed formulation, the results are presented for different operating conditions, in addition to the base specifications listed in Table 2.1.

The ripple current i_{r}, inverter output voltage v_{i}, current i_{i} and switching frequency f_{sw} obtained in simulation and experiment for 3 level inverter at various operating conditions are presented in Fig. 2.12. As per the existing literature, $f_{\mathrm{min-L}}$ is expected to be the minimum frequency. However, from Fig. 2.12a, it is observed that $f_{\mathrm{min-L}}$ is greater than f_{sw} for a certain range of time around the zero crossing points of i_{i} in both simulated and experimental results. This, if ignored, can cause distortions around the zero crossing in a 3 level inverter output. It is observed from the simulation result for 3 level inverter at base ratings shown in Fig. 2.12a that the actual minimum switching frequency is close to that calculated by the proposed formulation (2.23) i.e. $f_{\mathrm{min-NL}}$. Similar observations can be made for other operating conditions such as $V_{\mathrm{dc}} = 340\ V$ and $P = \frac{S_{\mathrm{rated}}}{2} = 0.75\ kW$, $Q = 0kVAr.$ in Fig. 2.12c and 2.12e as well.

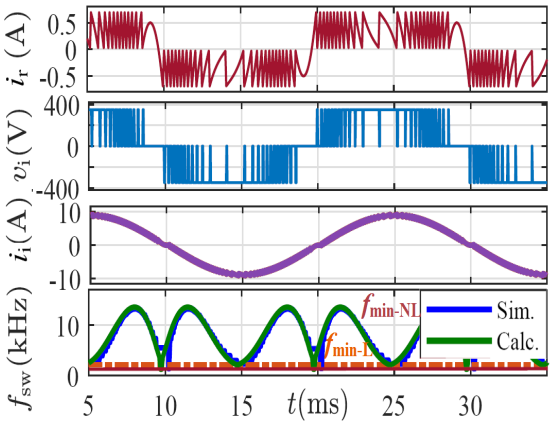
The minimum, maximum and average switching frequencies of a three-level single phase hysteresis controlled inverter for different values of hysteresis band



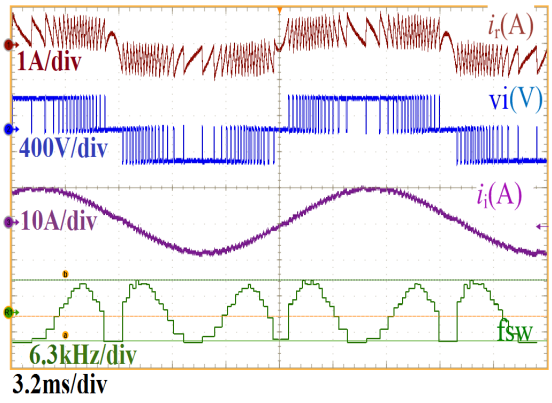
(a) Simulation results at base ratings



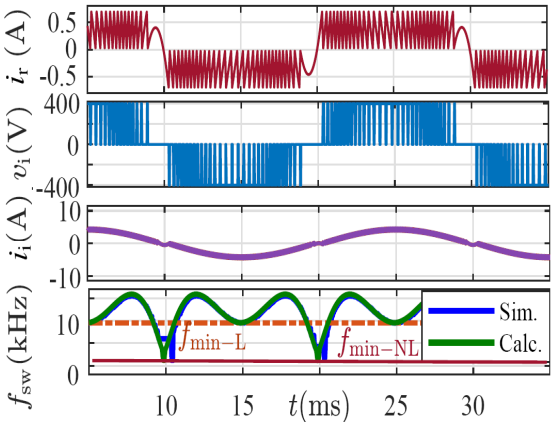
(b) Experimental results at base ratings



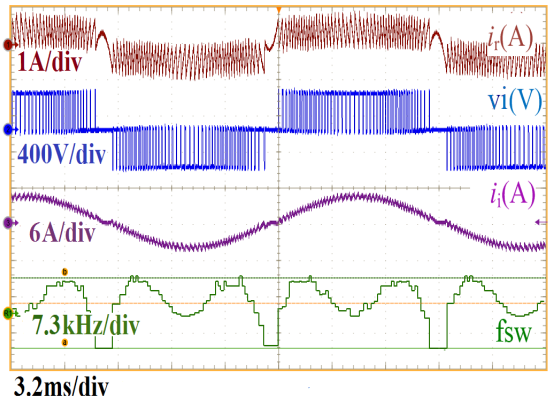
(c) Simulation results at V_{dc}=340 V



(d) Experimental results at V_{dc}=340 V



(e) Simulation results at P=0.75 kW, Q=0kVAr

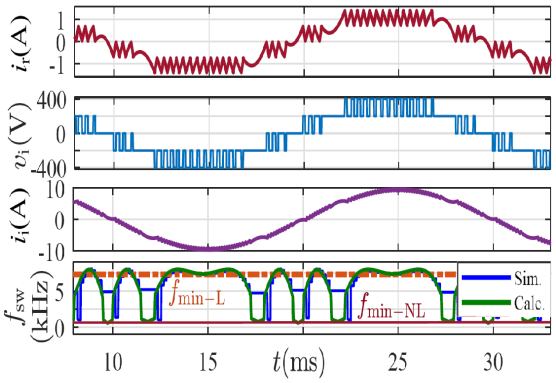


(f) Experimental results at P=0.75 kW,Q=0kVAr

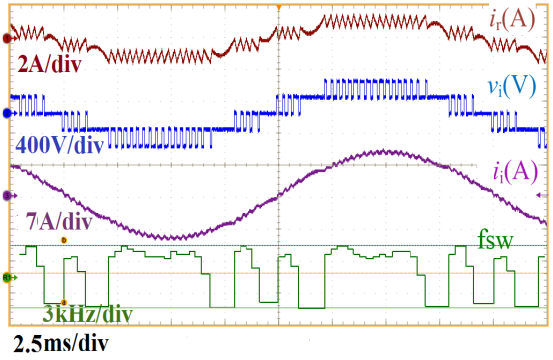
Figure 2.12: Simulation and experimental results for 3 level inverter at (a) base ratings listed in Table 2.1, (b)V_{dc}=340 V and (d)P=0.75 kW, Q=0kVAr

Table 2.2: Calculated, Simulated and Experimental Results for 3 level GTI

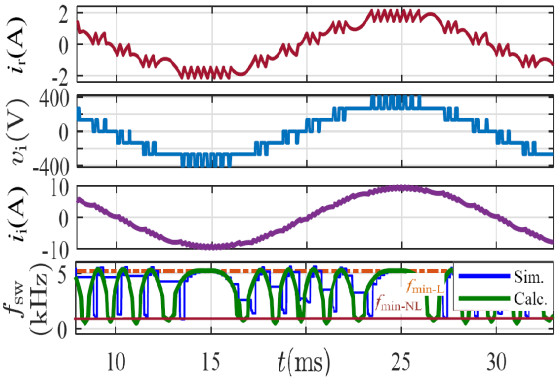
h	V_{dc}	f_{min}(kHz)				f_{max}(kHz)		
		f_{min-L} (2.12)	f_{min-NL} (2.23)	Sim.	Exp.	f_{max-NL} (2.22)	Sim.	Exp.
$0.2I_g$	340	1.82	0.84	1.49	1.05	6.91	7.0	6.85
	400	4.80	0.84	1.05	0.91	7.90	7.96	7.88
$0.1I_g$	340	3.63	1.19	1.68	1.61	13.8	13.8	14.4
	400	9.61	1.18	1.69	1.30	15.9	15.7	15.4
$0.05I_g$	340	7.27	1.66	2.15	1.7	27.7	27.4	27.8
	400	19.2	1.7	3.1	1.8	31.6	31.2	31.3



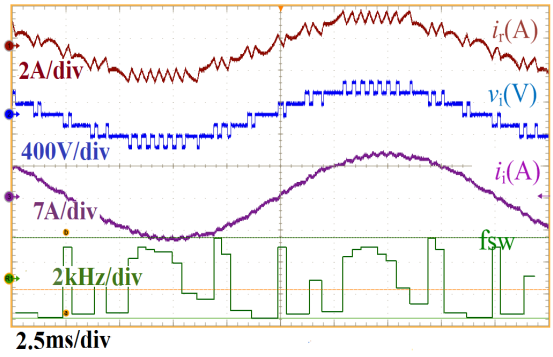
(a) Simulation results for 5 level inverter



(b) Experimental results for 5 level inverter



(c) Simulation results for 7 level inverter



(d) Experimental results for 7 level inverter

Figure 2.13: Results at rated condition for 5 level and 7 level inverters

h and DC voltage V_{dc} are listed in Table. 2.2 as f_{min}, f_{max}. The frequencies obtained by calculation, simulation and experimentation are enlisted as Calc., Sim. and Exp. respectively. The slight difference in switching frequencies obtained by experiment and by simulation specifically at smaller error bands is owing to the fixed sampling time. It is noticed that the minimum frequencies calculated by (2.12) assuming linear error current as in [Gautam and Gupta, 2014] are greater than those obtained by simulation and experiment specifically for higher values of V_{dc}. Since the minimum frequency is one of the key parameters for filter design, this can result in incorrect values of filter parameters causing problems such as resonance. When the non-linearity in error current is considered, the minimum frequency calculated by proposed equation (2.23) is comparable to those obtained by simulation and experimentation. The simulated and experimental results for f_{max} are observed to be in close agreement with the calculated values thus supporting the proposed equation(2.22).

In Fig. 2.13, the simulated and experimental results obtained for 5 and 7 level inverters at rated conditions mentioned in Table 2.1 are presented. From the ripple current profiles, it is noted that the current distortions occur at $2n-4$ instants in a fundamental cycle. For $n=5$ and $n=7$, $f_{\mathrm{sw}} \leq f_{\mathrm{min-L}}$ for a larger extent of time duration than for $n=3$. Nevertheless, $f_{\mathrm{min-NL}} \leq f_{\mathrm{min-L}}$ in all the cases which supports the theoretical claims in this work. Additionally, the experimental results are in good agreement with the simulation results.

The calculated values of f_{min} and f_{max} using the proposed and existing formulations are presented in Table 2.3 and are compared with the simulation and experimental results.The switching frequency obtained by experiment is slightly less than that in simulation owing to the fixed sampling time. For the base ratings in Table 2.1, the minimum frequency calculated as per [Gautam and Gupta, 2014] is $f_{\mathrm{min-L}}$=9.61 kHz. The values of f_{min} observed in simulation and experimentation is 1.623 kHz and 1.3 kHz respectively. The minimum frequency calculated based on the proposed formulation $f_{\mathrm{min-NL}}$=1.18 kHz is observed to be comparable with those obtained by simulation (1.62 kHz) and experiment (1.3 kHz). Similarly, for other operating conditions also, the values of minimum frequency calculated using the proposed formulation (2.23) is considerably less than that calculated using the existing equation (2.12). Moreover, the calculated values of f_{max} are comparable to those obtained from simulation and experimental results. For 5 and 7 level inverters, the calculated minimum frequencies using the proposed formulation are 0.96 kHz and 0.84 kHz respectively which are comparable with f_{min} obtained by simulation and experimentation. Furthermore, the values of calculated frequen-

cies using the proposed equations at base ratings and other operating conditions are comparable for the 3 level inverter. This suggests that for any MGTI, system design at rated power is sufficient.

Table 2.3: Comparison of Switching Frequency for Various Operating Conditions In Calculation, Simulation and Experimentation

Operating Condition	$f_{\min}$ Calculated $f_{\min-\mathrm{L}}$ (2.12)	$f_{\min}$ Calculated $f_{\min-\mathrm{NL}}$(2.23)	$f_{\min}$ Sim.	$f_{\min}$ Exp.	$f_{\max}$ Calc. (2.22)	$f_{\max}$ Sim.	$f_{\max}$ Exp.
Base rating	9.61	1.18	1.62	1.3	15.86	15.75	15.36
V_{dc} =340V	2.01	1.19	1.68	1.54	13.48	13.44	13.54
P =0.75kW	9.56	1.18	1.20	1.12	15.86	15.89	15.79
n =5	7.35	0.78	0.99	0.97	7.93	7.81	7.69
n =7	5.21	0.75	0.88	0.81	5.30	5.41	5.35

2.8 Conclusion

In this work, a generalized expression of switching frequency variation for a hysteresis current controlled MGTI is proposed. The requirement of proposed formulation for accurate frequency computation is emphasized by an example of second-order filter design. The derived expression is observed to yield a more accurate results compared to the existing switching frequency formulation. The proposed formulation is valid even at low switching frequencies since the non-linearity in error current is considered. The minimum and maximum frequency expressions for HC aid in filter sizing, switching device selection, loss analysis and current harmonic analysis. With the existing efficient and fast computational software, the effect of marginal increase in complexity is inconsequential. Also the computations are required to be carried out only once prior to system design. The simulated and experimental results are presented and are found to be in good agreement with the results calculated using the proposed switching frequency formulation.

Chapter 3

An AC Current Sensor-less Hysteresis Control for GTI

Contents

3.1 Introduction

As discussed in section 1.5.1, hysteresis control (HC) has advantages of simplicity, ruggedness and fast dynamic response [Komurcugil et al., 2017] over other common control strategies for grid tie inverters (GTIs). In HC, the inverter output current

is modulated by limiting the ripple current within a predefined hysteresis band (HB). Hence a high precision current sensor (CS) is required to sense changes as small as HB at varying switching frequency. These sensors contribute to overall cost and size and introduce measurement noises and delays. One solution to the aforementioned problem is to employ an AC current sensor-less hysteresis control (CSLHC).

The current emulation technique (CET) presented in [Su et al., 2019, Zhang et al., 2015] is most common method to eliminate current sensors in the available literature. It uses system parameters and switching states to emulate the required current. The method of CET can be modified to suit HC of GTIs in order to eliminate the AC current sensor and thereby implement CSLHC. However, in such a control, computations will be required at each sampling instant. This will lead to delays and cumulative errors. Moreover, the generation of hysteresis band and its comparison with ripple current is still required if CET is used to develop CSLHC.

An improved CSLHC can be implemented by calculating the switching instants from switching frequency formulation. On account of the above discussion, the major contributions in this objective are summarized as follows.

- A simple yet accurate expression for switching intervals is formulated considering the non-linearity in ripple current.
- The necessary changes considering the effect of dynamic variations and digital sampling are incorporated in the proposed formulation.
- A CSLHC for single-phase GTI is developed with the switching instants computed from the proposed equation.

3.2 Switching Intervals of Two-level GTI

Consider a single-phase two-level GTI with output voltage v_{i} and current i_{i}, connected to the grid with voltage v_{g}=$V_{\mathrm{g}}\sin(\omega t)$ via filter inductor L as shown in Fig. 3.1. Unity power factor operation along with a simple L filter is assumed. Nevertheless, the analysis can easily be modified for other cases. In conventional HC, the actual GTI output current (inductor current) i_{i} is compared to a reference current $i_{\mathrm{i}}^{*} = I_{\mathrm{i}}^{*}\sin(\omega t)$. Let the reference current i_{i}^{*} correspond to a reference voltage v_{i}^{*} is defined by (3.1), $V_{\mathrm{i}}^{*} = \sqrt{V_{\mathrm{g}}^{2} + (\omega L I_{L}^{*})^{2}}$ and $\theta = \tan^{-1}\left(\frac{\omega L I_{\mathrm{i}}^{*}}{V_{\mathrm{g}}}\right)$.

$$v_{\mathrm{i}}^{*} = V_{\mathrm{i}}^{*}\sin(\omega t + \theta) \tag{3.1}$$

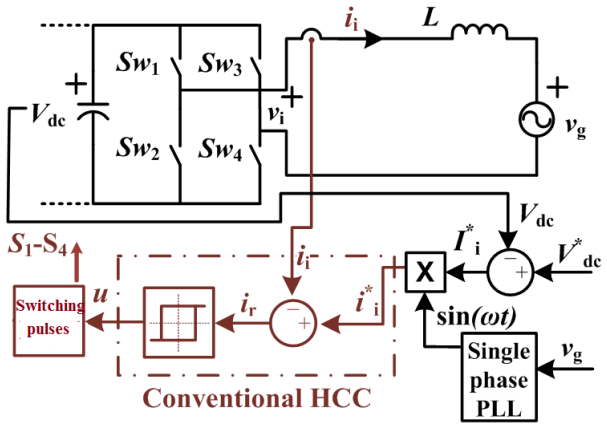
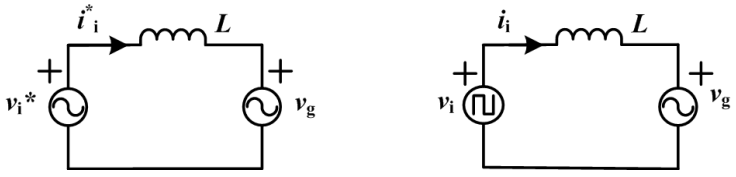


Figure 3.1: Single phase GTI employing conventional HC

If u represents the switching state, the actual GTI output voltage v_i can be expressed as in (3.2).

$$v_i = uV_{dc} \tag{3.2}$$

The equivalent circuits of the two-level single phase GTI with reference and actual voltages are shown in Fig.3.2. The difference between the reference and



(a)

Figure 3.2: Equivalent circuits with (a) reference and (b) actual inverter output

actual inverter output currents, $i^*_i - i_i$ is termed as ripple current i_r and is shown in Fig. 3.3. The switching pulses are generated such that i_r remains within the

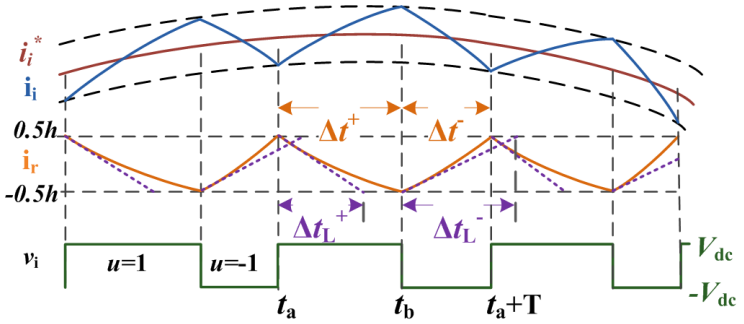


Figure 3.3: Reference and actual currents, ripple current and inverter voltage

predefined limits of, say $\pm 0.5h$. From the dynamic equations for i_{i}^{*} and i_{i} [Albanna and Hatziadoniu, 2010], the rate of change of i_{r}, is expressed as (3.3).

$$\frac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t} = \frac{v_{\mathrm{i}}^{*} - v_{\mathrm{i}}}{L} \tag{3.3}$$

Consider a switching interval t_{a} to $t_{\mathrm{a}} + T$, where T is the switching period as shown in Fig. 3.3. The ripple current is truly non-linear and is represented by $i_{\mathrm{r_{NL}}}$. It reaches the hysteresis limits $0.5h$ and $-0.5h$ at t_{a} and t_{b} respectively. Hence the switching state S is 1 and 0 respectively during the intervals $\Delta t^{+} = t_{\mathrm{b}} - t_{\mathrm{a}}$ and $\Delta t^{-} = (T + t_{\mathrm{a}}) - t_{\mathrm{b}}$. If a linear change in ripple current is assumed as in [Albanna and Hatziadoniu, 2010, Gupta, 2012, Kumar, 2018], the resulting ripple current is represented by $i_{\mathrm{r_L}}$. The change in $i_{\mathrm{r_L}}$ during $\Delta t_{\mathrm{L}}^{\pm}$ is obtained by linearising (3.3) as shown in (3.4). Here $\Delta i_{\mathrm{r}} = \mp h$.

$$\Delta i_{\mathrm{r}} = \frac{1}{L}\Delta t_{\mathrm{L}}^{\pm}(v_{\mathrm{i}}^{*} \mp V_{\mathrm{dc}}) \tag{3.4}$$

From Fig. 3.3, it is observed that if the existing equation is used to predict the switching instants, it would lead to incorrect switching at $\Delta t_{\mathrm{L}}^{\pm}$ instead of $\Delta t^{\pm}$. This incorrect switching cause the hysteresis band to vary due to which the actual output current i_{i} does not precisely follow the reference i_{i}^{*}. This introduces steady state errors such as DC shift and distortions in the actual output current i_{i}. Therefore in this research the non-linear nature of ripple current is considered.

3.2.1 Effect of Non-linearity in ripple Current

To consider the non-linear nature of ripple current, we derive Δi_{r} by integrating (3.3) over the switching interval. During Δt^{+}, i.e. t_{a} to t_{b}, the change in ripple current Δi_{r} is

$$\begin{aligned} -h &= \int_{t_{\mathrm{a}}}^{t_{\mathrm{b}}} \frac{1}{L}(v_{\mathrm{i}}^{*} - V_{\mathrm{dc}})\mathrm{d}t \\ &= \frac{1}{L}\left(-\frac{V_{\mathrm{i}}^{*}}{\omega}\left(\cos(\omega t_{\mathrm{b}} + \theta) - \cos(\omega t_{\mathrm{a}} + \theta)\right) - \Delta t^{+} V_{\mathrm{dc}}\right). \end{aligned} \tag{3.5}$$

Using trigonometric identities, (3.5) is simplified to (3.6).

$$-h = \frac{1}{L}\left(\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\frac{1 - \cos(\omega\Delta t^{+})}{\omega^{2}} + v_{\mathrm{i}}^{*}\frac{\sin(\omega\Delta t^{+})}{\omega} - \Delta t^{+} V_{\mathrm{dc}}\right)\Bigg|_{t_{\mathrm{a}}} \tag{3.6}$$

Similarly Δi_{r} during the interval Δt^{-} is obtained and the equations are generalized for $\Delta t^{\pm}$ to (3.7) evaluated at the respective switching instant (t_{a} or t_{b}).

$$\Delta i_{\mathrm{r}} = \frac{1}{L}\left(\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\frac{1-\cos(\omega\Delta t^{\pm})}{\omega^{2}} + v_{\mathrm{i}}^{*}\frac{\sin(\omega\Delta t^{\pm})}{\omega} \mp V_{\mathrm{dc}}\Delta t^{\pm}\right) \tag{3.7}$$

To solve for $\Delta t^{\pm}$, (3.7) is simplified using Maclaurin series expansions for trigonometric functions. For $\Delta t^{\pm}$ <1ms, the series is truncated to (3.8) with sufficient accuracy by second order approximation, also called small-angle approximation.

$$\cos(\omega\Delta t^{\pm}) + j\sin(\omega\Delta t^{\pm}) = 1 + j\omega\Delta t^{\pm} - 0.5(\omega\Delta t^{\pm})^{2} \tag{3.8}$$

Substituting values of sine and cosine functions from (3.8) in (3.7), Δi_{r} during $\Delta t^{\pm}$ can be simplified to (3.9).

$$\mp h = \frac{1}{L}\left(\Delta t^{\pm}(v_{\mathrm{i}}^{*} \mp V_{\mathrm{dc}}) + \frac{(\Delta t^{\pm})^{2}}{2}\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\right) \tag{3.9}$$

For the two possible switching states S =0 and 1, (3.4) and (3.9) are generalized as (3.10) and (3.11). Here $\Delta V = v_{\mathrm{i}}^{*} - V_{\mathrm{dc}}u$, $\Delta i_{\mathrm{r}} = -uh$, $\Delta t_{\mathrm{L}} \Rightarrow \Delta t_{\mathrm{L}}^{u}$ and $\Delta t \Rightarrow \Delta t^{u}$.

$$\Delta i_{\mathrm{r}} = \frac{1}{L}\Delta t_{\mathrm{L}}\Delta V \tag{3.10}$$

$$\Delta i_{\mathrm{r}} = \frac{1}{L}\left(\Delta t\Delta V + \frac{\Delta t^{2}}{2}\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\right) \tag{3.11}$$

It is observed that in (3.11) an additional second order term is incorporated to account for the non-linearity in ripple current. But, this converts the linear polynomial equation with single indeterminate in (3.10) to a quadratic polynomial in (3.11) thereby increasing the complexity of solution. In order to simplify (3.11), Δt^{2} is approximated to (3.12) by assuming $(\Delta t_{\mathrm{L}} - \Delta t)^{2} \approx 0$.

$$\Delta t^{2} = ((\Delta t - \Delta t_{\mathrm{L}}) + \Delta t_{\mathrm{L}})^{2} \approx -\Delta t_{\mathrm{L}}^{2} + 2\Delta t_{\mathrm{L}}\Delta t \tag{3.12}$$

Substituting (3.12) in (3.11) and equating with (3.10)

$$\begin{aligned} \Delta t_{\mathrm{L}}\Delta V &= \Delta t\Delta V + \frac{1}{2}\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\left(-\Delta t_{\mathrm{L}}^{2} + 2\Delta t\Delta t_{\mathrm{L}}\right). \\ \Longrightarrow \Delta t\left(1 + \frac{\Delta t_{\mathrm{L}}}{\Delta V}\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\right) &= \Delta t_{\mathrm{L}}\left(1 + \frac{\Delta t_{\mathrm{L}}}{2\Delta V}\frac{\mathrm{d}v_{\mathrm{i}}^{*}}{\mathrm{d}t}\right) \end{aligned} \tag{3.13}$$

Rearranging and simplifying (3.13), Δt is obtained as a function of $\frac{\mathrm{d}v_\mathrm{i}^*}{\mathrm{d}t}$, ΔV and Δt_L as shown in (3.14).

$$\Delta t = \Delta t_\mathrm{L}\left(1 - \frac{\frac{\Delta t_\mathrm{L}}{2}\frac{\mathrm{d}v_\mathrm{i}^*}{\mathrm{d}t}}{\Delta V + \Delta t_\mathrm{L}\frac{\mathrm{d}v_\mathrm{i}^*}{\mathrm{d}t}}\right), \tag{3.14}$$

$$\text{where } \Delta t_\mathrm{L} = \frac{\Delta i_\mathrm{r} L}{\Delta V} \quad \text{(from (3.10))}. \tag{3.15}$$

The additional terms in (3.14) account for the non-linear change in i_r and thereby accurately calculate the switching intervals.

Now, if the previous switching instant is t_sw^o, the next switching instant can be computed using (3.14) as $t_\mathrm{sw} = t_\mathrm{sw}^o + \Delta t$.

3.2.2 Effect of Dynamic Variations

Sudden variations in operating conditions such as DC input or grid voltage cause the reference current i_i^* to change, say from i_io^* to i_in^*. This effectively changes the ripple current i_r. If the effect of dynamics is not considered, Δt will be calculated from (3.14) to account only for the change in ripple current $\Delta i_\mathrm{r} = -uh$, i.e. the hysteresis band $\mp h$. But due to dynamic variation in i_i^*, the required change in i_i varies as shown in Fig. 3.4a. Therefore an additional change in i_r is required. If this additional change is not considered, the actual current i_i would follow the reference current i_io^* instead of i_in^*, resulting in a steady state error. To avoid this, when a change in i_i^* occurs, the required additional change in ripple current Δi_r is calculated as $\Delta i_\mathrm{i}^* = i_\mathrm{in}^* - i_\mathrm{io}^*$.

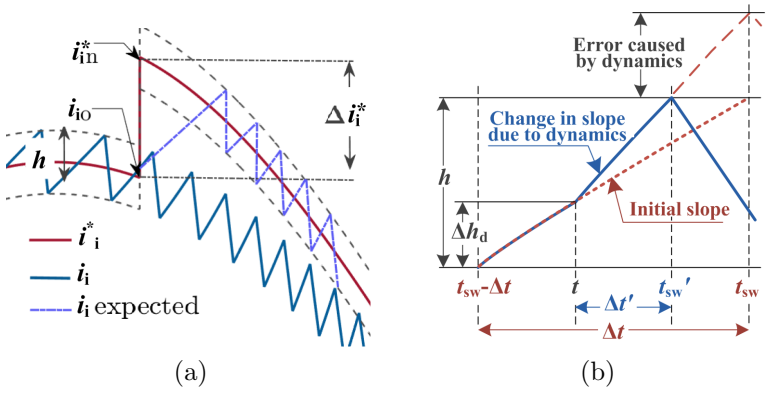


Figure 3.4: Effect of dynamic variations on switching period computation

Furthermore, as per (3.3), changes in operating conditions also cause the slope of ripple current $\frac{\mathrm{d}e}{\mathrm{d}t}$ to change as shown in Fig. 3.4b. Let t_sw be the previously

calculated switching instant and Δt be the switching interval. Due to the change in operating condition at t, the slope of ripple current i_{r} changes. Now i_{r} reaches the upper limit at t'_{sw} instead of t_{sw}. In order to compute the new switching instant $t'_{\mathrm{sw}}(= t + \Delta t')$, $\Delta t'$ is calculated from (3.14) with $\Delta i_{\mathrm{r}} = -uh - \Delta h_{\mathrm{d}}$. Here Δh_{d} is the change in ripple current from the previous switching instant to the instant at which the dynamic change occured, i.e $t_{\mathrm{sw}} - \Delta t$ to t. Based on (3.11), Δh_{d} can be calculated from (3.16), where ΔV_{o} and $\frac{\mathrm{d}v^*_{\mathrm{io}}}{\mathrm{d}t}$ corresponds to the values of ΔV and $\frac{\mathrm{d}v^*_{\mathrm{i}}}{\mathrm{d}t}$ at one sample prior to the dynamic change.

$$\Delta h_{\mathrm{d}} = \Delta i^*_{\mathrm{i}} + \frac{1}{L}\left(\left(t - (t_{\mathrm{sw}} - \Delta t)\right) \Delta V_{\mathrm{o}} + \frac{\left(t - (t_{\mathrm{sw}} - \Delta t)\right)^2}{2} \frac{\mathrm{d}v^*_{\mathrm{io}}}{\mathrm{d}t} \right) \tag{3.16}$$

3.2.3 Effect of Sampling in Digital HC

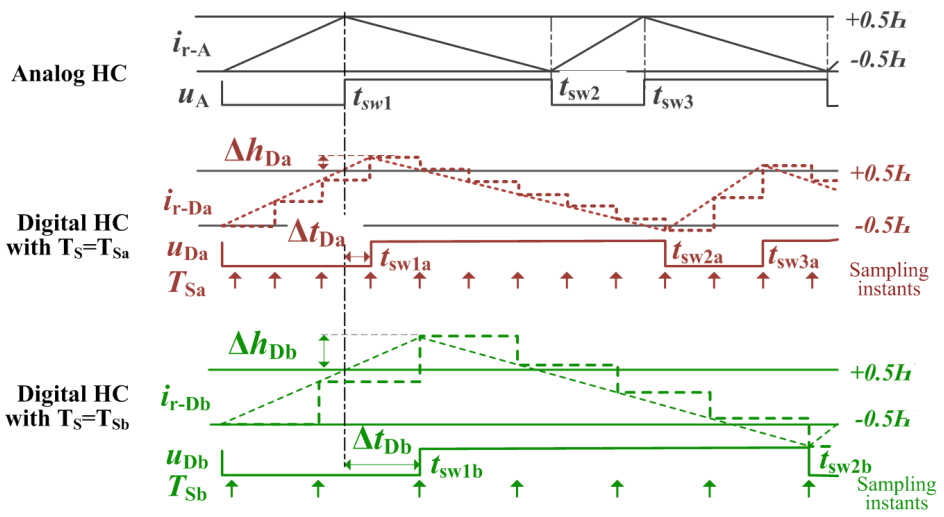


Figure 3.5: Effect of sampling in HC

The change in switching instants in HC owing to the constraints imposed by fixed sampling time in digital controllers is analysed to determine the exact switching instant. First, the effect of different sampling time in digital HC is compared along with the conventional analog HC. Consider the ripple current $i_{\mathrm{r-A}}$ with switching state u_{A} (subscript A denotes analog) shown in Fig. 3.5(a). The ripple current remains exactly within the defined hysteresis limits $\pm 0.5H$. However, in digital HC, the switching instants are required to be integer multiples of the sampling period T_{Sa}. Hence the ripple current $i_{\mathrm{r-Da}}$ in Fig. 3.5(b) does not remain within the defined hysteresis limits causing the band to widen by Δh_{da}. The switching instant also shifts from t_{sw1} to t_{sw1a} with an increment of Δt_{Da}. It

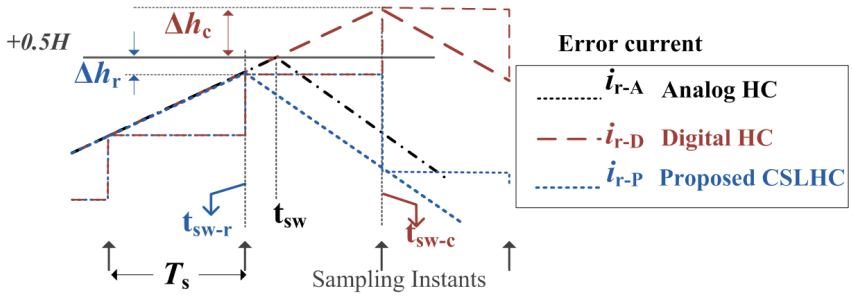


Figure 3.6: Comparison of analog HC, digital HC and proposed CSLHC

is observed that Δh_{Da} and Δt_{Da} are not constants. Furthermore as the sampling period increases from $T_{\mathrm{S_a}}$ to $T_{\mathrm{S_b}}$, the change in hysteresis band also increases from Δh_{Da} to Δh_{Db} thereby decreasing the number of switching instants in a given duration. This implies that for the same predefined hysteresis limit, the switching frequency decreases as the sampling time increases.

Based on the observations made, the switching instant formulation is modified to account for the effect of sampling. Consider the ripple currents in conventional analog HC and digital HC to be $i_{\mathrm{r-A}}$ and $i_{\mathrm{r-D}}$ respectively as shown in Fig. 3.6. The ripple current $i_{\mathrm{r-A}}$ remains within the hysteresis limits as u switches exactly at t_{sw} when $i_{\mathrm{r-A}} = \pm 0.5H$. For conventional digital HC, since switching occurs only at the succeeding sampling instant, $i_{\mathrm{r-D}}$ increases beyond hysteresis limits. Let $t_{\mathrm{sw-c}}$ be the sampling instant immediately succeeding t_{sw} and the band error Δh_{c} be the increase in hysteresis limit during $(t_{\mathrm{sw-c}} - t_{\mathrm{sw}})$. Here the mathematical operation $\lceil x \rceil$ signifies *ceil* that maps x to the next larger integer, $t_{\mathrm{sw-c}}$ is

$$t_{\mathrm{sw-c}} = nT_{\mathrm{s}}, \quad n = \left\lceil \frac{t_{\mathrm{sw}}}{T_{\mathrm{s}}} \right\rceil . \tag{3.17}$$

$$\Delta h_{\mathrm{c}} = (t_{\mathrm{sw-c}} - t_{\mathrm{sw}}) \frac{\Delta v}{L}. \tag{3.18}$$

From Fig. 3.6, we can critically observe that $i_{\mathrm{r-D}}$ is closer to $+0.5H$ at the preceding sampling instant $t_{\mathrm{sw-r}}$ than $t_{\mathrm{sw-c}}$. However $i_{\mathrm{r-D}}$ does not meet the condition for hysteresis switching $(i_{\mathrm{r-D}} \geq +0.5H)$ at $t_{\mathrm{sw-r}}$. Hence the switching would occur only at $t_{\mathrm{sw-c}}$. This results in an increased band error. As a solution, the nearest switching instant is chosen in this work thereby reducing the band error and more closely replicating the analog HC.

The sampling instant nearest to t_{sw} be $t_{\mathrm{sw-r}}$ and can be expressed by (3.19). Here, the mathematical operation $\lfloor x \rceil$ represents *round* to map x to the nearest

integer.

$$t_{\mathrm{sw-r}} = mT_{\mathrm{s}}, \quad m = \left\lfloor \frac{t_{\mathrm{sw}}}{T_{\mathrm{s}}} \right\rceil \tag{3.19}$$

If the switching occurs at $t_{\mathrm{sw-r}}$, the change in error current during the interval $(t_{\mathrm{sw-r}} - t_{\mathrm{sw}})$ i.e. the band error is Δh_{r}. Since $t_{\mathrm{sw-r}}$ is the nearest sampling point, $\Delta h_{\mathrm{r}} \leq \Delta h_{\mathrm{c}}$ always. Switching at $t_{\mathrm{sw-r}}$ can thus reduce the band error. Therefore in the proposed CSLHC, the switching state u is changed at $t_{\mathrm{sw-r}}$ instead of $t_{\mathrm{sw-c}}$. The change in error current during the switching interval $\Delta i_{\mathrm{r-P}}$ (subscript P denotes the proposed CSLHC) is modified as $-uH + \Delta h_{\mathrm{r}}$, where

$$\Delta h_{\mathrm{r}} = (t_{\mathrm{sw-r}} - t_{\mathrm{sw}}) \frac{\Delta v}{L}. \tag{3.20}$$

A CSLHC is now developed by calculating the switching instants which considers the non-linearity in error current, dynamic changes and reduces the effects of fixed sampling.

3.3 Proposed AC Current sensor-less HC

Based on the switching interval formulation derived in (3.14) is used to develop a two-level CSLHC for single phase GTI as shown in Fig. 3.7. The AC current sensor used in conventional HC for the inverter output current i_{i} is eliminated. No additional voltage or current sensor is required for the proposed sensor-less control. The switching instants at which the switching state u is varied are computed based

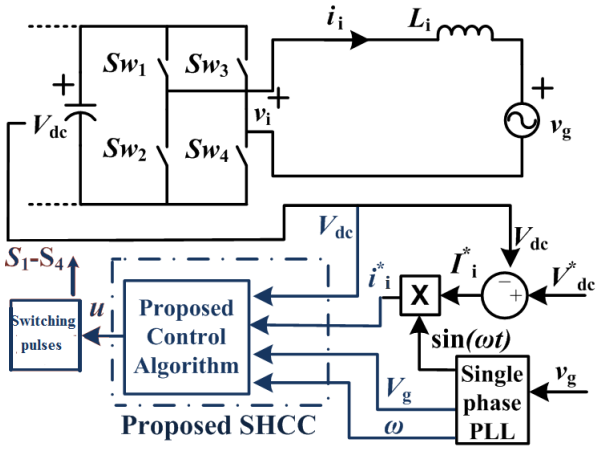


Figure 3.7: Single phase two-level GTI with the proposed CSLHC

on the intervals Δt. The effect of dynamics is considered using (3.16) with the proposed formulation in (3.14).

The algorithm of the proposed CSLHC is presented as a flowchart in Fig. 3.8 and explained as follows. At first, the constants such as hysteresis band h and filter inductance L are initialized. A binary variable $flag$ is reset to 0 to indicate the first iteration. The time elapsed from the start, t is initialized to 0.

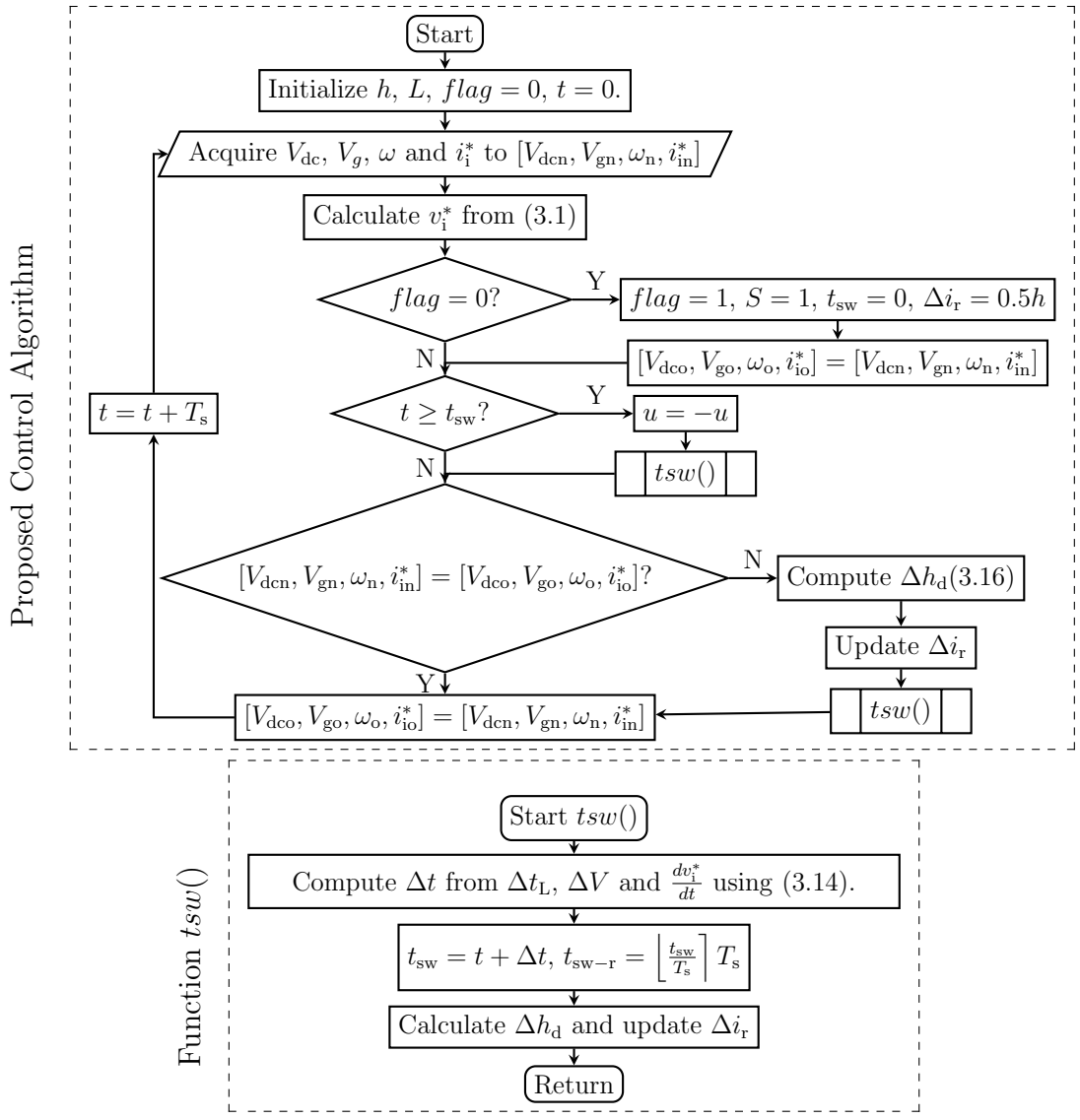


Figure 3.8: Flowchart of the proposed AC Current sensor-less HC

The iteration starts by acquiring DC voltage $V_{\rm dc}$ from DC voltage sensor, grid parameters $V_{\rm g}$ and ω from phase-locked loop (PLL) and reference current $i_{\rm i}^*$ from the preceding part of control. The values are stored to the array $[V_{\rm dcn}, V_{\rm gn}, \omega_{\rm n}, i_{\rm in}^*]$. The reference inverter output voltage $v_{\rm i}^*$ is calculated using (3.1). For the first iteration, i.e. if $flag = 0$, then $flag$ and switching state u are set to 1 and the switching instant $t_{\rm sw}$ is assigned 0. The initial ripple current $i_{\rm r}$ is assumed

to be 0. Hence the required change Δi_{r} is half the hysteresis band i.e. $0.5H$. The variables V_{dco}, V_{go}, ω_o and i^*_{io} represent the values of V_{dc}, V_{g}, ω and i^*_{i} at the previous sampling instant. In the first iteration, the array with previous values $[V_{\mathrm{dco}}, V_{\mathrm{go}}, \omega_{\mathrm{o}}, i^*_{\mathrm{io}}]$ are initialized to the acquired values $[V_{\mathrm{dcn}}, V_{\mathrm{gn}}, \omega_{\mathrm{n}}, i^*_{\mathrm{in}}]$. The occurrence of the calculated switching instant is indicated by $t \geq t_{\mathrm{sw}}$ at which the switching state u is toggled.

In the first iteration, $t = 0$ and $t_{\mathrm{sw}} = 0$. Thus the condition $t \geq t_{\mathrm{sw}}$ is satisfied and the switching state u is toggled to -1 using $u = -u$. The next switching instant t_{sw} is determined using the function $tsw()$ shown in Fig. 3.8. In the function $tsw()$, the switching interval Δt is calculated using (3.14) and is added to the time elapsed from the start t to obtain the switching instant t_{sw}. The condition for dynamics is now checked by comparing the present values of $[V_{\mathrm{dc}}, V_{\mathrm{g}}, \omega, i^*_{\mathrm{i}}]$ to those in the previous sample, i.e. $[V_{\mathrm{dco}}, V_{\mathrm{go}}, \omega_{\mathrm{o}}, i^*_{\mathrm{io}}]$. If a change in operating condition is observed, Δi_{r} is updated to $-uh - \Delta h_{\mathrm{d}}$ where Δh_{d} is obtained from (3.16). The function $tsw()$ is used to recalculate the switching instant. Before proceeding to the next iteration, the array $[V_{\mathrm{dco}}, V_{\mathrm{go}}, \omega_{\mathrm{o}}, i^*_{\mathrm{Lo}}]$ and t are updated. The next iteration starts with acquiring new values of i^*_{i}, V_{g}, ω and V_{dc} to the array $[i^*_{\mathrm{Ln}}, V_{\mathrm{gn}}, \omega_{\mathrm{n}}, V_{\mathrm{dcn}}]$. In the following iterations, the condition for binary variable $flag$ returns false. The further execution of the algorithm remains same as that explained for the first iteration.

3.4 Results and Discussion

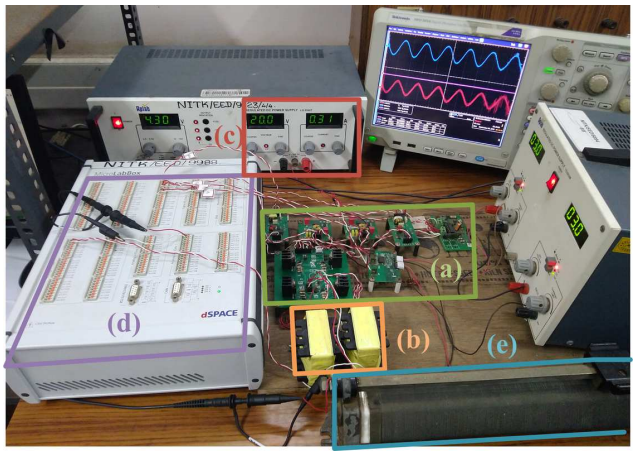


Figure 3.9: Experimental setup with (a) inverter with driver and voltage sensor circuit, (b) L filter, (c) DC source, (d) dSPACE Microlab box and (e) local load

The simulation and experimental results are presented to verify the perfor-

mance of the proposed CSLHC under various real-time operating conditions. The system parameters used for simulation and experiment are listed in Table 5.3. A single-phase H-bridge inverter with the proposed control shown in Fig. 3.7 is implemented in MATLAB/Simulink platform to obtain the simulation results. To justify the need to consider the effects of non-linear ripple current, digital sampling and dynamic variations, the results of the proposed formulation (3.14) is compared with those obtained assuming linear ripple current and neglecting sampling and dynamics. Further, the proposed CSLHC is compared with the conventional HC and CSLHC with CET based on the average computational time, DC shift and total harmonic distortion (THD). Experimental results are presented using a prototype of single-phase H-bridge inverter to validate the simulation results. The proposed control is implemented in dSPACE Microlab Box 1202 and the switching pulses are obtained via digital channels. The input voltage $V_{\rm dc}$ and load voltage $v_{\rm g}$ are sensed using voltage sensors via ADC channels. As mentioned earlier, unity power factor operation is considered here with an L filter. The filter design is done based on the hysteresis band (same as ripple current) and the minimum switching frequency calculated using the formulation presented in Chapter 2.

Table 3.1: System Specification for simulation and experimental results

Parameter	Value
Rated real power $P_{\rm rated}$	350 W
DC link voltage $V_{\rm dc}$	200 V
Grid voltage $v_{\rm g}$(rms),$f_{\rm g}$	110 V, 50 Hz
Rated peak grid current $I_{\rm rated}$	4.5 A
Predefined HB h (5%$I_{\rm rated}$)	0.225 A
Filter inductor L	30 mH

3.4.1 Non-linearity of Error Current

The simulation results considering linear and non-linear ripple currents by implementing (3.15) and (3.14) respectively are compared in Fig. 3.10(a) and Fig. 3.10(b). The calculated switching frequencies in both cases are close to each other. When the existing formulation (3.15) (assuming linear ripple current) is used, it is observed that the ripple current does not remain within the predefined bands especially during low switching frequencies. Therefore $i_{\rm i}$ does not precisely follow the reference $i_{\rm i}^*$. When the switching intervals are calculated considering non-linear ripple current using the proposed formulation (3.14), the switching instants are

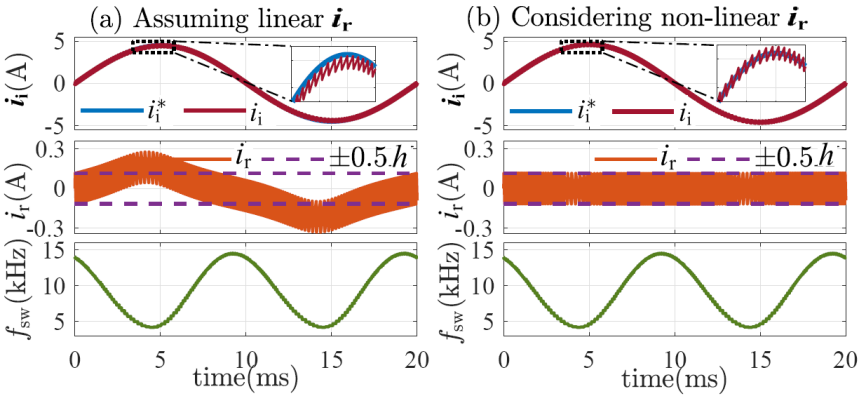
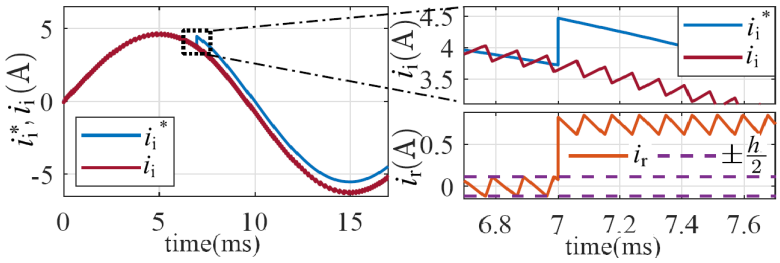


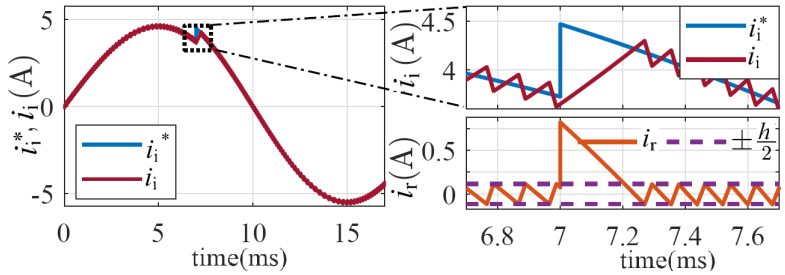
Figure 3.10: Results of i_i, i_r and $f_{sw}$with and without considering the non-linearity in ripple current

precisely computed. Hence i_r is observed to remain within the defined limits and i_i exactly follows i_i^*.

3.4.2 Effect of Dynamic Changes



(a) When the effect of dynamics is not considered

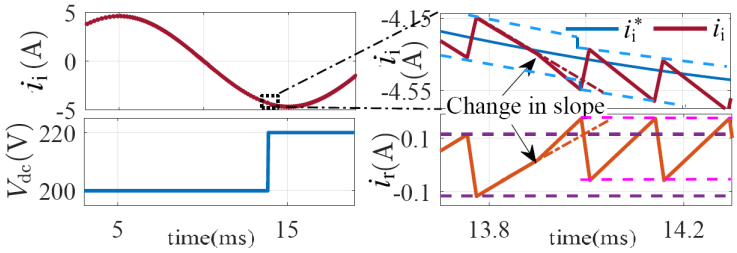


(b) when the effect of dynamics is compensated in proposed CSLHC

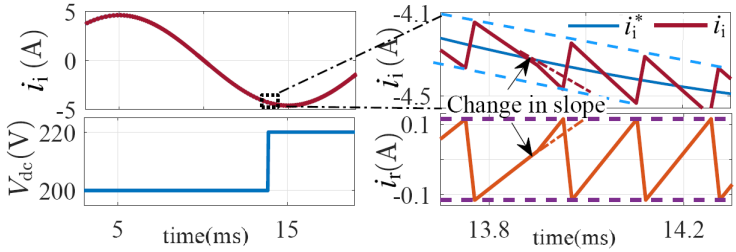
Figure 3.11: Simulation results showing change in reference current i_i^* with operating conditions specified in Table 5.3

In Fig. 3.11, a change in the reference current i_i^* from the rated value to $1.2I_{\text{rated}}$ (3.18 A to 3.82 A rms) is observed at $t = 7$ ms. Due to the sudden change in i_i^*, the ripple increases beyond the upper limit $+\frac{h}{2}$. As shown in Fig. 3.11a, if the effect of change in i_i^* is not considered, the change in ripple current Δi_r remains

to be $-uh$. This reflects as a DC shift in both i_{r} and i_{i}. In order to compensate for the increase in i_{i}^{*} and retain i_{r} within $\pm\frac{h}{2}$, Δi_{r} is recalculated as $-uh + \Delta h_{\mathrm{d}}$ in the proposed CSLHC as shown in Fig. 3.11b.



(a) Effect of dynamics is not compensated

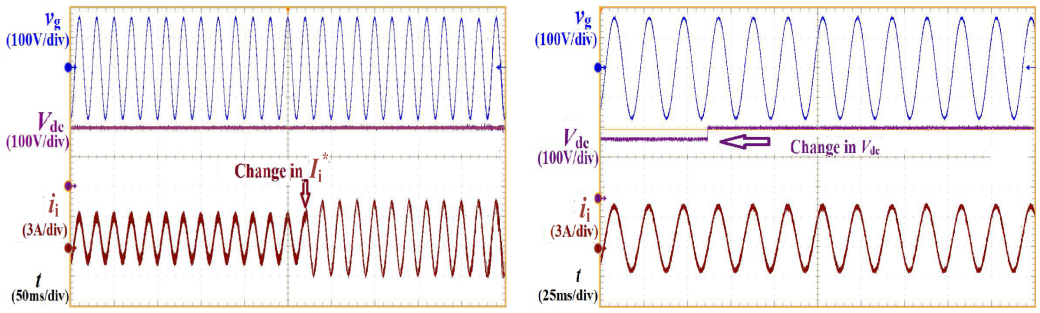


(b) Effect of dynamics is compensated in proposed CSLHC

Figure 3.12: Simulation results for change in DC input voltage V_{dc}

The effect of sudden changes in operating condition is illustrated with an example of DC voltage variation. Though in GTI applications, V_{dc} is maintained constant, a change in power balance cause V_{dc} to change. To validate the proposed CSLHC under such conditions, a step change in V_{dc} is considered from 200 V to 220 V at $t = 13.9$ ms as shown in Fig. 3.12. The slope of i_{r} changes as per (3.3). As in Fig 3.12b, if the effect of dynamics is not considered, the succeeding switching instant remains same as that calculated prior to dynamics. The ripple current increases beyond the upper hysteresis band resulting in a steady state error due to the DC shift in i_{i} and i_{r}. Though it may seem insignificant, the cumulative effect of subsequent dynamics can result in a grid current with large unwanted DC component. In the proposed HC, the effect of change in slope of i_{r} is considered by recomputing the change in ripple Δi_{r} at the point of dynamics as $-uh - \Delta h_{\mathrm{d}}$ as shown in Fig 3.12b. Hence i_{i} and i_{r} remain within predefined limits.

The effect of dynamics are verified in experimental results. In Fig. 3.13a, the effect of sudden change in reference current i_{i}^{*} is analysed. The reference current magnitude I_{L}^{*} is increased from I_{rated} to 1.2 I_{rated}. Since the additional change in ripple current Δi_{r} is considered in the proposed control, the actual inverter output current i_{i} precisely follows i_{i}^{*} without any steady state error. In Fig. 3.13b, the effect of change in V_{dc} from its rated value of 200 V to 220 V is demonstrated.

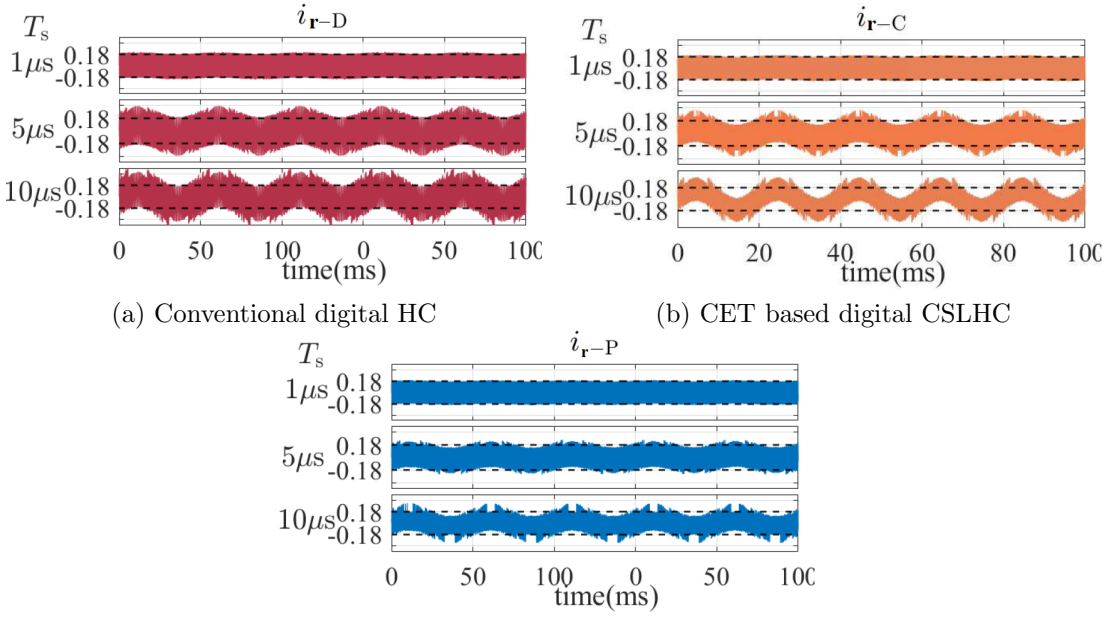


(a) change in magnitude of i_i (b) change in V_{dc}

Figure 3.13: Experimental results during dynamic changes in i_i and V_{dc}

Since the change in slope of i_r is taken into account in the proposed control, the change in V_{dc} does not cause a steady state error in the inverter output current i_i. The experimental results prove the feasibility of the proposed control due to satisfactory dynamic and steady state performance.

3.4.3 Effect of Digital Sampling



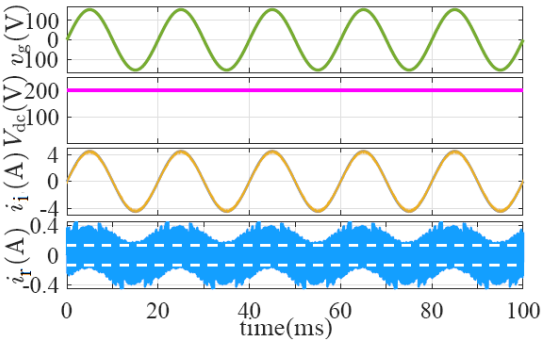
(a) Conventional digital HC (b) CET based digital CSLHC

(c) Proposed digital CSLHC

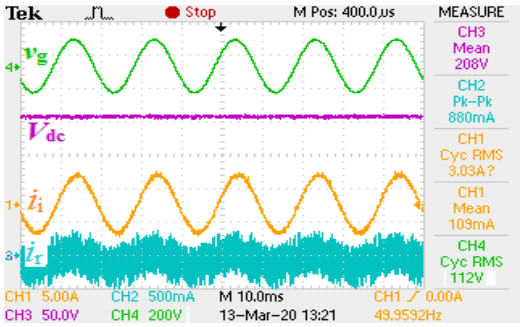
Figure 3.14: Simulation results with error current for digital HC, CET based CSLHC and proposed CSLHC, i_{r-D}, i_{r-C} and i_{r-P} for different sampling time

To analyse the effect of sampling time on digital HC, CET based CSLHC and proposed CSLHC, simulations were performed at different sampling times

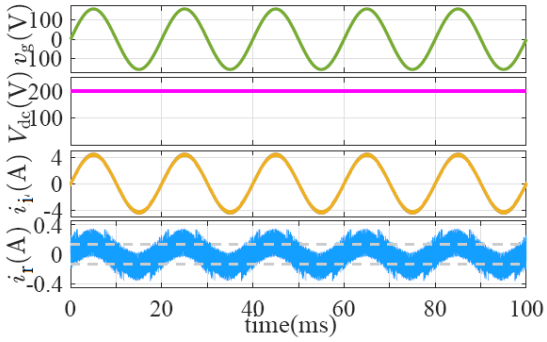
T_s =[1μs, 5μs, 10μs] and the error currents are presented in Fig. 3.14(a), (b) and (c) as i_{r-D}, i_{r-C} and i_{r-P} respectively. Here the predefined hysteresis limits are $\pm 0.5h = \pm 0.18$. The error currents of all the three controls are observed to remain closely within the hysteresis limits and have negligible band error when $T_s = 1\mu s$. However, as the sampling time increases to $T_s = 10\mu s$, we observe that the error currents of digital HC and CET based CSLHC do not remain within ± 0.18. However for the proposed CSLHC, i_{r-P} remains closer to the hysteresis limits. Thus the band error is less compared to the two other controls. Hence, the effect of sampling is considerably reduced in the proposed CSLHC.



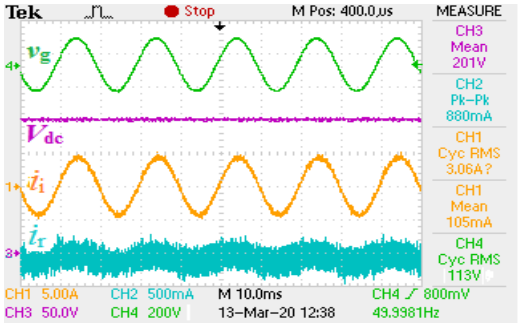
(a) Simulation Results of digital HC



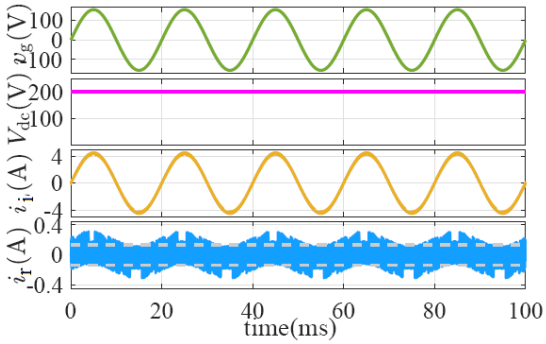
(b) Experimental Results of Digital HC



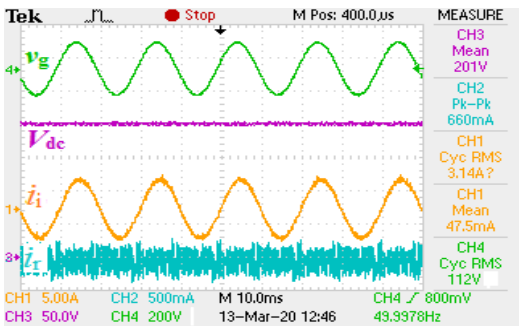
(c) Simulation Results of CET based CSLHC



(d) Experimental Results of CET based CSLHC



(e) Simulation Results of proposed CSLHC



(f) Experimental Results of Proposed CSLHC

Figure 3.15: Simulation and experimental results showing grid voltage, DC voltage, grid current and error current for conventional digital HC, CET based CSLHC and proposed CSLHC with $T_s = 10\mu s$

The simulation and experimental results showing the grid voltage, DC input voltage, grid current and error current for digital HC, CET based CSLHC and proposed CSLHC are presented in Fig. 3.15 for a sampling time of 10μs. The simulation and experimental results are observed to be in close agreement with each other. Furthermore, from Fig. 3.15, the simulation and experimental results of the proposed CSLHC is found to have reduced band error of i_{r} and hence is more identical to analog HCC thereby validating the theoretical claims and the simulations.

3.4.4 Comparison of Proposed CSLHC with Conventional HC and CET based CSLHC

Table 3.2: Comparison of Proposed Control with Prior Art

Control	Requisites		f_{avg}	t_{comp}	DC shift	THD
	CS	HB	(kHz)	(ns)	(mA)	(%)
Conventional HC	Yes	Yes	9.6	54	0.8	2.81
CET based CSLHC	No	Yes	9.5	240	146	2.84
Proposed CSLHC (Simulation)	No	No	9.65	115	2.1	2.80
Proposed CSLHC (Experiment)			9.7		2.7	3.90

The sensor-less control for conventional fixed band HC is not available in the existing literature; but CET in [Su et al., 2019, Zhang et al., 2015] can be adopted for any current sensor-less control, including CSLHC. Hence for the purpose of comparison, conventional HC and CSLHC with CET are implemented in simulation. On the basis of the results shown in Table 3.2, the proposed CSLHC is compared with the two existing controls. The average switching frequencies, f_{avg} in all the three cases are observed to be comparable and approximately 9.6 kHz. The requisites CS and HB in Table 3.2 represent the need for current sensor and generation of predefined HB followed by its comparison with ripple current respectively. Though the CS is eliminated in the CET based CSLHC, the generation of predefined HB and its comparison with ripple current for every sample is still required. On the other hand, the proposed sensor-less control eliminates the need for CS, emulation of current and its comparison with HB. Due to this, the average computational time t_{comp} of the proposed CSLHC is much less compared to CSLHC with CET. Additionally, the proposed control achieves grid current of better power quality in terms of reduced DC shift and THD compared to the CET based CSLHC.

3.5 Conclusion

A novel AC current sensor-less HC of a single-phase GTI using switching instant calculation is proposed and verified. The switching instants of the GTI are computed by time domain analysis. Since the existing formulations can give rise to dynamic and steady state errors, a more accurate estimation is obtained by considering the effects of non-linear ripple current and dynamic changes. Compared to the commonly used CET, the proposed control reduces the average computational time in a switching cycle. Also the generation and comparison of hysteresis limit is eliminated. With the existing signal processors having fast computational power, the proposed CSLHC can be efficiently implemented for HC of GTIs to improve system reliability and reduce cost by eliminating the inverter output AC current sensor.

Chapter 4

Hysteresis Control of Single Stage PCI using ZSI

Contents

4.1 Introduction

A single stage system with the possibility of independent control can improve the efficiency and solve the problem of shoot-through and dead bands. The Z-source inverter (ZSI) proposed in [Peng, 2003] provides a unique feature of boosting the input voltage by utilizing the shoot-through condition and thereby enabling independent control of input and output side in a single stage interface. The Z-source network is expected to be symmetric with two pairs of identical capacitors and

inductors. The capacitors and inductors of the network are capable of storing energy so as to provide the required boost in voltage. Such a network can thereby replace the DC-DC conversion stage for a more efficient single stage power converter interface (PCI) for a PV-grid interface. It also avoids harmonics caused by dead zones in voltage and current source inverters which is clearly depicted by [Huang et al., 2006] and [Gajanayake et al., 2007].

The control of such a single stage system is of prime importance. In this chapter, hysteresis control (HC) for the ZSI using is explored. A simple novel control technique to determine shoot-through states in a unipolar HC of single-phase ZSI acting as PCI for PV-grid integration is developed and presented. The proposed closed loop control is analogous to that for two stage PCI and does not require the knowledge of the system parameters or the previous switching states. The maximum constant boost ratio that can be obtained without causing ripples in Z-source network is derived as a function of modulation index.

4.2 System Description

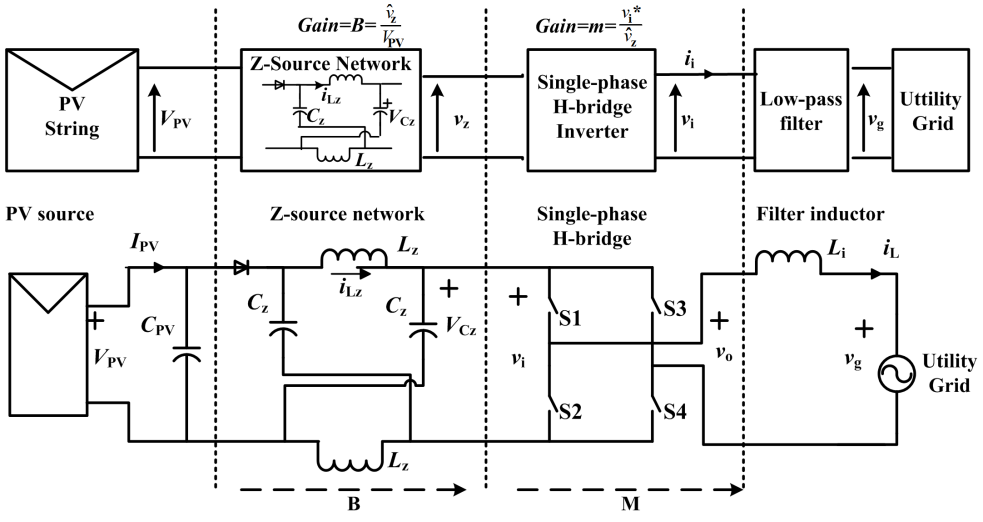


Figure 4.1: Single-phase Z-source inverter for PV to grid interface

A single stage power converter interface (PCI) for a PV-grid interface using ZSI is shown in Fig. 4.1. The ZSI utilizes intentionally applied shoot-through states in order to boost the input voltage. To avoid distortion of the output voltage, shoot-through should occur only when the inverter output voltage is expected to be zero. For an H-bridge inverter with bipolar switching, intentionally inserting shoot-through states distorts the inverter output voltage and current waveforms.

Hence unipolar switching is inevitable for a single phase H-bridge ZSI.

For unipolar switching, there exists three output states, namely positive, zero and negative output states. As the name suggests, these are states when the inverter output voltage v_i is positive, zero and negative respectively. To simplify the discussion, the positive and negative state are together termed as active state (AS). During an AS, the boosted voltage appears inverter input and hence the input voltage v_z is maximum, i.e. $v_z = \hat{v_z}$. When an intentional shoot-through occurs partially or completely during the zero state (ZS), an another additional state is introduced which is referred to as the shoot-through state (STS). During this state, both switches on the same leg of the inverter is switched ON such that a shoot-through occurs and the inverter input voltage v_z as well as the resultant output v_i are zero. To determine the ratio of ZS interval that has to be replaced with STS interval based on the required boost ratio, the time intervals of all the above mentioned states are derived for an ZSI with HC.

4.3 Active, Zero and Shoot-through Intervals

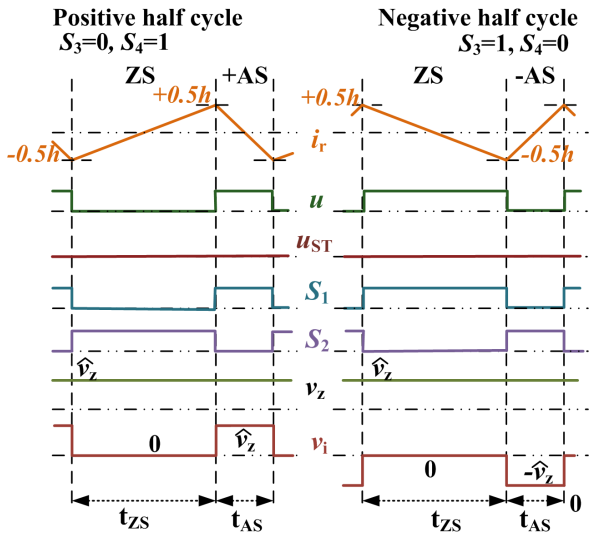


Figure 4.2: Switching pulses and inverter input and output voltage waveforms of the ZSI in Fig. 4.1 for HC without shoot-through

In this section, we analyse the time intervals of unipolar HC to determine the ratio of zero state to be replaced by shoot-through state from the boost ratio. Consider a unipolar HC for H-bridge inverter connected to the grid via a low pass filter as shown in Fig.4.1. The input voltage v_z appears at the input of the inverter. As discussed earlier, $v_z = 0$ during STS and v_z takes its maximum value, i.e. $\hat{v_z}$

during non-STS (i.e. AS and ZS) as shown in Fig. 4.2. Since for HC of GTIs, the time periods for each switching state and switching frequency varies with time, these can be represented as functions of time.

To determine the time interval of AS and ZS, we use the generalized switching interval analysis for HC of GTI discussed in detail in Chapter 3. The approximate switching intervals derived in (2.8) and (2.9) would suffice our requirement. The inverter input voltage V_{dc} is equal to $\hat{v_{\mathrm{z}}}$ during non-STS. Hence the three levels in the inverter output voltage are $v_{\mathrm{i}} = \{-\hat{v_{\mathrm{z}}}, 0, \hat{v_{\mathrm{z}}}\}$. The reference (or desired) output voltage is denoted by v_{i}^* and the modulating signal is $m = M\sin(\omega t + \theta)$, where θ is the phase shift w.r.t. the grid voltage $v_{\mathrm{g}} = V_{\mathrm{g}}\sin(\omega t)$. We also know that, for three-level switching, $n = 3$, $p_{\mathrm{n}} = \frac{n-1}{2} = 1$ and $k = \{0, 1\}$. These are substituted in (2.8) and (2.9) to obtain the time intervals for AS and ZS, denoted as t_{AS} and t_{ZS} respectively. The equations for t_{AS} and t_{ZS} are obtained as (4.1) and (4.2) respectively. Here $\pm 0.5h$ is the hysteresis limit and L_{i} is the filter inductance.

$$t_{\mathrm{AS}} = \frac{hL_{\mathrm{i}}}{\hat{v_{\mathrm{z}}}} \frac{1}{1 - |m|} \tag{4.1}$$

$$t_{\mathrm{ZS}} = \frac{hL_{\mathrm{i}}}{\hat{v_{\mathrm{z}}}} \frac{1}{|m|} \tag{4.2}$$

The total switching time interval T and the ratio of ZS interval to the total interval is derived from (4.1) and (4.2) and presented as (4.3) and (4.4) respectively.

$$T = \frac{hL_{\mathrm{i}}}{\hat{v_{\mathrm{z}}}} \frac{1}{|m|(1 - |m|)} \tag{4.3}$$

$$\frac{t_{\mathrm{ZS}}}{T} = 1 - |m| \tag{4.4}$$

The relation between the boost ratio B and the shoot-through time period to switching time period ratio, $\frac{t_{\mathrm{ST}}(t)}{T(t)}$ is derived by [Peng et al., 2005] as

$$\frac{t_{\mathrm{ST}}}{T} = \frac{1}{2}\left(1 - \frac{1}{B}\right). \tag{4.5}$$

From (4.4) and (4.5), a relation between the boost ratio B and the ratio of ZS interval required to be replaced by STS interval $\frac{t_{\mathrm{ST}}}{t_{\mathrm{ZS}}}$ is obtained as in (4.6). Based on the ratio of STS time interval to ZS interval, we develop a closed loop control.

$$\frac{t_{\mathrm{ST}}}{t_{\mathrm{ZS}}} = \frac{1}{2}\left(\frac{1 - \frac{1}{B}}{1 - |m|}\right) \tag{4.6}$$

4.4 Proposed Closed Loop Control

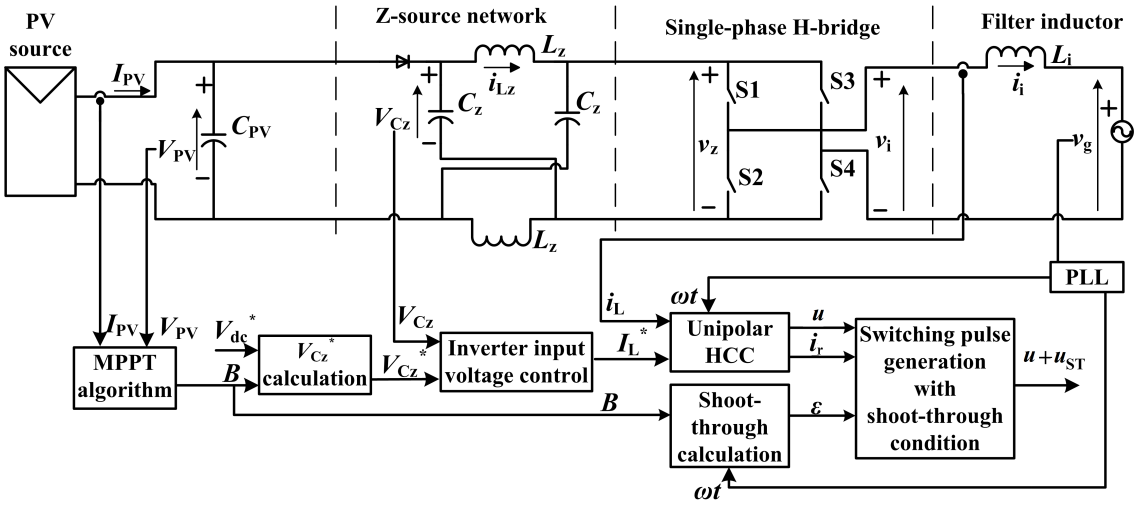


Figure 4.3: PV-grid integration using ZSI with the proposed closed-loop control

The proposed closed loop control structure for ZSI acting as PCI for PV to single-phase grid integration is shown in Fig. 4.3. The input side control is similar to the maximum power point tracking (MPPT) control for DC-DC converter in a two-stage PCI. Perturb and observe method is used as MPPT algorithm in order to obtain the reference boost ratio B^* based on the PV output current and voltage. The reference boost ratio is used to determine the shoot-through limits and to generate reference for the output side control. The output side control is analogous to the DC-link voltage control in a VSI and uses a PI controller that maintains the inverter input voltage at the required reference and generates reference power in terms of output current magnitude. However for a ZSI, the voltage at the input terminals of H-bridge v_z is not a constant as shown in Fig. 4.5 and hence cannot be used for control.

For symmetrical Z-source network, the voltages across the capacitors V_{C_z} is equal to the average inverter input voltage $\bar{v_z}$ [Peng, 2003]. During non-shoot through states, the inverter input voltage is $\hat{v_z}$, where $\hat{v_z}$ is the maximum value of v_z. The voltage across the Z-source capacitor V_{C_z} can be expressed as a function of $\hat{v_z}$ and B using (4.5) as shown in (4.7).

$$\begin{aligned} V_{C_z} &= \hat{v_z}\left(1 - \frac{t_{ST}}{T}\right) \\ &= \frac{\hat{v_z}}{2}\left(1 + \frac{1}{B}\right) \end{aligned} \tag{4.7}$$

Since the voltage across the inverter input terminals during the non-shoot through states is $\hat{v_z}$, it is sufficient to control V_{C_z} to $V^*_{C_z}=\frac{1}{2}\left(1+\frac{1}{B^*}\right)V^*_{dc}$ where V^*_{dc} is the reference inverter input voltage and is greater than the minimum inverter input voltage required.

4.4.1 Determining the Shoot-through Limit

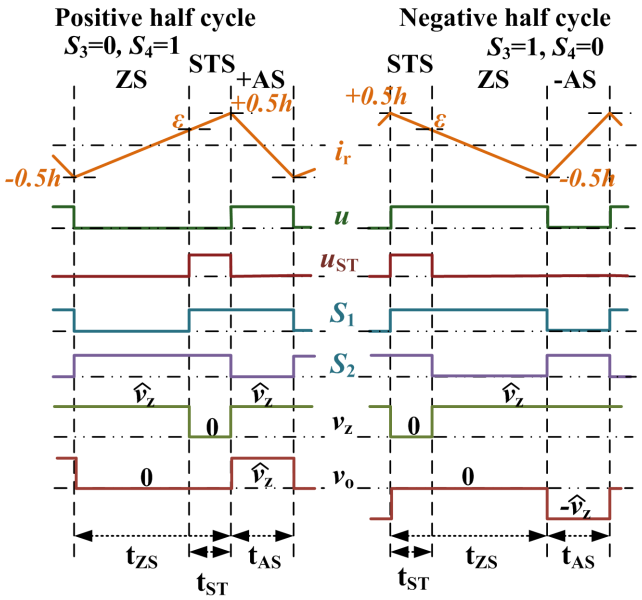


Figure 4.4: Switching pulses and inverter input and output voltage waveforms with shoot-through

With reference to Fig.4.4, the shoot-through limit of error current $\epsilon(t)$ for which the shoot-through state is to be intentionally applied can be obtained as in (4.8). From (4.4), (4.5) and (4.8), ϵ can further be simplified as a function of known variables $0.5h$, B and M as shown in (4.9). The shoot-through time period satisfies the inequality $(0 \leq t_{ST} \leq t_{ZS})$ and hence from (4.8) ϵ satisfies $(-0.5h \leq \epsilon \leq 0.5h)$.

$$\epsilon = 0.5h\left[1-2\frac{t_{ST}}{t_{ZS}}\right] \tag{4.8}$$

$$= 0.5h\left[1-\frac{1-\frac{1}{B}}{1-|m|}\right] \tag{4.9}$$

Since M vary as a function of v_g and V_{PV}, (4.9) is simplified using the relation in (4.10). The reference shoot-through limits $\epsilon^*(t)$ expressed as a function of B^*,

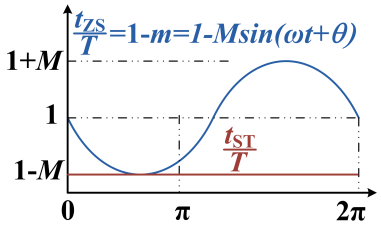


Figure 4.5: Ratio of Shoot-through and zero state time intervals with time period T for maximum constant boost ratio

v_g and V_{PV} is shown in (4.11).

$$BM\sin(\omega t+\theta)=\frac{v_g}{V_{PV}} \tag{4.10}$$

$$\epsilon=0.5h\left[\frac{1-\frac{v_g}{V_{PV}}}{B^*-\frac{v_g}{V_{PV}}}\right] \tag{4.11}$$

In the Fig. 4.5, the ratio of zero state interval to total switching time is observed to vary as an inverted and shifted sinusoidal waveform. Furthermore, the duty ratios of switches S_1 and S_2 vary based on ϵ. However, the switching frequencies do not change due to insertion of shoot-through states. The switching frequencies of S_3 and S_4 are same as the fundamental frequency of grid voltage.

4.4.2 Maximum Constant Boost Ratio

As per (4.5), maximum boost ratio can be obtained when all the zero states are replaced by shoot-through states [Peng et al., 2005]. The maximum boost ratio B_{max} is as shown in (4.12) and varies at a rate of twice the fundamental frequency which would cause undesirable low-frequency ripples on Z-source network [Shen et al., 2006].

$$\epsilon_{max}=-0.5h$$

$$B_{max}=\frac{1}{2|m|-1} \tag{4.12}$$

$$\text{Overall gain } A_{max}=MB_{max} \tag{4.13}$$

$$=\frac{M}{2|m|-1}$$

For the proposed control, in order to obtain maximum constant boost ratio $B_{k\text{-}max}$ which can be maintained constant throughout the fundamental cycle

to avoid ripples at the Z-source network, let the corresponding constant shoot-through to switching period ratio be $\left(\frac{t_{\mathrm{ST}}}{T}\right)_{\text{k-max}}$. Since zero states are replaced with shoot-through states and the ratio $\left(\frac{t_{\mathrm{ST}}}{T}\right)_{\text{k-max}}$ has to be constant for a fundamental cycle, it will correspond to the minimum zero state to switching period ratio, $\left(\frac{t_{\mathrm{ZS}}}{T}\right)_{\text{min}}$. The maximum constant boost ratio $B_{\text{k-max}}$, overall gain $A_{\text{k-max}}$ and error current limits to determine shoot-through states, $\epsilon_{\text{k-max}}(t)$ corresponding to $B_{\text{k-max}}$ can be expressed as in (4.14), (4.15) and (4.16) respectively.

$$B_{\text{k-max}} = \frac{1}{1-2\left(\frac{t_{\mathrm{ST}}}{T}\right)_{\text{k-max}}} = \frac{1}{1-2\left(\frac{t_{\mathrm{ZS}}}{T}\right)_{\text{min}}} = \frac{1}{2M-1} \tag{4.14}$$

$$A_{\text{k-max}} = \frac{M}{2M-1} \tag{4.15}$$

$$\epsilon_{\text{k-max}} = 0.5h\left(1 - \frac{2(1-M)}{1-M\sin(\omega t+\theta))}\right) \tag{4.16}$$

4.5 Results and Discussion

In order to validate the theoretical analysis, the proposed control is implemented using MATLAB-Simulink platform for a single-phase PV grid-tie Z-source inverter system with a rated power of 2.4 kW. The simulation results correspond to the following system parameters: input capacitance C_{PV}=1000 μF, Z-source network inductance L_{z}=5 mH, Z-source network capacitance C_{z}=1000 μF and filter inductance L_{i}=5 mH. The PV source provides a maximum output voltage and current of 293 V and 8.2 A at nominal operating conditions. The rated grid voltage is 230.9 V with a fundamental frequency of 50 Hz.

4.5.1 Initial dynamics

The initial dynamics with an irradiation G=1000W/m^2, rated grid voltage and zero initial conditions for capacitors and inductors, is as shown in Fig. 4.6. The boost ratio B varies in order to maintain V_{PV} at the voltage corresponding to MPP. It can be observed that the change in B causes $V_{\mathrm{C_z}}$ to change. The dynamic response settles down at t=0.5 s and is reasonably fast. The grid current is measured to be 10.3 A with output power of 2378 W. The total harmonic distortion (THD) of grid current is found to be 1.88%.

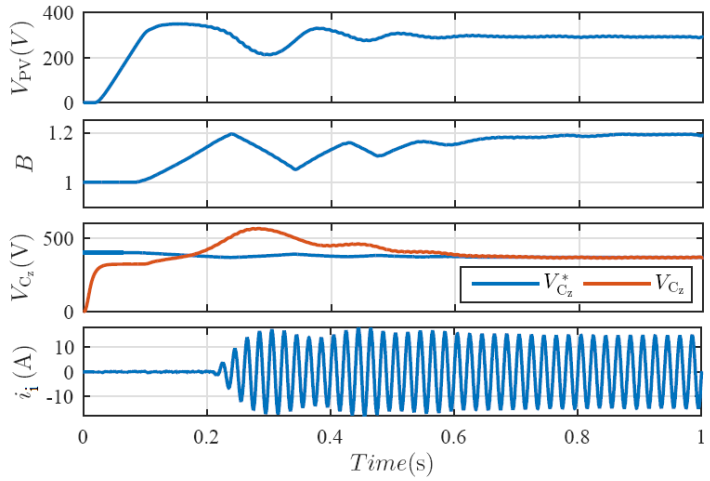


Figure 4.6: Results showing initial dynamic response of the system for G=1000W/m^2 and v_g=230.9 V

4.5.2 Change in irradiation

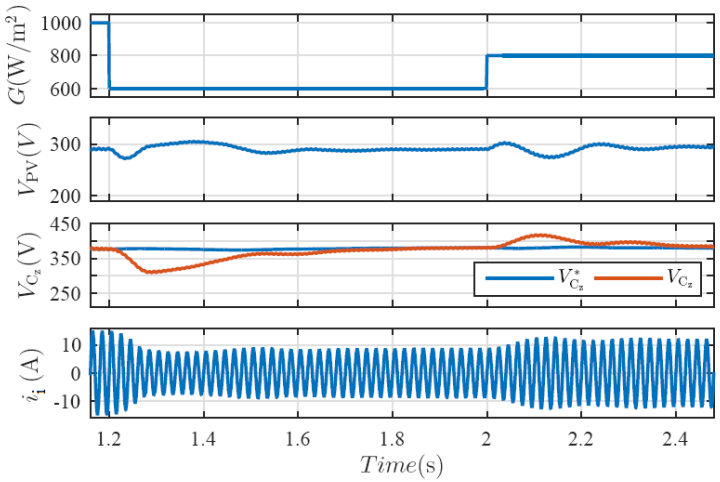


Figure 4.7: Results showing effect of sudden changes in irradiation

The effect of sudden change in irradiation is shown in Fig. 4.7. The irradiation is varied from 1000W/m^2 to 600W/m^2 at 1.2 s and the dynamics caused settles down in 0.3 s. The uniform irradiation of 600W/m^2 yields an output power of 1410 W with grid current of 6.107 A. At t=2 s, the sudden variation in irradiation to 800 W/m^2 causes the output power and grid current to increase to 1905 W and 8.25 A respectively. The settling time is approximately 0.2 s. The THD of grid current at steady state for G=600 W/m^2 and 800 W/m^2 are 2.95% and 2.26% respectively. At steady state, the PV output voltage V_{PV} is observed to settle at the voltage corresponding to that of MPP.

4.5.3 Change in grid voltage

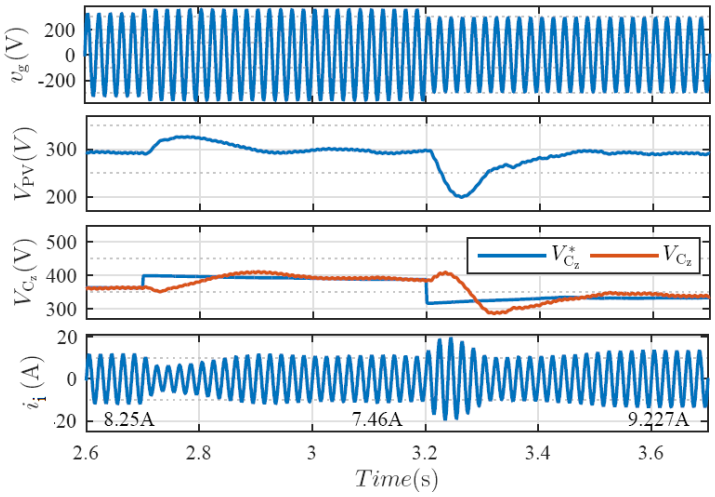


Figure 4.8: Simulation results showing effect of swell and sag in grid voltage

Fig 4.8 shows the effect of sudden change in grid voltage from rated value of 230.9 V to 1.1×230.9 V at t=2.7 s at a constant uniform irradiation of 800 W/m^2. The grid current increases from 8.25 A to 7.46 A in 0.26 s so as to maintain the output power constant at 1905W/m^2 at steady state. A sag of 0.9 pu appears at 3.2 s changing the grid voltage from 1.1×230.9 V to 0.9×230.9 V. The current settles to 9.227 A in 0.34 s thereby maintaining the output power constant. The THD of grid current for rated voltage, 1.1 times rated voltage and 0.9 times rated voltage are 2.26%, 2.6% and 2.04% respectively.

4.6 Conclusion

The analysis and implementation of a modified unipolar HC for a single phase ZSI for PV-grid interconnection by determining the shoot-through states by means of error current and voltage boost ratio is presented. The HC is known for its fast response and high tracking precision. When HC implemented for ZSI results in a PCI with high efficiency and fast dynamic response. The maximum constant boost ratio as a function of modulation index, that would avoid low frequency ripples at Z-source network, has been derived. The simulation results show that dynamics responses are reasonably fast and steady state responses are stable in all the cases. The THD of grid current at steady state is less than 3% for all the cases and hence is well within the limits specified for PV-grid interconnection.

Chapter 5

AC Module using pDC-l Inverter

Contents

5.1 Introduction

AC modules are low power PV module based systems capable of producing AC power output from PV modules. They use single PV modules and hence have the capability of eliminating losses under PV module mismatches in central or string inverters [Meneses et al., 2013, Çelik et al., 2018]. The micro-inverters (μIs,) also known as module-integrated-converters, are converter configurations developed for AC modules. For applications involving grid integration of AC modules, the alternating output to PV module voltage ratios are often high. Hence high gain converters are an inevitable part of AC modules. The high gain Z-source converters (ZSC) are capable of providing high gains without the use of transformers, coupling

inductors or other components that contribute to the losses. However their use in μI systems are not widely explored.

The high-gain converter in a μI for AC module is followed by an inverter which is generally single-phase due to the low power rating of the system. The choice of inverter is hence a trade-off between filter requirement and system efficiency which suggests that use of multi-level inverters is not advisable for low power applications, such as in AC modules. However, the psuedo DC-link inverters can help overcome this limitation [Meneses et al., 2013]. The pDC-l inverter is based the concept that an alternating output voltage can be obtained from a single-phase H-bridge inverter operating at fundamental frequency if its input DC-link voltage varies as a rectified sinusoid. The efficiency of these low power AC modules is expected to be considerably high. Hence, the control of such a system with high-gain converter and pDC-l inverter is of prime importance.

As discussed in the previous chapters, HC is a promising modulation technique that ensures simple, accurate and rapid control, thereby ensuring high efficiency control. However the use of HC for AC module based configurations have not been explored in the available literature.

Considering the limitations of the existing μIs and their controls, an improved μI with ZSC cascaded pDC-l is proposed in this work. The major contributions of this chapter are summarized as follows.

- A detailed analysis and design of one of the ZSCs for the specific application of AC module is presented.
- The modes of operation of the converter when controlled to provide pDC-l output is discussed.
- Based on the analysis, a closed loop control is proposed for the ZSC cascaded pDC-l μI configuration using voltage and current HC.

5.2 Proposed μI with ZSC cascaded by pDC-l

The configuration of the proposed AC module is shown in Fig 5.1. It consists of the ZSC cascaded with a single phase pDC-l acting as an unfolding circuit. The PV module and the single phase grid acts as the source and the load respectively. The grid is considered as an infinite AC power source or sink of constant voltage and frequency. For grid integrated AC module applications, converters capable of providing high gain ratios at optimal efficiency are required. Additionally, if

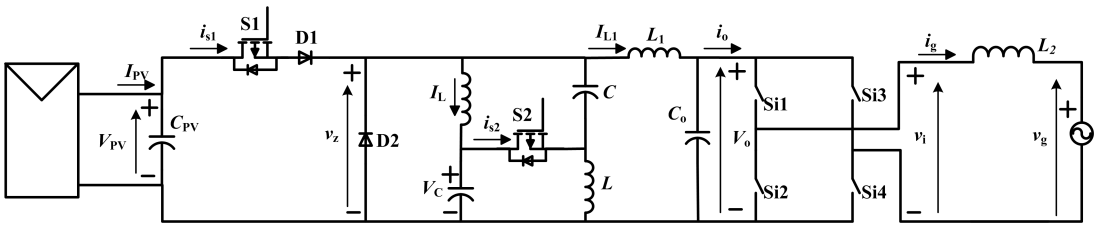
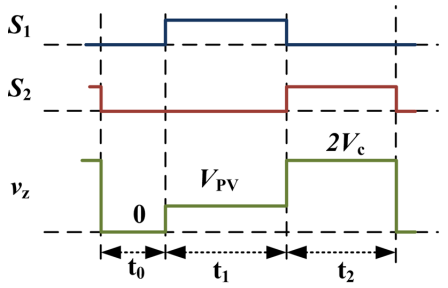


Figure 5.1: Proposed AC module with ZSC [Asano et al., 2011] cascaded pDC-l



State	S_1	S_2	Duration
State 0	OFF	OFF	t_0
State 1	ON	OFF	t_1
State 2	OFF	ON	t_2

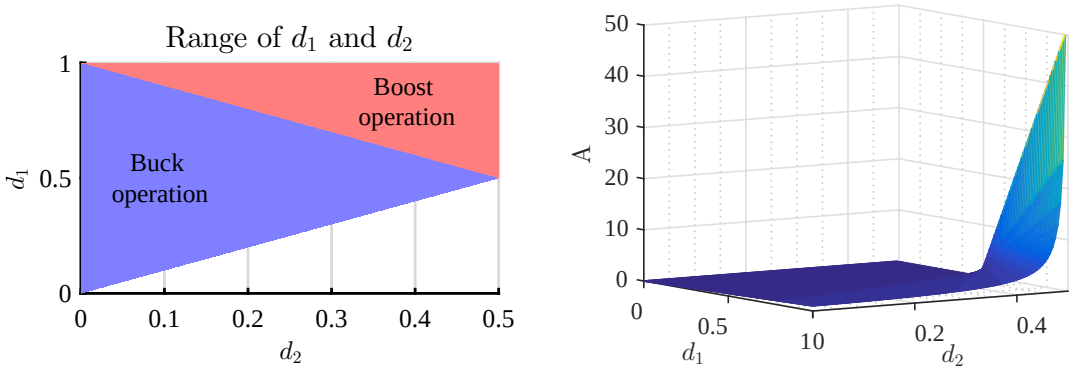
Figure 5.2: Switching states of ZSC

pDC-l inverters are employed, the high gain converter is expected to provide both buck and boost gains. The high-gain ZSC proposed in [Asano et al., 2011] is used for this purpose due to its advantages of reduced passive components and switching devices with availability of common ground and possibility of obtaining a wide range of voltage gain without affecting the efficiency. The high-gain ZSC is cascaded with the conventional two-leg H-bridge which is used here as an unfolding circuit to obtain a pDC-l output. The switches operate at fundamental frequency, thereby inverting the input at every alternate half cycle. A first order filter of low inductance value would be sufficient since the output of the inverter is sinusoidal. Moreover an LC network is present at the output of the high-gain converter. The LC network along with the filter inductor results in a second order network which may cause resonance. Hence care must be taken during design of filter parameters.

5.3 Existing Analysis of ZSC

As per the analysis presented by [Asano et al., 2011], the converter has three states of operation in each switching period T, as shown in Fig 5.2. The duty ratios $d_1 = \frac{t_1}{T}$ and $d_2 = \frac{t_2}{T}$ correspond to switches S_1 and S_2 respectively. In the analysis presented by [Asano et al., 2011], it is assumed that $V_{PV} < 2V_C$. Hence, when switch S_2 is ON, the diode D_1 is reverse biased and the input is isolated irrespective of the switching state of S_1. Under CCM, the gain of the converter is expressed as in (5.1), where $0 \leq d_2 < 0.5$ and $d_1 \leq 1$. The range of values of

d_1 and d_2 for buck and boost operations are shown in Fig. 5.3a. The variation of voltage gain, A, with respect to duty ratios, is shown in figure 5.3b.



(a) Range of duty ratio variations

(b) Voltage Gain M versus duty ratios

Figure 5.3: Range of duty ratios and variation of Voltage Gain A w.r.t. d and d_2

$$A = \frac{t_1}{t_1 - t_2 + t_0} = \frac{d_1 - d_2}{1 - 2d_2} \tag{5.1}$$

The circuit operation and gain derivation presented by [Asano et al., 2011] is, however, based on several assumptions which include constant output voltage V_o, non-overlapped switching pulses or gain ratio greater than 0.5 and CCM operation. Though these assumptions are not explicitly mentioned in [Asano et al., 2011], it is observed that other states can exist when they are violated. When the converter is cascaded with the pDC-l inverter, the converter output voltage is required to be varied as a rectified sinusoid. Hence, further analysis of the converter considering all possible operating states while providing a rectified sinusoidal output voltage is necessary.

5.4 Modes of Operation of High Gain Converter

The high gain converter has two switching devices and hence is expected to have $2^2 = 4$ states of operation in continuous conduction mode (CCM). However due to the diodes D_1 and D_2, there may exist additional states due to discontinuous conduction modes (DCM). The switching pulses can be obtained by any existing modulation technique. The possible combinations of switching pulse are no overlapping of switching pulses, complete overlapping of pulses and partial overlap of pulses. The possible states of operation assuming $V_{in} > 0$ and $V_C \geq 0$ are listed

Table 5.1: Switching States of high-gain buck-boost ZSC

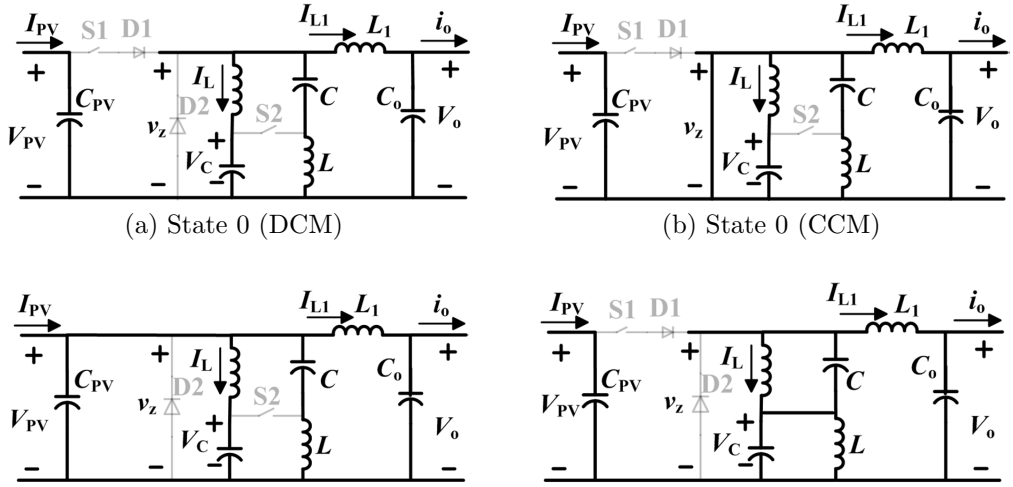
State	Mode	S_1	S_2	D_1	D_2	Condition	v_L	v_{L_1}	i_C
$0(t_{0_C})$	CCM	OFF	OFF	OFF	ON	$2I_L > -I_{L_1}$	$-V_C$	$-V_o$	I_L
$0(t_{0_D})$	DCM	OFF	OFF	OFF	OFF	$2I_L < -I_{L_1}$	0	0	I_L
$1(t_1)$	CCM	ON	OFF	ON	OFF	-	$V_i - V_C$	$V_i - V_o$	I_L
$2(t_2)$	CCM	OFF	ON	OFF	OFF	-	V_C	$2V_C - V_o$	$-I_L - I_{L_1}$
$3(t_{3_D})$	DCM	ON	ON	OFF	OFF	$V_{in} < 2V_C$	V_C	$2V_C - V_o$	$-I_L - I_{L_1}$
$3(t_{3_C})$	CCM	ON	ON	ON	OFF	$V_{in} > 2V_C$	V_C	$V_i - V_o$	0

in Table 5.1. The assumptions made are valid for all the steady state operating conditions of the converter when cascaded with a pDC-l inverter.

The voltage gain ratio can be derived as in (5.2).

$$A = \frac{V_o}{V_i} = \frac{t_1 + 0.5t_{3C}}{t_1 + 0t_{0C} - t_2 - t_{3D}} \tag{5.2}$$

In order to simplify the control and for ease of analysis, pulses are provided with no overlap. This eliminates the state 3 (CCM and DCM). The circuit based on each state of operation is shown in Fig.5.4 and the corresponding waveforms are presented in Fig.5.5. The gain ratio is simplified as in (5.3).



(a) State 0 (DCM)

(b) State 0 (CCM)

(c) State 1

(d) State 2

Figure 5.4: States of operation based on possible combinations of switching conditions considering no overlap of switching pulses

$$A = \frac{t_1}{t_1 + t_{0C} - t_2} \tag{5.3}$$

The above analysis is used further for the design and control of the proposed μI.

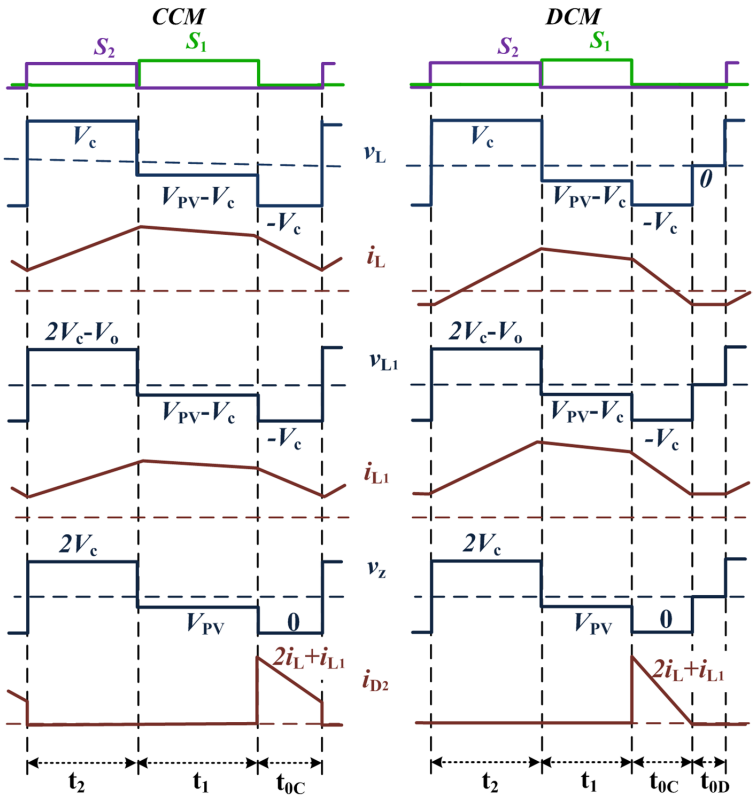


Figure 5.5: Switching pulses S_1 and S_2 and corresponding waveforms

5.5 Closed Loop Control of the proposed μI

Since the PV module is integrated with the grid, the two parameters that are expected to be controlled are the PV input voltage and the grid injected current. The PV module is expected to operate at V_{MPP}, i.e. the voltage at which maximum power output can be obtained. Hence, the voltage across the DC-link capacitor at the output of PV module, C_{PV} is controlled to V_{MPP} using a conventional PI controller as shown in Fig. 5.6. The controller is tuned to obtain a magnitude of the reference current to be injected into the grid in order to maintain power balance. Hysteresis current control is used to obtain switching pulses from the reference and actual grid current due to its advantages of simplicity, robustness and fast dynamic response. An additional control is employed for the voltage across Z-source capacitor. Since the concept of pDC-l is used, the capacitor voltage is controlled in proportion to the rectified grid voltage.

The filter impedance L_2 creates a phase shift, though small, on the output voltage, which when connected to the grid results in current distortions. Due to low power operation, even slight distortions can affect the harmonic content of grid current. To avoid this, a phase shift ϕ proportional to the magnitude of grid

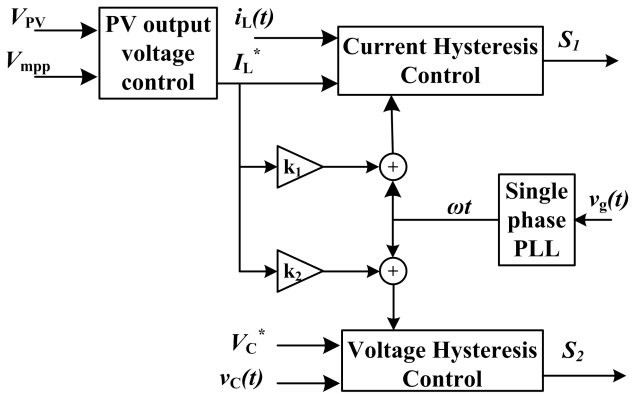


Figure 5.6: Proposed closed loop control using voltage and current HC

current is added to the output of phase locked loop (PLL) that senses the phase and frequency of grid voltage, $V_{\mathrm{g}} \sin(\omega t)$. The inverter is operated at zero crossings of $v_{\mathrm{g}} = V_{\mathrm{g}} \sin(\omega t + \phi)$. Only real power is fed into the grid to avoid any distortions in current. This is justified as low power renewable resources feeding the grid are expected to operate at unity power factor.

5.6 Parameter Design

The parameter design of the proposed AC module with ZSC and pDC-l inverter is discussed in this section. The voltages across and currents though each component is listed in Table. 5.2. The rated voltages and currents through each component is used as references for component selection.

5.6.1 Switches and Diodes

The switch S_1 and diode D_1 are connected in series. From the Table. 5.2, the maximum drain-to-source voltage across S_1 is V_{PV} and the maximum reverse voltage across D_1 is $V_{\mathrm{o}} - V_{\mathrm{PV}}$. Similarly the maximum drain-to-source voltage across S_2

Table 5.2: Switching variables as a function of state variables of high-gain ZSC

State	0(CCM)	0(DCM)	1	2
v_{S_1}	V_{PV}	$V_{\mathrm{PV}} - V_{\mathrm{C}}$	0	$V_{\mathrm{PV}} - V_{\mathrm{C}}$
v_{S_2}	$2V_{\mathrm{C}}$	V_{C}	$2V_{\mathrm{C}} - V_{\mathrm{PV}}$	0
v_{D_2}	0	$-V_{\mathrm{C}}$	$-V_{\mathrm{PV}}$	$-2V_{\mathrm{C}}$
i_{S_1}	0	0	$2i_{\mathrm{L}} + i_{\mathrm{L}_1}$	0
i_{S_2}	0	0	0	$2i_{\mathrm{L}} + i_{\mathrm{L}_1}$
i_{D_2}	$2i_{\mathrm{L}} + i_{\mathrm{L}_1}$	0	0	0

is $2V_o$ and the maximum reverse voltage across D_2 is $2V_o$. The maximum current through all the devices are equal and can be expressed in terms of output current as $I_o\left[\frac{T}{T-2t_2}\right]$ or input current as $I_{PV}\left[\frac{T}{t_1}\right]$.

5.6.2 Inductors and Capacitors

The converter operates in DCM when the current through diode D_2 reduces to zero as shown in Fig 5.5. The condition for boundary conduction mode, shown in (5.4), is obtained by equating the minimum current through D_2, $I_{D_2min} = \min(i_{D_2}) = 0$.

$$L_{eff} = \frac{R_o}{2f_{sw}}\frac{V_i}{V_o}\frac{t_1}{T}\left[\left(1-\frac{t_2}{T}\right)^2+\left(\frac{t_2}{T}\right)^2-\frac{t_1}{T}\right] \text{ where } \frac{1}{L_{eff}} = \frac{2}{L}+\frac{1}{L_1} \tag{5.4}$$

The design of inductors and capacitors are based on the maximum allowable ripple currents and voltages and the condition in 5.4.

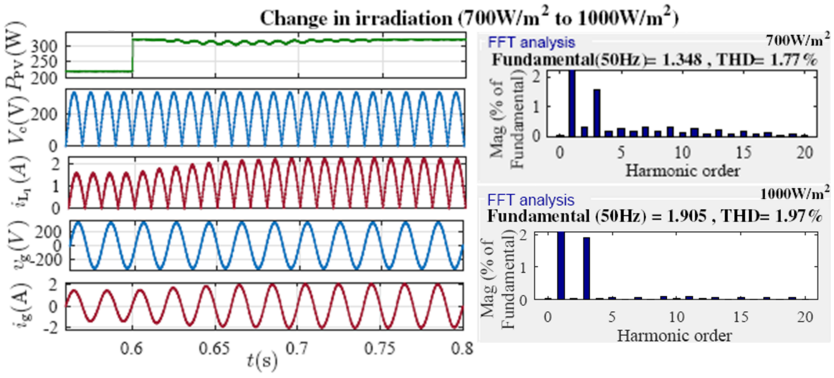
5.7 Results and Discussion

Table 5.3: System Specifications

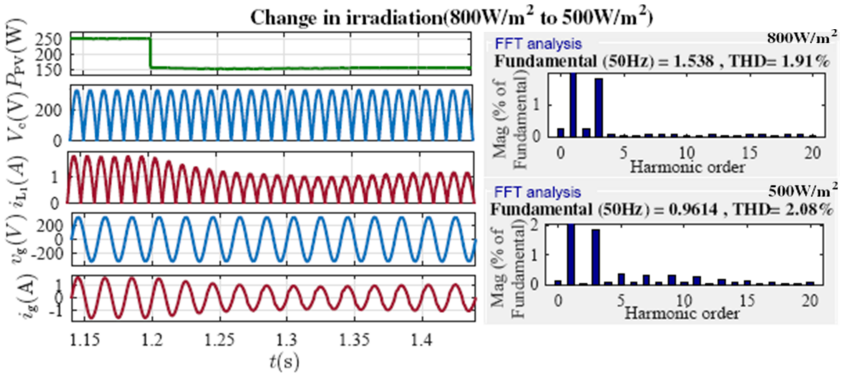
PV ratings at STC	P_{PV}	320 W
	V_{PV}	57.3 V
	I_{PV}	5.59 A
Grid ratings	V_g	230 V
	f_g	50 Hz
Z-Source converter	L	2.4 mH
	C	1 μF
	L_1	9.7 mH
	C_o	0.1 μF
Input Capacitor	C_{PV}	4800 μF
Filter inductor	L_2	1 mH

A simulation model of the proposed AC module using the high gain ZSC cascaded with pDC-l inverter integrated to the grid with the system parameters listed in Table 5.3 is built using MATLAB/Simulink platform. The dynamics caused due to changes in irradiation and grid voltage are shown in Fig. 5.7 and 5.8.

In Fig 5.7a, the results when irradiation G is varied from 700 W/m^2 to 1000 W/m^2 at t=0.6 s is shown. Since the voltage V_c, and hence V_o, are controlled based on the grid voltage v_g, the changes in irradiation does not cause dynamics in the voltage control loop. The change in irradiation causes the PV output power P_{PV}



(a)



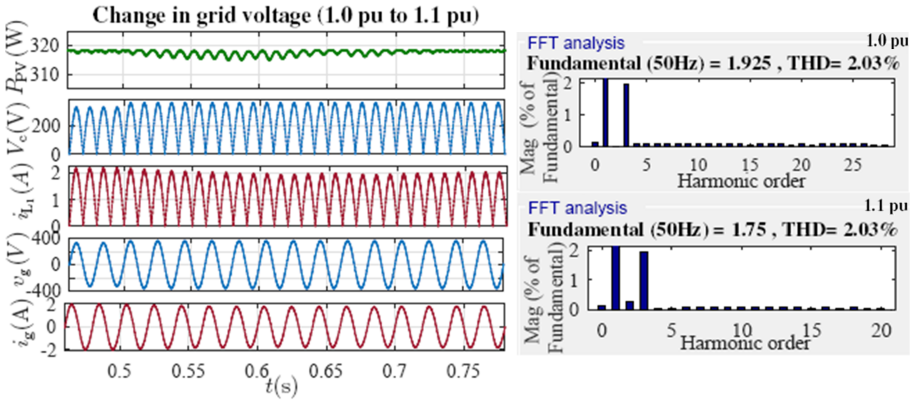
(b)

Figure 5.7: Results showing dynamics due to change in irradiation G (a) 700 W/m^2 to 1000 W/m^2, (b) 800 W/m^2 to 500 W/m^2

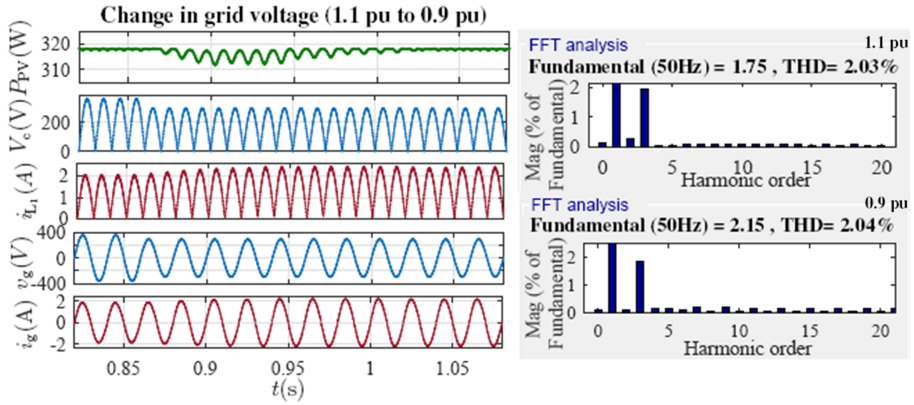
to increase from 223 W/m^2 to 319 W/m^2. The change in power is reflected as an increase in both i_{L_1} and i_g. The magnitude of the grid current i_g increases from 0.97 A to 1.38 A so as to maintain power balance. The THD of i_g in both cases is less than 2%. The dynamics takes approximately 0.15 s to settle and is observed to remain stable thereafter.

The irradiation now reduces from 800 W/m^2 to 500 W/m^2 at 1.2 s. The response of the proposed μI are presented in the results shown in Fig. 5.7b. The PV power P_{PV} at steady state is observed to be 254 W for G=800 W/m^2 and 157 W for G=500 W/m^2. While the voltage V_c remains stable, the dynamics in i_{L_1} and i_g can be observed to settle down in approximately 0.15 s for both cases. The grid current magnitudes for G=800 W/m^2 and 500 W/m^2 at steady state are 1.1 A and 0.69 A respectively and the THD is approximately 2%.

In Fig. 5.8a, we observe that a swell in grid voltage from 1.0 pu to 1.1 pu at 0.5 s causes the current i_{L_1} to decrease in order to maintain the power balance. Hence the grid current decreases from 1.38 A and settles to 1.26 A in 0.2 s. The grid voltage now varies from 1.1 pu to 0.9 pu at 0.86 s as shown in Fig. 5.8b.



(a)



(b)

Figure 5.8: Results showing dynamics due to changes in grid voltage (a) 1.0 pu to 1.1 pu and (b) 1.1 pu to 0.9 pu

The oscillations in the input power and grid current settles down in 0.24 s for the sag of 0.2 pu in the grid voltage. The grid current at steady states are 1.52 A is 0.9 pu. The THD is approximately 2% in all the cases. The ZSC output voltage V_o is indirectly controlled via V_C which varies in proportion with the grid voltage. However the grid voltage variation is observed to have negligible effect on the PV input power P_{PV}.

Based on these results, we observe that the proposed μI using ZSC and pDC-l inverter provides satisfactory responses in terms of THD as well as settling time due to changes in operating conditions.

5.8 Conclusion

An efficient AC module with a high gain Z-source buck boost converter and pDC-l inverter is proposed. The modes of operation, including DCM, of the high-gain

ZSC when cascaded with pDC-l inverter is analysed. A closed loop control of the proposed μI using voltage and current HC is developed in order to achieve power balance while maintaining the THD within that specified by grid requirements. The parameter design of switching and passive components aid in their proper choice. The simulation and experimental results support the theoretical analysis. The THD of the current injected to the grid by the proposed converter is found to be within the limits specified by IEEE standards.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Grid integration of PV sources overcome the shortcomings of intermittent and unpredictable power input that are prevalent in standalone and hybrid systems. However efficient, reliable and robust control is mandatory for such systems so as to meet the grid standard requirements. Several topologies are available for the PCIs used for grid integration of solar PV sources. Amongst the several controls available for these, HC is widely known to have several advantages over other modulation techniques. This makes HC a unique choice for the control of PCIs. Nevertheless, it has not been widely used for several applications including control of PCIs, due to its drawbacks of varying undetermined switching frequency and switching instants, requirement of high precision AC current sensor and widening of the current limits due to digital sampling. Furthermore, the control of PCI topologies such as ZSI and μIs using HC have not been explored. Therefore, in this thesis, these shortcomings of HC are discussed along with the possible solutions of the same.

The thesis presents the basic background of PCIs for grid integration of PV systems. A detailed literature review of PCIs and their modulation techniques, including HC, are discussed. A review of the existing switching frequency analysis of HC is presented. The commonly used sensorless control techniques for different power electronic converters are discussed. Further, a review of the existing controls for single stage ZSIs and AC modules is presented. The existing control techniques including HC for these topologies for PCI are also discussed in detail. Based on this literature review, the research gaps are identified and objectives are defined.

Switching frequency of GTIs is an important parameter in the system de-

sign. Hence a precise formulation of switching frequency of multi-level inverters is inevitable. The short-comings of the existing formulations are closely observed and an improved generalized formulation is obtained. The derived formulation is observed to produce better results, in comparison to those obtained using the existing equation, when used for system design of a three-level GTI. The switching frequency variations for different range of operating conditions have been analysed. This analysis can aid researchers to accurately design GTIs even when there is a posibility of wide variation in operating conditions. The simulation and experimental results are compared with the computed values of the existing and proposed equations. The proposed equation is observed to clearly provide values closer to those obtained in the results.

Followed by frequency estimation, an AC current sensor-less HC for GTIs based on switching instant analysis is presented. This overcomes the problems in HC, such as requirement of high precision AC current sensor and widening of current limits in digital control. Time-domain approach is used to compute the switching instants, while taking into account of the effects of non-linearity of ripple current, dynamic variations, and digital sampling. The results are compared with the conventional analog and digital HC and are found superior to those of the commonly used sensorless technique.

The HC for ZSIs used as PCI for grid integration is not a widely explored area. This is due to the undetermined switching intervals in HC. A detailed analysis of the switching intervals in a unipolar HC of ZSI is presented. Based on this, the shoot-through limits are identified and a closed loop control for ZSI based single stage PCI is developed. The results presented show satisfactory performance of the proposed HC based modulation of ZSI.

The shortcoming of partial shading losses in low power string inverters are eliminated by using AC modules. The PCIs and controls for AC modules is an emerging area of research. In this work, a μI with high gain ZSC cascaded by pDC-l inverter is proposed as a PCI for AC modules. The modes of operation of such a μI system is explored in detail and based on the analysis a closed loop control involving voltage and current HCs is proposed. The simulation results presented validate the theoretical claims.

To summarize, in this thesis, several shortcomings of HC were identified. These short comings were addressed and solutions were proposed. The results also validate the theoretical analysis in each of the contributions.

6.2 Future Scope of Work

On the basis of the research findings elaborated in this thesis, the future scope of work are identified as follows:

1. The switching frequency analysis can be expanded to different filter configurations and for different power factor operations.

2. Based on the switching frequency formulation, a user interface maybe created to aid researchers to design PCIs of required specifications that use HC for modulation.

3. The switching instant analysis may be carried out for other GTIs such as multilevel inverters, ZSIs and μIs, with a view to develop AC current sensorless HC.

4. The HC of other novel ZSI configurations can be developed by similar analysis and the hardware implementation and validation can be done.

5. The modes of operation in other ZSC topologies, when used to obtain pDC-l, can be analysed and a comparison among these can be carried out so as to choose a efficient μI topology.

Appendix A : Modelling of the μI

Further analysis of the μI discussed in Chapter 5 is presented here. These can aid in future work related to the chapter 5. The equations corresponding to the high gain ZSC and pDC-l inverter are as follows:

$$V_{\mathrm{PV}} = \frac{I_{\mathrm{PV}} - i_{\mathrm{S_1}}}{C_{\mathrm{PV}} S} \tag{6.1}$$

$$I_{\mathrm{L}} = \frac{v_{\mathrm{z}} - V_{\mathrm{c}}}{LS} \tag{6.2}$$

$$V_{\mathrm{c}} = \frac{I_{\mathrm{L}} - i_{\mathrm{S_2}}}{CS} \tag{6.3}$$

$$I_{\mathrm{L_1}} = \frac{v_{\mathrm{z}} - V_{\mathrm{o}}}{L_1 S} \tag{6.4}$$

$$V_{\mathrm{o}} = \frac{I_{L_1} - i_{\mathrm{o}}}{C_{\mathrm{o}} S} \tag{6.5}$$

$$I_{\mathrm{L_2}} = \frac{v_{\mathrm{i}} - v_{\mathrm{g}}}{LS} \tag{6.6}$$

All switches are MOSFET/IGBT devices with anti-parallel diodes. Switches and diodes are assumed to have negligible forward voltage drop and ON-state resistance. Since i_{i} and v_{i} are parameters related to the inverter, they may be dealt separately. Hence the variables to be expressed as functions of state variables and switching functions S_1, S_2, D_1 and D_2 are $i_{\mathrm{S_1}}$, $i_{\mathrm{S_2}}$ and v_{z}. The equations (6.1) to(6.6) are valid for all the possible switching conditions.
The converter has four switching components (S_1, S_2, D_1 and D_2) and therefore may have 2^4 possible operating conditions. However due to the series connection of switch S_1 and diode D_1, it can be considered as one switch S with conducting state considering switching conditions of both S_1 and D_1. Hence the possible states of operation are reduced to $2^4 = 8$. The switching conditions are detailed as follows. For simplicity, S_1, S_2, D_1, D_2 represent the conducting states of the corresponding devices. u_{S1} and u_{S2} represent switching pulses (not conducting state) of switches S_1 and S_2 respectively.

$$S = S_1.D_1 = u_{\mathrm{S1}}.(i_{\mathrm{S_1}} > 0)||(V_{\mathrm{PV}} - V_{\mathrm{z}} > 0) \tag{6.7}$$

$$S_2 = u_{\mathrm{S2}}||(i_{\mathrm{S_2}} < 0)||(2V_{\mathrm{c}} - V_{\mathrm{z}} < 0) \tag{6.8}$$

$$D_2 = (2i_{\mathrm{L}} + i_{\mathrm{L1}} - i_{\mathrm{S_1}} - i_{\mathrm{S_2}} > 0)||(v_{\mathrm{z}} < 0) \tag{6.9}$$

For the eight states shown in Fig. 6.1, i_{S_1}, i_{S_2} and v_z are expressed as follows.

State 0: S_1, S_2, D_2 are not conducting

$$i_{S_1} = 0$$
$$i_{S_2} = 0$$
$$v_z = \frac{L_1 V_c + \frac{L}{2} V_o}{L_1 + \frac{L}{2}}$$

State 1: Only D_2 is conducting

$$i_{S_1} = 0$$
$$i_{S_2} = 0$$
$$v_z = 0$$

State 2: Only S_2 is conducting.

$$i_{S_1} = 0$$
$$i_{S_2} = 2I_L + I_{L_1}$$
$$v_z = 2V_c$$

State 3: S_2 and D_2 are conducting.

$$i_{S_1} = 0$$
$$i_{S_2} = I_L$$
$$v_z = 0$$

State 4: Only S_1 is conducting.

$$i_{S_1} = 2I_L + I_{L_1}$$
$$i_{S_2} = 0$$
$$v_z = V_{PV}$$

State 5: S_1 and D_2 are conducting.

$$i_{S_1} = I_{PV}$$
$$i_{S_2} = 0$$
$$v_z = 0$$

State 6: S_2 and D_2 is conducting.

$$i_{S_1} = \frac{I_{PV}\frac{C}{2} + (I_L + I_{L_1})C_{PV}}{C_{PV} + \frac{C}{2}}$$
$$i_{S_2} = \frac{I_L(C_{PV}+C) + (I_{L_1} - I_{PV})\frac{C}{2}}{C_{PV} + \frac{C}{2}}$$
$$v_z = 2V_c$$

State 7: S_1, S_2 and D_2 are conducting.

$$i_{S_1} = I_{PV}$$
$$i_{S_2} = I_L$$
$$v_z = 0$$

Two port network representation

The two port network of the proposed μI consists of cascading of individual two port networks. Since transmission matrix of a system consisting of cascaded two port networks can be obtained by multiplying their individual transmission matrices, the transmission matrix for the proposed μI can be expressed as shown in (6.10). Here X_Z is the reactance of, say Z representing the inductance or capacitance of the μI.

$$A_{\mu I} = A_{C_{PV}} A_{ZSC} A_{pDC-l} A_{L_2} \tag{6.10}$$

$$A_{C_{PV}} = \begin{bmatrix} 1 & 0 \\ \frac{1}{X_{C_{PV}}} & 1 \end{bmatrix}$$

$$A_{L_2} = \begin{bmatrix} 1 & X_{L_2} \\ 0 & 1 \end{bmatrix}$$

In order to obtain A_{ZCS}, the converter is considered to consist of individual cascaded two port networks with Z_{S_1}, Z_Z, Z_{D_2}, X_{L_1} and X_{C_o} are the impedances of series connection of switch S_1 and diode D_1, the Z-source network with the switch

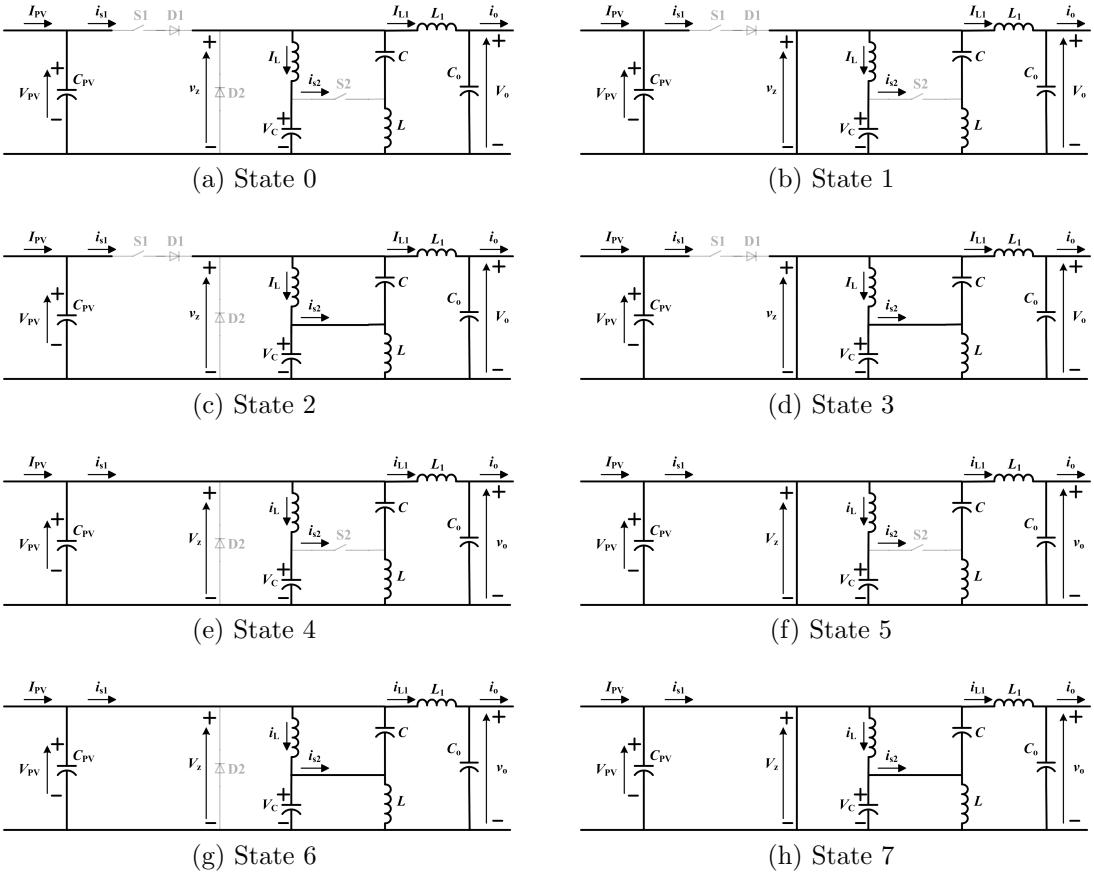


Figure 6.1: States of operation based on switching conditions

S_2, diode D_2, inductance L_1 and capacitance C_o respectively.

$$A_{\text{ZCS}} = \begin{bmatrix} \dfrac{1+s^2LC}{1-s^2LC} & \dfrac{2sL}{1-s^2LC} \\ \dfrac{2sC}{1-s^2LC} & \dfrac{1+s^2LC}{1-s^2LC} \end{bmatrix}$$

Appendix B: MicroLab Box

MicroLabBox, presented in Fig. 6.2, is designed for control prototyping as well as real time simulations. A DS1202 base board with a real-time dual-core processor enables to implement controls similar to those in an analog or digital platforms. A separate co-processor is used in order to manage host PC communications. An RTI blockset is provided in the software to model the user defined control algorithms using the MATLAB/Simulink platform. The control inputs and outputs can be virtually accessed through I/O and the capabilities of the MicroLabBox. All the results presented in this thesis have been obtained by implementing the control algorithms in the MicroLabBox. Certain results obtained using the MicroLabBox were also verified using the TMS320F28027 series microcontroller to implemet the control.

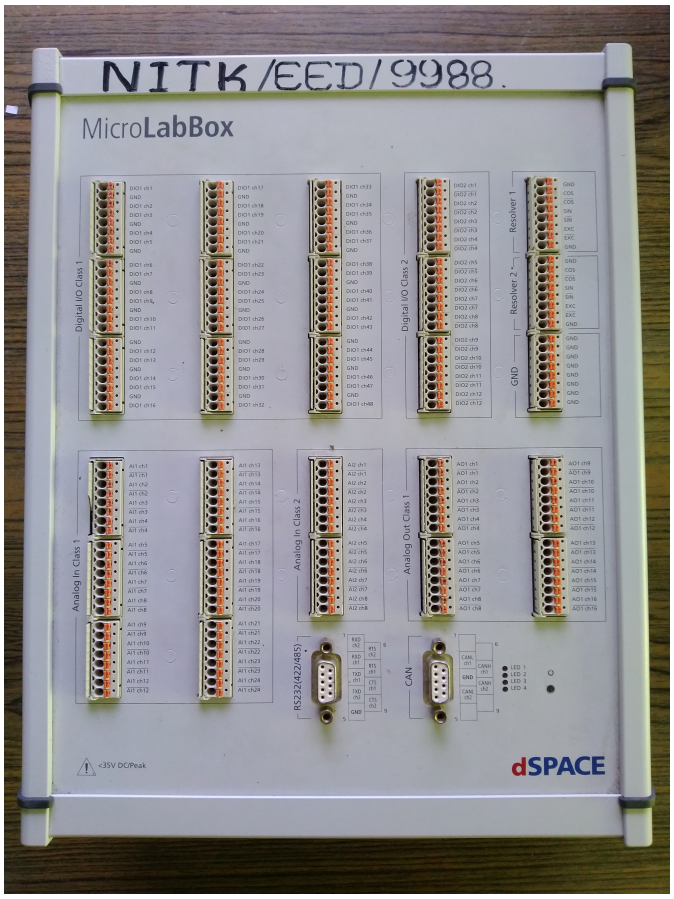


Figure 6.2: dSPACE MicroLab Box DS1202

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Publications based on the thesis

Paper in refereed journal

1. Roopa Viswadev, M. Arjun, V. V. Ramana, B. Venkatesaperumal and Sukumar Mishra, "A Novel AC Current Sensorless Hysteresis Control for Grid-tie Inverters," in *IEEE Transactions on Circuits and Systems II:Express Briefs (Early Access)(Accepted on December 2019)*

Papers published in referred conference proceedings

1. Roopa Viswadev, B. Venkatesaperumal, Arjun Mudlapur, Vanjari Venkata Ramana, and Sukumar Mishra. "Modified Hysteresis Current Control for Single Phase Solar Grid-tie Z-Source Inverter." in *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1-5. IEEE, 2018.

2. Roopa Viswadev, Vanjari Venkata Ramana, B. Venkatesaperumal, and Sukumar Mishra. "Real and reactive power control of solar grid-tie inverter under distorted grid conditions." *2018 International Conference on Power, Instrumentation, Control and Computing (PICC)*, pp. 1-6. IEEE, 2018.

3. Navami S.Prabhu, Roopa Viswadev, B. Venkatesaperumal, and Sukumar Mishra. "A Transformerless Photovoltaic Microinverter using High-gain Z-Source Boost Converter for Single-phase Grid connected Applications." In 2020 *IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, pp. 1-6. IEEE, 2020.

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Indian Patent

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