PULSE AMPLITUDE MODULATION CONTROL OF BLDC MOTOR USING BRIDGELESS SEPIC WITH COUPLED INDUCTORS

Thesis

Submitted in partial fulfilment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

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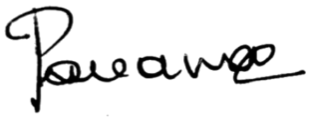

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CERTIFICATE

This is to certify that the Research Thesis entitled **Pulse Amplitude Modulation Control of BLDC Motor using Bridgeless SEPIC with Coupled Inductors** submitted by **Ms. Pavana** (Register Number: **148027EE14F09**) as the record of the research work carried out by her, is accepted as *the Research Thesis submission* in partial fulfilment of the requirements for the award of the degree of **Doctor of Philosophy**.

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Abstract

This thesis presents a novel approach for the control of brushless direct current (BLDC) motor using pulse amplitude modulation (PAM) control of voltage source inverter (VSI). The PAM control of VSI is accomplished by using a one-cycle controlled bridgeless single ended primary inductance converter (SEPIC) with coupled inductors. The PAM control also known as DC link voltage control of VSI, reduces switching losses by allowing the operation of VSI at fundamental frequency. The adoption of the coupling between the input and output side inductors in the bridgeless SEPIC converter reduces the value of the inductance required, allows better integration of magnetic components and hence lowers the overall size compared to conventional bridgeless SEPIC.

In the work presented in this thesis, the design of coupled inductors for the bridgeless SEPIC is done using the split winding scheme. The conventional method of achieving the desired coupling by adjusting the air-gap is tedious. Using the split winding scheme, a mathematical approach is proposed to obtain the closed form solution for distribution of windings over three limbs of E-core to achieve the desired coupling. The bridgeless SEPIC with coupled inductors is designed to get a wide variation of DC link voltage and is operated in discontinuous conduction mode (DCM) for the complete range of DC link voltage. The DCM operation simplifies power factor correction (PFC) control scheme to a voltage mode control, since it has inherent input current shaping feature. One-cycle control technique which is a nonlinear control technique, applied in the voltage mode scheme improves the quality of supply current by reducing the distortion compared to proportional-integral (PI) control technique. The one-cycle control also enhances the performance of DC link voltage control, with improved start-up and transient state response.

The proposed BLDC motor drive is modelled. The superiority of one-cycle control technique over PI control for a wide range of speed control is validated using simulation results. Using the laboratory prototype of bridgeless SEPIC with coupled inductors, the achievement of supply current shaping and adjustable speed in the BLDC motor drive is verified experimentally using field programmable gate array (FPGA) based digital PI controller.

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List of Abbreviations

AC	Alternating Current
BLDC	Brushless Direct Current
CCM	Continuous Conduction Mode
CF	Crest Factor
DBR	Diode Bridge Rectifier
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCVM	Discontinuous Capacitor Voltage Mode
DICM	Discontinuous Inducor Current Mode
EMI	ElectromagneticInterference
FPGA	Field Programmable Gate Array
GND	Ground
IAE	Integral Absolute Error
ISE	Integral Square Error
ITAE	Integral Time Absolute Error
ITSE	Integral Time Square Error
OCC	One Cycle Control
PAM	Pulse Amplitude Modulation
PFC	Power Factor Correction
PI	Proportional Integral
PM	Permanent Magnet
PQ	Power Quality
PWM	Pulse Width Modulation

SEPIC	Single Ended Primary Inductor Converter
SLMC	Sliding mode control
VSI	Voltage Source Inverter
THD	Total Harmonic Distortion

List of Nomenclature

α	Steinmetz coefficient for frequency
a	Area of cross section of winding
a_i, a_o	Area of cross section of input and output side inductors
A_e	Area of cross section of core
A_P	Area Product
A_w	Area of cross section of window
β	Steinmetz coefficient for flux density
B_{CI}	Flux density of coupled inductors
B_i	Flux density of input side inductor
B_o	Flux density of output side inductor
B_{SI}	Total flux density of input and output side inductors
B_m	Maximum flux density
C_1, C_2	Intermediate Capacitors of Bridgeless SEPIC
C_{Core}	Cost of core
C_{Copper}	Cost of copper
C_d	DC link Capacitor
δ	skin depth of the winding
D	Duty Ratio
D_1, D_2	Fast switching Diodes of Bridgeless SEPIC
D_p, D_n	Rectfier Slow Diodes
E	Energy handling capability of the core
E_{on}	Switching energy loss during turn-on
E_{off}	Switching energy loss during turn-off

e_{an}, e_{bn}, e_{cn}	Stator back emf voltages
f_l	Line frequency
f_r	Resonance frequency
f_s	Switching frequency
I	RMS value of current through winding
I_{av}	Average current through the switching device
I_{Crms}	RMS value of current through capacitance
I_{rms}	RMS current through the switching device
$I_{(av)}$	Average value of current through winding
i_a, i_b, i_c	Stator phase currents
i_{Li1}, i_{Li2}	Input side Inductor currents
i_{Lo1}, i_{Lo2}	Output side Inductor currents
I_{ip}, I_{op}	Peak currents through input and output side inductors
I_{mp}	Peak current through magnetising inductance
i_s	Supply Current
i_{D1}, i_{D2}	Diode currents
I_{dc}	DC link current
i_{sw1}, i_{sw2}	Switch currents
i_{swmax}	Maximum current through switch
J	Current density
H_a, H_b, H_c	Hall sensing signals
k_c	Coupling coefficient
K_c	Crest factor
K_e	Back EMF constant
K_F	Multiplication factor for winding voltage shape
k_i	Integral gain for speed control loop
k_{iv}	Integral gain for voltage control loop
k_p	Proportional gain for speed control loop
k_{pv}	Proportional gain for voltage control loop
K_t	Torque constant

k_v	voltage constatnt of BLDC motor
K_w	Window factor
l	length of the winding
L_a, L_b, L_c	Stator phase inductances
L_{ph}	Stator phase inductance value
L_f, C_f	Filter Inductor, Filter Capacitor
L_i	Input side self-inductance
L_{i1}, L_{i2}	Input side Inductors
L_o	Output side self-inductance
L_{o1}, L_{o2}	Outut side Inductors
L_m	Magnetising inductance
L_s	Stator winding inductance per phase
M	Mutual inductance
N	Speed in RPM
n_{11}, n_{1C}, n_{12}	Number of turns of input inductor over E core
n_{21}, n_{2C}, n_{22}	Number of turns of output inductor over E core
N_i	Total number of turns of input inductor
N_o	Total number of turns of output inductor
N_e	Speed error in RPM
N^*	Reference speed in RPM
N_{max}	Maximum speed in RPM
P	Number of poles
P_C	Conduction loss
$P_{C(esr)}$	Conduction loss in ESR of capacitance
P_{Co}	Core loss
P_{Cu}	Copper loss
P_{SW}	Switching loss
ρ	Resistivity of the winding
$\Re_1, \Re_C, \Re_2, \Re_{den}$	Reluctance matrices
R_a, R_b, R_c	Stator phase resistances

R_{ac}	AC resistance of the winding
R_{dc}	DC resistance of the winding
R_C	Effective Series Resistance (ESR)
R_{on}	On-state resistance of switching device
R_{ph}	Stator phase resistance value
$S_1, S_2, S_3, S_4, S_5, S_6$	Switches of VSI
SW_1, SW_2	Switches of bridgeless SEPIC
T_e (T, T_{max})	Electromagnetic torque (Average, Maximum value)
v_{an}, v_{bn}, v_{cn}	Stator phase voltages
V_{core}	Volume of core
V_{copper}	Volume of copper
V_{dc}	DC link voltage
V_{dc}^*	DC link voltage Referenc
V_{cc}	Control voltage
V_e	Error voltage
v_{D1}, v_{D2}	Diode voltages
V_{on}	On state voltage of switching device
v_s	Supply Voltage
v_{sw1}, v_{sw2}	Switch voltages
ω	Speed in rad/sec
ω^*	Speed Reference in rad/sec
W_{Core}	Weight of core
W_{Copper}	Weight of copper
ϕ_1, ϕ_C, ϕ_2	Flux over E core

Chapter 1

Introduction

1.1 Introduction

The research work on Pulse Amplitude Modulation (PAM) control based brushless direct current (BLDC) motor drive using one cycle controlled bridge-less SEPIC with coupled inductors is presented in this thesis. The background of the research, and the motivation for the present research are discussed in this chapter. The objectives formulated for the research work are presented. Finally, the chapter wise organization of the thesis is also discussed.

1.2 Research background

The rising living standards and extreme climatic conditions demand sophisticated household equipments like air conditioniner, refrigerators etc. In appliances like air-conditioning systems, the compressor motor and its control play major role in electricity consumption. The utilization of the conventional on/off control based single phase induction motor for compressor leads to high energy consumption (Ching, 2008). This necessitates the development of energy efficient compressor systems with high-efficiency compressor motors associated with adjustable speed control techniques. The BLDC motor is drawing attention in adjustable speed drives in the recent market due to its significant advantages like high efficiency, high power density, low maintenance, and high torque inertia ratio (Michael et al., 2017).

The BLDC motor is a three-phase synchronous motor having a back emf pattern of trapezoidal nature. The commutation in BLDC motor is achieved electronically using a three-phase voltage source inverter (VSI). The rotor position sequence determines the switching pattern for the operation of VSI. The rotor position information at 60^0 intervals is sufficient due to the trapezoidal nature of back emf; this reduces the computations required for the controller (Xia, 2012). The speed control of BLDC motor can be achieved by controlling the VSI output voltage supplied to the BLDC motor, either by pulse width modulation (PWM) control of VSI, where the switching pulse width for the VSI is controlled, keeping DC link voltage constant or by PAM control of VSI where the DC link voltage of VSI is controlled. Based on the approach of speed control, BLDC motor drives are categorised as PWM controlled BLDC motor drives and PAM controled BLDC motor drives.

1.2.1 PWM controlled BLDC motor drive

Conventional PWM controlled BLDC motor drive comprises of a diode bridge rectifier supplied from a single phase main, feeding a fixed DC link voltage to the three-phase VSI connected to the BLDC motor as shown in Figure 1.1. In this case, the voltage at the DC link is constant due to the uncontrolled rectifier. Also, the speed control of BLDC motor is achieved using PWM control of VSI. PWM control method uses speed and motor current control loops to generate pulse width modulated switching signals for VSI. It has several disadvantages like increased cost due to the requirement of motor current sensors, high-frequency switching losses in VSI, complicated control design and a highly distorted supply current with low power factor.

In order to improve the quality of supply current, it requires a power factor correcting circuit at the front end. The supply current shaping is commonly achieved by appropriately controlling the DC-DC converter following the diode bridge rectifier, as shown in Figure 1.2. The duty ratio of the DC-DC converter needs to be modulated to obtain supply current in phase with supply voltage. This necessitates increased sensing and control requirements of the overall circuit for the BLDC motor drive.

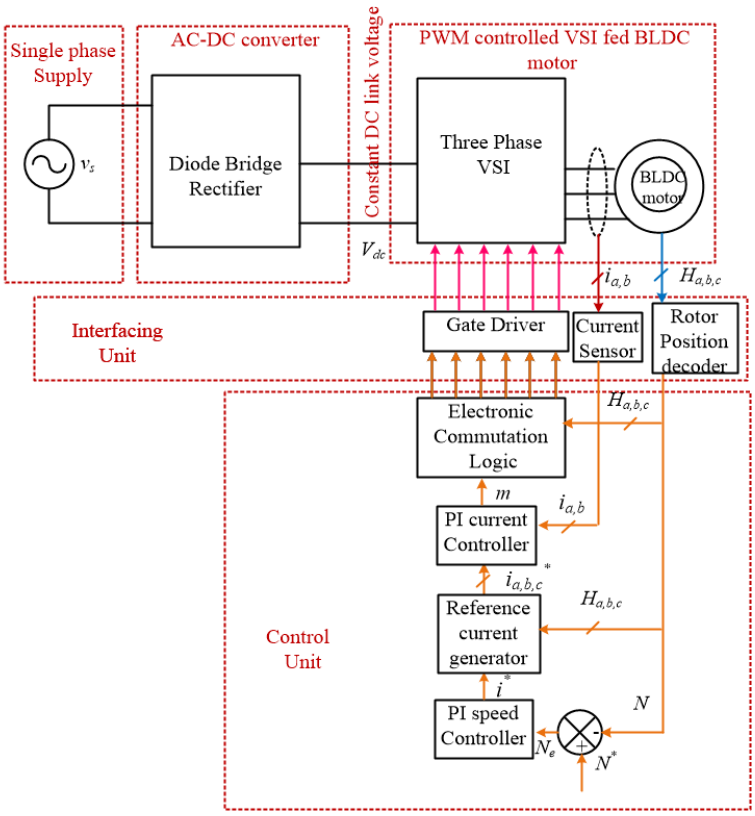


Figure 1.1: Conventional PWM controlled BLDC motor drive

1.2.2 PAM controlled BLDC motor drive

The simplest and more efficient approach to control speed with improved quality supply current is to operate three-phase VSI at fundamental frequency and control the DC link voltage proportional to the speed (Krishnan, 2009). The BLDC motor drive employing this approach is commonly described as PAM controlled BLDC motor drive. In this approach, the control of DC link voltage is achieved using a DC-DC converter with variable output voltage.

The conventional PAM controlled BLDC motor drive is shown in Figure 1.3. The system is supplied from single phase mains, and has two stages of conversion at the front end namely power factor correction converter and DC -DC converter with wide range of output voltage. Such arrangement with two-stage front-end circuit to supply variable DC voltage and also to improve quality of input current is illustrated and analyzed in (Orabi and Ninomiya, 2003). In the work presented in the paper, separate controllers are

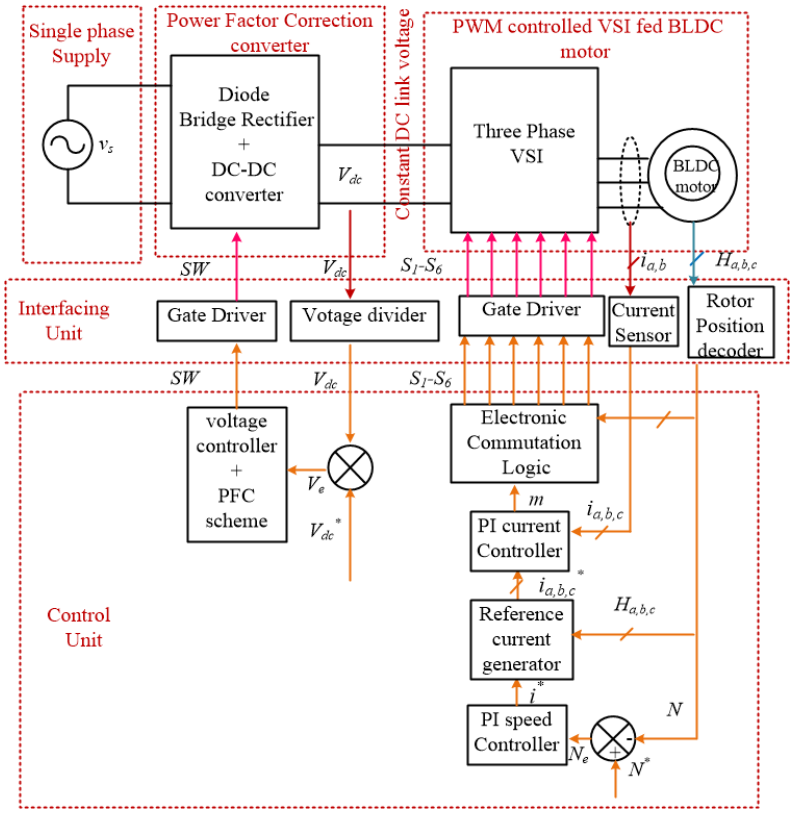


Figure 1.2: PWM controlled BLDC motor drive of improved quality supply current

required for two front end DC-DC converters which increases number of components and hence, size of the motor drive.

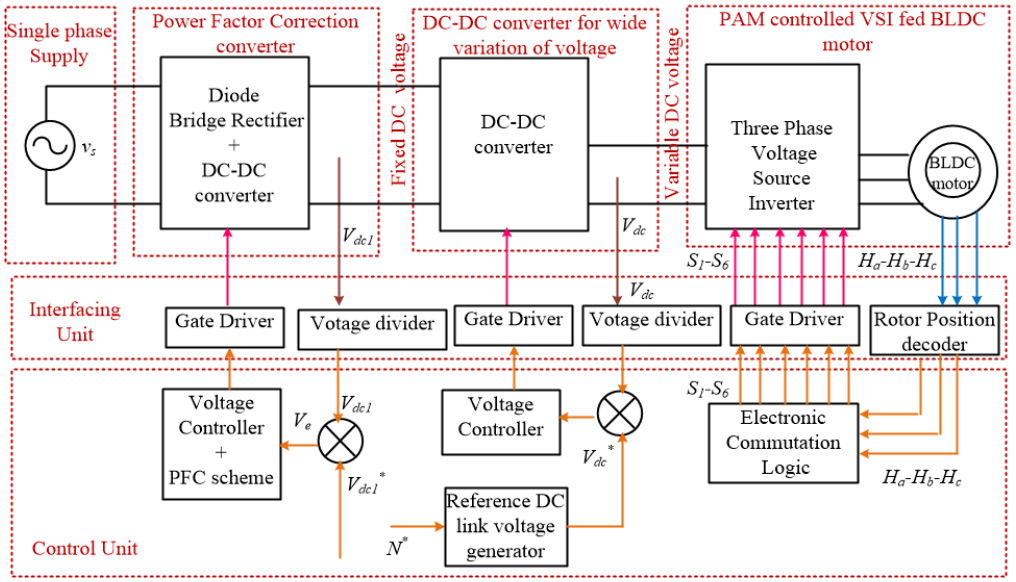


Figure 1.3: Conventional PAM controlled BLDC motor drive with two-stage front end circuit

The drawback of conventional PAM controlled BLDC motor drive with two-stage front end circuit can be over come if two stage front end circuit is replaced by a single stage front-end circuit which can provide wide variation of dc link voltage and improved input current shaping. Such a conventional PAM controlled BLDC motor drive with single-stage front end circuit is shown in Figure 1.4. Comparatively, this system minimizes the complexity in the power and control circuit at the front end for BLDC motor drive.

1.3 Research Motivation

In order to achieve superior accomplishment of PAM controlled BLDC motor drive in terms of size, cost and efficiency, it is necessary to choose the appropriate converter topology for the power factor correction converter. It is also important to adopt simple and efficient control technique for DC link voltage control and supply current shaping.

The converter topologies capable of providing wide range output voltage can serve the dual purpose of both DC link voltage control for PAM controlled BLDC

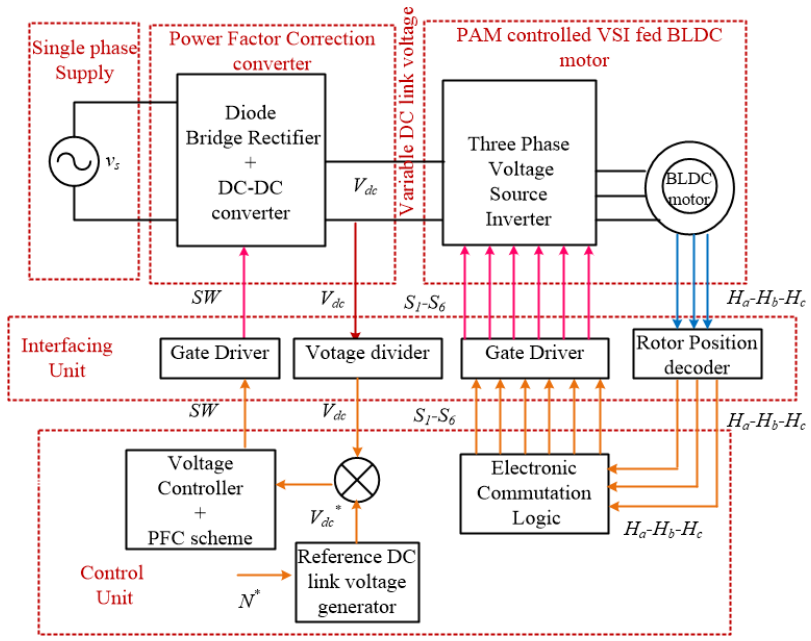


Figure 1.4: Conventional PAM controlled BLDC motor drive with single-stage front end circuit

motor drive and power factor improvement. Only the converters of buck-boost category can supply both lower and higher range of voltages than input voltage. Hence, the PAM controlled BLDC motor drive supplied using buck-boost converter configurations provide more simplified and efficient front-end circuit. Deciding the suitable converter configuration from buck-boost category and augmenting it to get improved features is the motivation for the research work.

Identifying the suitable control technique for enhancing the performance of the PAM controlled BLDC motor drive is another research motivation. The control scheme for the front-end converter to obtain power factor correction depends on its mode of operation. If the converter is operated in discontinuous conduction mode (DCM), it provides inherent power factor correction. Hence eliminates the need of inner current control loop as required in converters operating in continuous conduction mode (CCM) for power factor correction. Therefore the converter operating in DCM can adopt simple voltage follower control, which requires sensing of only a DC link voltage. Linear proportional-integral (PI) controller used for DC link voltage control, may not perform satisfactorily under parameter variation, non linearity, load disturbance, etc. This de-

mands sophisticated control technique for voltage mode control.

1.3.1 Converter topologies for PAM controlled BLDC drive

The buck-boost configurations commonly used for power factor correction application are buck-boost, Cuk converter, Zeta and the Single Ended Primary Inductance Converter (SEPIC) (García et al., 2003). The buck-boost and Cuk converters have the limitation of negative output voltage polarity and whereas the Zeta converter has the switching device placed in series with the supply, which leads to higher EMI issues (Singh et al., 2011). Hence the SEPIC converter configuration is preferred due to its positive polarity output voltage and lower EMI issues. Improved efficiency can be obtained using a bridge-less counterparts of converters due to reduction in conduction losses in rectifier diodes.

1.3.2 Control technique for PAM controlled BLDC drive

The PAM control is achieved by duty ratio modulation of bridge-less SEPIC converter using voltage mode control. The conventional PAM control unit involves generation of the reference DC link voltage by multiplying the reference speed with the motor voltage constant (Bist et al., 2015), (Singh and Vashist, 2013). The generation of the reference DC link voltage using the outer speed control loop is required for accurate speed control. The conventional PI controller employed in the inner voltage control loop exhibit poor performance, causing transient oscillations and large peak overshoots under parameter variation, load disturbance etc. This demands for sophisticated control technique for DC link voltage control.

1.4 OBJECTIVES OF THE RESEARCH WORK

This research work focuses on identifying the best solution in the perspective of front end converter topology and control technique for the speed control of BLDC motor using PAM control of VSI. The main objectives proposed for the research work are given below. The objectives are represented in overall block diagram of proposed sytem shown in Figure 1.5.

1. Design, analysis, and implementation of laboratory prototype of bridgeless SEPIC converter with coupled inductors.

2. Study and implement PAM controlled BLDC motor drive using one cycle controlled bridgeless SEPIC with coupled inductors and compare the performance with PI controlled bridgeless SEPIC with coupled inductors.

3. FPGA based experimental evaluation of BLDC motor drive fed from bridgeless SEPIC with coupled inductors.

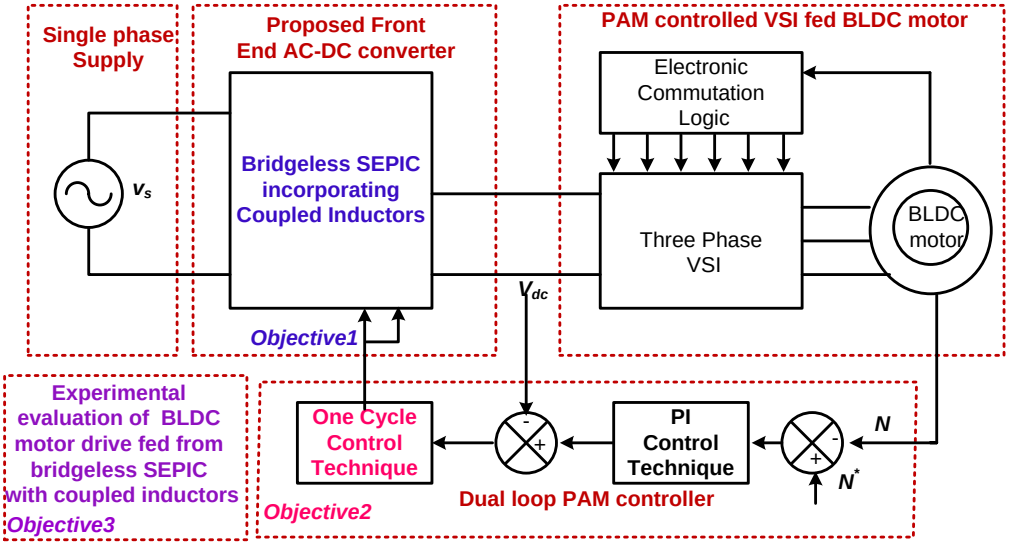


Figure 1.5: Research proposal

This work presents bridgeless SEPIC with coupled inductors controlled by one-cycle control technique for the PAM control-based BLDC drive. Incorporation of coupled inductors in SEPIC converter results in compact size, reduced cost, improved efficiency along with the advantages of possessing only one low side gate driver and the absence of capacitive coupling loop. The SEPIC converter is designed to operate in DCM and hence eliminates the need for inner current control loop. One-cycle control adopted in DC voltage control loop achieves better control performance over a wide speed range, along with improving the quality of current drawn from the supply.

1.5 THESIS ORGANISATION

This thesis includes six chapters and appendix as described below.

Chapter 1: This chapter presents a brief introduction to the research work carried out. The research background, motivation for the work and objectives framed to carry out the research work are discussed. Finally, the oraganisation of the thesis is given.

Chapter 2: This chapter focuses on the literature survey on adjustable speed BLDC motor drive. The different methods of speed control are reviewed. Different converter topologies and control techniques for PAM controlled BLDC motor drive are studied. The limitations in existing converter topologies and control techniques are identified and improved converter topology and control technique is proposed for PAM controlled BLDC motor drive.

Chapter 3: This chapter discusses the design and analysis of bridgeless SEPIC converter with coupling for the wide variation of output voltage and inherent supply current shaping. The selection of components based on voltage and current ratings of the converter is discussed. The design of coupled inductors using split winding scheme for the bridgeless SEPIC is illustrated. The comparison of volume, weight, cost, and efficiency of the converter with and without coupling for the same rating is given. The performance of the converter with coupling is evaluated using MATLAB/Simulink simulation.

Chapter 4: In this chapter, the PAM controlled BLDC motor drive using one cycle controlled bridgeless SEPIC converter with coupling is explained. The dual loop speed controller with an outer speed control loop and the inner voltage control loop is described. The performance of dual-loop PAM control based BLDC motor drive with PI and one cycle control employed in the voltage control loop is evaluated using simulation carried out in MATLAB/Simulink. Also, the adequate performance of the dual loop controller in a real-time system is evaluated using the co-simulation feature of the FPGA digital controller.

Chapter 5: This chapter deals with the hardware implementation of the BLDC motor drive fed from bridgeless SEPIC with coupled inductors. The experimental results of PI controlled bridgeless SEPIC with coupled inductors for resistive load and BLDC motor drive is presented.

Chapter 6: Summarizes the major contributions and conclusions of the research work. It also includes some discussions on scope for future work.

Chapter 2

Literature review

2.1 INTRODUCTION

In this chapter, the literature survey on speed control of BLDC motor is presented. The block schematic depicting the literature survey on the research area highlighting the prominent subareas of the work is shown in Figure 2.1. The literature survey on PWM controlled BLDC motor drive and PAM controlled BLDC motor drive is presented. The literature review on converter topologies and control strategies for PAM controlled BLDC motor drive is given. The literature on utilisation of coupled inductor concept for reducing the size and cost of the converter and one cycle control strategy for minimising the control complexity are discussed.

2.2 PWM CONTROLLED BLDC MOTOR DRIVE

As discussed in chapter 1, conventional PWM controlled BLDC motor drive comprises of three-phase VSI fed BLDC motor supplied through a diode bridge rectifier from sigle phase mains. The increased electromagnetic interference and power quality issues in this method need to be addressed according to the international standards of power quality. Improving power quality with the minimum cost and lesser circuit complexity becomes important. The passive filters increase size and power losses. Active filter circuit at the input stage is more effective, efficient and a economic approach (Consoli et al., 2004). The additional circuit and control requirement at the front end increases circuit complexity. Few attempts have been made by researchers in order to

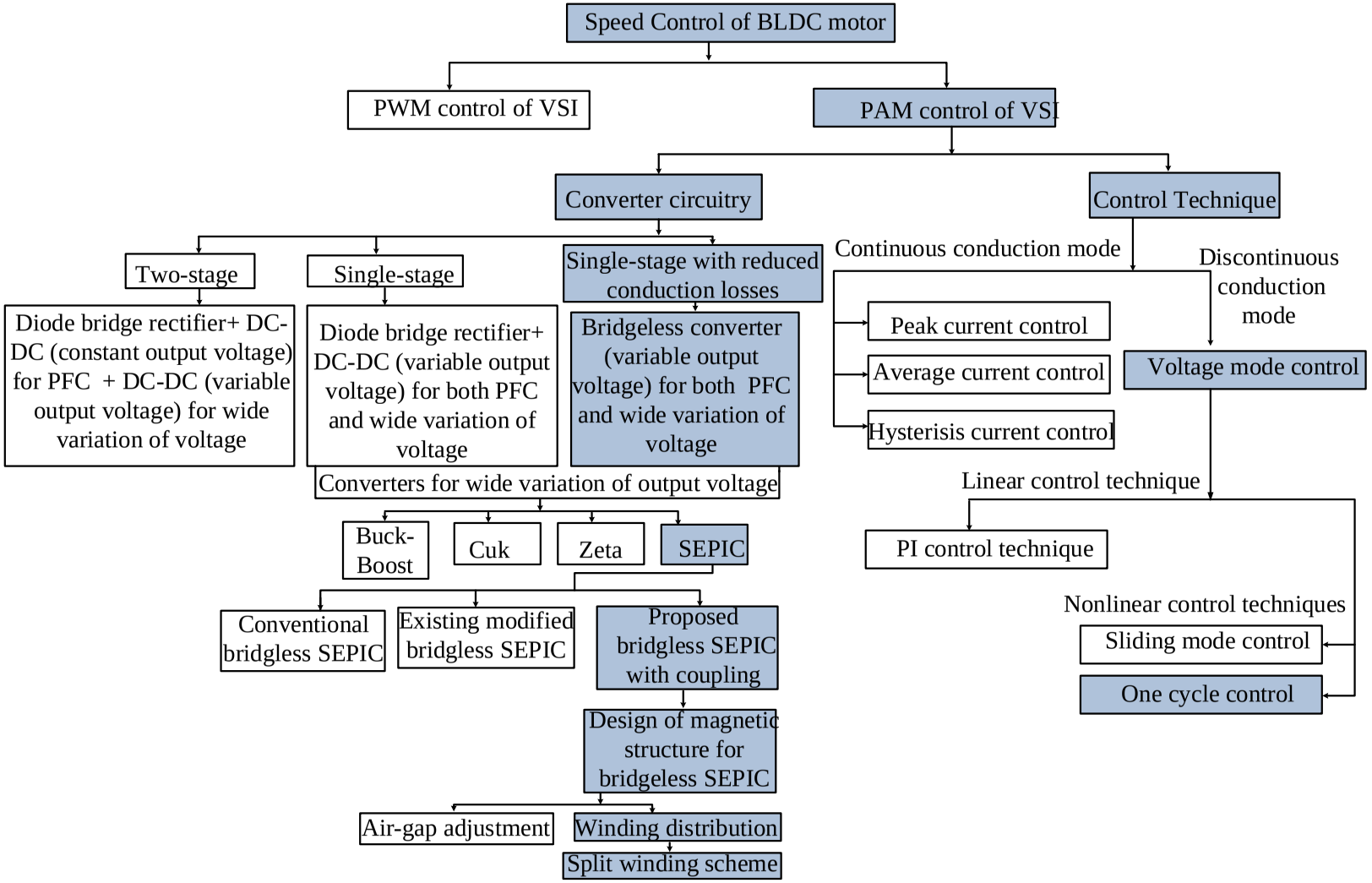


Figure 2.1: Block schematic of literature survey

simplify complications involved in power circuit and control strategies used in PWM controlled BLDC motor drives.

To reduce the number of components involved in overall drive, unified converter topologies are studied (Lee, B. et al. 2001), where single phase AC to DC and DC to three phase AC operations are performed by a single converter. The power factor correction and the speed control are achieved with such unified converter topology. However, the PWM generation becomes complicated due to merged control characteristics.

The BLDC motor drive with unipolar switching of three phase VSI is used by Gopalarathnam and Toliyat (2003) to reduce number of switching devices. The DC-DC SEPIC converter is used to perform power factor correction. Unipolar excitation limits the current conduction to only one direction and hence, the motor windings are poorly utilised. So it is not recommended to use unipolar excitation for BLDC motors beyond 300 W power rating (Gopalarathnam and Toliyat, 2003).

An attempt is made to reduce sensing requirement using direct torque control method for PWM generation of three phase VSI by Ozturk et al. (2007). Only two phase currents are sensed for direct torque control implementation. But this control strategy involves complicated computations which limits its usage.

Dual mode control for PFC and speed control is developed (Wu and Tzou, 2009), where control need to switch between PWM control of inverter and PAM control of inverter to avoid high switching frequency operation at lower speeds. However, this brings more complexity in control. The PFC converter configuration uses additional MOSFET and a diode.

The literature study on PWM control of VSI reveal that the unavoidable high frequency switching losses in three phase VSI reduce the efficiency of the drive. The alternatives used to increase efficiency could not reduce complexity involved in the control circuit.

2.3 PAM CONTROLLED BLDC MOTOR DRIVES

The significance of PAM controlled permannent magnet BLDC motor drives has been evaluated by Isao Takahashi et.al (1994). The utilisation of a step-down chopper circuit to obtain near unity power factor and DC link voltage control was verified (Takahashi et al., 1994). This drive does not work when desired dc link voltage is higher than the supply voltage.

A performance comparison of the PWM controlled and PAM controlled BLDC motor drives for sensorless operation is presented by Kim and Youn (2002), and it is found that the PAM controlled drive gives more stable operation. However, this paper presented buck chopper circuit itself for the PAM control.

Schwager et al. (2013), presented modeling of machine and converter losses of buck chopper based PAM controlled synchronous motor drive for comparison of efficiency with PWM controlled motor drive and results show that PAM produces a higher overall efficiency.

The power quality improvement of permanent magnet BLDC motor driven air-conditioner using a boost converter at the front-end is proposed, which is also used to perform PAM control of VSI (Sanjeev and Bhim, 2009). Here, the range of voltage variation is limited to the voltage higher than the supply voltage.

The effciency comparison of BLDC motor drive with PWM and PAM controllers is dealt using boost converter based front-end circuit (Yen-Shin et al., 2007). Improved efficiency is observed for PAM control technique. However, the shortcoming of limited variation of output voltage of the boost converter based front-end circuit calls for a second stage using flyback or forward converter for the control of output voltage over a desired range.

A single-stage circuit with converters of step up-down capability to obtain the variation of output voltage over a wide range along with power factor correction is shown to be to be favourable for PAM controlled BLDC motor drive in (Singh and Singh, 2010). In the work presented, Zeta converter is used for PAM controlled BLDC

motor drive which contributes to increased EMI issues owing to the placement of the switch in series with the supply.

Another significant converter with wide-range output voltage is Cuk, which can provide wide range of speed control with improved quality of supply current (Singh and Singh, 2012). This offers valuable features such as low-noise level, adaptation of integrated magnetics and capability of energy transfer through capacitors, etc. (Brkovic and Cuk, 1992). However, negative polarity output voltage limits the frequent use of the converter.

Alternate best option with positive polarity output voltage and low EMI for AC-DC conversion is SEPIC converter. Optimally designed SEPIC converter can offer the following benefits like fast dynamic response, improved power quality with low value of crest factor, low total harmonic distortion of input current and high-power factor along with reduction in size (Sebastian et al., 1998). PAM controlled BLDC motor drive using SEPIC DC-DC converter following a diode bridge is presented by (Sanjeev and Singh, 2010).

The conventional front-end circuit configuration, consisting of a diode bridge followed by a DC-DC converter, is getting replaced with bridgeless configurations in the recent years. The bridgeless topologies ensure the improved efficiency of single-stage front-end circuit compared to diode-bridge counterparts due to reduction in conduction losses. The researchers have presented bridgeless configurations of buck-boost, CUK, Zeta and SEPIC for PAM controlled BLDC motor drive.

Improved power quality is achieved using buck-boost with wide range of DC link voltage in PAM-controlled BLDC motor drive (Bist and Bhim, 2013). As the buck-boost converter has negative output voltage polarity, it imposes difficulty during implementation of control circuit.

Reduction in conduction losses is achieved for PAM controlled BLDC motor drive using bridgeless CUK compared to use of DC-DC CUK following diode bridge (Bhim and Bist, 2013). However, the complexity due to negative polarity of output voltage

persists.

The bridgeless Zeta is also presented by Singh and Vasisht (2013), to provide improved efficiency with positive polarity output voltage for PAM controlled BLDC motor drive. However, it endures higher EMI issues.

The conventional configuration of bridgeless SEPIC converter is presented in (Bist et al., 2015) for PAM control of BLDC motor. With this topology, there is a reduction in the conduction losses and the size. However, number of components of the converter will be increased compared to bridge rectifier connected SEPIC for PAM control. Since the conventional bridgeless configuration for SEPIC increases the number of elements, it draws attention towards reducing the component count by some topological alterations, retaining its positive features.

2.4 BRIDGELESS SEPIC TOPOLOGIES

Bridgeless SEPIC converter is highly preferred single-stage front end AC-DC converter for applications requiring a wide variation of DC voltage due to its adaptibility to improve performance in terms of the quality of supply current. Conventional bridgeless SEPIC topology shown in Figure 2.2 consists of two DC-DC SEPIC converters to operate during positive and negative supply cycles through the rectifier diodes (D_p, D_n) (Bist et al., 2015).

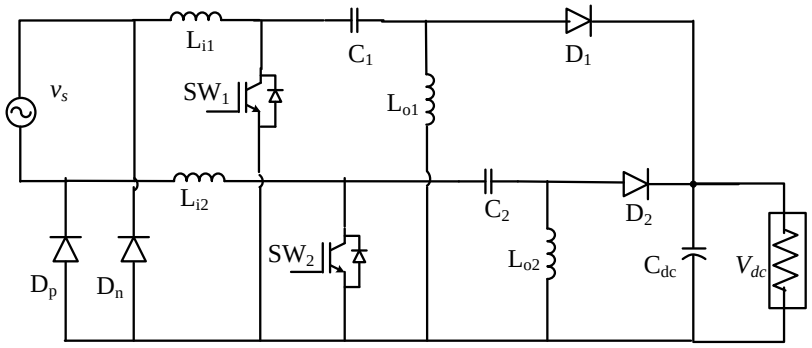


Figure 2.2: Conventional bridgeless SEPIC converter

The researchers have attempted several modifications for bridgeless SEPIC in order to reduce the number of components and hence the size. Few modified bridgeless

SEPIC topologies present in the literature are shown in Figure 2.3.

Figure 2.3 (a) shows bridgeless SEPIC rectifier with unity power factor and reduced conduction losses proposed by Ismail (2009). This bridgeless SEPIC topology has only three inductors, but it requires an additional gate drive transformer. The number of capacitors is increased and the structure is more complex with load floating between two capacitors as shown in Figure. 2.3 (a). Although the number of inductors is reduced, this topology suffers from increased complexity in the structure.

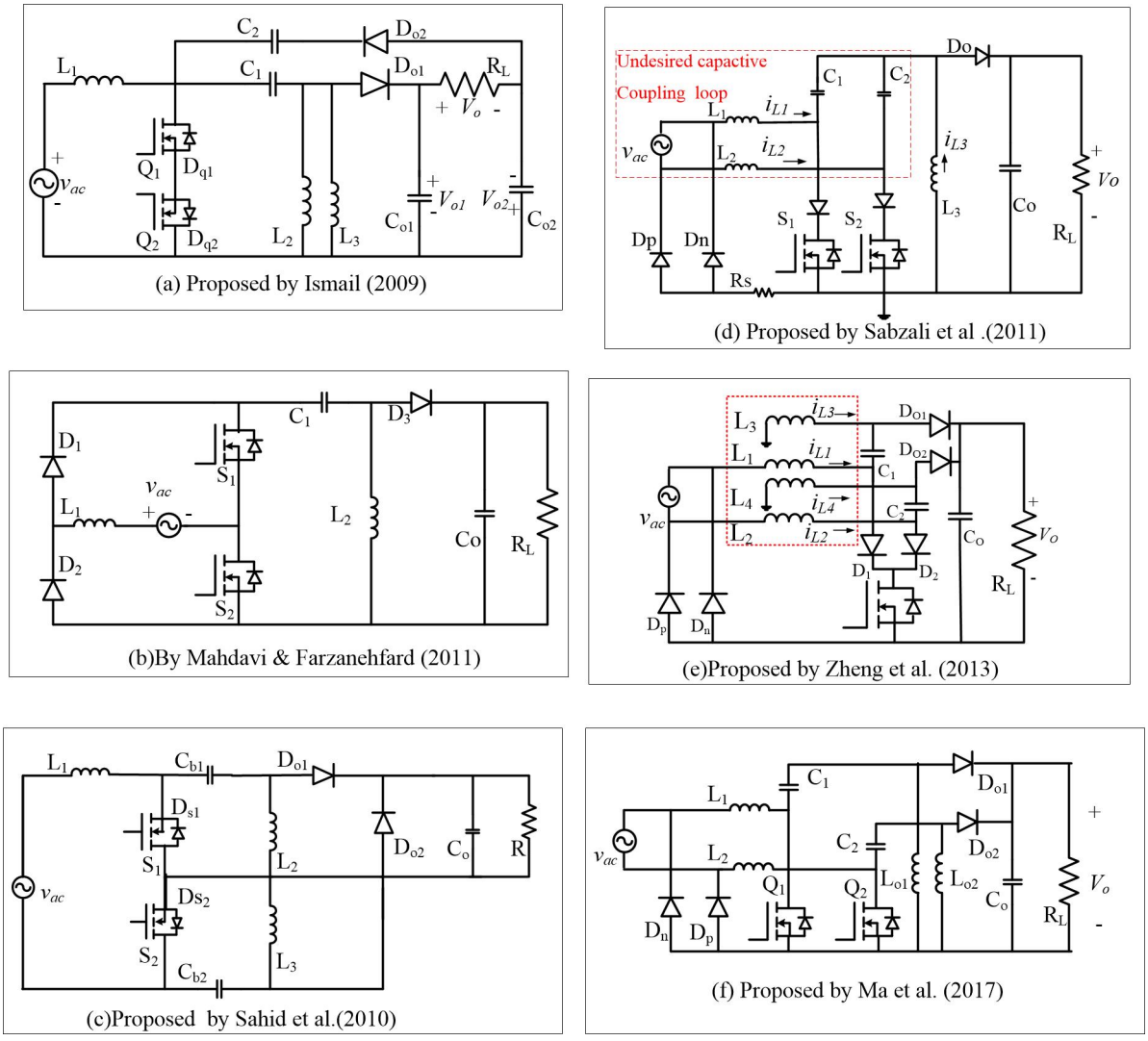


Figure 2.3: Existing bridgeless SEPIC topologies

Figure 2.3 (b) shows bridgeless SEPIC rectifier with reduced number of components and thereby reduction in conduction losses proposed by Mahdavi and Farzaneh-

fard (2010). However, this topology demands for high side additional gate drive circuitry.

Figure 2.3 (c) shows the new AC-DC converter using bridgeless SEPIC proposed by Sahid et al. (2010). In this system, number of inductors are reduced and driving the switch is simpler since both the source terminals of the switch are connected to ground potential and so does not require high side driver (Sahid et al., 2010). But this topology would be only suitable to be used as a switch mode regulated power supply for low power equipments.

The bridgeless SEPIC topology shown in Figure 2.3 (d) with a reduced number of inductors, using only one low side gate driver introduced by Sabzali et al. (2011), is observed to suffer with circulating current due to the capacitive coupling loop as discussed in Ma et al. (2017).

An improved bridgeless SEPIC PFC rectifier with optimized magnetic utilization, minimized circulating losses, and reduced sensing noise proposed by Zheng et al. (2013) is shown in Figure 2.3 (e). This work has presented the incorporation of coupled inductors in the SEPIC topology operating in CCM. Hence it requires sensing of the current for inner current control loop. The magnetic design of four inductors over same core suggested in the work is hard to implement.

An improved bridgeless SEPIC converter without circulating losses and input-voltage sensing is proposed by (Ma et al., 2017) as shown in Figure 2.3 (f). The requirement of supply voltage during CCM mode of operation of converter is avoided using UCC28019 control IC. However, the inductor current sensing for control implementation along with sensing of the output voltage is indispensable.

The limitations in the existing topologies demand a bridgeless SEPIC topology which can provide all the following features like (i) compact size, (ii) reduced structural complexity (iii) no requirement of extra/high side gate driver circuitry, (iii) no circulating current, due to the capacitive coupling loop (iv) elimination of inner current control loop. This motivated the research work to arrive at the toplogical improvisation

for the conventional bridgeless SEPIC.

2.4.1 Incorporation of coupled inductors feature for bridgeless SEPIC

The feature of the coupling of the inductors with identical voltage waveforms in a switching converter is introduced for the Cuk converter in (Cuk, 1983). In the work done by Cuk (1983), two windings are integrated into a single magnetic circuit to obtain a similar performance possible with inductors having self-inductance values equal to the effective value of inductance in the integrated circuit.

The reluctance models and mathematical approach on controlling the leakage inductance of windings to obtain the desired ripple current magnitude is presented by Zhang (1987). The effect of sensitivity due to residual ripple for adequate tuning of the coupling coefficient is also described. The inevitable error caused due to residual ripple requires further research.

The possibility of reducing the weight, size and cost of the magnetic content of converters due to coupling, without compromising the performance of the converter is highlighted by Slobodan (1983).The complex analytics involved are simplified by considering only first order effects.

The use of coupled inductors to obtain the same performance with reduced size in the DC-DC SEPIC converter used for the power factor correction application is presented in (Spiazzi and Rossetto, 1994). From the work presented, it is noticed that there is no closed form solution for the magnetic circuit design.

The analysis of the effect of the coupling coefficient on the current ripple in the SEPIC circuit is detailed in (Di Capua and Femia, 2014). The work investigated the correlation existing among the size of intermediate capacitor, the coupling coefficient, the voltage conversion ratio, and the ripple current magnitude. The sensitivity of ripple current with changing coupling coefficient is addressed along with variation of intermediate capacitance of SEPIC topology. The work was presented for low power DC-DC power conversion.

The DC-DC SEPIC with coupled inductors is used in a three-phase power fac-

tor correction circuit (Foroozeshfar and Adib, 2018). The magnetic design and implementation of coupled inductors to meet desired converter performance by tuning the coupling coefficient is not detailed in the paper.

Conventionally, the coupled inductors are designed by placing both the windings on the same bobbin and then correctly adjusting the air gap between the two windings of the inductors that are to be coupled. Practically, it is a very challenging task to adjust the gap length to fine-tune the coupling coefficient.

Wong et al. (2001) presented a reluctance model design approach using EI core for interleaving voltage regulator modules. Achieving the desirable ripple by winding the inductors over two side limbs is given.

The other approach to build coupled inductor is to use the method of the distribution of windings over side and centre limbs of an E-core as suggested by Chen and Lai (2015). But, closed form solution for distribution over three limbs is not given.

The split winding design method using the distribution of windings over all three legs of an E-core is presented for interleaved converters by Zheng et al. (2008). There exists, equality of inductors coupled in interleaved converters and simplifies reluctance model.

In the work proposed in this thesis, for the SEPIC converter, inductors of different values at input and output sides are coupled. The reluctance model, and mathematical approach to arrive at closed form solution for the design of coupled inductors is one of the main contribution of this thesis.

2.5 CONTROL TECHNIQUES FOR PAM CONTROLLED BLDC DRIVE

The PAM control unit consists of DC link voltage control loop to obtain adjustable speed ($N \propto V_{dc}$) of BLDC motor. In a conventional PAM controlled BLDC motor drive, the generation of the reference DC link voltage is done by multiplying the reference speed with the motor voltage constant ($V_{dc}^{*} = k_v \times N^{*}$) (Bist et al., 2015; Singh and Vashist, 2013). However, with this approach the actual speed may not match the reference speed, because the DC link voltage for BLDC drive is also a function of load

torque and motor winding parameters such as resistance and inductance.

(Singh and Singh, 2010) presents a rate limiter in PAM control unit to incorporate the effect of winding parameters. This is useful to limit the rate of rise of current drawn from dc link during the transient state.

The incorporation of effect of load torque, motor winding resistance and inductance for generation of reference DC link voltage, in the PAM control unit for modified bridgeless SEPIC fed BLDC motor drive is presented in (Lin and Tzou, 2014). An equation incorporating the effect of motor winding parameters and the dc link current corresponding to load torque is presented in (Ho et al., 2015) for obtaining the reference DC link voltage.

The speed control can be achieved precisely, if the reference DC link voltage is generated with outer speed control loop as discussed in (Yadav et al., 2016), (Kim and Youn, 2002). Hence, the generation of the reference DC link voltage using the outer speed control loop is required for accurate speed control.

From the literature survey, it is noticed that adoption of simple and efficient technique for DC link voltage control to serve PAM control of VSI along with supply current shaping plays a crucial role in enhancing the overall performance of PAM controlled BLDC drive.

2.5.1 Voltage mode controller for PAM controlled BLDC motor drive

The implemnetation of voltage mode control is achieved conventionally using a linear control technique. However the effectiveness required in applications like speed control of BLDC motor may not be gauranteed using linear control technique. The conventional PI controller used in the voltage control loop exhibit poor performance, causing transient oscillations and large peak overshoots under parameter variation, load disturbance etc. This demands for sophisticated control technique for DC link voltage control. Hence the research work, investigates for nonlinear control techniques to improve the performance.

Commonly used classical control theory based design of PID family controllers

requires precise linear mathematical models. The PID family of controllers fail to perform satisfactorily under parameter variation, non linearity, load disturbance, etc. The most widely used method for small signal linearization of dc-dc converters is state-space averaging method. These linearised models are inadequate to demonstrate the accurate system behaviour (Raviraj and Sen, 1997).

The modern control theory based controllers such as state-feedback controllers, self-tuning controllers, and model reference adaptive controllers etc. also need mathematical models and are therefore sensitive to parameter variation (Sen,1990). To alleviate the need for accurate mathematical models, sliding mode controllers (SLMC) were introduced (Spiazzi et al., 1995).

The SLMC does not need accurate mathematical models, but requires the knowledge of a range of parameter variation to ensure stability (Raviraj and Sen, 1997). Since SLMC uses a discontinuous switching function, the performance is affected by a phenomena called chattering. Chattering causes high frequency variation in the control signal and the magnitude of this variation in the control signal varies with the amount of uncertainty present in the system.

Further, (Wang et al., 2007) reports complexity existing in SEPIC converter controlled from sliding mode control technique. In the paper, it is noted that the SEPIC converter can exhibit complex dynamical behavior including limit cycle, double limit cycle, quasi-periodicity etc. when controlled by SLMC technique.

2.5.2 One-cycle control techique for PAM controlled BLDC motor drive

One cycle control is a large-signal nonlinear control technique, which controls the duty-ratio of a switch such that in each cycle the average value of a switched variable of the switching converter is exactly equal to or proportional to the control reference under steady-state or in transient conditions (Smedley and Cuk, 1995). One cycle control rejects power source perturbations in one switching cycle, the average value of the switched variable follows the dynamic reference in one switching cycle and the controller corrects switching errors in one switching cycle. So the OCC achieves zero error at steady state and during dynamic tracking (Smedley, 1991).

Furthermore, the dynamics of one cycle controlled Cuk converter is explained by Smedley, Cuk (1995), where it becomes clear that even when an one cycle controlled switch is embedded in a complex system, where the input of the switch is a function of other state variables, the zero-error property is preserved.

One cycle control extended to power factor correction schemes, is proved to be simple and effeicient in CCM operation of converter, because it eliminates the need of input current sensor (Lai and Smedley, 1998), compared to conventional CCM power factor control schemes.

(Lai et al. 1997) presented one cycle control for boost converter operated in DCM used to achieve power factor correction, where it controls the time duration of the switching pulse such that the average value of the input current follows the input voltage in each cycle. As a result, unity power factor and low distortion are achieved.

The simplicity of one cycle control favors its utilisation in bridgeless converters for power factor correction (Lu et al., 2005). This does not require input line current sensing and can operate in peak current mode. Thus provides a simple and high performance solution.

The one cycle control techinque is widely accepted and appreciated as power factor control scheme for converters operating in both CCM and DCM modes. This feature has inspired in the present research work to adapt the robust control technique for voltage mode control scheme of proposed front-end AC-DC converter feeding BLDC motor drive.

2.6 SUMMARY

In this chapter, the literature survey on the research area is presented. A detailed survey on PWM controlled and PAM controlled BLDC motor drive is given. The converter topologies and control techniques used for PAM control in the literature are described. The conventional and modified bridgeless SEPIC converters are presented. The literature on the incorporation of the coupled inductor in the converter, for size reduction is explored. Linear and non-linear control techniques for the voltage mode

controller of the front-end converter are discussed. The survey on a simple and effective non-linear controller using one cycle control technique is done to ascertain its feasibility for PAM controlled drive.

Chapter 3

Design and Analysis of Bridgeless SEPIC with Coupled Inductors

3.1 INTRODUCTION

A bridgeless SEPIC is a highly preferred single-stage front end AC-DC converter for applications requiring a wide variation of DC voltage and to give improved performance in terms of the quality of supply current. Even though the conventional bridgeless SEPIC converter results in a reduction in the conduction losses due to the elimination of one rectifier diode in the conduction path, it has the limitation of larger size and more number of components compared to the conversion using a diode bridge rectifier and a dc-dc converter. Several modifications for bridgeless SEPIC have been attempted to reduce the number of components and size. The modified topologies of bridgeless SEPIC existing in the literature (Ismail, 2009; Ma et al., 2017; Mahdavi and Farzanehfard, 2010; Sabzali et al., 2011; Zheng et al., 2008) possess limitations of either the complex structure, high side gate drive requirement, circulating current loss or need of inner current control loop.

In this work, the incorporation of coupled inductors for the conventional bridgeless SEPIC is excercised to achieve compactness. The bridge less SEPIC converter can provide both supply current shaping and control of output voltage with the only volt-

age control loop. Additionally, with the feature of coupling incorporated between the input and output inductances, it offers the advantage of compact size, reduced structure complexity, the requirement of only one low side gate driver, and the absence of circulating current. In this work, a split winding scheme is proposed for the distribution of windings over three limbs of E core for obtaining the desired coupling coefficient. This overcomes the difficulties existing in the conventional approach of adjusting the air-gap to achieve the desired coupling.

In this chapter, the operation, design, and selection of components of the proposed front end converter with coupling is described. The magnetic structure using a split winding scheme for the coupled inductors of bridgeless SEPIC is illustrated. The comparison of volume, weight, cost, and efficiency of the converter with and without coupling for the same rating is presented. The performance of the converter with the coupling is evaluated using MATLAB/Simulink simulation.

3.2 BRIDGELESS SEPIC CONVERTER WITH COUPLED INDUCTORS

The circuit diagram of a bridgeless SEPIC converter with coupling is shown in Figure 3.1. The compactness in the circuit is achieved with the incorporation of coupled inductors in the conventional SEPIC configuration, avoiding the structural complexity (Ismail, 2009). This configuration helps to overcome circulating currents, compared to the configuration proposed in (Sabzali et al., 2011). The switches (SW_1, SW_2) of the converter operate with the same switching signal, in alternate supply cycles, sufficing only one low side gate driver. The SEPIC converter is designed to ensure the DCM operation in order to provide inherent power factor correction. Hence, demands only a voltage control loop, eliminates supply current sensing and inner current control loop.

The converter shown in Figure 3.1, has two DC-DC SEPIC converters with coupling of the input and output side inductors. The DC-DC SEPIC converter with the components L_{i1}, L_{o1}, C_1, C_d, D_1, SW_1 operate during the positive cycle of the supply voltage, through the rectifier diode D_p to connect the converter to the supply. The SEPIC converter with the components L_{i2}, L_{o2}, C_2, C_d, D_2, SW_2 operate for the negative half cycle along with rectifier diode D_n which connects the converter to the supply.

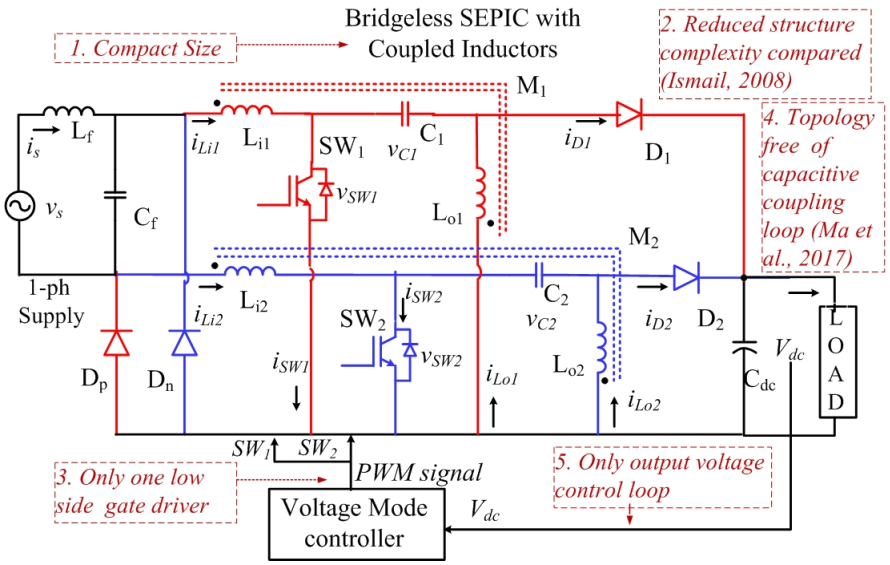


Figure 3.1: Circuit diagram of Bridgeless SEPIC converter with coupled inductors

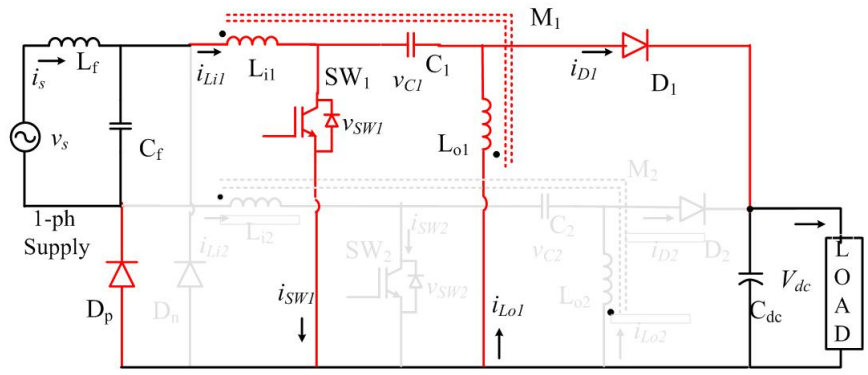
Dotted lines represent the magnetic coupling between the two inductors. The coupled inductors L_{i1}, L_{o1} of the DC-DC SEPIC operating for positive half of supply voltage have a mutual inductance of M_1, similarly coupled inductors L_{i2}, L_{o2} of the DC-DC SEPIC operating for negative half of the supply have a mutual inductance of M_2.

The equivalent circuits formed during two modes of operation over a period of supply voltage are shown in Figure 3.2. Two modes of operation of the converter over the period of supply voltage are:

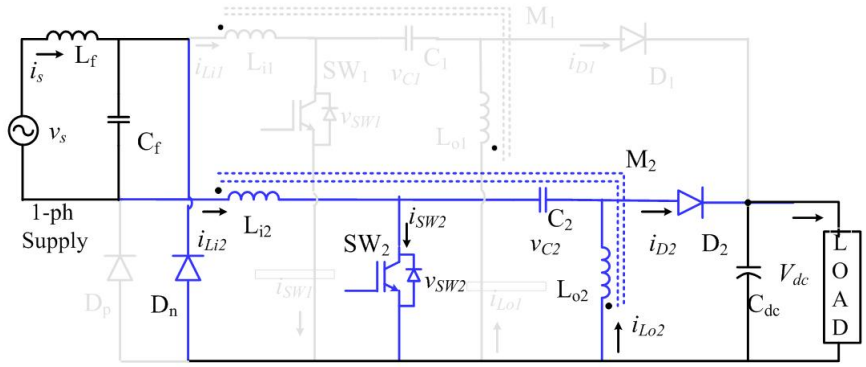
- Operation during positive half cycle
- Operation during negative half cycle

The equivalent circuit shown in Figure 3.2a is formed during positive cycle duration of the supply with the components L_{i1}, L_{o1}, C_1, C_d, D_1, SW_1, D_p and the equivalent circuit shown in Figure 3.2b is formed during negative cycle duration of the supply with the components L_{i2}, L_{o2}, C_2, C_d, D_2, SW_2, D_n.

The operation of SEPIC in DCM constitutes three intervals in each switching cycle as shown in Figure 3.3. Three intervals of operation over the switching period are



(a) Operation during positive half cycle



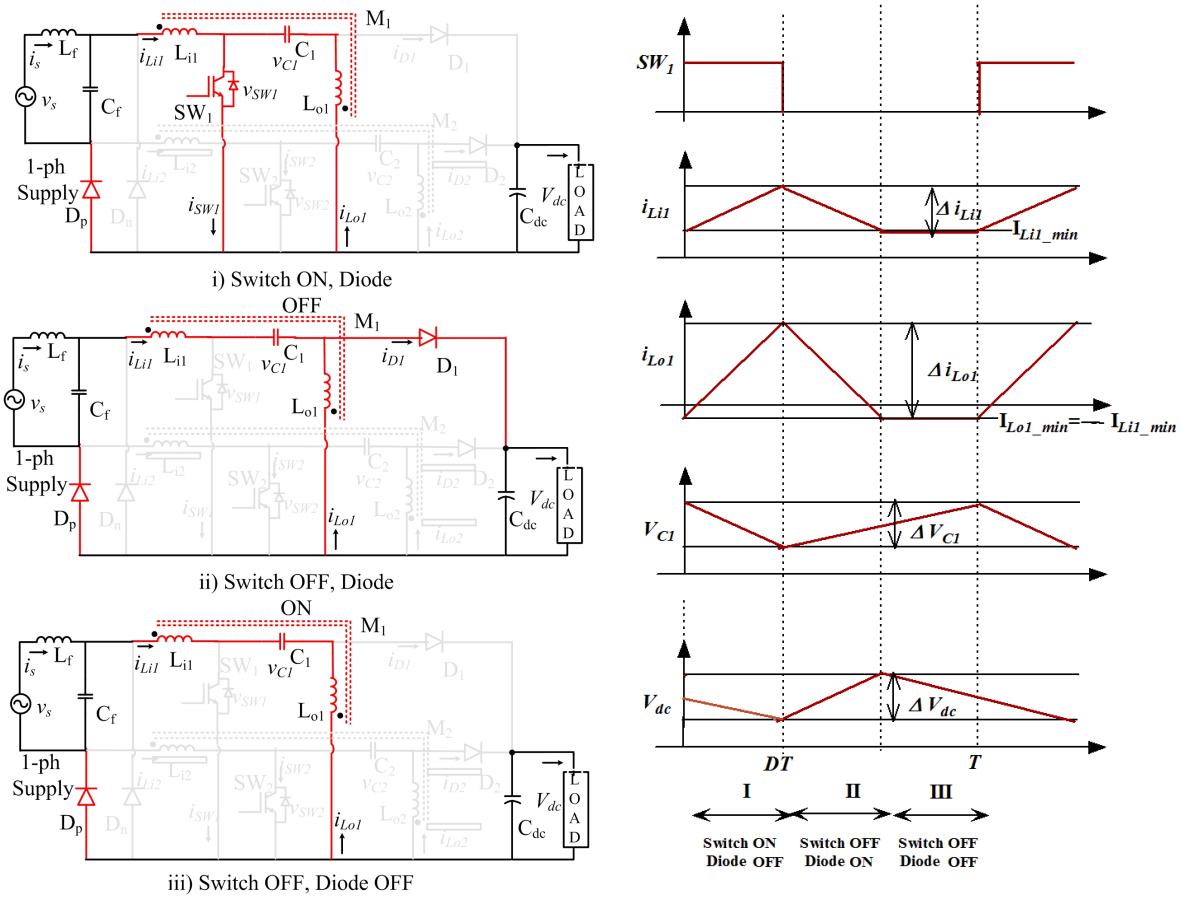
(b) Operation during negative half cycle

Figure 3.2: Converter operation during the period of one supply cycle

formed as below:

- Interval I: When switch is ON, diode is OFF
- Interval II: When switch is OFF, diode is ON
- Interval III: When switch is OFF, diode is OFF

The switching cycle operation is explained here considering the SEPIC converter operating during positive half cycle of the supply (Figure 3.2a). The equivalent circuits during three intervals of operation are shown in Figure 3.3a. The corresponding voltage and currents for the circuit elements in a switching interval are shown in Figure 3.3b.



(a) Equivalent circuits for three intervals of DCM operation **(b)** Waveforms for three intervals of DCM operation

Figure 3.3: Operation of Bridgeless SEPIC during positive half cycle of supply

In interval I, where switch is ON, diode is OFF as shown in circuit (i) of Figure

3.3a, the input inductor (L_{i_1}) and output inductor (L_{o_1}) start charging. The intermediate capacitor (C_1) discharges via output side inductor (L_{o_1}) and the voltage across it decreases. The diode (D_1) remains in OFF state and the capacitor (C_d) at the DC bus supplies the required energy to the load.

In interval II, where switch is OFF, and diode is ON as described in circuit (ii) of Figure 3.3a, the input inductor (L_{i_1}) and output inductor (L_{o_1}) start discharging via diode (D_1). The intermediate capacitor (C_1) charges in this interval of operation. The DC link capacitor (C_d) also charges in this interval. Inductors transfer energy to the load.

In interval III, depicted in circuit (iii) of Figure 3.3a, the switch is OFF, and the diode is also OFF. The inductors (L_{i_1}) and (L_{o_1}) are completely discharged. A non zero remaining current will flow through inductors and intermediate capacitor. The DC link capacitor (C_d) supplies the required energy to the load.

The same sequence of operation occurs in the negative half cycle of the supply voltage, with respective converter components (L_{i2}, L_{o2}, C_2, C_d, D_2, SW_2) and rectifier diode (D_n).

The effect of coupling the inductors in SEPIC topology is analysed in following section 3.3.

3.3 EFFECT OF COUPLING THE INDUCTORS IN BRIDGELESS SEPIC

The bridgeless SEPIC in Figure 3.1 has two identical SEPIC converters, each operating in alternate half cycles of supply, depending on the voltage polarity. Two SEPIC converters have equal self-inductances at the input side, namely $L_{i1} = L_{i2} = L_i$ and the self-inductances at the output side, namely $L_{o1} = L_{o2} = L_o$. The mutual inductance between the input and output side is $M_1 = M_2 = M$. The coupling coefficient (k_c) in terms of self and mutual inductance is given by (3.1).

$$k_c = \frac{M}{\sqrt{L_i L_o}} \tag{3.1}$$

The voltages $v_{L_{i1}} = v_{L_{i2}} = v_{L_i}$ and $v_{L_{o1}} = v_{L_{o2}} = v_{L_o}$ across inductors L_i and L_o respectively are given by equation (3.2) and (3.3).

$$v_{L_i} = L_i \frac{di_i}{dt} + M \frac{di_o}{dt} \tag{3.2}$$

$$v_{L_o} = M \frac{di_i}{dt} + L_o \frac{di_o}{dt} \tag{3.3}$$

The turns ratio n of the two coils is as given by (3.4)

$$n = \frac{v_{Li}}{v_{Lo}} = \frac{N_i}{N_o} = \sqrt{\frac{L_i}{L_o}} = \frac{M}{k_c L_o} \tag{3.4}$$

For the SEPIC converter, it is known that the voltage across input and output side inductors is the same in each switching interval, i.e., $v_{L_i} = v_{L_o}$. Under this condition, rearranging the equations (3.2) and (3.3), ripple current through inductors is obtained as (3.5) and (3.6).

$$\frac{di_{L_i}}{dt} = \frac{v_{L_o} L_o - v_{L_i} M}{L_i L_o - M^2} = \frac{v_{L_i}}{L_i(\frac{1-k_c^2}{1-k_c\sqrt{\frac{L_i}{L_o}}})} \tag{3.5}$$

$$\frac{di_{L_o}}{dt} = \frac{v_{L_i} L_i - M v_{L_o}}{L_i L_o - M^2} = \frac{v_{L_o}}{L_o(\frac{1-k_c^2}{1-k_c\sqrt{\frac{L_o}{L_i}}})} \tag{3.6}$$

It can be seen from equations (3.5) and (3.6) that the ripple currents in converter with coupled inductors due to the effective inductance values determined by coupling coefficient k_c and the turns ratio $\sqrt{\frac{L_i}{L_o}}$.

The equivalent values of inductances at input side L_{ieq} and output side L_{oeq} produced as a effect of coupling are given by (3.7) and (3.8) respectively.

$$L_{ieq} = L_{i1eq} = L_{i2eq} = L_i \frac{1 - k_c^2}{1 - k_c\sqrt{\frac{L_i}{L_o}}} \tag{3.7}$$

$$L_{oeq} = L_{o1eq} = L_{o2eq} = L_o \frac{1 - k_c^2}{1 - k_c\sqrt{\frac{L_o}{L_i}}} \tag{3.8}$$

Solving (3.7) and (3.8), the turns ratio $n = \sqrt{\frac{L_i}{L_o}}$ can be represented in terms of equivalent inductance values and coupling coefficient k_c and is given by (3.9),

$$\sqrt{\frac{L_i}{L_o}} = \frac{-k_c(L_{ieq} - L_{oeq}) + \sqrt{k_c^2(L_{ieq} - L_{oeq})^2 - 4L_{ieq}L_{oeq}}}{2L_{oeq}} \tag{3.9}$$

The desired ripple current steering in both windings of coupled inductors can be achieved by properly tuning the coupling coefficient k_c and turns ratio $\sqrt{\frac{L_i}{L_o}}$.

The solution of equations (3.7), (3.8) and (3.9) show that the desired values of L_{ieq} and L_{oeq} can be obtained with different combinations of L_i, L_o and k_c. The selection of an appropriate combination of L_i, L_o and k_c to obtain the desired value of equivalent, is realized by considering the equivalent circuit T-model of coupled inductor shown in Figure 3.4.

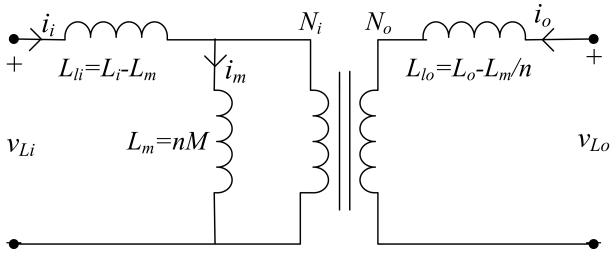


Figure 3.4: Equivalent circuit transformer model

From the T-model the self inductance values L_i, L_o can be expressed in terms of leakage inductance L_{li}, L_{lo} and magnetising component L_m as given by (3.10), (3.11) (Erickson and Maksimovic, 2007).

$$L_i = L_{li} + L_m \tag{3.10}$$

$$L_o = L_{lo} + L_m/n \tag{3.11}$$

The effective inductances as seen from equivalent T-model namely L_{ei}, L_{eo} are given by equations (3.12) (3.13) (Ranganathan and Umanand, 1999).

$$L_{ei} = \frac{L_m \times (L_{li} + L_{lo})}{L_{lo}} + L_{li} \tag{3.12}$$

$$L_{eo} = \frac{L_m \times (L_{li} + L_{lo})}{L_{li}} + L_{lo} \tag{3.13}$$

The combination of L_i, L_o and k_c to obtain the desired value of equivalent inductance can be obtained by solving (3.7-3.13).

The design of bridgeless SEPIC converter with coupling is discussed in section 3.4 below.

3.4 DESIGN OF BRIDGELESS SEPIC CONVERTER WITH COUPLED INDUCTORS

The bridgeless SEPIC converter of power (P) of 500 W, output voltage (V_{dc}) of 70 V - 310 V, switching frequency (f_s) of 20 kHz is considered. The design of converter is done to get operation of converter in discontinuous conduction mode for the output voltage of entire range and for supply voltage (V_s) variation of universal range (90-270 V RMS).

The converter design specifications are as follows:

- Ripple current (Δi_{in}) = 30 % of input current (I_{in}); where $I_{in} = \sqrt{(2)} \times \frac{P}{\eta V_m}$ is a RMS value of supply current at supply voltage of $v_s = V_m sin\omega t$.
- Ripple voltage at intermediate capacitor (Δv_C) = 30 % of capacitor voltage (v_C)

- Output voltage ripple (ΔV_{dc}) = 1 % of output voltage (V_{dc})

3.4.1 Duty ratio for discontinuous operation

The voltage conversion ratio M_I for discontinuous conduction operation with a duty ratio d is given by (3.14).

$$M_I = \frac{V_{dc}}{v_s} = \frac{V_{dc}}{V_m|sin\omega t|} = \frac{d}{\sqrt{k}} \tag{3.14}$$

where $k = \frac{2L_{eq_T}}{RT_s}$ is the conduction parameter with $L_{eq_T} = \frac{L_{ieq} \times L_{oeq}}{L_{ieq}+L_{oeq}}$, a parallel combination of input and output side inductors.

The discontinuous conduction mode can be obtained for $k < k_{critical}$, where $k_{critical}$ is given by equation (3.15)

$$k < k_{critical} = \frac{1}{2(M_I + 1)^2} \tag{3.15}$$

For the converter with coupled inductors, the ripple current specification is met from equivalent inductance values at the input and output side.

3.4.2 Design of input side inductors

The equivalent inductance at input side is obtained for the ripple current of Δi_{in} as given by (3.16)

$$L_{ieq} = \frac{|V_m sin\omega t| \times d}{\Delta i_{in} \times I_{in} \times f_s} \tag{3.16}$$

where $I_{in} = \frac{d^2 V_m |sin\omega t| T_s}{2L_{T1}}$ is average input current.

3.4.3 Design of output side inductors

The equivalent inductance at the output is designed to ensure DCM operation (3.17)

$$L_{oeq} = \frac{V_{dc} d}{2 I_{in} f_s} \tag{3.17}$$

The self inductance L_i of input side inductors and and the self inductance L_o of output side inductor of the bridgeless SEPIC to obtain desired equivalent values can be obtained as disussed in section 3.3.

3.4.4 Design of intermediate capacitor

The intermediate capacitance is designed using (3.18) (Singh and Bist, 2013).

$$C_{1,2} = \frac{1}{4\pi^2 f_r^2 \times (L_T)} \tag{3.18}$$

where $L_T = L_{ieq} + L_{oeq}$ is total inductance & f_r is the resonance frequency. The design of capacitance follows the criteria of $f_l < f_r < f_s$, where f_l is line frequency and f_s is a switching frequency.

The design value of intermediate capacitor significantly affect the quality of the supply current. The voltage across the capacitor should follow the rectified supply voltage for line frequency (f_l) operation and maintain constant value during the operation over a switching frequency (f_s). The resonant frequency (f_r) should be higher than the line frequency to avoid low-frequency oscillations in the supply current. It should be smaller than the switching frequency to obtain constant value of voltage across capacitor in a switching period.

3.4.5 Design of DC link capacitor

The DC link capacitor C_d needs to be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power. As the output ripple frequency is two times the input line frequency f_l, the output capacitor must be large enough to minimize the output voltage ripple δV_{dc}.

The DC link capacitor C_d, for the ripple voltage of δV_{dc} is obtained from (3.19)

$$C_d = \frac{P_i}{4\pi f_l \delta V_{dc}^2} \tag{3.19}$$

3.4.6 Design of EMI filter

The maximum value of filter capacitance is expressed by equation (3.20)

$$C_{max} = \frac{I_m}{f_l V_m} tan\theta \tag{3.20}$$

with the phase angle θ, which is the angle subtended between the current and voltage at the output of filter.

The filter inductance is designed for $f_c = f_s/10$, since $f_l < f_c < f_s$ using (3.21)

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \tag{3.21}$$

3.4.7 Design summary

The values of components of bridgeless SEPIC with coupling for the power rating of 500 W, DC link voltage of 70 V - 310 V, switching frequency of 20 kHz obtained from the design are listed in Table 3.1.

Table 3.1: Component Values of for Bridgeless SEPIC with Coupled Inductors

Sl.No.	Components	Notation	Values
1	Input Side Inductors	L_{ieq}	3.8 mH
2	Output side inductors	L_{oeq}	98 µH
3	Intermediate capacitor	$C_{1,2}$	1.5 µF
4	DC link capacitor	C_{dc}	2200 µF
5	Filter Capacitor	C_f	0.06 µF
6	Filter Inductor	L_f	3.2 mH

3.5 SELCTION OF COMPONENTS OF SEPIC CONVERTER

The selection of active devices of SEPIC such as fast switching IGBT, fast switching diode, the passive elements such as intermediate capacitor, DC link capacitor based on the voltage and current stresses is discussed below.

3.5.1 Selection of rating of the controlled switch:

Selection of switch is done, depending on the maximum voltage and current stresses on the switch and on the maximum switching frequency requirement.

The maximum current through the switch is given by (3.22),

$$i_{sw_{max}} = \frac{V_m \times t_{on}}{L_{eq}} \tag{3.22}$$

The maximum voltage across the switch is as shown in equation (3.23),

$$v_{sw_{max}} = V_m + V_o. \tag{3.23}$$

SW_1 and SW_2 of the converter are chosen depending on the ratings decided by (3.22) and (3.23).

3.5.2 Selection of rating of the fast switching diode :

Fast recovery diode is chosen depending on the switching frequency, as well as maximum voltage and current stresses on it. Maximum switching stresses on the diode remains same as the switch and can be obtained by (3.24, 3.25),

$$i_{D_{max}} = \frac{V_m \times t_{on}}{L_{eq}} = i_{sw_{max}} \tag{3.24}$$

$$v_{D_{max}} = V_m + V_o = v_{sw_{max}}. \tag{3.25}$$

The average current through the diode is equal to the load current, which is given by (3.26),

$$i_{D_{av}} = \frac{P_o}{V_{dc}}. \tag{3.26}$$

Fast switching diodes D_1 and D_2 of the converter are chosen depending on ratings decided by (3.24 - 3.26).

3.5.3 Selection of rating of Intermediate Capacitor:

Intermediate capacitor voltage follows the rectified line voltage, and it should withstand the ripple voltage specified in the design. The peak voltage stress across the intermediate capacitance can be calculated as (3.27)

$$V_{C1_{max}} = V_m + \frac{\triangle V_{C1}}{2}. \tag{3.27}$$

The intermediate capacitors C_1 and C_2 are chosen depending on the rating specified by the equation (3.27).

3.5.4 Selection of rating of DC link Capacitor:

DC link capacitor should withstand the maximum allowable DC link voltage. Capacitor C_d is chosen based on the maximum value of DC link volatge.

3.5.5 Selection of coupling parameters and determining the current rating of inductor

The selection of combination of k_c, L_i, L_o which gives desired equivalent value to meet the current ripple specification at the input of the converter has to be done as discussed in section 3.3. The peak and RMS value of currents are required in order to determine the magnetic structure geometry (size of the core and area of cross section of the wire).

3.5.5.1 Selection of coupling parameters

Desired value of equivalent inductance as listed in Table 3.1, can be obtained for a combination of L_i, L_o, and k_c as expressed in (3.7) and (3.8). Different combination of L_i, L_o, and k_c can result in the same value of equivalent indutance. So selecting the appropriate combination of L_i, L_o, and k_c needs to be addressed. For this, the T-model is considered as explained in section 3.3 and equations (3.7-3.13) are solved. Plot of variation of effective inductances L_{ei}, L_{eo} and self inductances L_i, L_o for varying k_c is

shown in Figure 3.5.

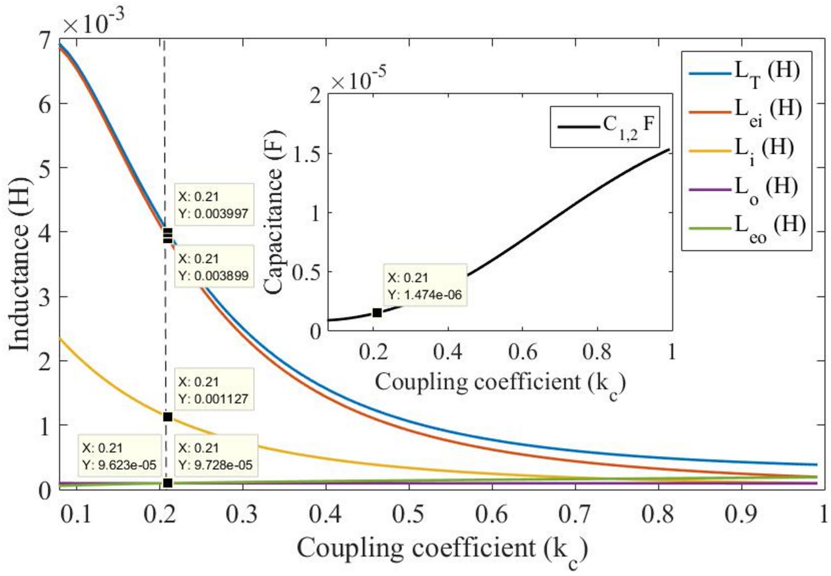


Figure 3.5: Variation of effective inductances L_{ei}, L_{eo} and self inductances L_i, L_o with varying k_c obtained using transformer model

The value of k_c for which L_{ei} becomes equal to desired value of L_{ieq} is obtained from Figure 3.5 (shown by the dotted line) and then the corresponding values of L_i, L_o are chosen for the implementation of the coupled inductor in this work. The value of k_c obtained is 0.21, indicating the need for loose coupling.

The desired current ripple at the input side of the SEPIC converter can also be achieved with tightly coupled inductors (higher value of coupling coefficient) with a tradeoff of the higher value of intermediate capacitor $C_{1,2}$.

The variation of $C_{1,2}$ for varying k_c is plotted and is shown as an inset in Figure 3.5, taking the same value of resonance frequency ω_r, that is considered for converter without coupling. It can be observed that the value of intermediate capacitance increases for higher values of k_c to achieve the same performance. However, the tightly coupled inductor design has the disadvantage of being sensitive to turns ratio, residual flux, etc., which can result in additional ripple current (Santi, 1994). Also, the higher value of capacitance will increase the overall size and cost. Hence low value of k_c is selected, which can give effective value of input side inductance equal to desired value L_{ieq}.

3.5.5.2 Determination of peak and rms currents through inductor

The peak and RMS currents of input and output side inductors of SEPIC converter are given as follows.

For the input side inductor, the peak current capability can be decided by (3.28)

$$I_{L_{ip}} = I_m + \frac{\triangle I_{Li}}{2} = \frac{\sqrt{2}P_o}{V_m} + \frac{V_m \times t_{on}}{2L_i}. \tag{3.28}$$

And, the RMS current through input side inductor is obtained by (3.29),

$$I_{L_i} = \frac{\sqrt{2}P_o}{V_m} \tag{3.29}$$

For the output side inductor, the peak current capability can be decided by (3.30)

$$I_{Lo_p} = \frac{V_m \times t_{on}}{L_o} + I_{L_{omin}} \tag{3.30}$$

where $I_{L_{omin}} = -\frac{d^2 V_m T_s}{2}\left[\frac{1}{L_o} - \frac{1}{L_i(\frac{V_o}{V_{in}})}\right]$.

And, the RMS current through output side inductor is obtained by (3.31),

$$I_{L_o} = \frac{P_o}{V_{dc}} \tag{3.31}$$

3.5.6 Summary on selection of components

The 500 W bridgeless SEPIC with the incorporation of coupled inductors designed for the specifications mentioned in section 3.4 has the component values specified in the Table 3.1. The selection of components depends on the voltage and current stresses on the components as discussed before. The mathematical representations of major design and selection parameters (voltage and current stresses) for the components of bridgeless SEPIC are tabulated in 3.2.

Table 3.2: Theoretical represntations of major parameters for bridgeless SEPIC

Sl.No	Parameter	Notation	Equation
1	Conduction Parameter	k	$\frac{2Leq}{RT_s}$
2	Voltage Conversion Ratio	M	$\frac{Vo}{Vm}$
3	Duty ratio	d	$M \times \sqrt{2k}$
4	Ripple Current	Δi	$\frac{V_m dT_s}{L_i}$
5	Input current	I_{in}	$\frac{P_o}{\eta V_s}$
6	Input Inductor Current(Max)	$i_{Li_{max}}$	$i_{in}+\frac{\Delta i}{2}$
7	Input Inductor Current(Min)	$i_{Li_{min}}$	$i_{in}-\frac{\Delta i}{2}$
8	Output Inductor Current(Max)	$i_{Lo_{max}}$	$\frac{V_m dT_s}{L_o} - i_{Lo_{min}}$
9	Output Inductor Current(Min)	$i_{Lo_{min}}$	$-i_{in}$
10	Voltage Ripple	Δv_c	$\frac{I_o dT_s}{C_i}$
11	Voltage across Capacitor	v_{Cmax}	$v_C + \frac{\Delta v_c}{2}$
12	Voltage across Capacitor	v_{Cmin}	$v_C - \frac{\Delta v_c}{2}$
13	Current through Switch	i_{SW}	$\frac{V_m * t_{on}}{L_{eq}}$
14	Voltage across Switch	v_{SW}	$V_m + V_o$
15	Current through Diode	i_D	$\frac{V_m * t_{on}}{L_{eq}}$
16	Voltage across Diode	v_D	$V_m + V_o$

3.6 DESIGN OF MAGNETIC STRUCTURE USING SPLIT WINDING SCHEME FOR COUPLED INDUCTORS OF BRIDGELESS SEPIC

The practical implementation of a coupled inductor with desired k_c, L_i, L_o requires accurate design of the magnetic structure which gives high value of leakage inductance (at low coupling coefficient). Introducing the higher leakage in the design can be realized using either the closely coupled inductor approach, interleaved winding inductor approach, or loosely coupled inductor approach (Kimura et al., 2016).

In a closely coupled inductor approach, it has two windings tightly coupled over one core and an external inductor is used to provide desired leakage inductance. Since there is an additional inductor, it cannot provide a reduction in size. The interleaved winding inductor approach uses three windings instead of two. Here, the design requires tuning of coupling between three windings to get the desired value of leakage inductance. In the loosely coupled inductor approach, two coils are wound over two side limbs of E-core. Among above mentioned methods, the loosely coupled inductor approach is generally used in the coupling of two inductors at input and output sides of

converters like CUK, SEPIC.

The problem of no existence of a closed-form solution of winding design for loosely coupled inductors is identified in (Spiazzi and Rossetto, 1994). This issue calls for an accurate leakage model. In (Santi, 1994), an improved reluctance model is proposed to predict the effect of air-gap position to achieve required coupling. Two winding UI core with special gap arrangements are introduced. However, the best core utilization is not obtained as the flux density in the two legs are unequal.

In work presented in this paper, the reluctance model is adopted for E-core, and the desired coupling is achieved by distribution of the number of turns in all the three legs (split winding scheme) with fixed air-gap. The magnetic design using the area product approach to achieve the required coupling coefficient with the split winding scheme is described below.

3.6.1 Determination of core geometry and wire gauge

The significant parameters required to be considered in the design and implementation of inductors are peak and RMS values of current through inductor and frequency of operation.

The peak currents (I_{ip}, I_{op}) flowing through windings (L_i, L_o) decide energy handling capability of the core, which is given by (3.32).

$$E = \frac{1}{2}\left[L_i I_{ip}^2 + L_o I_{op}^2 + 2M I_{ip} I_{op}\right] \tag{3.32}$$

where E is the energy.

Depending on energy handling capability, the area product of core can be calculated as given (3.33).

$$A_P = A_W \times A_e = \frac{2E}{K_w K_c J B_m} \tag{3.33}$$

where

A_P is the Area Product of the core, which is the product of window cross-section area A_W and core cross-section area A_e.

K_w is the window utilisation factor

$K_c = \frac{peak}{rms}$ is the crest factor.

J is the current density.

B_m is the maximum flux density.

The wire gauge of input and output side inductors is selected depending on the RMS current flow through the windings and, in general, is given by (3.34).

$$a = \frac{I}{J} \tag{3.34}$$

where a is the area of cross-section of the conductor; I is the RMS value of current through the inductor.

Finally, the design of the inductor is required to be cross verified by checking for the inequality, as shown by (3.35).

$$A_w K_w > a_i N_i + a_o N_o \tag{3.35}$$

where N_i and N_o are total number of turns of input and output side inductors of SEPIC converter.

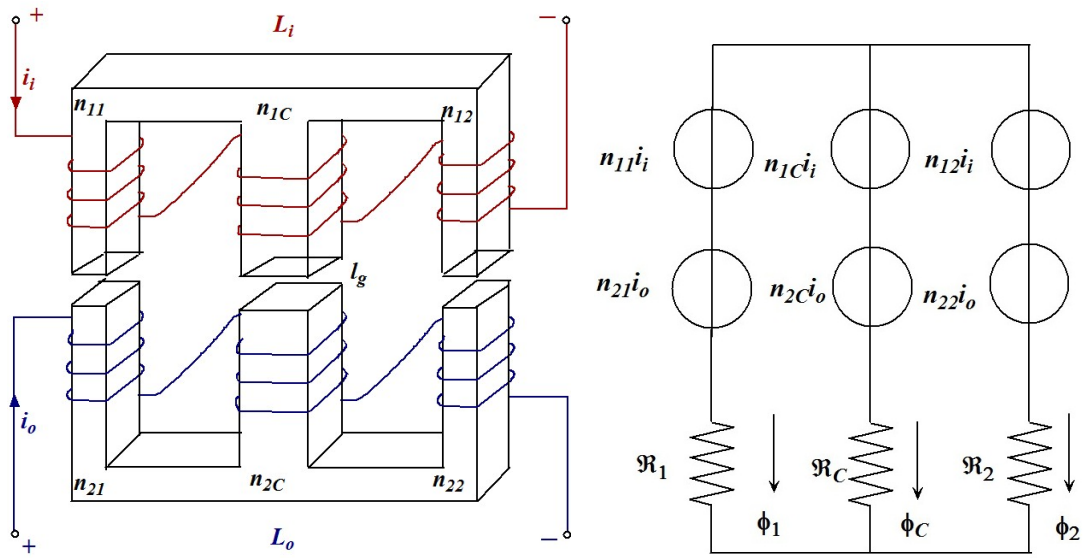
A single core of size meeting the inequality (3.35) is needed to accommodate two windings. The area of cross-section of the inductor at input side a_i=$\frac{I_{Li}}{J}$; and the area of cross-section of windings at output side a_o=$\frac{I_{Lo}}{J}$; where I_{Li} and I_{Lo} are RMS currents through inductors at input and output side respectively.

The approach of split winding scheme to obtain desired coupling parameters by the distribution of windings over three limbs of E-core is described in section 3.6.2

below.

3.6.2 Determination of Winding distribution (Split winding scheme)

The coupling feature for bridgeless SEPIC is implemented using E-core. The desired coupling coefficient is obtained by the distribution of two windings over three limbs of E-core. The input side inductor carrying current i_i with total number of turns N_i has to be distributed over the three limbs; first limb (n_{11}), centre limb (n_{1c}) and second limb (n_{12}). Similarly the output side inductor carrying current i_o with total number of turns N_o has to be distributed over the three limbs; first limb (n_{21}), centre limb (n_{2c}) and second limb (n_{22}) as shown in Fig. 3.6a.



(a) Winding distribution **(b)** Reluctance model

Figure 3.6: Reluctance model for split winding distribution over an EE core

The split winding distribution to meet the desired coupling coefficient can be obtained using the reluctance model shown in Fig. 3.6b. $\Re_1$, $\Re_2$, and $\Re_c$ are the reluctances of limbs 1, 2, and C of the core, respectively. The MMF developed by windings 1 and 2 over each limb is represented as MMF sources. The magnetic reluctances for each limb ($i = 1, 2, C$) can be determined by the following formula (3.36).

$$\Re_i = \sum \frac{l_k}{\mu_k A_k} \tag{3.36}$$

where l_k is length of magnetic flux path.

u_k is corresponding permeability of the material.

A_k is cross section area of flux path.

When L_i is connected to a supply and L_o is left floating, the fluxes through three legs are represented by equation (3.37).

$$\begin{bmatrix} \phi_1 \\ \phi_C \\ \phi_2 \end{bmatrix} = \begin{bmatrix} \frac{\Re_c+\Re_2}{\Re_{den}} & \frac{-\Re_2}{\Re_{den}} & \frac{-\Re_c}{\Re_{den}} \\ \frac{-\Re_2}{\Re_{den}} & \frac{\Re_1+\Re_2}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} \\ \frac{-\Re_c}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} & \frac{\Re_c+\Re_1}{\Re_{den}} \end{bmatrix} \begin{bmatrix} n_{11}i_i \\ n_{1c}i_i \\ n_{12}i_i \end{bmatrix} \tag{3.37}$$

where $\Re_{den} = \Re_1\Re_c + \Re_1\Re_2 + \Re_c\Re_2$. The self inductance of L_i is given by (3.38).

$$L_i = \frac{\begin{bmatrix} n_{11} & n_{1c} & n_{12} \end{bmatrix}}{i_i} \begin{bmatrix} \phi_1 \\ \phi_C \\ \phi_2 \end{bmatrix} = [N_1]\,[\Re]\,[N_1]^T \tag{3.38}$$

where $[N_1] = \begin{bmatrix} n_{11} & n_{1c} & n_{12} \end{bmatrix}$ and

$$\Re = \begin{bmatrix} \frac{\Re_c+\Re_2}{\Re_{den}} & \frac{-\Re_2}{\Re_{den}} & \frac{-\Re_c}{\Re_{den}} \\ \frac{-\Re_2}{\Re_{den}} & \frac{\Re_1+\Re_2}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} \\ \frac{-\Re_c}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} & \frac{\Re_c+\Re_1}{\Re_{den}} \end{bmatrix}$$

Similarly the self inductane L_o of winding 2 is given by (3.39).

$$L_o = \frac{[N_2]}{i_o} \begin{bmatrix} \frac{\Re_c+\Re_2}{\Re_{den}} & \frac{-\Re_2}{\Re_{den}} & \frac{-\Re_c}{\Re_{den}} \\ \frac{-\Re_2}{\Re_{den}} & \frac{\Re_1+\Re_2}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} \\ \frac{-\Re_c}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} & \frac{\Re_c+\Re_1}{\Re_{den}} \end{bmatrix} \begin{bmatrix} n_{21}i_o \\ n_{2c}i_o \\ n_{22}i_o \end{bmatrix} \tag{3.39}$$

$L_o = [N_2]\,[\Re]\,[N_2]^T$ where $N_2 = \begin{bmatrix} n_{21} & n_{2c} & n_{22} \end{bmatrix}$.

The mutual inductance is obtained as shown below by (3.40).

$$M = \frac{[N_2]}{i_o} \begin{bmatrix} \frac{\Re_c+\Re_2}{\Re_{den}} & \frac{-\Re_2}{\Re_{den}} & \frac{-\Re_c}{\Re_{den}} \\ \frac{-\Re_2}{\Re_{den}} & \frac{\Re_1+\Re_2}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} \\ \frac{-\Re_c}{\Re_{den}} & \frac{-\Re_1}{\Re_{den}} & \frac{\Re_c+\Re_1}{\Re_{den}} \end{bmatrix} \begin{bmatrix} n_{11}i_o \\ n_{1c}i_o \\ n_{12}i_o \end{bmatrix} \tag{3.40}$$

$$M = [N_2]\,[\Re]\,[N_1]^T$$

The total number of turns of two windings are sum of turns distribution on three limbs, which is given in (3.41) below.

$$\begin{aligned} N_i &= n_{11} + n_{1c} + n_{12} \\ N_o &= n_{21} + n_{2c} + n_{22} \end{aligned} \tag{3.41}$$

The equations (3.38), (3.39) and (3.40) can be simplified in terms of total number of turns by assuming the winding over single limb. Considering the L_i over limb 1 and L_o over limb 2, simplified equations can be obtained as shown below by (3.42) (Wong et al., 2001).

$$\begin{aligned} L_i &= \frac{N_i^2(\Re_2 + \Re_c)}{\Re_{den}} \\ L_o &= \frac{N_o^2(\Re_1 + \Re_c)}{\Re_{den}} \\ M &= \frac{N_i N_o \Re_c}{\Re_{den}} \end{aligned} \tag{3.42}$$

By solving for (3.38-3.42), winding distribution over three limbs ($N_i = n_{11} + n_{1c} + n_{12}$ and $N_o = n_{21} + n_{2c} + n_{22}$) can be obtained.

The practical realization of the coupled inductor using the split winding scheme for 500 W bridgeless SEPIC operating at 20 kHz is evaluated theoretically to verify the size and cost reduction compared to the converter without the coupling of the same rating as shown in Table 3.3. The converter without coupling uses two separate cores for winding copper wire of 45 % larger volume for input side inductor and 13 % larger

volume for output side inductor compared to the converter with coupling which uses single core for two windings. This implementation leads to a 42% reduction in weight and a 45 % reduction in cost due to the coupling of inductors in the converter, as can be seen in Table 3.3.

Table 3.3: Magnetic design detail

Sl.No	Parameters	Notation	Separate Inductors		Coupled Inductors	
		Unit	L_i	L_o	L_i	L_o
1	Inductance	$L(mH)$	3.82	0.098	1.2	0.095
2	Energy	$E\ (mJ)$	122	62	115.62	
3	***Core Size***					
	Area Product	$A_P\ (mm^4)$	679	344	642.375	
	Core selected	EE100/60/28				
	Area Product	$A_P\ (mm^4)$	906	906	906	
	Core Area	$A_c(mm^2\ )$	738	738	738	
	Window Area	$A_w(mm^2\ )$	1227	1227	1227	
4	***Winding Design***					
	Conductor Area	$a_{cal}(mm^2\ )$	2	5	2	5
	Wire gauge		SWG 15	SWG 12	SWG 15	SWG 12
	Conductor Area	$a\ (mm^2\ )$	2.627	5.48	2.627	5.48
	Total No of Turns	N	207	28	142+24=166	
	Total winding area	$aN\ (mm^2\ )$	543.789	153	288	131
5	Design validation	$A_wK_w > aN$	$736 > 543.789$	$736 > 153$	$736 > 419$	
6	***Volume comparison***					
	Core	$V_{core}(mm^3\ )$	201400	201400	201400	
	Copper	$V_{copper}(mm^3\ )$	57930.07	12497	31970.59	10850
7	***Weight comparison***					
	Core	$W_{core}\ (g)$	987	987	987	
	Copper	$W_{copper}(g)$	1371	614	756.7	533.82
	Total	$W_{total}(g)$	3959		2297.52	
8	***Cost comparison***					
	Core	$C_{core}(Rs)$	2358.9	2358.9	2358.9	
	Copper	$C_{copper}(Rs)$	890	399	491	346
	Total	$C_{total}(Rs)$	6006.8		3198.9	

3.7 LOSS AND EFFICIENCY ESTIMATION

The loss estimation for the bridgeless SEPIC with and without coupling is done mathematically, and the efficiency of the converter for varying output power is evaluated. The total power loss in bridgeless SEPIC involves losses in active devices of the circuit such as IGBTs, high frequency diodes and rectifier diodes as well as losses in passive elements like intermediate capacitors, DC link capacitor, and the losses in input

Table 3.4: Selection of components for Bridgeless SEPIC with Coupled Inductors

Sl.No	Component	Part No.	Rating
1	Rectifier Diodes (2)	D8020L	20 A, 800 V
2	Fast recovery diode (2)	DSEI60-12A	52 A, 1200 V
3	IGBT switches (2)	IKW40N120T2	50 A,1200 V
4	Inductor Core (2)	E100/60/28 N97	A_{min}=735 mm^2
5	Input side inductor coil:	SWG 15	a = 2.6268 mm^2
6	Output side inductor coil:	SWG 12	a=5.4805 mm^2
7	Intermediate Capacitors (2)	C4BSWBX4150ZANJ	1.5uF/2000 V
8	DC link capacitor (3)	LGL2G102MELC50	1000 uF / 450 V

and output side inductors. The components selected following the design and selection process are listed in Table 3.4. Losses in the components are estimated based on device parameters, which can be obtained from datasheets.

3.7.1 Estimation of switching and conduction losses

The high-frequency switching IGBTs and diodes contribute losses during switching and conduction which can be estimated knowing the operating conditions and are given by (3.44 and 3.43) (Graovac and Purschel, 2009), (Reddivari and Jena, 2019).

$$P_{SW} = (E_{on} + E_{off}) \times f_s \tag{3.43}$$

where E_{on}, E_{off} are energy losses during turn-on and turn-off instants respectively.

$$P_C = V_{on} I_{AV} + R_{on} I_{rms}^2 \tag{3.44}$$

where V_{on} is the on state voltage; I_{AV} is average current through the device; R_{on} on state resistance; I_{rms} is rms current through the device.

3.7.2 Estimation of losses due to ESR

The passive elements of the circuit, such as intermediate capacitors, DC link capacitor, contribute to conduction losses due to its Effective Series Resistances (ESR).

The losses during conduction in the ESR (R_C) of capacitor is given by (3.45)

$$P_{C_{(esr)}} = I_{Crms}^2 \times R_C \tag{3.45}$$

The total loss in inductors include core and copper losses. The core and copper losses in the inductor can be estimated as follows.

3.7.3 Estimation of core loss

The core loss (P_{Co}) is commonly estimated using the Steinmetz equation. A generalized Steinmetz equation to find core losses taking into consideration the non-sinusoidal voltage wave shapes across the windings is given by (3.46).

$$P_{Co} = K_F \times p_{vsin} \times \left(\frac{f_s}{f_b}\right)^{\alpha} \times \left(\frac{B}{B_m}\right)^{\beta} \times V_e \tag{3.46}$$

where α is Steinmetz coefficient for frequency, β is Steinmetz coefficient for flux density, K_F is a multiplication factor for winding voltage shape. Also, f_s (kHz) is the actual operating frequency and B(mT) in the actual operating peak flux density. Here, p_{vsin} is the loss density in kW/m^3 for the sinusoidal voltage wave shape of operating frequency f_b (kHz) and peak flux density B_m (mT) (Vrazdil, 2019).

The flux density B and inductance L are related as given by (3.47).

$$B = \frac{L \times I_p}{N \times A_e} \tag{3.47}$$

where I_p is the peak value of current flowing through the winding, N is the number of turns, (A_e) is area of core cross section.

The peak current (I_{mp}) flowing through magnetising inductance (L_m) is used in the calculation of the flux density B_{CI} for inductors with coupling. The peak magnetising current is given by (3.48).

$$I_{mp} = I_{ip} + I_{op}/n \tag{3.48}$$

where n is turns ratio, and the flux density is obtained as $B_{CI} = \frac{L_M \times I_{mp}}{N_i \times A_e}$.

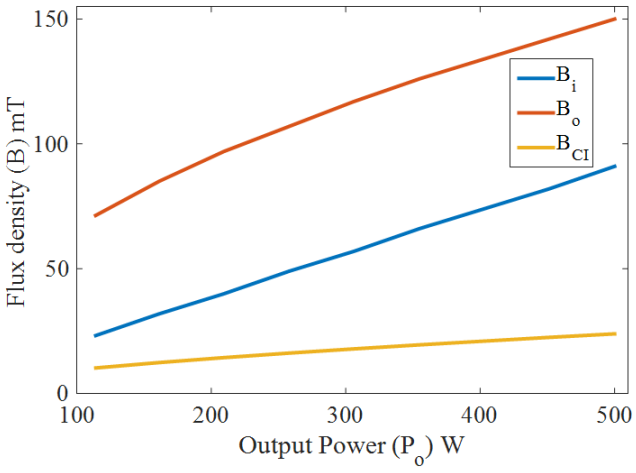


Figure 3.7: Variation of flux density with output power

The plot of flux density (B_i, B_o) for inductors at input and output side without coupling and a flux density (B_{CI}) for inductors with coupling (designed for desired k_c, L_i, L_o) is shown against output power (P_o) in Figure 3.7. It can be seen that the flux density is lesser for inductors with coupling.

The core loss without coupling $P_{Co(SI)}$, and with coupling $P_{Co(CI)}$ is evaluated using (3.46) and is plotted against the output power as shown in Figure 3.8. From the plot it is observed that, the core loss is reduced significantly with coupling.

The conventional loosely coupled method of placing two windings on side limbs of E-core results in increased core loss since the flux through the center leg is the sum of flux due to currents of two windings (Wen and Lee, 2004). In the split winding method used in this work, windings are distributed over all three limbs of E-core and the coupling required is chosen to be smaller as discussed in section 3.5.5, the flux gets reduced, and hence the core loss also gets reduced as shown in Figure 3.8.

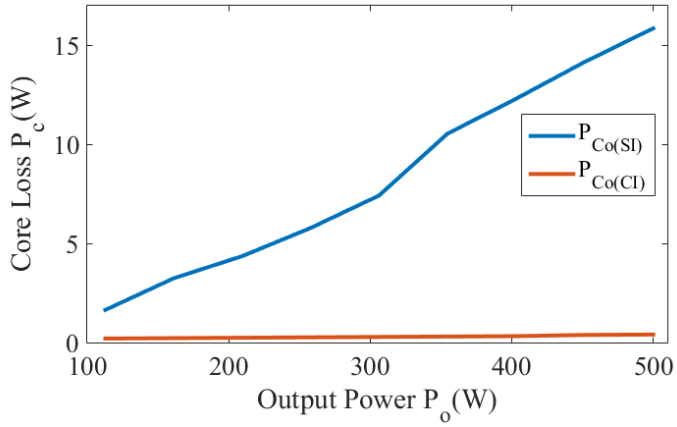


Figure 3.8: Variation of core loss with output power

3.7.4 Estimation of copper Losses

The copper losses (P_{Cu}) in the inductor carrying RMS current I , of average value I_{av} is given by (3.49).

$$P_{Cu} = (I_{(av)}^2 \times R_{dc}) + (I^2 \times R_{ac}) \tag{3.49}$$

where the DC resistance of the winding is given by $R_{dc} = \frac{N\rho l}{a}$; the AC resistance of the winding is $R_{ac} = \frac{h}{\delta} R_{dc}$; The skin depth is $\delta = \sqrt{\frac{\rho}{\pi \mu f}}$ and h is the thickness of the winding (Reddivari and Jena, 2019).

3.7.5 Estimation of efficiency

The total loss can be obtained by adding all the losses due to active elements and passive elements of the circuit. The efficiency for different output powers is calculated and is plotted against output power, as shown in Figure 3.9. The efficiency of converter drops as the output power increases due to the increase in peak value of currents flowing through inductors, which increases the flux density and result in more core losses. With coupling, the operating flux density is smaller, and its variation with output power is lesser compared to the conventional SEPIC converter without coupling, as seen in Figure 3.7. Hence the efficiency with coupling is higher and does not drop much with the output power.

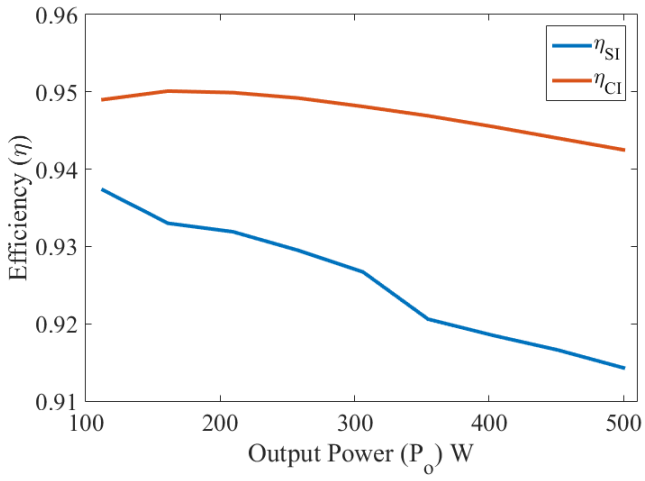


Figure 3.9: Efficiency curve

3.8 Simulation Results and Discussion

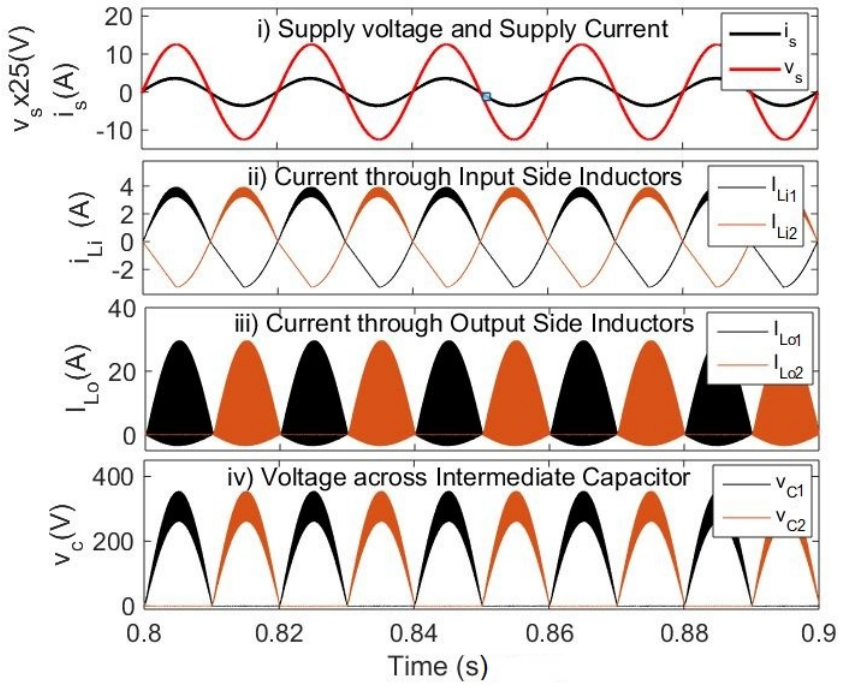
A 500 W, 20 kHz bridgeless SEPIC with loosely coupled inductors of low coupling coefficient (k_c=0.21) with component values mentioned in Table 3.1 is built in MATLAB simulink. The converter operation is evaluated with resistive load at rated conditions.

The simulation is carried out for rated conditions of supply voltage ($V_s = 220V$), output voltage (V_{dc} = 310 V) and resistive load ($R = \frac{310^2}{500}$). The voltage and current stresses on all components are evaluated at steady state also the power quality indices such as power factor and THD are observed.

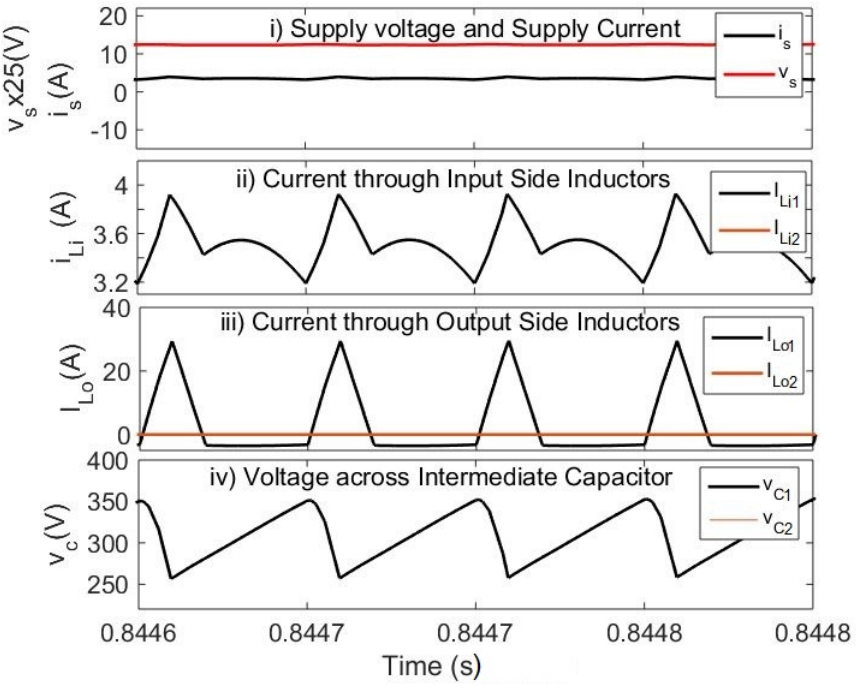
3.8.1 Voltage and current stresses on components

The converter with coupled inductors having reduced size is evaluated for its performance of bridgeless operation at rated condition with resistive load.

Figure 3.10, shows the waveforms of (i) Supply voltage (v_s) and supply current (i_s) (ii) Current through input side inductors (i_{Li1}, i_{Li2}) (iii) Current through output side inductors (i_{Lo1}, i_{Lo2}) and (iv) Voltage across intermediate capacitors (v_{C1}, v_{C2}) of proposed bridgeless SEPIC converter. Figure 3.10a shows the waveforms for supply cycle operation and Figure 3.10b shows the operation for switching cycle.



(a) For supply cycle



(b) For switching cycle

Figure 3.10: Voltage and current stresses on components of bridgeless SEPIC

Similarly, Figure3.11 shows the waveforms of (i) Voltage across switches (v_{SW1}, v_{SW2}) (ii) Current through switches (i_{SW1}, i_{SW2}) (iii) Voltage across diodes (v_{D1}, v_{D2}) and (iv) Current through diodes (i_{D1}, i_{D2}) at steady state. Figure 3.11a shows the waveforms for suply cycle operation and Figure 3.11b shows the waveforms of switching cycle operation.

The component stresses are evaluated mathematically using the expressions from Table 3.2 and compared with the values obtained using simulation as tabluted in Table 3.5. It is found that the proposed converter with reduced size matches the theoretical analysis of component stresses as that of the converter designed without coupling for the same rating.

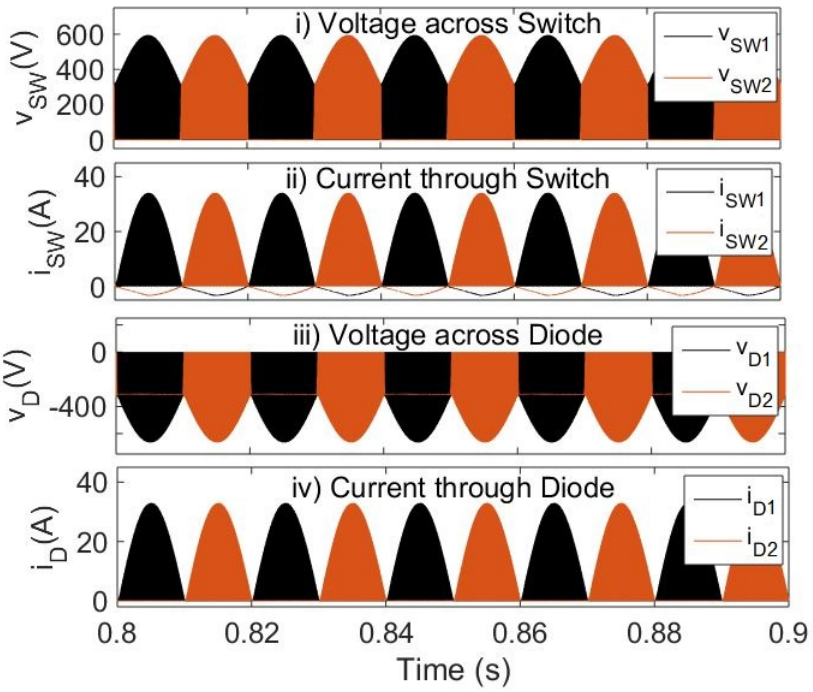
Table 3.5: Comparison of theoretical and simulation values of component stresses for proposed converter

Sl.No	Parameter	Magnitude	
		Theoretical	Simulation
1	Ripple Current	0.774 A	0.726 A
2	Input current	3.547 A	3.547 A
3	Input Inductor Current(Max)	3.934 A	3.927 A
4	Input Inductor Current(Min)	3.16 A	3.201 A
5	Output Inductor Current(Max)	29.88 A	29.51 A
6	Output Inductor Current(Min)	-3.547 A	-3.201 A
7	Voltage Ripple	93.3 V	90 V
8	Voltage across Capacitor	357.6 V	350 V
9	Voltage across Capacitor	264.3 V	260 V
10	Current through Switch	33.72 A	33.91 A
11	Voltage across Switch	621+40 V	660 V
12	Current through Diode	33.72 A	33.9 A
13	Voltage across Diode	621+40 V	660 V

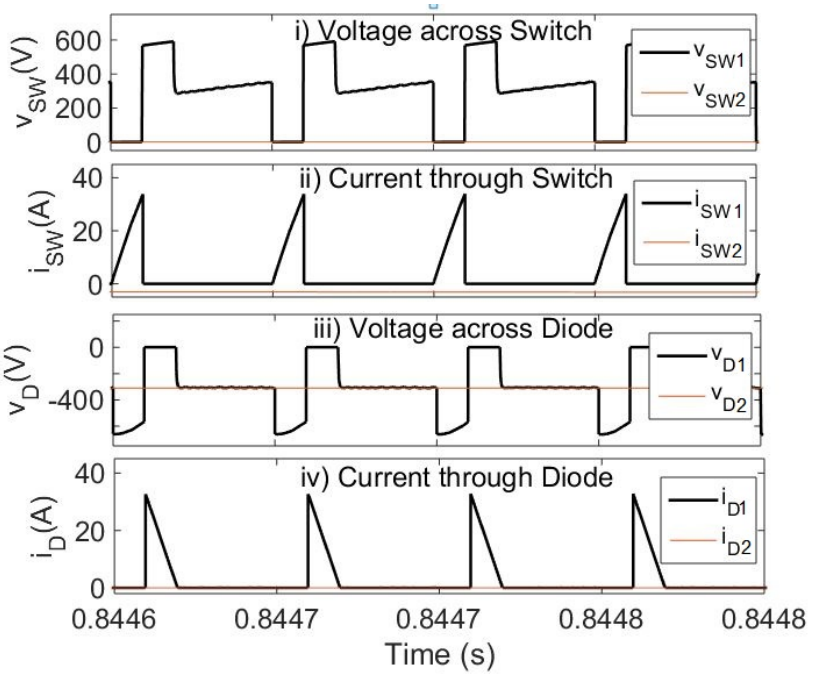
3.8.2 Power quality indices

The feature of inherent supply current shaping of the bridgeless SEPIC converter with coupling is evaluated and compared with converter without coupling at rated supply voltage and load conditions.

The Figure 3.12 shows the comparison of harmonic spectrum of supply current for bridgeless SEPIC with coupling (Figure 3.12a) and for the converter without coupling (Figure 3.12b). The converter topology with coupled inductors draws supply current



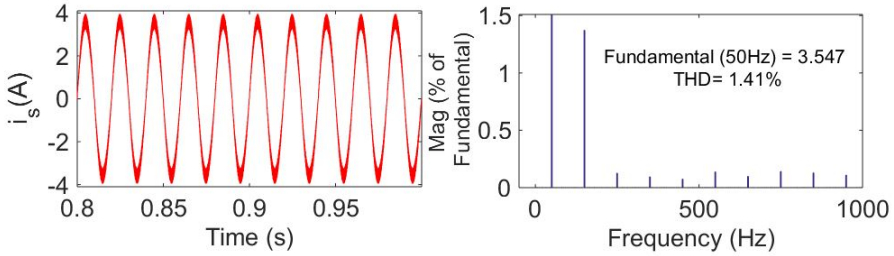
(a) For supply cycle



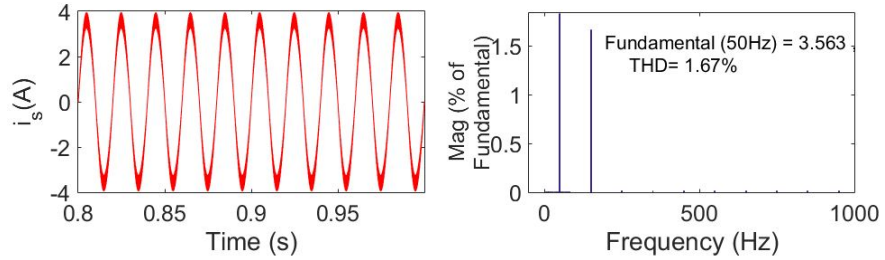
(b) For switching cycle

Figure 3.11: Voltage and current stresses on switching devices

of reduced THD (1.41 % $<$ 1.67 %) and improved PF (0.9991 $>$ 0.9989) for the same controller parameters. This ensures the selection of coupling parameters is effective in diminishing the impact of resonance between SEPIC inductance and intermediate capacitance at rated conditions.



(a) For SEPIC converter with coupling



(b) For SEPIC converter without coupling

Figure 3.12: Harmonic spectrum of supply current

3.8.3 Conclusion

In this work, a compact and efficient bridgeless SEPIC is presented with reduced structure complexity to obtain an improved quality of supply current and to get a wide variation of DC output voltage. The compactness in the circuit is achieved with the incorporation of coupling between input and output side inductors. With coupling, effectively, the self-inductance required for the same performance gets reduced. Coupling of the input side and output side inductors are judiciously done by using the split winding scheme. The split winding scheme is presented for achieving the desired coupling coefficient in this work. The magnetic design involving the calculation of core and winding geometry for coupled inductors are given. The theoretical evaluation of magnetic design is demonstrated, which shows the reduction in size, cost, and increase in efficiency compared to converter without coupling for the same rating. From the simulation results, it can be concluded that the proposed converter exhibits the desired performance as that of the conventional converter with a reduction in the size, cost, and

improved efficiency. The quality of supply current is also improved comparatively with improvement in power factor and THD.

3.9 SUMMARY

In this chapter, bridgeless SEPIC with coupled inductors is exhibited as a compact and efficient solution comprising of qualities like reduced structure complexity, single low side gate driver requirement, absence of circulating current, and use of voltage-mode control. The effect of coupling on the converter design is analyzed, the design of the converter with coupling is discussed, and the selection of components is detailed. The major contribution of the work, realizing the magnetic structure for loosely coupled inductors, is presented. Loss and efficiency estimation are done mathematically; simulation results are discussed, which shows the effectiveness of the front end circuitry proposed for the wide range output voltage and improved quality supply current. The next chapter deals with the speed control of BLDC motor employing the proposed bridgeless SEPIC converter at the front end to accomplish PAM control of VSI. One cycle controlled Bridgeless SEPIC converter with coupling is proposed for PAM control based BLDC motor drive. The performance of PAM control based BLDC motor drive with PI and one cycle control employed in the voltage control loop is evaluated.

Chapter 4

PAM controlled BLDC motor drive using one-cycle controlled bridgeless SEPIC with coupled inductors

4.1 INTRODUCTION

PAM controlled BLDC motor drive using bridgeless SEPIC with coupled inductors presented in Chapter 3, is proposed to improve the efficiency and to achieve the reduction in size and cost of the front end circuitry of the BLDC motor drive. In the proposed work presented in chapter 3, the speed feedback is utilised to generate the reference DC voltage using PI controller in the outer speed control loop. This approach provides accurate speed control as compared to the conventional methods used to generate reference voltage without sensing the speed. The objective of the work presented in this chapter, is to introduce one-cycle control (OCC) technique in the inner voltage control loop for PAM controlled BLDC motor drive possessing bridgeless SEPIC with coupled inductors at the front end to enhance the performance with improved start-up and transient state response and to improve the quality of supply current.

The system description of proposed PAM controlled BLDC motor drive is explained in Section 4.2. The control sytem of PAM controlled BLDC motor drive is de-

scribed in Section 4.3. The simulation results are discussed in Section 4.4. The model based implementation of digital controller using Xilinx System Generator design tool is analysed using Co-simulation results as discussed in Section 4.5. The conclusion of the work is given in 4.6 and chapter is summarized in Section 4.7.

4.2 SYSTEM DESCRIPTION OF PROPOSED PAM CONTROLLED BLDC MOTOR DRIVE

The block diagram of PAM controlled BLDC motor drive using bridgeless SEPIC with coupled inductors is shown in Figure 4.1. Wide variation of DC link voltage for VSI is supplied by bridgeless SEPIC with coupled inductors at the front end. Bridgeless SEPIC with coupled inductors is operated in DCM mode, in order to apply simple voltage follower approach to control the DC link voltage and also to give the benefit of inherent power factor correction. Three-phase VSI is operated at fundamental switching frequency for electronic commutation of BLDC motor. Switching logic for VSI is implemented according to the hall sensing signals.

Coupled inductors make use of single core for two windings of lesser self inductance values compared to conventional converter of same rating. Thus reduces size and cost of the system, also reduces core losses as discussed in Chapter 3. So the proposed system can achieve speed control with less cost, compactness and higher efficiency compared to conventional bridgeless SEPIC fed BLDC motor drive.

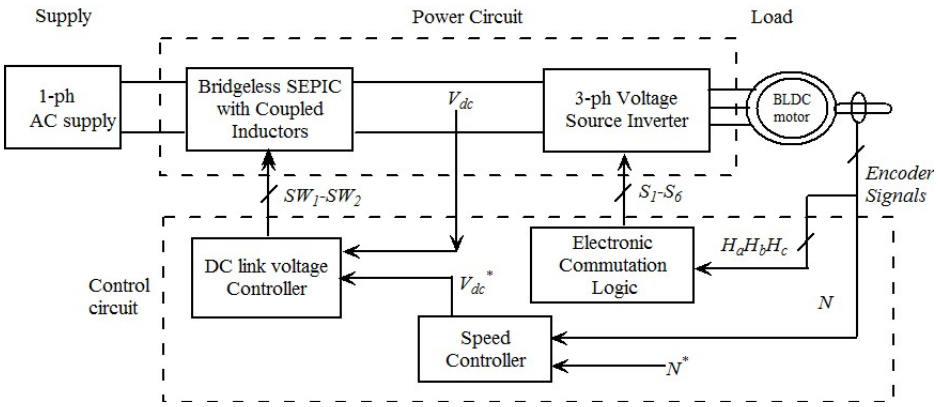


Figure 4.1: Block diagram of proposed BLDC drive with PAM control using Bridgeless SEPIC with Coupled Inductors

A dual loop speed control unit consisting of outer speed control loop and inner

DC link voltage control loop is utilized to improve accuracy of the speed control. The dual loop controller provides switching signals for front end SEPIC converter to control DC link voltage. The reference DC link voltage is obtained from outer speed controller which processes error between actual speed and reference speed. The VSI is switched at frequency corresponding to synchronous speed using electronic commutation logic which generates switching signals corresponding to rotor position.

The overall system shown in Figure 4.2, consists of the proposed front end converter to supply adjustable DC link voltage to the VSI fed BLDC motor. The VSI serves as an electronic commutator operating at frequency corresponding to synchronous speed. The switching signals for SEPIC are obtained by dual loop speed controller and switching signals for VSI are obtained from electronic commutation logic. The performance of proposed system is further improved by using one cycle control technique in the DC link voltage control loop.

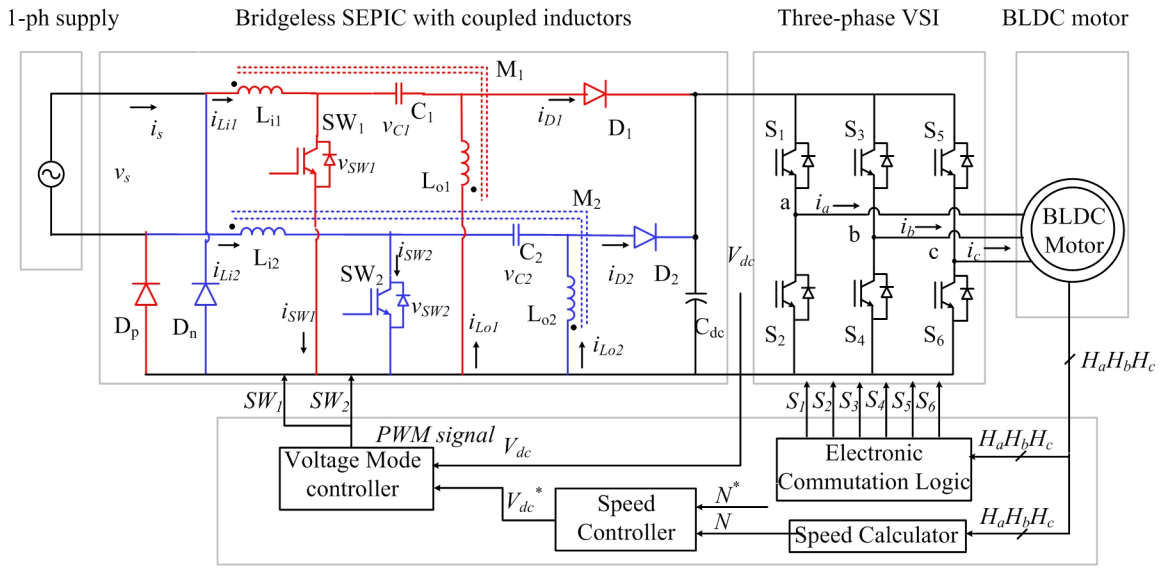


Figure 4.2: Circuit diagram of proposed BLDC drive with PAM control using Bridgeless SEPIC with Coupled Inductors

The operation, design and analysis of front-end AC-DC converter is presented in the previous chapter. The approach of voltage follower control scheme for the front end converter to obtain the supply current shaping along with output voltage control is dealt in following subsection. The design of VSI and determining the rating of VSI

corresponding to BLDC motor rating is also given.

4.2.1 Voltage follower based bridgeless SEPIC with coupled inductors

It is well known from the literature that, the SEPIC converter operating in DCM gives inherent power factor correction and suffices voltage follower PFC control scheme. This can be understood by cosidering the nature of supply current during a switching interval. The expanded view of supply current for switching duration is shown in Figure 4.3.

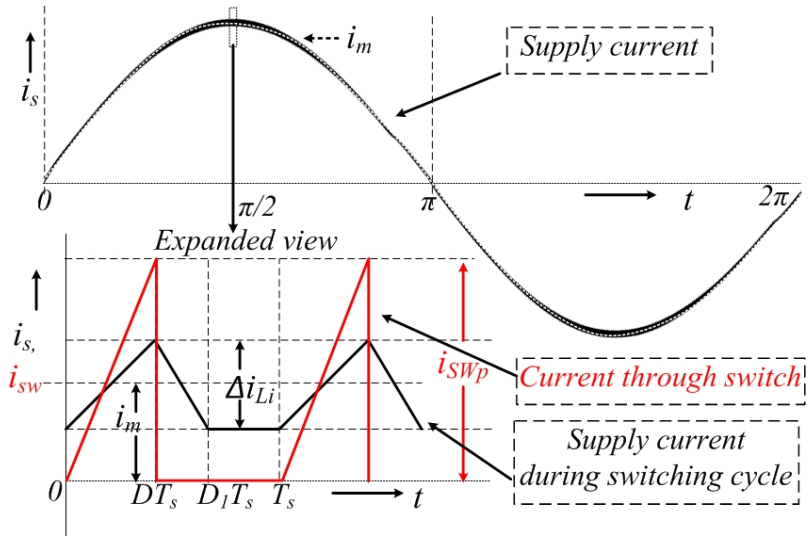


Figure 4.3: Supply current

The average current i_m over a switching period can be calculated using i_{sw}, the current through switch, as given by (4.1).

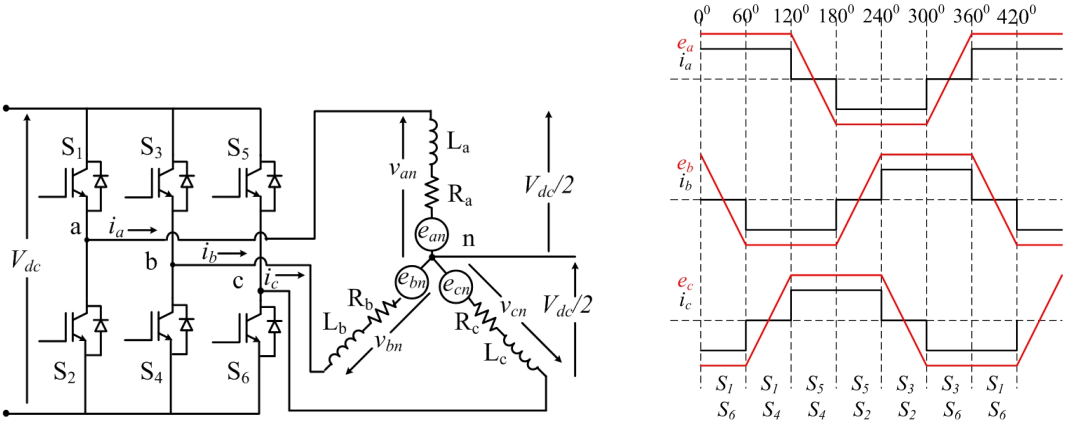
$$i_m = \frac{1}{2} \times D \times i_{swp} = \frac{1}{2} \times D \times \frac{v_s D T_s}{L_{Teq}} = \frac{D^2 T_s}{2 \times L_{Teq}} \times V_m |sin\omega t| \qquad (4.1)$$

From (4.1), it is obvious that, the average value of supply current over a switching period is proportional to supply voltage v_s, for a fixed duty raio and switching period. The supply current follows the supply voltage, updating its value proportional to $V_m|sin\omega t|$ at every high frequency switching interval. Thus achieves inherent power factor correction, and hence it eliminates the need for supply current sensing and inner current control loop. The converter can be operated in voltage mode control to obtain wide range of output voltage. Accordingly, it can be used for speed control of BLDC

motor using PAM control approach, operating the VSI only to serve the purpose of commutation of motor phase currents.

4.2.2 Three phase VSI for electronic commutation

The BLDC motor is electronically commutated using three phase VSI. The VSI is operated in 120^0 conduction mode to supply symmetrical square current pulses of 120^0. The circuit diagram of VSI fed BLDC motor and waveforms of back emf and phase current corresponding to 120^0 commutation are shown in Figure 4.4.



(a) Circuit Diagram of VSI fed BLDC motor

(b) 120º commutation: Back EMF and phase current waveforms

Figure 4.4: VSI fed BLDC motor

The VSI is switched depending on rotor position to energize the correct phase of motor windings. The switching devices required to be turned ON at each interval of 60^0 to provide corresponding back emf are identified from the circuit diagram shown in Figure 4.4a and are mentioned in the Figure 4.4b for each interval.

The motor terminal voltage can be expressed in terms of motor parameters like winding resistance ($R_{ph} = R_a = R_b = R_c$), inductance ($L_{ph} = L_a = L_b = L_c$) and back emf (e_{ab}) as given by (4.2) (Ho et al., 2015).

$$v_{ab} = 2iR_{ph} + 2L_{ph}\frac{di}{dt} + e_{ab} \tag{4.2}$$

where $e_{ab} = K_e N$; K_e is the back emf constant of motor.

The line voltage (v_{ab}) across terminals 'a' and 'b' due to six step inverter operation

is given by $v_{ab} = 0.78V_{dc}$ (Krishnan, 2017). Hence the speed of the motor (N) in terms of DC link voltage can be obtained by (4.3).

$$N = \frac{0.78V_{dc} - 2iR_{ph} - 2L_{ph}\frac{di}{dt}}{K_e} \tag{4.3}$$

Thus the speed of the motor (N) can be controlled by controlling DC link voltage of the VSI (V_{dc}). Commonly, the reference DC link voltage V_{dc} for the PAM controlled BLDC motor drive systems, is generated approximately by multiplying with the proportionality constant as ($N = k_v \times V_{dc}$). Precise speed control necessitates speed feedback to generate reference DC link voltage. Dual loop speed control using speed feedback is dealt more in detail in Section 4.3. The design of VSI and selection of rating of switching devices is discussed below.

4.2.2.1 Design of VSI

The design of VSI for BLDC motor drive involves choosing the DC link voltage and current ratings depending on motor ratings. The switching devices are selected based on the corresponding voltage and current rating.

The DC link voltage (V_{dc}) is a function of motor speed (N), given as $V_{dc} \propto k_v N$. The control of speed using PAM control of VSI, requires wide range of variation in V_{dc}. The voltage rating of VSI can be decided based on the DC link voltage corresponding to maximum speed(N_{max}) and is given by $V_{dc} > k_v N_{max}$.

The DC link current (I_{dc}) in BLDC motor drive is a function of motor torque (T), as given by $I_{dc} \propto k_t T$. The DC link current is decided based on maximum motor loading (T_{max}), which is given as $I_{dc} \propto k_t T_{max}$.

4.2.2.2 Selection of switching devices

The switching devices for VSI are choosen based on maximum voltage stress on the device, the maximum current flow through the device and switching frequency. The maximum voltage stress when the switch is open is V_{dc}. The maximum current through

the switch is line current of the three-phase system which is equal to I_{dc}. Generally, the switching device ratings are chosen with voltage and currents much greater than the design values to avoid device failure.

Another major parameter for switching device selection is switching frequency (f_s). The frequency of operation in PAM control method, depends to speed of motor and it is given by $f_s = \frac{PN}{120}$. The device with switching frequency much greater than frequency corresponding to maximum speed of motor is choosen and is expressed as $f_s > \frac{PN_{max}}{120}$.

4.3 CONTROL SYSTEM OF PROPOSED PAM CONTROLLED BLDC MOTOR DRIVE

PAM control of three-phase VSI is used to achieve the speed control in the proposed BLDC motor drive. The control flow schematic of proposed drive is as shown in Figure 4.5. It consists of

- **Generation of switching logic for VSI:** The VSI is switched at fundamental frequency corresponding to rotor position signals obtained using hall sensors. Switching logic implemented for VSI is known as Electronic Commutation Logic.

- **Outer speed control loop:** The actual speed is sensed and compared with reference speed. The reference DC voltage is generated by using a PI controller, for which the input is the difference between actual speed and desired speed. The reference DC voltage so obtained is given as input to the inner voltage control loop.

- **Inner DC bus voltage control loop:** Inner voltage control loop generates the switching signal for the for the switches of the bridge-less SEPIC with coupled inductors.

4.3.1 Generation of switching logic of VSI

The switching logic for VSI depends on rotor position.

The electronic commutation logic to generate switching signals for VSI is de-

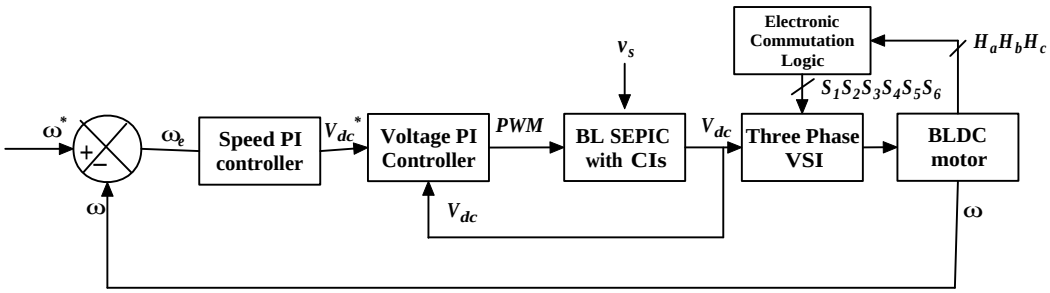


Figure 4.5: Control flow schematic

termined by hall sensing signals. The switching pattern for the corresponding rotor position is shown in Table 4.1. The switch-on and switch-off conditions of the IGBT's are represented as '1' or '0', respectively. From Figure 4.4a, the output voltage of the inverter of phase 'a' with respect to the potential at point 'n' is given as:

$V_{an} = V_{dc}/2$ for $S_1 = 1$

$V_{an} = -V_{dc}/2$ for $S_2 = 1$

$V_{an} = 0$ for $S_1 = 0, S_2 = 0$

where '1' and '0' represent the 'on' and 'off' conditions of the IGBT's, respectively.

The voltages for other two phases of the VSI feeding BLDC motor i.e v_{bn}, v_{cn} and the switching pattern of other IGBTs of the VSI (i.e.S_3, S_4, S_5, S_6) is generated in a similar way as can be seen in Table 4.1.

4.3.2 Outer speed control loop using PI controller

In this work, the PAM approach for speed control is realized using dual loop control using the inner voltage control loop and outer speed control loop. The outer speed control loop consists of a PI controller, which is used to generate the reference DC voltage V_{dc}^* for the inner voltage control loop.

The outer loop has a comparator to produce the speed error N_e, by comparing actual speed N with reference speed N^*. Speed error at k^{th} instant is given by (4.4).

Table 4.1: Excited phase voltages and corresponding switching states based on hall effect position sensor signal.

θdeg	Hall signal			Switching Sequence						Phase Voltages		
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6	V_{an}	V_{bn}	V_{cn}
NA	0	0	0	0	0	0	0	0	0	–	–	–
0-60	1	0	1	0	0	1	0	0	1	0	$V_{dc}/2$	$-V_{dc}/2$
60-120	1	0	0	0	1	1	0	0	0	$-V_{dc}/2$	$V_{dc}/2$	0
120-180	1	1	0	0	1	0	0	1	0	$-V_{dc}/2$	0	$V_{dc}/2$
180-240	0	1	0	0	0	0	1	1	0	0	$-V_{dc}/2$	$V_{dc}/2$
240-300	0	1	1	1	0	0	1	0	0	$V_{dc}/2$	$-V_{dc}/2$	0
300-360	0	0	1	1	0	0	0	0	1	$V_{dc}/2$	0	$-V_{dc}/2$
NA	1	1	1	0	0	0	0	0	0	–	–	–

$$N_e(k) = N^* - N \tag{4.4}$$

This speed error is processed by PI controller, which generates reference voltage V_{dc}^* for the DC voltage controller as given by (4.5).

$$V_{dc}^*(k) = V_{dc}^*(k-1) + k_p\{N_e(k) - N_e(k-1)\} + k_i N_e(k) \tag{4.5}$$

where k_p is proportional gain and k_i is integral gain of the speed PI controller. Using this reference DC link voltage inner voltage control loop facilitates control of DC link voltage by modulating switching signals of bridgeless SEPIC converter.

4.3.3 Inner voltage control loop using PI controller

The inner voltage control loop, generates the duty ratio d signal for front end converter. The DC link voltage controller using conventional PI voltage controller consists of a comparator to obtain DC bus voltage error V_e, by comparing actual voltage V_{dc} with reference voltage V_{dc}^*.

Voltage error at k^{th} instant is given by (4.6).

$$V_e(k) = V_{dc}^* - V_{dc} \tag{4.6}$$

This voltage error is processed by PI controller, which gives duty ratio d for modulating pulse width for front end SEPIC converter as given by (4.7).

$$d(k) = d(k-1) + k_{pv}\{V_e(k) - V_e(k-1)\} + k_{iv}V_e(k) \tag{4.7}$$

where k_{pv} is proportional gain and k_{iv} is integral gain of the speed PI controller.

To overcome limitations of PI controller and to improve the performance during starting and transient states, the one cycle control technique is adopted in inner voltage control loop as described below.

4.3.4 Inner voltage control loop using one-cycle control technique

The schematic diagram for implementation of One Cycle Control technique is illustrated in Figure 4.6. The main components are resettable integrator, a comparator, and a D-flipflop. A clock of constant frequency ($f_s = 1/T_s$) for flipflop determines turning ON of the switch. The integrator starts operating immediately when the switch is turned ON. The sensed output voltage from the SEPIC converter is fed to the integrator. The integrator output is given to comparator, which compares it with the reference signal V_{dc}^*. The instant at which the output from the integrator matches the reference voltage V_{dc}^*, a high pulse is produced by the comparator which resets the flipflop. Immediately, the switching device turns OFF and the integrator is reset. Thus, it helps in maintaining the average value of the actual voltage to be equal to the reference voltage.

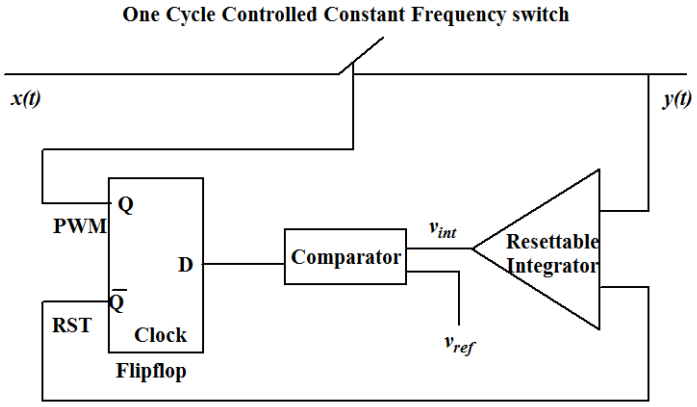


Figure 4.6: One Cycle Controlled constant frequency switch

The operation of the switch in each cycle is determined by the switching function

$d(t)$ at a frequency $f_s = \frac{1}{T_s}$, as shown in (4.8)

$$d(t) = \begin{cases} 1 & 0 \leq t \leq T_{ON} \\ 0 & T_{ON} \leq t \leq T_s \end{cases} \tag{4.8}$$

In this work, the $x(t)$ marked in Figure 4.6 represents the input DC voltage $v_{in}(t)$ of the SEPIC converter and the output $y(t)$ represents the output voltage $V_{dc}(t)$ of SEPIC converter.

Assuming the input to the switching converter as $x(t)$, the signal transmitted to the output of the converter is given by (4.9)

$$\begin{aligned} y(t) =& x(t) \times d(t) \\ i.e., y(t) =& \frac{1}{T_s} \int_0^{T_{ON}} x(t)dt \end{aligned} \tag{4.9}$$

If the duty ratio of the switch is adjusted such that integration of the the output voltage over a switching cycle is exactly equal to the integration of the reference voltage as shown in (4.10)

$$\int_0^{T_{ON}} x(t)dt = \int_0^{T_s} V_{dc}^*(t) \tag{4.10}$$

then the mean of the signal becomes equal to the mean value of reference voltage in each cycle, as given in the (4.11)

$$y(t) = \frac{1}{T_s} \int_0^{T_{ON}} x(t)dt = \frac{1}{T_s} \int_0^{T_s} v_{ref}(t) = V_{dc}^*(t)$$

$$y(t) = \frac{1}{T_s} \int_0^{dT_s} x(t)dt = V_{dc}^*(t) \tag{4.11}$$

This operation is repeated for every switching cycle and the output voltage is controlled to be equal to the reference voltage.

4.4 SIMULATION RESULTS AND DISCUSSIONS

BLDC motor rated for speed of 3000 rpm, with rated power of 375 W and rated torque of 1.2 Nm has been used in the proposed BLDC drive. The design of bridgesless SEPIC with coupled inductors is done for rated power of 500 W and the design values of components are given in Table 3.1. The simulink model of the proposed BLDC drive is developed and is tested for speed control performance under rated load torque and rated supply voltage of 220 V under steady-state and dynamic conditions. Table 4.2 shows the BLDC motor parameters used in the simulation.

Table 4.2: BLDC motor parameters

Sl.No	Parameters	Value
1	No.of Poles	4
2	Rated Power	375 W
3	Rated Voltage	310 V
4	Rated Torque	1.2 Nm
5	Rated Speed	3000 RPM
6	Stator phase resistance, R_s	14.56Ω
7	Stator phase inductance, L_s	25.71mH
8	Back emf constant	78 V/krpm
9	Torque constant	0.74 Nm/A

Performance of the drive is analysed for one cycle controller and compared with conventional PI control technique.

4.4.1 Performance of proposed BLDC drive with PAM control during steady-state for rated speed

Steady state performance of PAM controlled BLDC motor drive is analysed for rated torque of the motor. Waveforms of (i) DC link voltage, (ii) speed, (iii) back emf (iv) stator current and (v) electromagnetic torque are shown in Figure 4.7.

Waveform (i), shows the DC link voltage of rated value supplied to VSI fed BLDC motor. The speed of BLDC motor settles to rated value as shown in waveform (ii) of Figure 4.7. BLDC motors with trapezoidal back EMF as shown in waveform (iii), must be ideally supplied from three phase square current pulses of 120° duration with 60° phase difference to get constant torque without ripples. As can be seen in waveform (iv), Figure 4.7, the phase current is not perfect square wave. The currents through

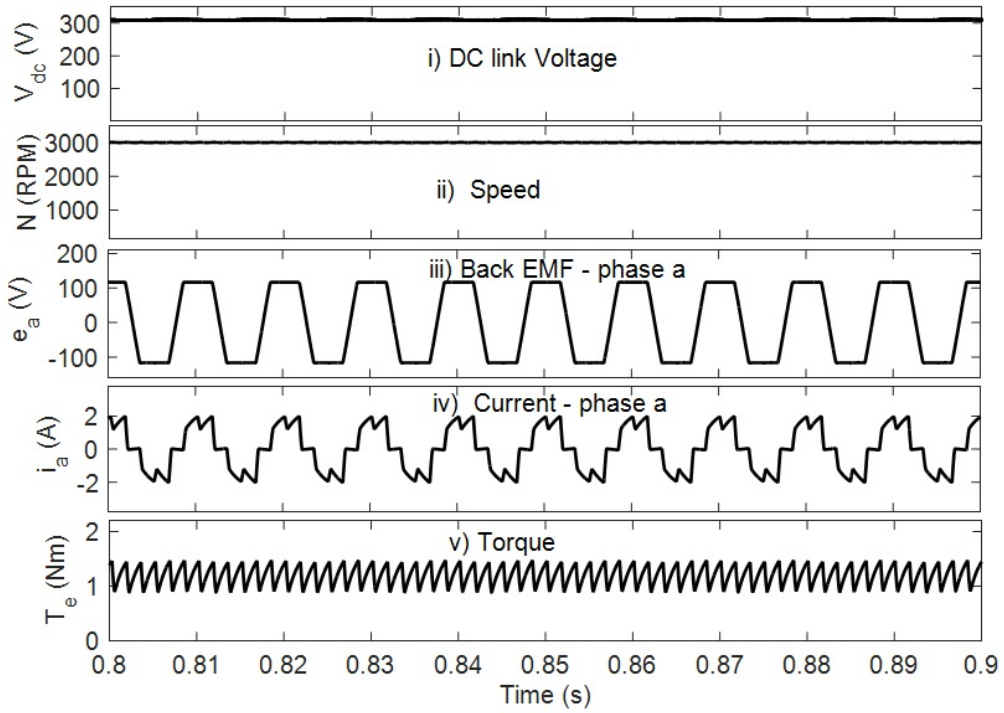


Figure 4.7: Performance of PAM controlled BLDC motor drive

phase windings cannot rise or fall instantaneously because of winding inductance. So the phase current commutations cause ripple in the torque as seen in waveform (v), Figure 4.7.

4.4.2 Performance comparison of proposed BLDC drive with PAM control during starting

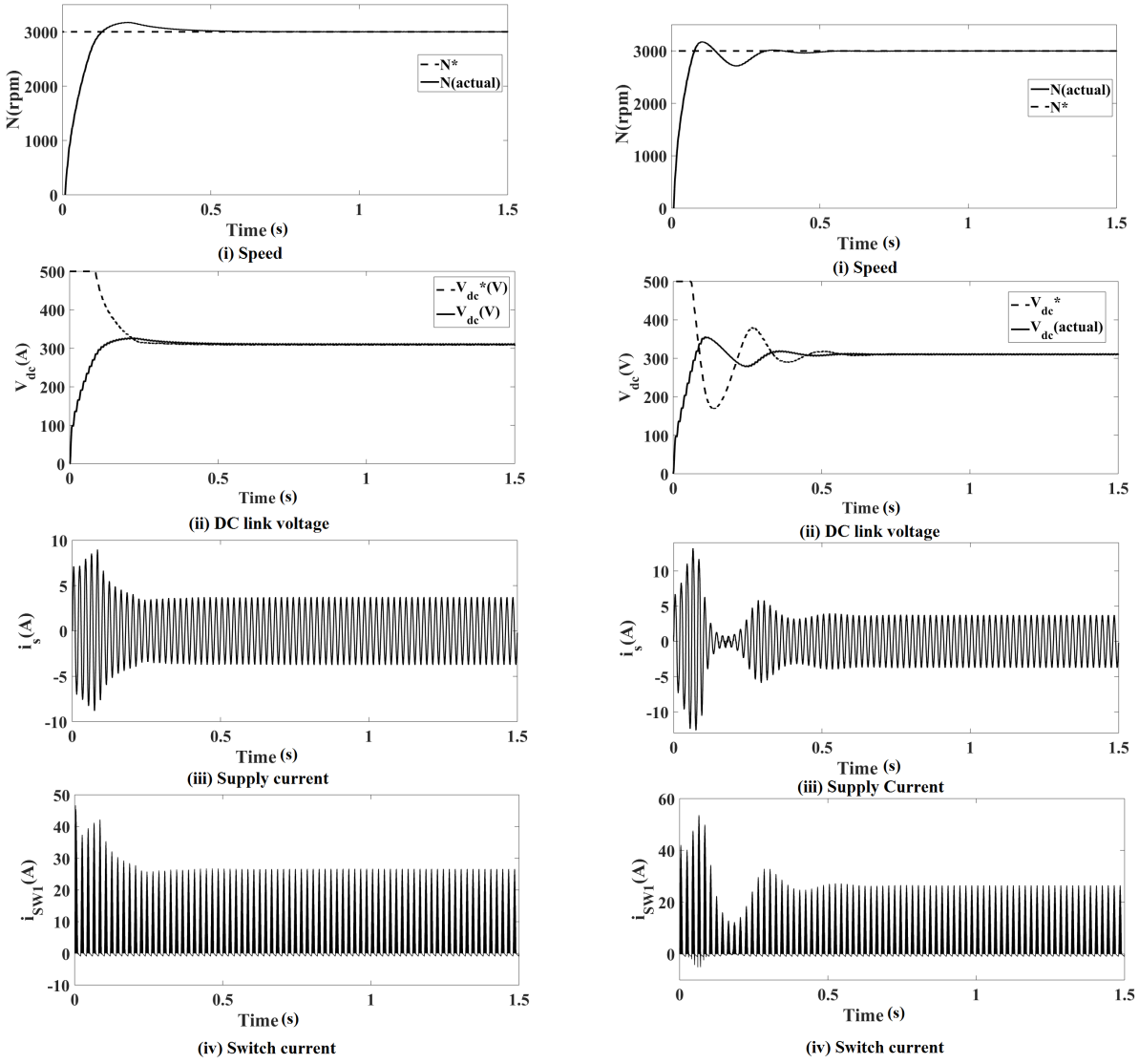
Dual loop control is used with an outer speed control loop and inner voltage control loop. PI controller is used in the outer speed control loop. The inner voltage control is implemented using PI and also one cycle controller. The inner voltage control loop has faster response compared to the outer speed control loop. So the PI controller in inner voltage loop has to be tuned first. The MATLAB/Simulink auto tuning algorithm is used to obtain the PI controller paarameters for the inner voltage control loop. The output voltage to control transfer function $\frac{vo(t)}{d(t)}$ of pulse width modulated SEPIC in DCM is obtained reffering to (De Vicuna et al., 1989). This linearised plant model is utilised in the controller design using auto-tuning method in MATLAB software. The controller

is tuned such that, it gives optimal performance in terms of its response to a step voltage input. Also, THD of the supply current is checked to be within the specified limits given by IEC-61000-3-2. Similar procedure is adopted for tuning the outer speed control loop considering the speed to dc link voltage transfer function $\frac{\omega(t)}{V_{dc}(t)}$.

The PI controller in the speed control loop (outer loop) is designed to obtain a speed response with peak overshoot of 5.6 % and settling time of 0.6 s. The performance of BLDC drive is evaluated for One Cycle Control and PI control in the DC bus voltage control loop (inner loop). Achievement of better transient state performance of the BLDC drive with One Cycle Control in the inner loop is discussed.

Figure 4.8 shows the comparison of speed control performance of the drive with One Cycle Control and PI control techniques for speed reference set to rated value of 3000 rpm, under rated supply voltage and load torque conditions. Figure 4.8a shows the performance waveforms of (i) speed (N) (ii) DC link voltage (V_{dc}) (iii) supply current (i_s) and (iv) switch current (i_{sw1}) for PAM-BLDC drive with One Cycle Control Technique and Figure 4.8b depicts the respective performance waveforms of PAM-BLDC drive with PI Control Technique.

From the Figure 4.8, it can be seen that, PI controller (4.8b) has more oscillatory transients at the starting compared to One Cycle Controller (4.8a). It is evident from the speed response waveform (i) of Figure 4.8b and this gets reflected in the inner voltage control loop as depicted by DC link voltage waveform (ii). Further, the supply current shown in waveform (iii) of 4.8b and 4.8a, has larger peak overshoot of 2.8 times the rated current with PI controller, and 1.5 times the rated value with One Cycle Controller respectively. Because of this, the current stress on switching devices is more in case of PI controller as shown in waveform (iv) of Figure 4.8b. One Cycle Controller results in low stress on switching devices and similarly on other components of the circuit such as inductors and capacitors. Hence, the ratings of components of PAM-BLDC drive gets reduced with One Cycle Controller.



(a) Performance of the drive with One Cycle Control

(b) Performance of the drive with PI Control

Figure 4.8: Transients at start of BLDC drive with PAM control using Bridgeless SEPIC with Coupled Inductors for rated speed, under rated load and rated supply voltage conditions

4.4.3 Performance comparison of proposed BLDC drive with PAM control at steady-state for different speeds

Comparison based on power quality indices like power factor and % THD is done at different speeds under steady state for the PAM BLDC drive using One Cycle Control and PI control techniques. The supply voltage and load torque are maintained at rated values. Speed reference is changed and performance is analysed, power quality indices have been tabulated in Table.4.3 for different speeds. Inherent power factor correction with voltage mode control of bridgeless SEPIC with Coupled Inductors is evident from the results for the entire range of speed control (300 rpm-3000 rpm). One Cycle Control enhances the performance of the system compared to the PI controller in regards to reduction in % THD of supply current and improvement in power factor.

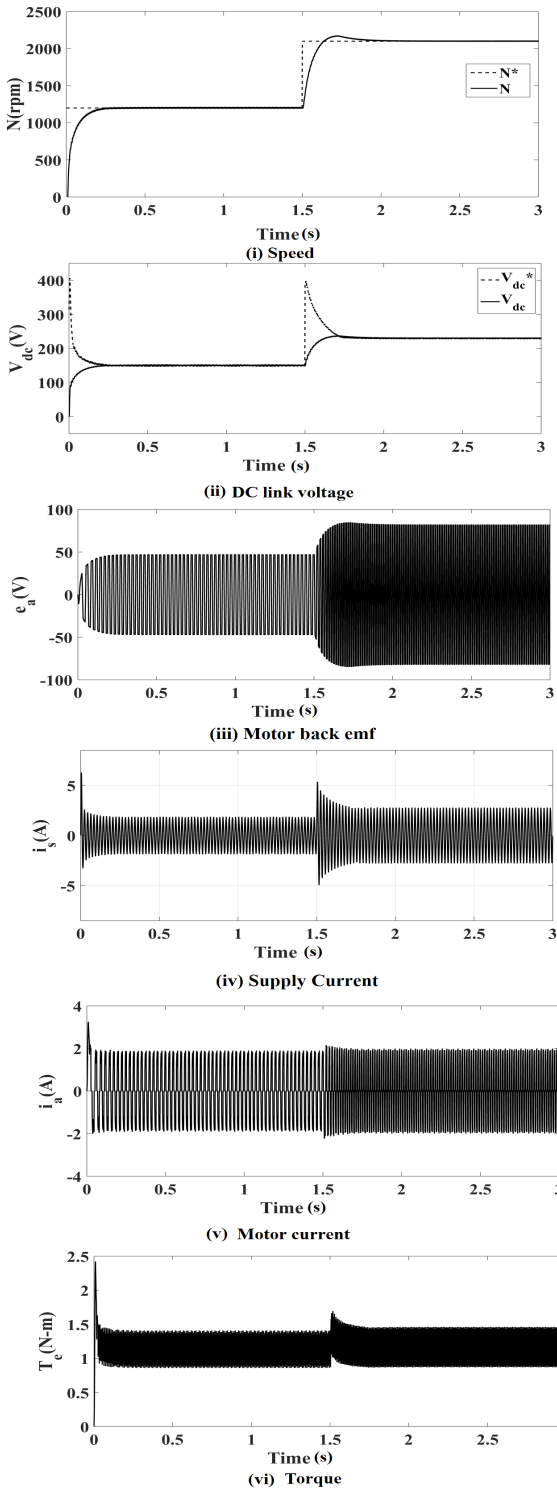
Table 4.3: Steady state performance of proposed BLDC drive with PAM control at different speeds.

$N*$(rpm)	N(rpm)	V_{dc}^{*}(V)	V_{dc}(V)	I_s(A)	%THD		PF	
					OCC	PI	OCC	PI
300	300	72.5	72.5	0.6266	5.79	6.13	0.9951	0.9950
600	600	98.2	98.2	0.8287	5.26	5.27	0.9978	0.9965
900	900	124.5	124.5	1.0330	4.39	4.67	0.9986	0.9973
1200	1200	150.5	150.5	1.2395	4.26	4.28	0.9991	0.9989
1500	1500	176.8	176.8	1.4495	4.00	4.07	0.9992	0.9991
1800	1800	203	203	1.6630	3.42	3.80	0.9995	0.9992
2100	2100	230	230	1.879	3.22	3.62	0.9995	0.9994
2400	2400	257	257	2.0986	3.01	3.49	0.9994	0.9993
2700	2700	283	283	2.32	2.96	3.38	0.9992	0.9992
3000	3000	310	310	2.547	2.81	3.29	0.9992	0.9990

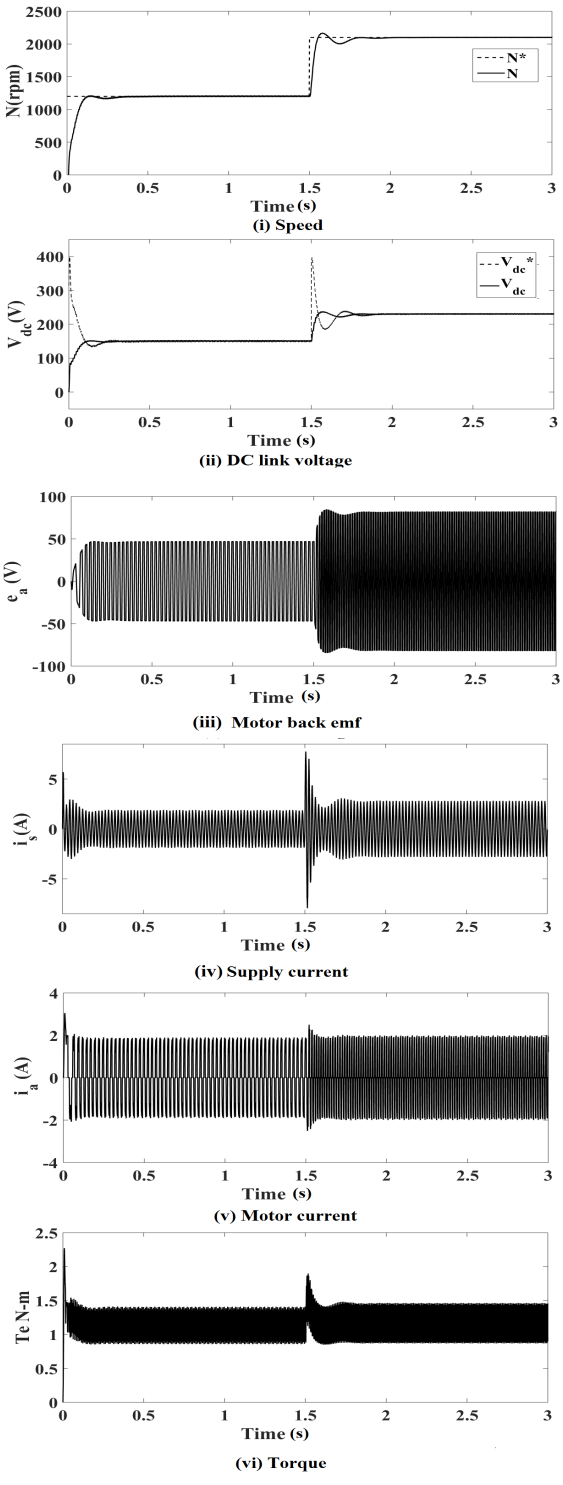
4.4.4 Performance comparison of proposed BLDC drive with PAM control for dynamic step change in reference speed

The dynamic performance of proposed BLDC drive with PAM control is evaluated for a step change in the reference speed. This is achieved by giving a step change in the reference speed from 1200 rpm to 2100 rpm at the time of 1.5 s, at rated torque and supply voltage conditions as shown in Figure 4.9. Figure 4.9a presents the performance waveforms of (i) speed (N) (ii) DC link voltage (V_{dc}) (iii) motor back emf (e_a) (iv) supply current (i_s) (v) motor phase current (i_a) and (vi) motor torque (T_e) for PAM-BLDC drive with One Cycle Control technique, and Figure 4.9b shows the

respective performance waveforms of PAM-BLDC drive with PI Control technique for step change in speed.



(a) Performance of the drive with One Cycle Control



(b) Performance of the drive with PI Control

Figure 4.9: Dynamic performance of the BLDC Drive PAM- for step change in refrence speed

BLDC drive with PI controller has comparatively higher dynamic transient oscillations in the speed response at the step change instant of 1.5 s, as shown in waveform (i) of Figure 4.9b. The change in DC bus voltage from 150 V to 230 V, corresponding to step change in speed reference from 1200 rpm to 2100 rpm respectively can be seen in the DC link voltage waveform (ii) of Figure 4.9a and Figure 4.9b. The larger transient oscillations in the DC link voltage of PI controlled BLDC drive results in higher transients in the back emf as shown in waveform (iii) of Figure 4.9b. The supply current waveform (iv) of Figure 4.9b, shows that the BLDC drive with PI controller has larger overshoot of 2.8 times the steady state value at the instant of step change. The supply current transient at the step change, effects in the motor current overshoot at step change instant which is shown in waveform (v) of Figure 4.9b. This causes higher torque overshoot for the BLDC drive with PI control as shown in waveform (vi) of Figure 4.9b. Overall analysis, shows the better performance by BLDC drive with One Cycle Control for dynamic step change in reference speed.

4.4.5 Control Performance assessment

The control performance for step response can be analysed using the significant performance indices like, Integral Absolute Error (IAE), Integral Square Error (ISE), Integral Time Absolute Error (ITAE) and Integral Time Square Error (ITSE) per unit basis, where

Integral Absolute Error is given by (4.12)

$$IAE = \int |e| dt \tag{4.12}$$

Integral Square Error is given by (4.13)

$$ISE = \int e^2 dt \tag{4.13}$$

Integral Time Absolute Error is given by (4.14)

$$ITAE = \int t|e| dt \tag{4.14}$$

Integral Time Square Error is given by (4.15)

$$ITSE = \int te^2 dt \tag{4.15}$$

Control performance assessment indices is given in Table 4.4. The results are tabulated for reference speeds of 3000 rpm, 2100 rpm and 1200 rpm. It can be seen from Table 4.4 that, the One Cycle Control displays the improved values of performance indices compared to PI control, indicating the enhanced control performance.

Table 4.4: Control Performance Assessment Indices.

Performance Index	N=3000		N=2100		N=1200	
	OCC	PI	OCC	PI	OCC	PI
ISE	0.04129	0.04783	0.0348	0.0359	0.02162	0.02631
IAE	0.08384	0.101	0.07913	0.0828	0.06182	0.06569
ITSE	0.001828	0.003486	0.0015	0.0024	0.0007685	0.0009227
ITAE	0.01011	0.01454	0.01034	0.0192	0.01275	0.01431

4.5 CO-SIMULATION RESULTS AND DISCUSSIONS

Generally, DSP, microcontroller, FPGA, etc. are used for the real-time implementation of control algorithms. Due to the parallel processing feature, FPGA has the higher speed. The FPGA is also recommended due to the characteristics like adaptability, higher accuracy, easiness of control implementation, etc.

The Xilinx FPGA provide a model-based design tool known as System Generator for implementation of control algorithm (Rajesh et al., 2014). The hardware co-simulation feature in the system generator environment enables automatic generation of the bitstream file for programming the FPGA. The controller designed and tested with FPGA in the hardware co-simulation ensures its use directly with the actual system which allows the designer for faster development of the circuits using FPGA (Pinto et al., 2017). The proposed work utilizes the benefit of hardware co-simulation feature to assess the overall control system.

The Simulink model of the proposed BLDC drive with PAM control is developed and is evaluated for its control performance at rated load torque. The control system

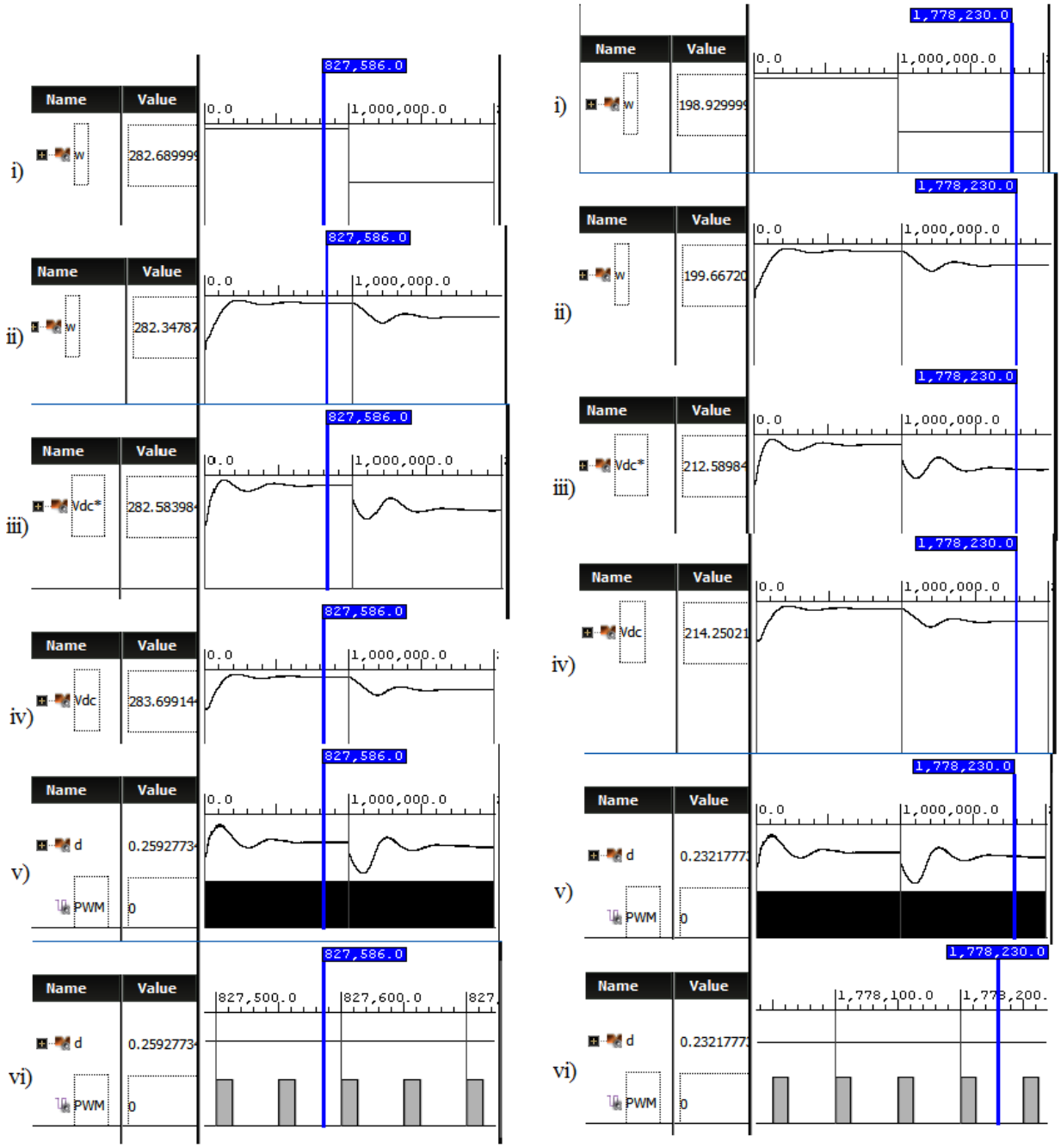
of proposed BLDC drive is implemented digitally in a Xilinx FPGA. This work uses Xilinx System Generator model-based design tool that enables the use of the Simulink design environment for FPGA design. The built in feature of hardware co-simulation of the Zynq-7000 SoC ZC702 FPGA board is used to validate the controller with the results obtained in Xilinx waveform viewer. The controller implementation is verified, by co-simulation with the converter model implemented using Power System blocksets library of Simulink. The results are obtained for the dynamic step change conditions for both reference speed as well as supply voltage with Xilinx Waveform Viewer.

Figure 4.10a and 4.10b, are shown to describe steady state readings before and after the step change instant, for the reference speed command. Similarly, Figure 4.11a and 4.11b illustrate the steady state readings for a step change in supply voltage.

4.5.1 Step change in reference speed

The dynamic performance of the proposed BLDC drive with PAM control is evaluated for a step change in the reference speed. This is achieved by giving a step change in the reference speed from 2700 rpm (282.7 rad/s) to 1900 rpm (198.9 rad/s) at 1 s, for the rated torque of 1.2 Nm and supply voltage of 220 V conditions as shown in Figure 4.10. The steady state readings of performance waveforms of PAM controlled BLDC drive for the reference speed of 2700 rpm are depicted in of Figure 4.10a with i)reference speed ii)actual speed iii)referene DC voltage iv)actual DC voltage v) duty ratio and vi) PWM. Figure 4.10b displays the steady state values of the corresponding waveforms of PAM controlled BLDC drive for the reference speed of 1900 rpm.

The waveform i) of Figure 4.10a, is the reference speed command, with the value of 2700 rpm and waveform (i) of Figure 4.10b shows the reference command of 1900 rpm. The waveforms ii) of Figure 4.10a and 4.10b, show that the actual speed follows the reference command for the dynamic step change condition. The speed error processed through the PI controller results in the reference DC voltage command which is shown in waveform iii), with corresponding values of 282 V in Figure 4.10a and 212 V in Figure 4.10b respectively. The actual DC output voltage following the reference voltage command is seen in waveform iv) with a steady state value of 283 V in Figure



(a) Steady state value at speed of 2700 rpm (282.68 rad/s) **(b)** Steady state values at speed of 1900 rpm (198.92 rad/s)

Figure 4.10: Dynamic performance of the PAM controlled BLDC Drive for step change in reference speed. i)Reference speed ii) Actual speed iii) Referene DC voltage iv) Actual DC voltage v) Duty ratio vi) PWM

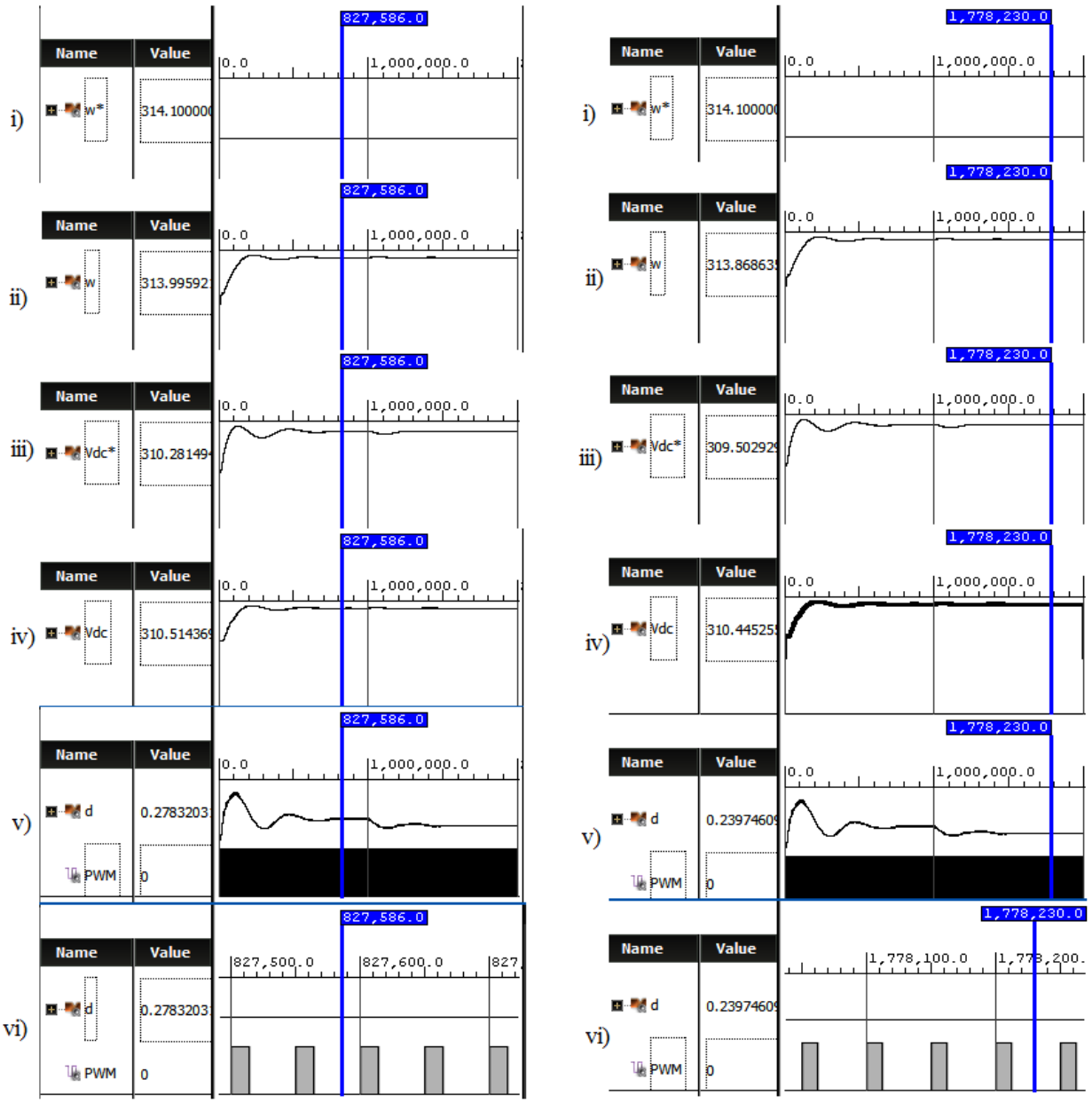
4.10a and with a steady state value of 214 V for the corresponding speed of 1900 rpm in Figure 4.10b.

The corresponding duty ratio and PWM generated for the SEPIC converter are also viewed using Xilinx waveform viewer and are shown in waveforms v) and vi) respectively of Figure 4.10a and 4.10b. This validates the adequate performance of the designed PAM controller with results obtained from hardware co-simulation for dynamic step change conditions in the reference speed.

4.5.2 Step change in supply voltage

The dynamic performance for a step change in the supply voltage for the proposed BLDC drive with PAM control is evaluated, by giving a step change in the supply voltage from 210 V to 250 V at the time of 1 s, at rated torque (1.2 Nm) and rated speed (3000 rpm) conditions as shown in Figure 4.11. Figure 4.11a demonstrates the performance waveforms of i)reference speed ii)actual speed iii)referenec DC voltage iv)actual DC voltage v) duty ratio and vi) PWM to display the steady state readings of PAM controlled BLDC drive for the supply voltage of 210 V and Figure 4.11b describes the steady state values of the respective performance waveforms for PAM controlled BLDC drive at the supply voltage of 250 V.

The reference command for speed as shown in waveform i) of Figure 4.11a and 4.11b is set to rated value of 3000 rpm for the step change in supply voltage condition. Waveform ii) of Figure 4.11a shows the actual speed following the reference command of 3000 rpm. When the supply voltage dynamic change is applied at 1 s, the actual speed settles to 3000 rpm, undergoing the transients at the step change instant as shown in waveform ii) of Figure 4.11b. The output of speed PI controller, which is a DC voltage reference command, is obtained to be 310 V at steady state as shown in the waveform iii) of Figure 4.11a and Figure 4.11b for the supply voltages of 210 V and 250 V respectively. The actual voltage at DC link is controlled at 310 V as shown in waveform iv) of Figure 4.11a and Figure 4.11b. The duty ratio variation for obtaining the 310 V output voltage with respective supply voltage variations is demonstrated with waveforms v) of Figure 4.11a and Figure 4.11b. The enlarged view for PWM



(a) Steady state values at supply voltage of 210 V

(b) Steady state values at supply voltage of 250 V

Figure 4.11: Dynamic performance of the PAM controlled BLDC Drive for step change in supply voltage. i)Reference speed ii) Actual speed iii) Referene DC voltage iv) Actual DC voltage v) Duty ratio vi) PWM

with switching period of 50 μs for corresponding duty ratios at steady state is illustrated in waveforms vi) of Figure 4.11a and Figure 4.11b. This ensures the satisfactory performance of FPGA based controller for the PAM controlled BLDC drive during the dyanamic condition of step change in supply voltage. The efficient design of controller in FPGA is justified with hardware co-simulation results and this guarantees its effective execution in the real time system.

4.6 CONCLUSION

One cycle controlled bridgeless SEPIC embedded with coupled inductors is presented for BLDC drive using PAM control of VSI. With the adoption of coupled inductors, the proposed bridgeless SEPIC converter employs lower self-inductance when compared to conventional bridgeless SEPIC topology. Hence two inductor windings of converter with less number of turns, wound on a same core results in reduction of size and cost. One cycle control for controlling DC bus voltage enhances the performance of the BLDC drive compared to PI controller. The evaluation of power factor and THD at steady state, shows better performance by one cycle control with improved power factor and reduced source current THD, over a wide speed range. With One Cycle Controller, oscillatory transients in the speed response at starting are reduced compared to PI controller. This lowers the supply current overshoot and thereby reduces the stress on the switch. Dynamic response of the BLDC drive for the step change in reference speed is also better with One Cycle Controller compared PI controller with lower supply current and torque overshoots at the instant of the step change. The control performance is assessed using IAE, ISE, ITAE, ITSE indices. Improved values of indices are obtained with One Cycle Controller, for different speeds. Hence one cycle control technique ensures the better performance of BLDC drive by improving the transient state.

The proposed PAM controlled BLDC drive is simulated in MATLAB/ Simulink with control algorithm implemented on FPGA using Xilinx System Generator for dynamic step change conditions of reference speed and supply voltages. The dual loop speed controller having outer speed PI controller and inner voltage loop using PI controller is implemented digitally. The results obtained on Xilinx Waveform Viewer validates the effectiveness of controller design for dynamic step change conditions of both

reference speed and supply voltage, subsequently it ensures the adequate performance of the dual loop controller in real time system.

4.7 SUMMARY

In this chapter the PAM controlled BLDC motor drive employing the bridgeless SEPIC converter with coupling at the front end is described. The control system of proposed BLDC motor drive is explained. The dual loop speed controller with outer speed control loop and inner voltage control loop is designed. The performance of dual loop PAM control based BLDC motor drive with PI and one cycle control employed in the voltage control loop is evaluated using simulation carried out in MATLAB/Simulink. It has been also attempted to evaluate adequate performance of the dual loop controller in real time system, using co-simulation feature of FPGA digital controller. The next chapter deals with experimental evaluation of the PAM controlled BLDC motor drive fed from bridgeless SEPIC with coupled inductors.

Chapter 5

FPGA based experimental evaluation of BLDC motor drive fed from bridgeless SEPIC with coupled inductors

5.1 INTRODUCTION

The PAM control based BLDC motor drive using bridgeless SEPIC with coupled inductors is discussed in Chapter 4. The simulation results of dual-loop PAM controlled BLDC drive is evaluated for its performance with PI and OCC controller in the DC link voltage control loop. The experimental realization of proposed concepts gives a better understanding and greater insight into the overall system. The objective of this chapter is the experimental evaluation of PAM controlled BLDC motor drive fed from the coupled inductor based bridgeless SEPIC.

This chapter deals with the hardware implementation of the proposed BLDC motor drive. The overall experimental setup is explained in Section 5.2. The details of the power circuit consisting of three-phase VSI, bridgeless SEPIC with coupled inductors is given in Section 5.3. The interfacing circuits between power and control circuits

such as voltage sensing, encoder signal processing, gate driver circuit, and voltage level shifting circuits are discussed in Section 5.4. The implementation of the control algorithms using FPGA is presented in Section 5.5. Finally, the experimental results are presented in Section 5.6. Initially, the experimental results of PI controlled bridgeless SEPIC with coupled inductors for resistive load are presented (in subsection 5.6.1) to understand the effectiveness of the proposed front end AC-DC converter. The work is later extended to realize PAM controlled BLDC motor drive using the proposed front end converter with PI controller, and results are presented in subsection 5.6.2.

5.2 EXPERIMENTAL SETUP

The block diagram of overall experimental set-up for BLDC motor drive fed from Bridgeless SEPIC with coupled inductors is shown in Figure 5.1.

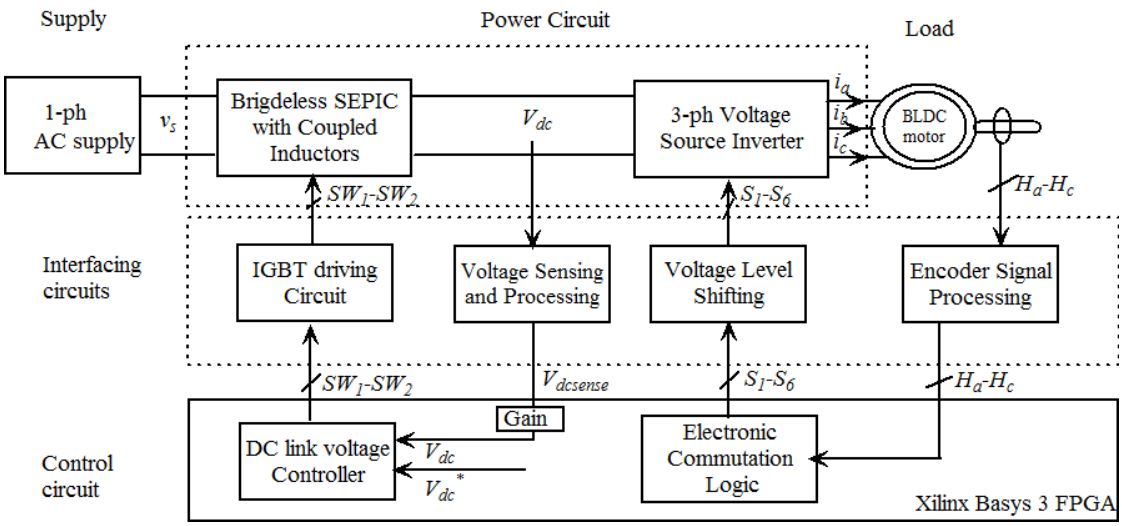


Figure 5.1: Block diagram of proposed BLDC drive with PAM control using Bridgeless SEPIC with Coupled Inductors

The BLDC motor BSM33C-2177MEQ rated for 375 W, 310 V is chosen for the proposed work. The BLDC motor is connected to a three-phase VSI (SKM75GB12T4 from Semikron), which is fed from the bridgeless SEPIC with coupled inductors (laboratory prototype). This front end AC-DC converter is supplied from single phase mains. Xilinx Artix 7 (XC7a35t cpg236-1) FPGA board is used to implement the digital control system consisting of DC link voltage controller for duty ratio modulation of SEPIC converter and the electronic commutation logic to generate switching signals for VSI. The hardware set up also consists of sensing and interfacing circuitry as shown in Figure

5.1. The laboratory prototype is shown in Figure 5.2.

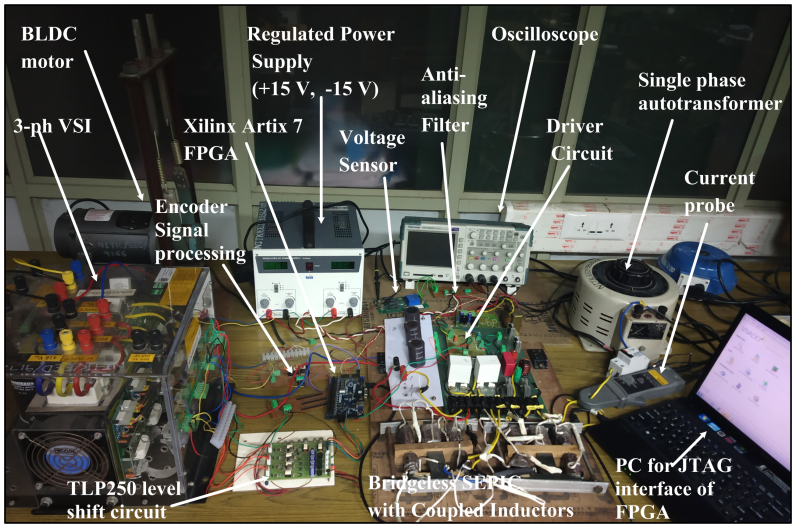


Figure 5.2: Laboratory prototype of the closed loop controlled bridgeless SEPIC converter with coupling for resistive load

The major parts of experimental set up are listed below:

- **The Load**: BLDC motor (BSM33C2177MEQ)
- **The Power Circuit**: Three-phase VSI (SKM75GB12T4) + Brigeless SEPIC with Coupled Inductors (a prototype implemented in the laboratory.)
- **The Feedback and interfacing circuits** : Voltage Sensor, Rotor Position Sensor, Voltage Level shift optocoupler, IGBT driver.
- **The Control Circuit**: Xilinx FPGA Artix 7-XC7a35t cpg236-1

The hardware implementation of BLDC motor drive fed from Bridgeless SEPIC with Coupled Inductors involves following stages as listed below and detailed discussion is given in forthcoming sections.

- Selection of three phase VSI for electronic commutation with the ratings suitable for the BLDC motor chosen for the work.
- Implementation of Bridgeless SEPIC with Coupled Inductors to supply wide range input voltage to three phase VSI.

- Implementation of sensing and interfacing circuits.
- Implementation of Control Technique using FPGA.

The BLDC motor BSM 33C-2177 MEQ, from Baldor Electric Company manufacturers, rated for 375 W, 310 V is chosen for the proposed work. The power circuit is designed to supply the selected motor based on the motor ratings. Different electrical and mechanical parameters of the motor are listed in Table 5.1.

Table 5.1: BLDC motor model BSM33C-2177MEQ parameters

Sl.No	Parameters	Value
1	No.of Poles	8
2	Rated Power	375 W
3	Rated Voltage	310 V
4	Continuous stall Torque	3.1 Nm
5	Peak Torque	9.3 Nm
6	Continuous current	2.55 A
7	Peak current	7.6 A
8	Maximum Speed	7000 RPM
9	Stator phase resistance, R_s	11.3Ω
10	Stator phase inductance, L_s	45.66mH
11	Back emf constant (k_e)	93 V/krpm
12	Torque constant (k_t)	1.52 Nm/A

The implementation of the power circuit is discussed in section 5.3 below.

5.3 Implementation of Power Circuit for BLDC motor

The BLDC motor is fed from three phase VSI, which performs as electronic commutator, by operating based on the rotor position sensed by hall position sensors. The VSI is supplied by Bridgeless SEPIC with coupled inductors, having output voltage of wide range. The selection of VSI and implementation of SEPIC are discussed further in subsections presented below.

5.3.1 Selection of three-phase VSI

The design of VSI for BLDC motor drive is discussed in chapter 4, section 4.2.1. The selection of VSI meeting the design requirement is discussed here. Three phase inverter rated for maximum DC voltage of 600 V developed by Semikron, named as Power Electronics Teaching Kit System is used in this work. It has maximum RMS out-

put current capability of 30 A. The module is built with IGBT stacks SKM75GB12T4, DC link capacitor 4700 μF/450V and IGBT gate driver SKYPER 32 R.

5.3.2 Implementation of bridgeless SEPIC with coupled inductors

The proposed front end AC-DC converter circuit is implemented for DC link voltage control over a wide range of (70 V - 310 V). To compensate the conduction and switching losses associated with SEPIC and VSI stages, the power rating of Bridgeless SEPIC with Coupled Inductors is chosen as 500 W. The converetr is operated with switching frequency of 20 kHz.

The laboratory prototype of bridgeless SEPIC with coupled inductors is built by following the steps of designing the components, selecting the component ratings and then setting up the circuit board. The individual component design is given in Chapter 3. The selection of components of SEPIC depending on the voltage and current stresses is discussed in section 3.5. The coupled inductors for the converter are designed and built as discussed in section 3.6. The other components are selected are listed in Table 3.4. The power circuit built accordingly is controlled digitally using Artix 7 FPGA.

Sensing and signal conditioning circuits are required to interface the power and control circuitry. The next section describes the implementation of the same.

5.4 Implementation of Interfacing Circuits

In order to establish a closed loop control, feedback and interfacing circuits are essential to match the voltage levels of power and control circuit. The experimental setup for BLDC motor drive with front end SEPIC requires:

1. Encoder signal processing circuit
2. Voltage sensing and processing circuit
3. Voltage level shifting circuit
4. IGBT driving circuit

5.4.1 Encoder signal processing

The encoder 7BOE0300A04 (ENCODER, EPC, 1000L,8 POLE, 40MM BC) inbuit in motor is used to obtain speed and rotor position feedback from the motor. A 5 V DC supply is connected to encoder supply terminals. The rotor position signals from encoder have voltage level of 5 V. The encoder signals are processed through a 3.3 V regulator to match the I/O port voltage level of Artix 7 FPGA.

The encoder signal processor is built using LD3.3V voltage regulator as shown in Figure 5.3. The rotor position signals (H_a, H_b, H_c) are processed through an individual LD3.3V regulator. The datasheet recommended input and output side capacitances of C_{in} = 100 nF and C_{out} = 10 μF are connected for each regulator. The signals (H_a, H_b, H_c) collected at the output of regulators are given to FPGA input port.

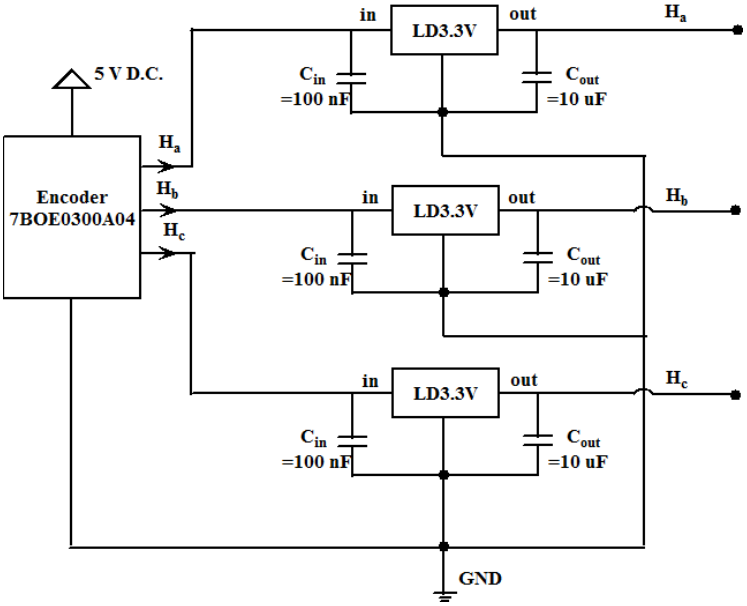


Figure 5.3: Block diagram of encoder signal processing

5.4.2 Voltage sensing and processing circuit

For implementing the DC link voltage controller, the feedback of voltage at the DC link is given to the FPGA digital controller. The actual voltage of high value is appropriately scaled-down through the sensing circuit to match the inbuilt ADC input voltage level of the FPGA. The input of ADC is configured as differential inputs. Hence, the analog input traces from the sensing circuit are routed as tightly coupled differential pairs. The sensed signal is processed accordingly, and the aliasing effect is addressed.

The following sections discuss the DC link voltage sensing and processing in detail. The circuit diagram for the same is shown in Figure 5.4.

5.4.2.1 DC link voltage sensing

The DC link voltage is sensed using a LEM voltage sensor module LV 25-600. The LV 25-600 is a Hall Effect closed loop transducer circuit using the sensor LV 25-P. It has primary resistance R_p and protection diodes mounted on board. The primary side resistance R_p mounted on borad LV 25-600 is 60 kΩ. The primary side resistance is designed to limit the current at primary side I_p within 10 mA at nominal primary side voltage of 600 V. The turns ratio of sensor is given as 2500:1000. Then the secondary side current is $I_s = \frac{V_{dc}}{R_p} \times 2.5$. Hence the maximum current at secondary is limited to 25 mA.

The selection of measuring resistance R_M is decided based on the maximum voltage to be sensed and the mode of operation of inbuilt ADC of the FPGA. For the unipolar mode of operation, the analog inputs (v_p and v_n) of FPGA have an input range of 0 V to 1.0 V. For the safer operation, the input to ADC is limited to a maximum of 0.780 V for measuring the maximum voltage level of 375 V at primary side. The input to ADC is voltage at secondary side V_s of sensor. Then, the measuring resistance is designed as $R_M = \frac{V_s}{I_s}$, which gives R_M = 50 Ω.

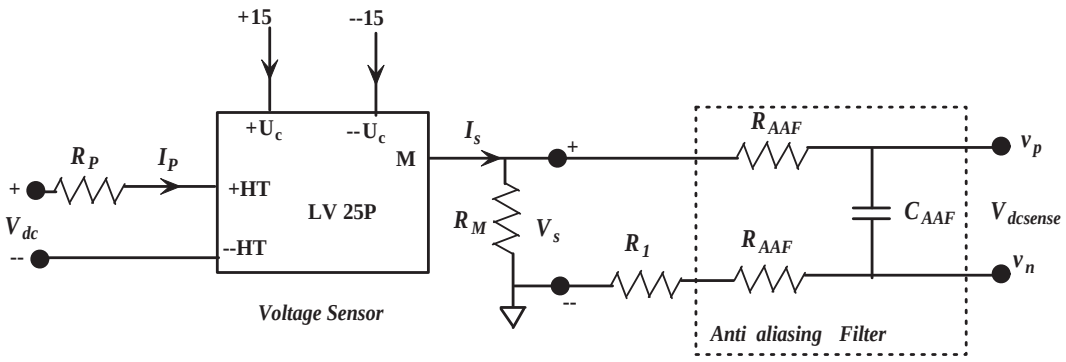


Figure 5.4: DC link voltage sensing and processing circuit

5.4.2.2 *Sensed signal processing*

The analog inputs of the ADC use a differential sampling scheme to reduce the effects of common-mode noise signals. This common-mode rejection improves the ADC performance in noisy digital environments. The analog signals are connected in a differential configuration (v_p and v_n) to take advantage of the high common-mode rejection. An intermediate stage of the anti-aliasing filter using passive components is built as shown in Figure 5.4. This circuit transfers the sensed signal as a differential pair of v_p and v_n as required at the inputs of ADC.

5.4.2.3 *Design of Anti aliasing filter*

An anti-aliasing filter stops unwanted high-frequency components of the signal from aliasing back into the bandwidth of interest and impacting the performance of the ADC. The anti-aliasing filter can be a simple passive filter made from resistors and capacitors. The design of components of the anti-aliasing filter is done depending on the requirement of settling time T_{settle} as given by (5.1)

$$T_{settle} = \tau \times (R_M + R_1 + 2R_{AAF}) \times C_{AAF} \tag{5.1}$$

For 12 bit resolution, number of time constant τ is 9.01. The resistance R_1 equal to R_M is placed on n terminal to balance impedance on both p and n terminals. Assuming the settling time T_{settle} to be less than 5 μs, and R_{AAF} as 100 Ω the C_{AAF} is designed as 1.8 nF.

The selection of R_{AAF} and C_{AAF} is taken care to satisfy the Nyquist criteria of cutoff frequency ($f_{cAAF} \leq \frac{f_{sFPGA}}{2}$). The cutoff frequency f_{cAAF} of anti alising-filter is given by (5.2).

$$f_c = \frac{1}{2\pi \times 2 \times R_{AAF} \times C_{AAF}} \tag{5.2}$$

For the single channel operation of ADC, the sampling frequency f_{sFPGA} is 1

MHz for Artix 7 FPGA. The cutoff frequency of anti aliasing filter designed (f_c = 442 kHz) satisfies the Nyquist criteria ($f_{cAAF} \leq \frac{f_{sFPGA}}{2}$).

5.4.3 Voltage level amplifier

The implementation of TLP250 opto-coupler based interfacing circuit for FPGA based BLDC Motor drive is discussed in this section.

5.4.3.1 Introduction

The switching signals for the three phase VSI used in motor drive are generated from the Xilinx Artix 7 FPGA based on rotor position information. The logic voltage levels of FPGA I/O ports is 0 - 3.3 V. However, the input voltage requirement of SKYPER 32R, the in-built gate driver of SEMIKRON VSI, used in the BLDC drive setup is 15 V. The voltage level amplification from 3.3 V to 15 V is done using the optocoupler based interfacing circuit, to provide the necessary switching pulses for the inverter switches. The optocoupler based interfacing circuit also provides the benefit of opto-isolation between the controller and converter, along with the amplification of voltage level. A

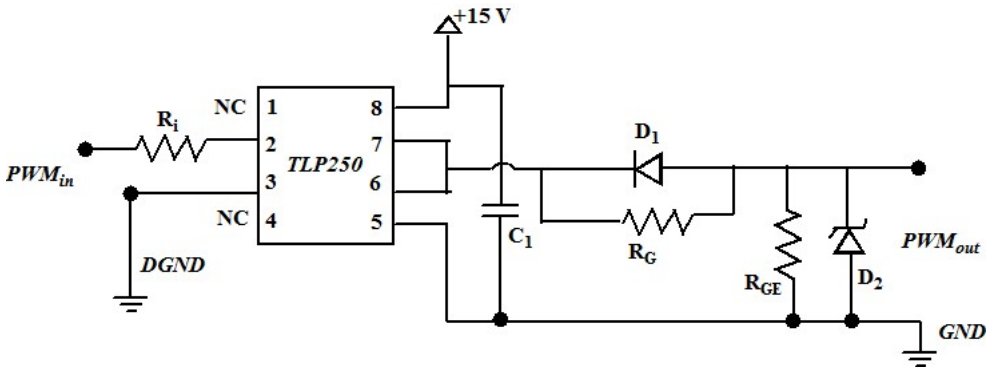


Figure 5.5: Voltage level Amplifier

TLP250 opto-coupler based level amplifier circuit is shown in Figure 5.5.

5.4.3.2 Working principle

The TLP250 is a photocoupler consisting of infrared Light-Emitting Diode (LED) optically coupled to an integrated high-gain, high-speed photo transistor. It has a totem-pole output. When a signal from FPGA is applied to optocoupler input, it passes through the

input LED which emits an infrared light whose intensity is proportional to the electrical signal. This emitted light falls upon the base of the photo-transistor, causing it to switch-ON and conduct in a similar way to a normal bipolar transistor. PWM_{in} is the input drive signal that dictates the FPGA output state which is referenced to the ground ($DGND$). PWM_{out} is the amplified drive signal with reference to ground (GND).

5.4.3.3 Design of voltage level amplifier circuit

As can be seen in Figure 5.5, the circuit consists of input side resistance R_i, diode D_1 gate resistance R_G, output side resistance R_{GE}, diode D_2 and bypass capacitor C_1. The design task of voltage level amplifier using TLP250, involves determining the ratings of the components mentioned earlier.

The input side resistance R_i is designed to limit the current through LED. The forward voltage drop (V_F) of LED is around 1.4-1.8 V. The forward current needs to be limited to 10 mA. For the signal voltage (V_{sig}) level of of 3.3 V, the input side resistance can be designed as given by equation (5.3).

$$R_i = \frac{V_{sig} - V_F}{I_F} = \frac{3.3 - 1.8}{10m} \tag{5.3}$$

The input side resistance R_i is selected to be 150 Ω.

The gate resistance R_G is selected such that the maximum peak output current rating of the gate driver optocoupler ($I_{OL(peak)}$) is not exceeded. The design equation (5.4) is given as follows.

$$R_G \geq \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OL(peak)}} = \frac{15 - 0 - 0}{0.5} \tag{5.4}$$

where V_{CC} is supply voltage 15 V and V_{EE} is 0 V (ground potential). The gate resistance is selected as 100 Ω. An anti-parallel fast switching diode D_1 conncted across the resitor R_G enhances the turn-off speed.

The output resistance R_{GE} also known as pull-down resistance ensures a low

level for the IGBT by preventing accidental turn-on due to noise or voltage due to other factors such as miller capacitance. The recommended resistance value is between 1 kΩ to 10 kΩ. This is decided based on time constant $\tau_{GE} = R_{GE}C_{GE}$. Larger the time constant faster the discharge rate. The output resistance R_{GE} is selected to be 10 kΩ in this work. A zener diode D_2 of 15 V connected across gate and emitter, is effective for protection against electrostatic discharge and gate surge voltage.

The bypass capacitor C_1 is connected between VCC and GND. This capacitor stabilizes the operation of the high gain linear amplifier in the optocoupler. It eliminates the power supply noise.

5.4.4 IGBT driving circuit

The switching device of the SEPIC converter operates at high voltage. A 1200 V rated IGBT IKW40N120T2 is selected for the circuit. The gate drive circuits for such high voltage operating conditions need to be selected carefully, considering the isolation voltage levels and other safe operating features such as Under Voltage Lock Out, active shutdown, short circuit clamping etc.

An Infeneon based IGBT driver 1EDI20I12MF is found to be providing all protection features necessary for driving the high voltage device. This also has an active miller clamping characteristics, which prevents erratical dynamic turn-on of the IGBT. These basic control and protection features support fast and easy design of highly reliable gate drive circuit. The IGBT gate driver circuit using 1EDI20I12MF IC is shown in Figure 5.6.

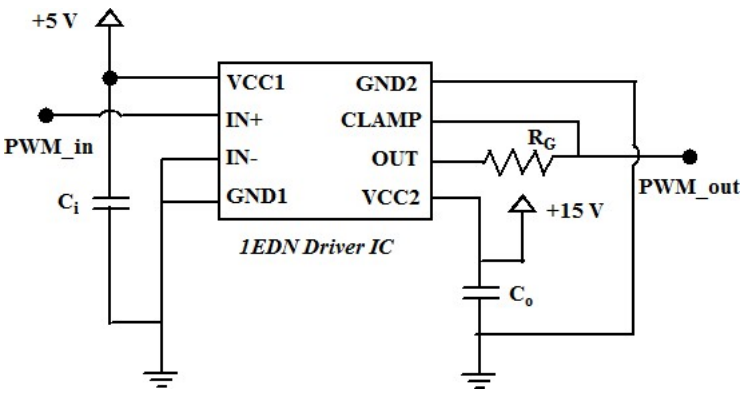


Figure 5.6: Gate driver for SEPIC

The typical positive supply voltage is 15 V at VCC2 and a supply voltage of 5 V is connected to VCC1 at the input side. The datasheet recommended bypass capacitance values are connected in parallel with signal side supply (VCC1) to ground (GND1) and output side supply (VCC2) to ground (GND2). The signal side by pass capacitor C_i is 100 nF and output side capacitor C_o is 1 uF.

The gate resistance R_G is designed following the equation (5.4) mentioned in section 5.4.3.3. With the supply voltage at VCC2 of 15 V and peak current ($I_{OL(peak)}$) of 4.1 A as given in datasheet, the gate resistance is calculated as R_G = 3.65 Ω, and is selected to be larger than calculted value, which is 10 Ω.

The driver IC provides active Miller clamp function, hence providing option externally for gate to source discharge is not necessary. The CLAMP output is directly connected to the gate of IGBT to avail the miller clamp feature.

The implementation of interfacing circuits is discussed in this section. The implementation of FPGA based controller is discussed in section below.

5.5 IMPLEMENTATION OF CONTROL CIRCUIT

Artix 7, Basys 3 FPGA by Xilinx manufacturers is choosen for implementing control system of proposed BLDC motor drive. This work uses System Generator, a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink design environment for FPGA design. Hence minimal knowledge of Hardware Description Languages is adequate. The control circuit modelled using Xilinx System Generator blocksets can be used in the loop with Simulink power circuit models to overview the performance of system under digitally implemented controller.

Implementation of control techniques and developing the programmable bit file for FPGA involves following steps:

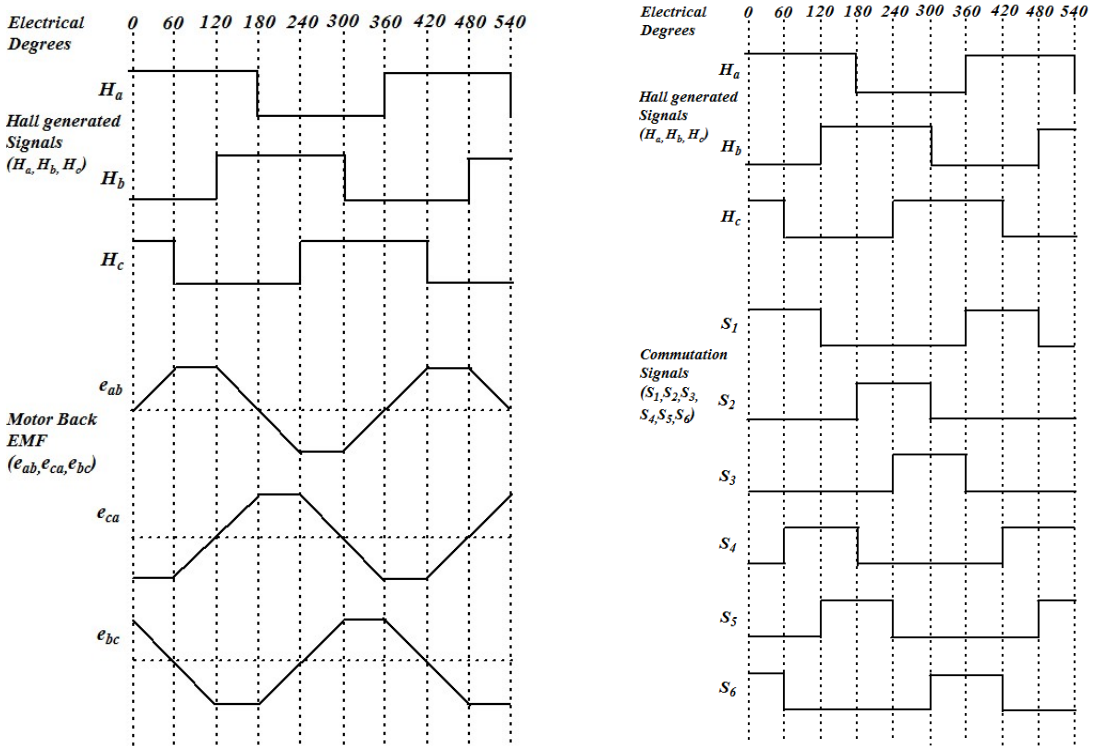
- Implementing the algorithm using Xilinx system generator blocksets in MATLAB/Simulink.
- Generating the IP core using Sytem Generator token.

- Importing the IP core into the Vivado design suite and generate test bench.
- Verifying the algorithm using behavioural simulation in Vivado design suite.
- Generating the bit stream by following synthesis and implementation stages in Vivado design suite.
- Programming the FPGA with bit file generated.

In this work, the overall control unit of the BLDC motor drive consists of an electronic commutation logic to generate switching signals for VSI and a DC link voltage controller to generate switching signals for SEPIC converter.

The imlementation of Electronic Commutation logic and PI control algorithm in FPGA is discussed in following section.

5.5.1 Implementation of Electronic Commutation Logic using FPGA



(a) Back EMF pattern **(b)** Commutation Signals

Figure 5.7: Electronic Commutation Logic

Three phase VSI acting as electronic commutator for BLDC motor operates based

on information provided by processing the rotor position signals.

The sequence of switching signals can be decided with reference to back emf pattern corresponding to the rotor position sensor output. The information of back emf pattern and respective rotor position are available in the datasheet of the motor. The back emf profile of BLDC motor BSM33C2177MEQ is as shown in Figure 5.7a.

Table 5.2: Switching signals with respect to hall sensor signals

Rotor Position (^{0})	Hal sensor output			Phase voltages	S_1	S_2	S_3	S_4	S_5	S_6
	H_a	H_b	H_c							
0-60	1	0	1	-ca	1	0	0	0	0	1
60-120	1	0	0	+ab	1	0	0	1	0	0
120-180	1	1	0	-bc	0	0	0	1	1	0
180-240	0	1	0	+ca	0	1	0	0	1	0
240-300	0	1	1	-ab	0	1	1	0	0	0
300-360	0	0	1	+bc	0	0	1	0	0	1

Table 5.3: Design of switching logic using K-map

(a) $S_1 = H_aH_b'$

H_c	0	1
H_aH_b		
00	0	0
01	0	0
11	0	0
10	1	1

(b) $S_2 = H_a'H_b$

H_c	0	1
H_aH_b		
00	0	0
01	1	1
11	0	0
10	0	0

(c) $S_3 = H_a'H_c$

H_c	0	1
H_aH_b		
00	0	1
01	0	1
11	0	0
10	0	0

(d) $S_4 = H_aH_c'$

H_c	0	1
H_aH_b		
00	0	0
01	0	0
11	1	0
10	1	0

(e) $S_5 = H_bH_c'$

H_c	0	1
H_aH_b		
00	0	0
01	1	0
11	1	0
10	0	0

(f) $S_6 = H_b'H_c$

H_c	0	1
H_aH_b		
00	0	1
01	0	0
11	0	0
10	0	1

Refering to the placement of switches in VSI (Figure 4.4 shown in section 4.2.1), the ON/OFF conditions of particular IGBTs of VSI to obtain the corresponding back emf is tabulated in Table 5.2. The expected switching pattern as per the tabulation in Table 5.2, is depicted using waveform representation in Figure 5.7b. The design of commutation logic is obtained using K-Map as shown in Table 5.3.

The hall signals to switching logic derived in Table 5.3a, 5.3b, 5.3c, 5.3d, 5.3e and 5.3f for switches S_1, S_2, S_3, S_4, S_5 and S_6 respectively is implemented using Xilinx System Generator blocksets in MATLAB/Simulink. It is compiled to generate IP core using System Generator token. The IP core is used in Vivado Design suite to perform further stages of obtaining programmable file to FPGA.

5.5.2 Implementation of DC link voltage controller using FPGA

The DC link voltage is sensed using LEM voltage sensor. The sensed signal in the analog form is given to FPGA analog input ports. The inbuilt ADC in the Artix 7 FPGA known as XADC processes the analog signal into the digital form for processing further through a digitally implemented control module. The Vivado design stage incorporates the XADC IP core to set necessary ADC design specifications. The data output signal from XADC IP is fed to voltage controller IP core.

For obtaining IP core of PI controller to process it in Vivado Design suite, PI controller is discretised and implemented in MTLAB simulink using Xilinx system generator blocksets. The following section describes digital implementation of PI controller.

5.5.2.1 Implementation of PI controller using FPGA

In order to operate the bridgeless SEPIC with coupled inductors in closed loop, PI voltage controller is designed. The controller is tuned to obtain the control of DC link voltage over a wide range.

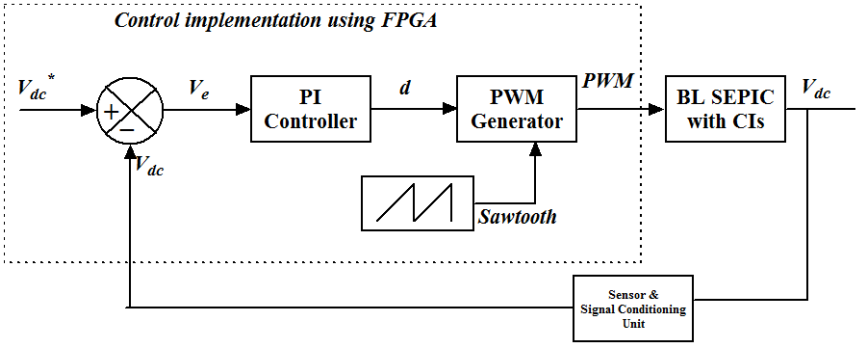


Figure 5.8: Implementation of closed loop control using PI controller

The control schematic is shown in the Figure 5.8. Autotuning algorithm of MATLAB/Simulink is used to tune the controller, by obtaining linearised transfer function

of the converter.

The implementation of PI controller in FPGA requires the discretization of the controller given by equation (5.5).

$$d(t) = k_p V_e(t) + k_i \int V_e(t)dt \tag{5.5}$$

where d is the PI controller output, which is a duty ratio of the converter. V_e is the error voltage, obtained by comparing, actual DC output voltage (V_{dc}) with the reference DC output voltage (V_{dc}^*).

The discretization is achieved by obtaining z-domain transfer function of the controller using bilinear transformation and is as shown by (5.6)

$$d(z) = [k_p + \frac{k_i T}{2}\frac{(1+z^{-1})}{(1-z^{-1})}]V_e(z). \tag{5.6}$$

The control output of PI controller is compared with a sawtooth waveform of frequency equal to switching frequency of the converter, to generate the PWM for the converter.

The discretized PI controller and the sawtooth waveform are implemented in MATLAB/Simulink, using Xilinx System Generator blocksets for generation of PWM using FPGA. The system generator model is later compiled and IP core is obtained. The IP cores of control logics obtained using MATLAB simulink, are processed further in Vivado design suite to obtain a programmable bit file following the steps discussed in the beginning of this section.

The detailed discussion on overall implementation of hardware setup consisting of power and interfacing circuits and a digital controller is discussed in previous sections. The following section describes the experimental results.

5.6 EXPERIMENTAL RESULTS AND DISCUSSION

The experimntal setup for the BLDC motor drive fed from bridgeless SEPIC with coupled inductors is implemented. The laboratory prototype of proposed SEPIC converter is built to supply SEMIKRON inverter module feeding BLDC motor load. The Xilinx FPGA based control circuit is interfaced through appropriate sensing and signal processing circuits as discussed in Section 5.4.

In this section, the experiments conducted on hardware setup are discussed and results obtained are evaluated. The experiments are conducted to evaluate:

1. The performance of bridgeless SEPIC with coupled inductors for resistive load of 192.3 Ω in:
    - open loop with fixed duty ratio switching signal
    - closed loop with voltage controlled PWM signal
2. The performance of BLDC motor drive fed from single phase mains through:
    - diode bridge rectifier
    - bridgeless SEPIC with coupled inductors

The results are discussed in following sections.

5.6.1 Experimental evaluation of bridgeless SEPIC with coupled inductors for resistive load

The performance of laboratory prototype of bridgeless SEPIC with coupled inductors rated for 500 W, 310 V is evaluated for rated load resistance of 192.3 Ω.

The performance of the converter in the open-loop is evaluated to understand converter operation and component stresses. The performance of the converter in closed-loop voltage-controlled mode using the PI technique is also analyzed during steady-state and dynamic change conditions.

5.6.1.1 *Performance of proposed Bridgeless SEPIC in open loop (Voltage and current stresses on components of proposed converter)*

The proposed converter with coupling in open loop is simulated in MATLAB/Simulink for the supply voltage of 90 V with a 20 kHz switching signal of duty ratio 18 % to evaluate the voltage and current stresses on circuit components. The experiment is carried out on the laboratory prototype of the converter with coupling to validate the same, by comparing the experimental results with simulation and theoretical values.

The simulation and experimental results are observed to depict the operation of the bridgeless converter at supply voltage of 90 V for the resistive load of 192.3 Ω. The voltage and current waveforms across the circuit elements such as inductors at the input side, inductors at the output side, and intermediate capacitors are observed and are shown in Figure 5.9. Figure 5.9a shows the waveforms from simulation and Figure 5.9b shows results obtained from hardware experimentation.

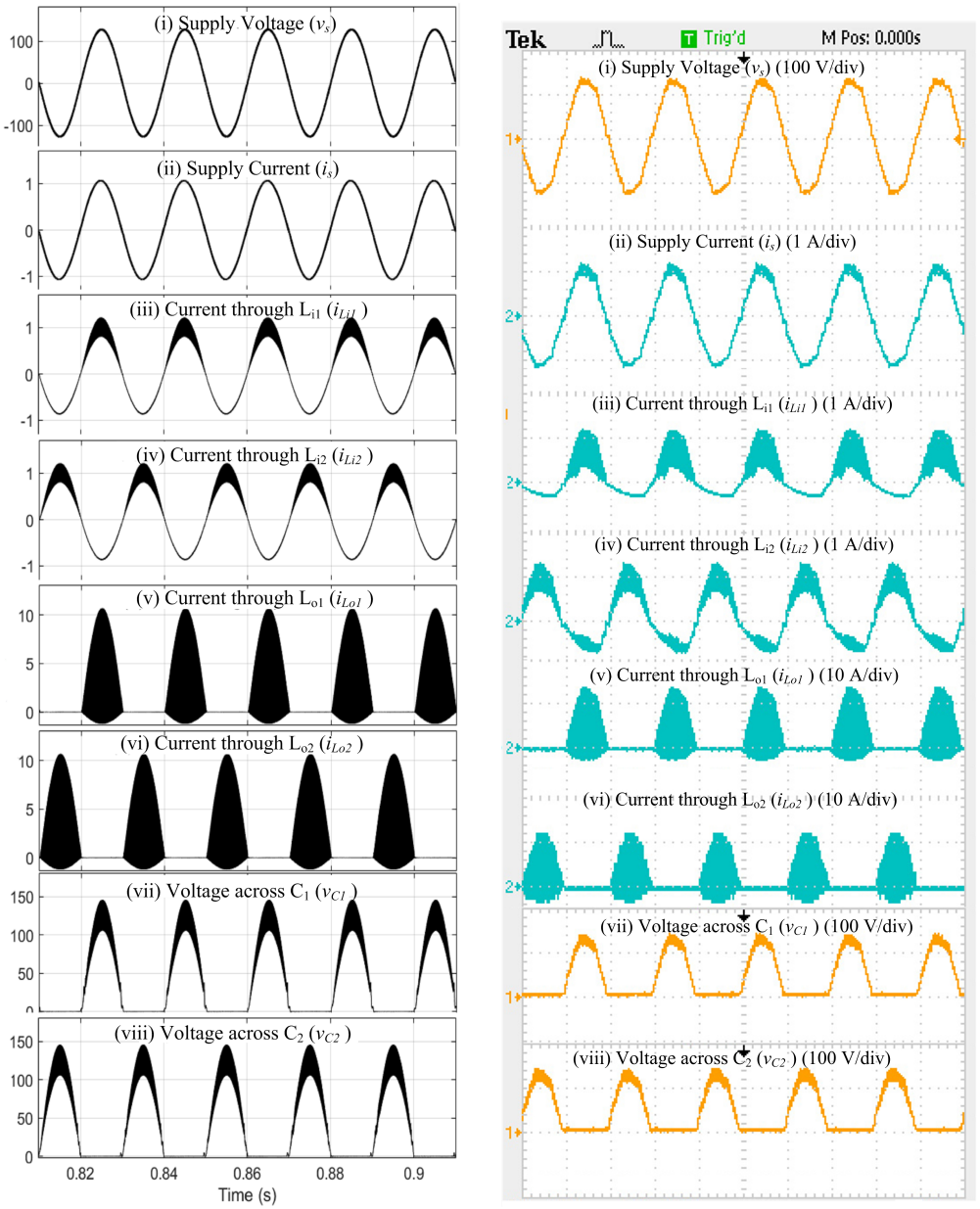
The waveforms (i) Supply Voltage (v_s) (ii) Supply current (i_s) (iii) Current through input side inductor L_{i1} (i_{Li1}) (iv) Current through input side inductor L_{i2} (i_{Li2}) (v) Current through output side inductor L_{o1} (i_{Lo1}) (vi) Current through output side inductor L_{o2} (i_{Lo2}) (vii) Voltage across intermediate capacitor C_1 (v_{C1}) (viii) Voltage across intermediate capacitor C_2 (v_{C2}) of proposed bridgeless SEPIC converter are given.

The input current, the peak current of input inductor, the peak current of output inductor, and peak voltage of the capacitor obtained by simulation and hardware compared with theoretical values are presented in Table 5.4.

From the results of Table 5.4, it is found that the proposed converter exhibits a similar performance in terms of voltage and current stresses on components as that of the converter without coupling for the same power rating but with reduced size and cost.

5.6.1.2 *Performance of proposed Bridgeless SEPIC in closed loop with PI controller*

The performance of bridgeless SEPIC with coupled inductors is evaluated in closed-loop with PI controller for its performance under steady-state and dynamic conditions



(a) Evaluation using Simulation **(b)** Evaluation using experiment

Figure 5.9: Voltage and current stresses on components of bridgeless SEPIC with coupled inductors

Table 5.4: Comparison of voltage and current magnitudes over components of proposed converter

Sl.No	Parameter	Equation	Magnitude		
			Theoretical	Simulation	Hardware
1	$v_s\ (V)$	v_s	90	90	90
2	$I_{in}(A)$	$\frac{P_o}{\eta V_s}$	1.1051	1.021	1.02
3	$i_{Li_{max}}(A)$	$i_{in} + \frac{\Delta i}{2}$	1.2506	1.221	1.32
4	$i_{Lo_{max}}(A)$	$\frac{V_m dT_s}{L_o} - (-I_{in})$	9.509	10.6	10.88
5	$v_{Cmax}(V)$	$v_C + \frac{\Delta v_c}{2}$	146.37	145.9	144

with resistive load. The reference voltage tracking and power factor correction features of closed-loop controlled converter are evaluated for different DC link voltage references and different supply voltage conditions under steady state. The performance is also assessed under dynamic changes in reference DC link voltage and supply voltage variations for fixed load resistance.

Performance of converter in closed loop under steady state

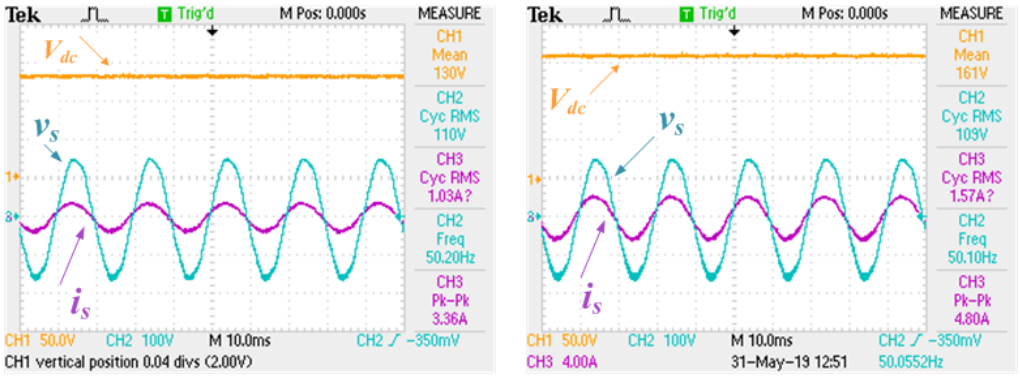
The performance of bridgeless SEPIC with coupled inductors is tested in closed-loop under steady-state, for different reference DC link voltage and supply voltage conditions with the fixed load resistance.

The reference voltage tracking, power factor, and THD are verified for :

- Different reference DC link voltage values of 130 V and 160 V at the supply voltage of 110 V AC.
- Different supply voltages of 90 V and 125 V at reference DC link voltage of 160 V.

Figure 5.10 shows the response of DC link voltage (V_{dc}), supply voltage (v_s) and supply current (i_s) at steady state for different DC link voltages with a fixed supply voltage of 110 V. The control of DC link voltage to its given reference value is achieved as seen in Figure 5.10a and 5.10b for reference DC link voltage of 130 V and 160 V respectively. The achievement of near unity power factor can be observed from the

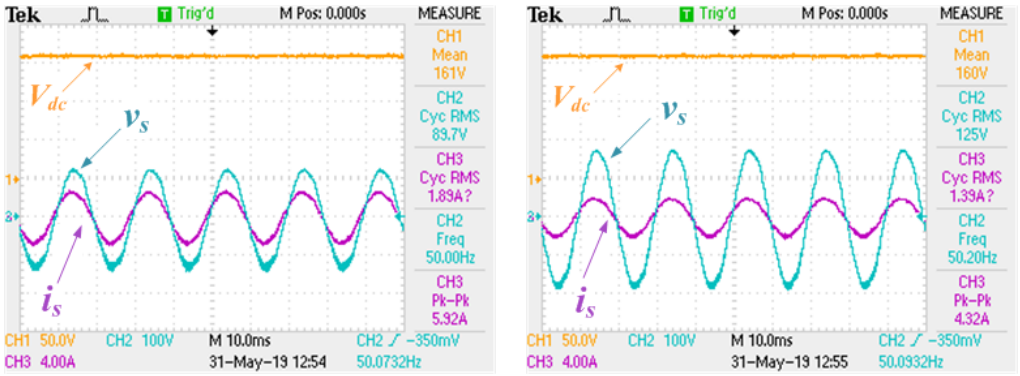
supply current and voltage waveforms given in Figure 5.10.



(a) At DC link voltage of 130 V **(b)** At DC link voltage of 160 V

Figure 5.10: Performance of converter at steady state for different DC link voltages at supply voltage of 110 V

Figure 5.11 shows the response of DC link voltage (V_{dc}), supply voltage (v_s) and supply current (i_s) at steady state for different supply voltages, at a fixed DC link voltage refrence of 160 V. It is seen from Fig 5.11a and 5.11b that the tracking of DC link voltage to its reference value is obtained for supply voltages of 90 V and 125 V, respectively. The achievement of near unity power factor is also observed from the supply current and voltage waveforms given in Figure 5.11.



(a) At supply voltage of 90 V **(b)** At supply voltage of 127 V

Figure 5.11: Performance of converter at steady state under different supply voltages for DC link voltage of 160 V

From Table 5.5, it can be observed that, for the fixed DC link voltage of 160 V, as the supply voltage increases from 90 V to 125 V, THD improves from 5.82 % to 5.51 % and PF improves from 0.9429 to 0.9546 as measured by the experimental setup.

Similarly, at fixed supply voltage of 110 V, the power factor and THD is better at higher DC link voltage for both simulation (THD of $2.43 < 2.79$, and PF of $0.9881 > 0.9872$) and experimental (THD of $5.51 < 5.77$ and PF of $0.9546 > 0.9468$) results.

Table 5.5: Performance evaluation of closed loop converter at steady state with resistive load

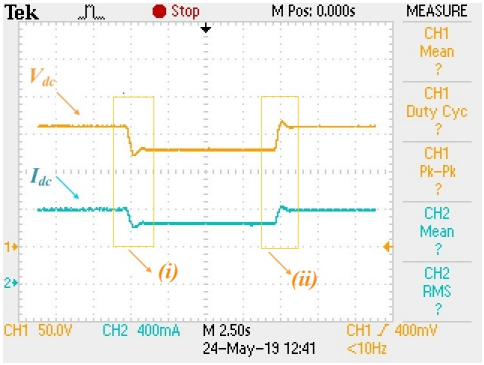
Sl.No	Parameters	$V_{dc}(V)$	$v_s(V)$	$i_s(A)$	$THD(\%)$	PF
Case (i)		Different DC link voltage				
1.	Simulation	160	110	0.989	2.43	0.9881
	Hardware			1.03	5.51	0.9546
2.	Simulation	130	110	1.56	2.79	0.9872
	Hardware			1.57	5.77	0.9468
Case (ii)		Different supply voltage				
1.	Simulation	160	90	1.89	2.86	0.9867
	Hardware			1.89	5.82	0.9429
2.	Simulation	160	125	1.35	2.00	0.9893
	Hardware			1.39	5.22	0.965

Performance of proposed converter during dynamic step change conditions

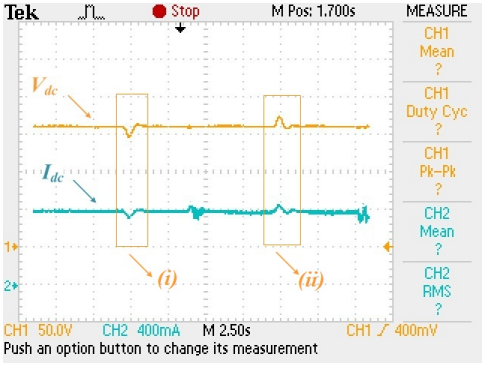
The closed-loop bridgeless SEPIC is tested for its performance under sudden change in reference DC link voltage and supply voltages for a fixed resistive load. The experimental results (the waveforms of DC link voltage V_{dc}, and current i_{dc}) for dynamic step change in DC link voltage and supply voltage are shown in Figure 5.12.

Figure 5.12a, 5.12c show the response of DC link voltage (V_{dc}) when reference value is changed from (i) 160 V to 130 V at $t = 3.96s$ and (ii) 130 V to 160 V at $t = 4.6s$. The time taken to settle from 160 V to 130 V is 1.32 s, and the settling time for a change in actual DC link voltage value from 130 V to 160 V is 1.04 s, as shown in (i) and (ii) respectively of Figure 5.12c.

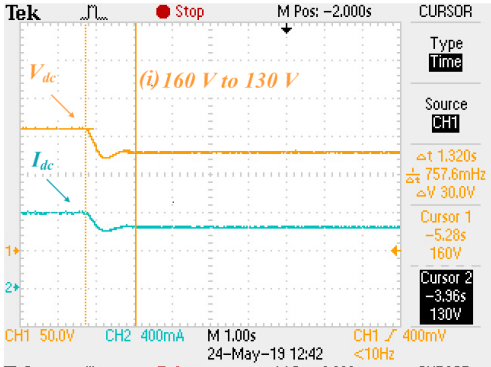
Figure 5.12b, 5.12d show the response of DC link voltage when supply voltage is changed from (i) 110 V to 90 V at $t = 2.44s$ and (ii) 90 V to 110 V at $t = 6.3s$. The DC link voltage settles to its reference value of 160 V after a transient period and it takes 1.28 s to settle to its reference value, whereas for the change in supply voltage of 90 V to 110 V it takes 1.08 s to settle as shown in (i) and (ii) respectively of Figure 5.12d.

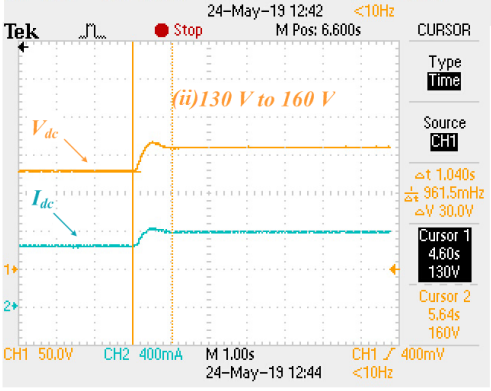


(a) Step change in DC link voltage

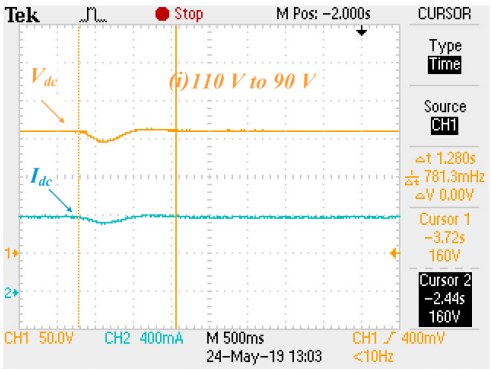


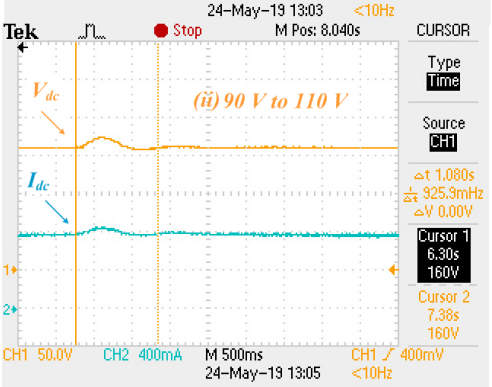
(b) Step chnege in supply voltage





(c) Step change in DC link voltage (zoomed view)





(d) Step change in supply voltage (zoomed view)

Figure 5.12: Performance of converter during dynamic step change in DC link voltage [(a), (c)] and supply voltage [(b), (d)]

5.6.2 Experimental evaluation of BLDC motor drive

The performance of BLDC motor drive for different DC link voltage is evaluated with uncontrolled rectifier at the front end, and using bridgeless SEPIC with coupled inductor at the front end. The variable speed with variable DC link voltage is verified with theoretical value of speed. The quality of supply current drawn when BLDC motor drive is fed from uncontrolled rectifier and proposed AC-DC converter is evaluated. The experiment is conducted on the BLDC drive fed from single phase mains with no load on motor.

5.6.2.1 Experimental evaluation of BLDC drive fed from single phase mains through Diode Bridge Rectifier

The experiment is conducted on BLDC motor drive fed from single phase mains through bridge rectifier. The sequence of switching pattern for VSI, the phase voltages of VSI supplied to the motor and the nature of supply current drawn from single phase mains for DC link voltage (V_{dc}) of 135 V are observed.

The Figure 5.13 shows the commutation signals (S_1, S_2, S_3, S_4, S_5 and S_6) of 15 V supplied to the switching devices of the VSI, with respect to phase voltage (v_{an}). The switching signals of 3.3 V voltage level from FPGA are stepped up to 15 V through optocoupler based circuit. The commutation pattern obtained is verified with the expected switching pattern tabulated in Table 5.2.

The Figure 5.14a shows the phase volatge waveforms (v_{an}, v_{bn}, v_{cn}) supplied to motor corresponding to V_{dc} of 135 V. The voltage spikes can be seen in the phase voltage waveforms at the phase commutation instants, due to the sudden change in the phase currents at the instant of commutation. The switching frequency of VSI is same as the frequency of voltage supplied to motor as can be seen from Figure 5.13 and 5.14a.

Figure 5.14b shows the performance waveforms of DC link voltage (V_{dc}) and corresponding phase voltage (v_{an}) at the output of VSI, supply voltage (v_s) and supply current (i_s) at steady state for V_{dc} of 135 V. The supply current with low Power Factor (PF) of 0.53 and high Total Harmonic Distortion (THD) of 156 % is seen with BLDC

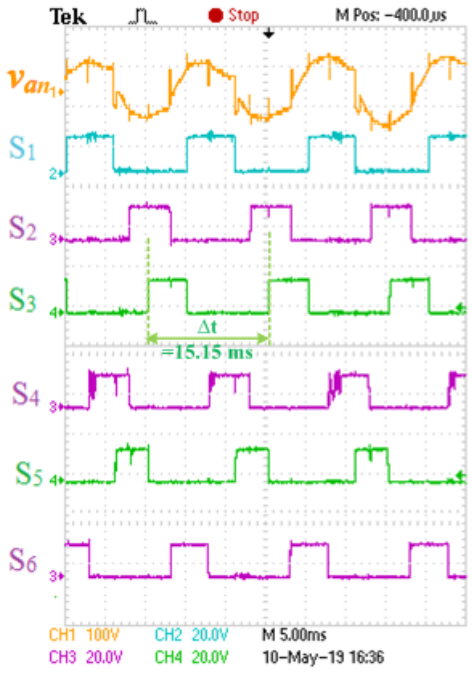
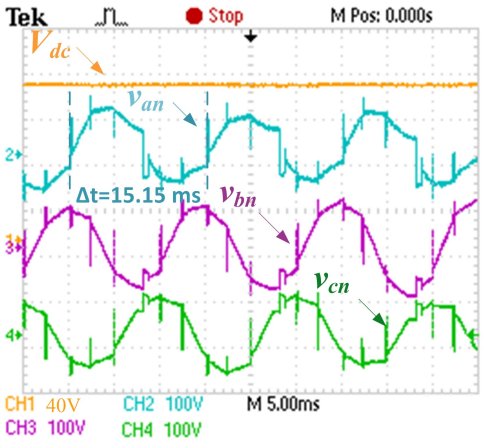
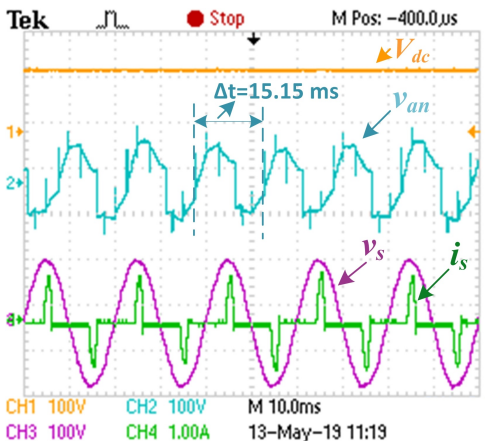


Figure 5.13: Electronic commutation Logic

motor drive fed with conventional bridge rectifier.



(a) Phase voltages of VSI supplied to BLDC motor



(b) Supply side performance of BLDC motor drive

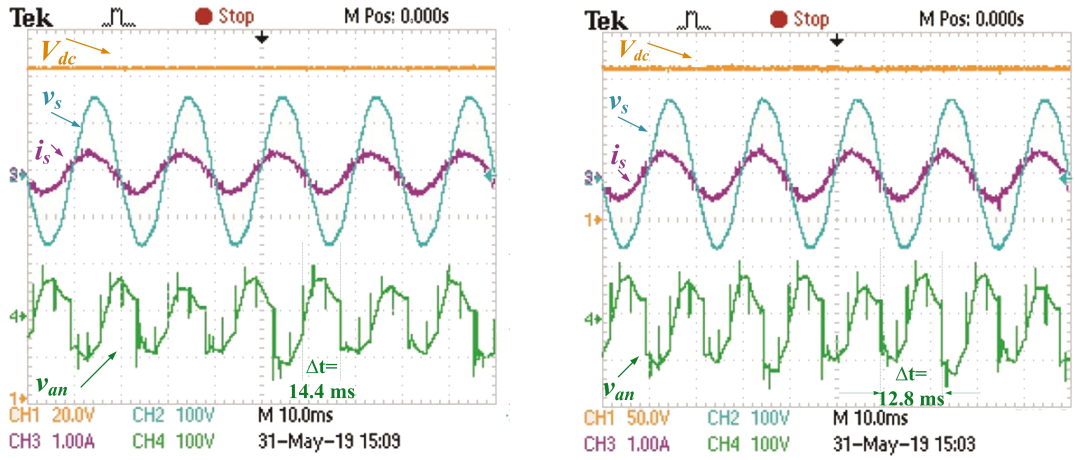
Figure 5.14: BLDC motor drive fed through diode bridge rectifier at steady state for DC link voltage of 135 V

The tabulation of experimental measurements for DC link voltage, phase volatge, frequency of phase voltage, experimental and theoretical value of speed, supply current THD and PF are given in Table 5.6. It is seen that the experimental value of speed is

close to the theoretical speed calulated using (4.3).

5.6.2.2 *Experimental evaluation of BLDC motor drive fed from coupled inductor based bridgeless SEPIC*

The experiment is conducted to evaluate the performance of BLDC motor drive fed from coupled inductor based Bridgeless SEPIC in close loop. The waveforms of DC link voltage (V_{dc}), supply voltage (v_s), supply current (i_s), the output phase voltage of VSI (v_{an}) connected to motor at steady state are observed for different reference DC link voltage values at a supply voltage of 110 V as shown in Figure 5.15. The waveforms under consideration are analysed for reference DC link voltage values of 140 V and 160 V as shown in Figure 5.15a and Figure 5.15b respectively.



(a) At DC link voltage of 140 V **(b)** At DC link voltage of 160 V

Figure 5.15: Performance of BLDC motor drive fed from coupled inductor based bridgeless SEPIC at steady state for different DC link voltages

Figure 5.15a and 5.15b show the supply current of improved quality for the BLDC motor drive fed from coupled inductor based Bridgeless SEPIC. The respective phase voltage fed to motor at different DC link voltages is also shown. The experimental measurements tabulated in Table 5.6 shows the supply current of improved quality for the BLDC drive fed from coupled inductor based Bridgeless SEPIC.

5.6.3 Conclusion

The experiments are conducted to evaluate the operation of bridgeless SEPIC with coupled inductors for resistive load and for BLDC motor drive. The adjustable

Table 5.6: Experimental evaluation of BLDC motor drive with adjustable DC link voltage

Sl.No	$V_{dc}(V)$	$v_{an}(V)$	$v_{ab}(V)$	$\Delta t(ms)$	$f(Hz)$	$N(rpm)$		THD	PF
						Exp	Cal		
BLDC motor drive fed through diode rectifier									
1	135	60.75	105.2	15.15	66	990	1016	156.89	0.53
BLDC motor drive fed through coupled inductor based bridgeless SEPIC									
2	140	63.04	109.2	14.40	69	1041	1100	5.23	0.9895
3	160	72.05	124.8	12.80	78	1171	1256	5.11	0.9901

speed operation of BLDC motor using adjustable DC link voltage ($N \propto V_{dc}$) is verified experimentally. Control of DC link voltage for different reference DC link voltage and different supply voltages is verified. The supply current of near unity power factor and lower total harmonic distortion is ensured for both resistive load and BLDC drive.

5.7 SUMMARY

Hardware implementation of BLDC motor drive fed from Bridgelesss SEPIC with coupled inductors is discussed. The laboratory prototype of bridgeless SEPIC with coupled inductors rated for 500 W is implemented. The interfacing circuits consisting of encoder feedback processing, DC link voltage sensing and processing, optocoupler based voltage level amplifying interface circuit, and high voltage IGBT gate drive circuit are built. The digital controller consisting of electronic commutation logic and DC link voltage controller is implemented using Xilinx Artix 7 FPGA. Experimental evaluation of BLDC motor drive fed from bridgeless SEPIC with coupled inductors is presented. The next chapter presents the conclusion and scope for future works of the research work carried out.

Chapter 6

Conclusion and Recommendations for Future Work

6.1 INTRODUCTION

In this chapter, the conclusions and major contributions of the research work are described, followed by the scope for the future work.

6.2 CONCLUSION

In the work presented in this thesis, the control of BLDC motors using PAM control of VSI is chosen which eliminates high frequency switching losses in the three-phase VSI. This method also eliminates the need of motor current sensors and complicated control required to generate PWM signals for the VSI. One cycle controlled bridgeless SEPIC with coupled inductors is proposed to accomplish PAM control of VSI in this reasearch work. The proposed bridgeless SEPIC converter employs lower self-inductance when compared to conventional bridgeless SEPIC topology by adopting coupled inductors in the structure. Input and output two inductor windings of converter with less number of turns, wound on a same core results in reduction of size and cost. The one cycle control technique, presented in this work overcomes the transient oscillations and large peak overshoots under parameter variation and load disturbance compared to PI controller. The experimental results obtained validate the satisfactory performance of proposed converter for PAM controlled BLDC motor drive.

The design and analysis of bridgeless SEPIC with coupled inductors is detailed in chapter 3. Major contribution of the work involves, the design of coupled inductors, which is realized using split winding scheme. The desired coupling parameters for the design of coupled inductors are obtained using T-model. The magnetic design involving the calculation of core and winding geometry are obtained using area product approach. The theoretical evaluation of magnetic design is demonstrated, which shows the 42 % reduction in weight, 45% reduction in cost, and approximately 2 % increase in efficiency at rated power compared to converter without coupling for the same rating. The simulation results conclude that the proposed converter exhibits the desired performance as that of the conventional converter with a reduction in the size, cost, and improved efficiency.

The PAM controlled BLDC motor drive using one cycle controlled bridgeless SEPIC with coupled inductors is dealt in chapter 4. One cycle control for controlling DC bus voltage enhances the performance of the BLDC drive compared to PI controller. At steady state, a better performance is shown by one cycle control with improved power factor and reduced source current THD, over a wide speed range. The oscillatory transients in the speed response at start-up and transient states are reduced with one cycle controller compared to the PI controller. This lowers the supply current overshoot and thereby reduces the stress on the switch. At the instant of step change, an overshoot of 1.5 times the steady-state value is observed in the supply current with one cycle controller, whereas it is 2.8 times with PI controller. This has influenced the overshoots in the motor current and torque proportionately, resulting in better dynamic response of the BLDC drive with one cycle controller. The control performance is assessed using IAE, ISE, ITAE, ITSE indices, improved values of indices are obtained with one cycle controller for different speeds. Hence this control technique ensures the better performance of BLDC drive by improving both the steady-state and transient performance.

The proposed PAM controlled BLDC drive is simulated in MATLAB/ Simulink with control algorithm implemented on FPGA using Xilinx System Generator for dy-

namic step change conditions of reference speed and supply voltages. The dual loop speed controller having outer speed PI controller and inner voltage loop using PI controller is implemented digitally. The results obtained on Xilinx Waveform Viewer validates the effectiveness of controller design for dynamic step change conditions of both reference speed and supply voltage, ensuring the adequate performance of the dual loop controller in real time system.

The implementation and evaluation of PAM controlled BLDC motor drive fed from the PI controlled bridgeless SEPIC with coupled inductor is explained in chapter 5 of the thesis. The experiments are conducted to evaluate the operation of bridgeless SEPIC with coupled inductors for resistive load and for BLDC motor drive for different reference voltages of 130 V and 160 V, and for different supply voltages of 90 V and 125 V. From the PI-controlled closed-loop experimental results conducted on resistive load, it is observed that performance under steady-state and dynamic conditions is satisfactory. The response of DC link voltage under steady-state and dynamic conditions is fast. Also, the power factor of supply current is near unity. The adjustable speed operation of BLDC motor using adjustable DC link voltage (N/V_{dc}) is also verified experimentally. Control response of DC link voltage for different reference DC link voltage is quick with the response time of 1.04 s for a change in actual DC-link voltage value from 130 to 160 V and 1.32 s for 160 to 130 V. The control response of DC link voltage for different supply voltages observed to be faster with 1.08 s for the change in supply voltage of 90 to 110 V and 1.28 s for change in supply voltage of 110 V to 90 V. The supply current of near unity power factor is also validated. From the results it is also found that the total harmonic distortion is within the IEEE standard IEC61000-3-2.

6.3 CONTRIBUTIONS

The major contributions of the research work are listed as given below:

- Design and development of laboratory prototype of an improved, compact and efficient bridge-less SEPIC with coupled inductors.
  - Theoretical analysis of the effect of coupling between the input and output side inductors of SEPIC on its performance, size and cost.

  - Determination of the desired coupling parameters using T-model and Design of magnetic structure for coupled inductors of bridge-less SEPIC using split winding scheme, which has resulted in the closed form solution for desired coupling parameters using the mathematical approach.

  - Experimental evaluation of supply current shaping and DC link voltage control for resistive load.

- Design of PI and one cycle controllers to control the dc link voltage of bridge-less SEPIC with coupled inductors for PAM controlled BLDC motor drive.

  - Performance analysis of PAM controlled BLDC motor drive using bridge-less SEPIC with coupled inductors for PI and one cycle controller through simulation.

  - Digital implementation of dual loop PAM controller using FPGA and evaluation using co-simulation.

- Development of laboratory prototype of PAM controlled BLDC drive fed from PI controlled bridge-less SEPIC with coupled inductors.

  - Digital implementation of electronic commutation logic and PI control technique in Artix-7 FPGA using Xilinx system generator design tool.

  - Implementation of interfacing circuits of voltage sensing and signal conditioning, encoder signal conditioning, voltage level amplifier for gating signals of VSI, driver circuit for PWM signals of bridge-less SEPIC with coupled inductors.

  - Experimental evaluation of system performance under steady state and dynamic conditions.

6.4 SCOPE FOR FUTURE WORK

The recommendations for future research, based on this work are as follows:

- The experimental validation of PAM controlled BLDC motor drive using one

cycle controlled bridgeless SEPIC with coupling.

- The bridgeless configurations of CUK, Zeta converters can be improved with coupling feature and can be used for PAM controlled BLDC motor drive.
- The study on improved design of magnetic structure for coupled inductors of desired coupling parameters can be done. Possibility of design with different core shapes and studies on optimising the design can be evaluated.

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Curriculum Vitae

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List of Publications based on PhD Research Work

Sl.No	Title of the paper	Authors (In the same order as in the paper. Underline the Research Scholar's name)	Name of the Journal/ Conference/ Symposium, Vol., No., Pages	Month & Year of Publication	Category*
1	Design of coupled inductors using split winding scheme for bridgeless SEPIC	Pavana Prabhu, Vinatha Urundady	IET Power Electronics, 13(7), 1434-1444.	May, 2020	1
2	One-cycle controlled bridgeless SEPIC with coupled inductors for PAM control-based BLDC drive	Pavana Prabhu, Vinatha Urundady	Arabian Journal for Science and Engineering, 44(8), 6987-7001.	February, 2019	1
3	FPGA based experimental evaluation of BLDC motor drive fed from coupled inductor based bridgeless SEPIC	Pavana Vinatha U	IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020) (pp. 1-6). IEEE.	April, 2020	3
4	One cycle controlled bridge-less SEPIC converter fed BLDC motor drive.	Sonu Jayachandran, Pavana Vinatha U	IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES)	November, 2017	3
5	Speed control of BLDC motor using bridgeless SEPIC PFC with coupled inductors.	Pavana Vinatha U	11th International Conference on Industrial and Information Systems (ICIIS), IEEE (pp. 798-803).	January, 2018	3
6	One Cycle Control based SEPIC PFC for PAM-BLDC Motor drive	Pavana Vinatha U	2nd International Conference on Systems, Energy and Environment (ICSEE– 2017), pages 271–276	December,2017	3

*Category: 1: Journal paper, full paper reviewed 2: Journal paper, Abstract reviewed
3: Conference/Symposium paper, full paper reviewed 4: Conference/Symposium paper, abstract reviewed
5: others (including papers in Workshops, NITK Research Bulletins, Short notes etc.)
(If the paper has been accepted for publication but yet to be published, the supporting documents must be attached.)
**The travel grant is approved through DST (ITS scheme). Likely to attend the conference, if the procedures for VISA are completed in-time. Further, the paper will be invited for publication in an SCI indexed journal.

PAVANA

Research Scholar
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