LOW POWER NONBINARY WEIGHTED SUCCESSIVE APPROXIMATION REGISTER ANALOG TO DIGITAL CONVERTERS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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September, 2021

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **LOW POWER NONBINARY WEIGHTED SUCCESSIVE APPROXIMATION REGISTER ANALOG TO DIGITAL CONVERTERS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to certify that the Research Thesis entitled **LOW POWER NON-BINARY WEIGHTED SUCCESSIVE APPROXIMATION REGISTER ANALOG TO DIGITAL CONVERTERS** submitted by **Mrs. KALPANA G BHAT** (Reg. No. 100543EC10P01) as the record of the research work carried out by her, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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Acknowledgements

Pursuing Ph.D degree in ECE department, NITK in the field of Analog and Mixed signal IC design is one of the greatest experience of my life. It was filled with lot of challenges and never ending issues to address at each and every step of my research work. This work is being accomplished with the grace of my guru and with the love, support and understanding of many people, who gave themselves, knowingly or unknowingly, willingly or unwillingly, consciously or unconsciously. I am grateful to them all and dedicating this to each one of them.

I would like to express my gratitude to my first research supervisor and HOD, Prof. Laxminidhi. T., for not only providing me technical and research guidance but also practical advice in my work. As my exposure to analog IC design before taking up research was minimal, he was very instrumental in driving me to work towards research objectives as well as completion of thesis. I always remember that during our meetings he would challenge me to push the boundaries of my research further when I strongly believed it wasn't possible. This really helped me to become more critical in thinking about the research problem. And I also express my heart felt thanks for his support in bringing out the thesis in its present form.

I am very much thankful to Prof. M S Bhat, my second research supervisor for his able guidance and valuable inputs he provided during discussions, presentations and thesis writing. I would also like to thank my research committee members, Prof. Sripathi Acharya and Prof. Subba Rao. In the limited time during meetings they always pointed me towards right direction and helped me put my research into perspective. My heartfelt thanks to Dr. Muralidhar Kulkarni, earlier HOD, for his wholehearted

support in taking up this research work at the right time and supporting me throughout in this journey.

I would also like to thank MeitY, Government of India, for providing the EDA tool through SMDP-VLSI project.

I sincerely thank research scholars Yajunath, Kiran Lad, Hanumanthu, Jayram, Jagadish and Sreenivasulu for their timely help in understanding simulation tools and sharing their knowledge.

This work wouldn't have been possible without the support of my colleagues at NITK. Their help in terms of sharing teaching loads as well as guidance and providing moral support during difficult phases of research work. I am also thankful to Mr. Sanjeeva Pujari, Mr. Subrahmanya Karanth, Mr. Gurutilak S, Mrs. V Prabha, Mrs. Sowmya and Mr. Ratish of our department for all help and support.

I am very fortunate to have wonderful sons Shreesha and Shreeharsha, as they were guiding force for me to work towards successful completion of research. Most of the times I was getting inspiration from them to work harder. My beloved husband Dr. Gopalakrishna Bhat, his constant support and encouragement during this period helped me to believe in my strength, which made me to progress in the work.

I am very grateful to Dr. Sumam David for her encouragement and support to take up the research work. Dr. Vinod V Thomas, thank you for being like a big brother to me. You truly touched and transformed my life.

Last but not the least, I bow down to my Guru again, for his grace as well as teachings in the form of yogic practices and meditation which helped me to regain my health, without which I would not reached this stage in the research.

Kalpana G Bhat

Dedicated to my beloved parents

Abstract

Modern instrumentation systems and data acquisition (DAQ) systems demand low to medium resolution, medium speed analog to digital converters (ADC). For DAQ systems with dedicated ADCs per channel, ADC core area is of prime concern to minimize cost/chip. For DAQ systems with a single ADC for multiple channels, it may be required to operate the ADC at different resolutions depending on the channel it is digitizing. In such a case, programmable resolution ADC is an added advantage. Even though the traditional successive approximation register (SAR) ADCs are popular in these applications, they consume large chip area.

To optimize ADC over area, nonbinary weighted capacitive (NBWC) digital to analog converter (DAC) architectures are proposed in this work, which makes use of a fixed number of nonbinary weighted capacitors, low power transconductors and switches.

Initially, as a proof of concept, a DAC architecture using minimum number of unit size capacitors and buffers is designed for the SAR ADC. In order to enhance sampling speed, a 2 bit per cycle algorithm is developed instead of the conventional 1 bit per cycle evaluation. The designed 8 bit ADC is simulated in 180 nm technology and supply voltage of 3.3 V. The ADC designed could achieve a conversion speed of 500 kS/s with a power dissipation of 1.8 mW. Integral non linearity (INL) error and differential non linearity (DNL) error are less than 0.5 LSB. The simulated signal to noise and distortion ratio (SNDR) at the input frequency of 56.64 kHz is 48.14 dB and at 232.42 kHz is 47.03 dB.

Though the proof of concept ADC simulation results were encouraging, the voltage dependent nature of the parasitic capacitance posed by the switches were found to be the bottleneck in achieving a low value of area efficiency (AE). Therefore, the switched capacitor DAC architecture used in the proof of concept ADC is modified so that the reference generation circuit for the 2 bit per cycle evaluation is least sensitive to parasitics as well as the ADC resolution is made programmable. A programmable 4 to 8 bit DAC is further designed for the SAR ADC with increased sampling rate of 1.2 MS/s at 8 bit mode. Passive charge sharing and charge recycling

through low power buffers is adopted in the NBWC DAC. A mathematical analysis has also been carried out to justify the parasitic insensitive nature of the reference generation scheme. The proposed idea has been validated by designing a 4 to 8 bit ADC in 90 nm CMOS technology for operations on 1 V supply. The post layout simulation of the designed ADC has 1.2 MS/s sampling rate at 8 bit mode with a power consumption of 185 μW achieving an effective number of bits (ENOB) of 7.6. The active area of the designed ADC is 0.06 mm^2, resulting in an AE as low as 295.66 μm^2/code. The DAC resolution scaling and the use of variable sampling rate maximizes efficiency at lower resolutions. Therefore figure-of-merit (FOM) degrades only by a factor 4.7 for resolution scaling from 8 bits to 4 bits. This is a significant improvement over the 16x degradation expected from 8 bit to 4 bit resolution scaling by truncating the bits.

Another work, as part of this thesis, is exploring switched capacitor integrator (SCI), NBW-CDAC based SAR ADC. The objective is to develop resolution independent, programmable resolution architecture using minimum number of NBW capacitors and switches for fully differential approach. A compact SC integrator based nonbinary weighted 10 bit SAR ADC is designed for low power portable devices and data acquisition systems. This technique requires an operational transconductance amplifier (OTA), a comparator and six equal sized capacitors of moderate value for fully differential approach. The reference voltage is generated by charge sharing between a reference capacitor and the input capacitor of an switched capacitor (SC) integrator. The DAC voltage for comparison is generated by accumulating the charges on the integrating capacitor. ADC being fully differential, has a wide input range and is largely parasitic insensitive. As a stand alone data converter it has a small capacitance spread and hence its input capacitance is easy to drive. A 10 bit 0.9 MHz sampling rate SAR ADC is designed using 180 nm CMOS technology, operating at 1.8 V supply, has ENOB of 9.5 at Nyquist frequency. The area occupied by the designed ADC is 0.05 mm^2, resulting in an AE as low as 69.32 μm^2/code. It is found that the designed ADCs are having better AE as compared to state of the art binary weighted capacitive (BWC) and NBWC SAR ADCs in the literature. These designs are also useful

to build high resolution, low power, high speed ADCs such as pipelined, sub-ranging, folding and interpolating ADCs.

Keywords: SAR ADC, low power, charge recycling, 2 bit per cycle, parasitic insensitive, programmable resolution, nonbinary, charge sharing, switched capacitor integrator, SC, OTA.

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Abbreviations

ADC	Analog to Digital Converter
AE	Area Efficiency
BWC	Binary Weighted Capacitor
CDAC	Capacitive Digital to Analog Converter
CMOS	Complementary Metal Oxide Semiconductor
CMFB	Common Mode Feed Back
DAC	Digital to Analog Converter
CPh	Comparison Phase
D-FF	D-type Flip Flop
DNL	Differential Non Linearity
DAQ	Data Acquisition System
ENOB	Effective Number of Bits
ECG	Electrocardiography
FFT	Fast Fourier Transform
FOM	Figure of Merit
FSM	Finite State Machine
FPBW	Full Power Bandwidth
IC	Integrated Circuit
INL	Integral Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	N-channel Metal Oxide Semiconductor
NBW	Nonbinary Weighted
NBWC	Nonbinary Weighted Capacitor
OSR	Over-Sampling Ratio
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PMOS	P-channel Metal Oxide Semiconductor
PVT	Process, Voltage and Temperature
PE	Power Efficiency
RMS	Root Mean Square
REF-DAC	Reference DAC
RPh	Recycling Phase
RC	Resistance Capacitance

S/H	Sample and Hold
SAR	Successive Approximation Register
SoC	System-on-Chip
SC	Switched Capacitor
SIG-DAC	Signal DAC
SCI	Switched Capacitor Integrator
SBC	Split Binary Weighted Capacitor
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
SBW	Split Binary Weighted capacitor array
TWC	Two stage Weighted Capacitor array
TG	Transmission Gate
TSMC	Taiwan Semiconductor Manufacturing Company
UGB	Unity Gain Bandwidth
UMC	United Microelectronics Corporation

Chapter 1

INTRODUCTION

1.1 MOTIVATION

Analog to digital converters and digital to analog converters are essential building blocks of many portable systems providing interface between the physical world and the digital signal processing systems. In order to reduce the size and cost/chip often analog interfaces and the digital signal processing blocks are co-integrated on a single die. With the fast advancement of CMOS fabrication technology, lot more signal processing functions are implemented in the digital domain as benefits are manifold such as low cost, low power consumption, higher yield and re-configurability. In bringing the interface between the analog and digital world to as close as possible, ADCs and DACs play a significant role. There is a great demand for low power, low voltage designs that can be realized in a mainstream deep submicron CMOS technology.

However, low supply voltage constraint makes the analog circuit design challenging due to the reduced signal swing. On the other hand, scaling down of the CMOS technology results in the degradation of the device characteristics, making the analog integrated circuit (IC) design in nanometer CMOS technologies even more challenging. Although technological developments bring a part of the performance upgrade, continual efforts are being made in the form of research to improve the performance further. As the saying goes "No free lunch", any improvement on one front will definitely have an adverse effect on the other and that is how nature is. Therefore,

research towards bringing out innovative ADC conversion algorithms and circuits to suit many application is worth trying. This has been one of the main motivations for this research work.

A survey of ADCs reported between 1997 to 2015 presented at the IEEE International Solid State Circuit Conference (ISSCC), reveals SAR ADC is the most preferred architecture due to low power consumption and low area (Murmann et al. 2016). The SAR ADCs show excellent power performance at medium resolution and low to medium speed range (refer Figure 1.1(a) and (b)). The area performance is excellent as can be seen from Figure 1.1(c). The plot of area vs FOM shown in Figure 1.1(d) reveals that SAR ADCs are area and power efficient.

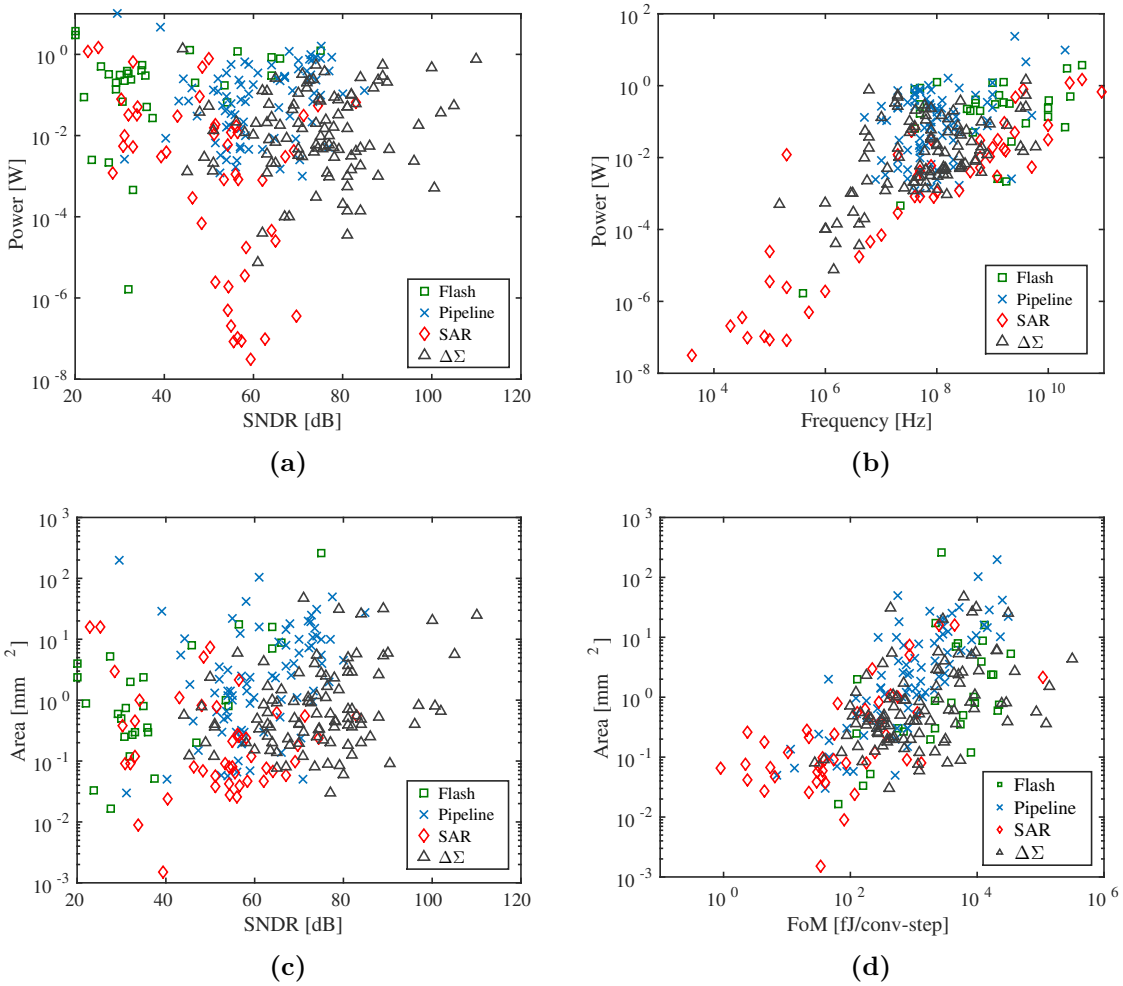

Figure 1.1: Performance plots of published ADCs in ISSCC (a) power vs SNDR (b) power vs Nyquist frequency (c) area vs SNDR (d) area vs FOM.

The continuous scaling of technology has had an impact on analog and mixed signal designs. This has prompted the designers to look closely into existing architectures and algorithms and suggest modifications necessary to overcome the limitations. As ADCs are a vital building block in typical signal processing systems, ADCs suitable for applications demanding low/medium power with emphasis on lower area, to save on silicon real-estate are found to be attractive to take up as a research problem.

Data acquisition applications invariably involves digitizing analog signals for analysis. Signals are pre-processed by amplifiers and filters and then digitized by ADCs before feeding it to processors for performing the required data analysis. In multi-channel DAQ systems, SAR ADCs are the preferred choice as they allow system designers to achieve a very good channel density (Peje 2018).

Figure 1.2 shows the block diagram of a typical DAQ system used in a process control application (Kester 1995).

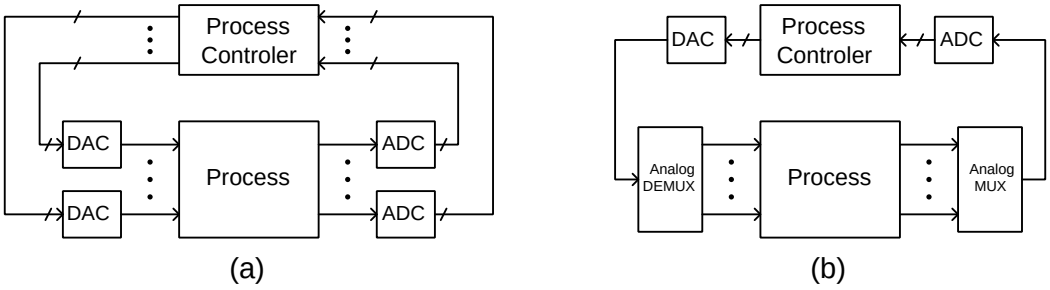

Figure 1.2: Typical DAQ used for a process control (a) DAQ using ADC/DAC per channel (b) DAQ system with channels multiplexed/demultiplexed into a single ADC/DAC

In process control applications, the process controller generates feedback signals that are necessary for controlling the process. These feedback signals are converted back into analog form using a DAC. Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term data acquisition generally refers to multi-channel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as data distribution. Figure 1.2(a) shows a data acquisition/distribution process system where each channel has a dedicated ADC and DAC. Another approach is shown in Figure 1.2(b), where all process signals are multiplexed/demultiplexed into a single ADC/DAC using analog multiplex-

ers/demultiplexers. For multi-channel DAQ, in most cases, the latter approach provides an economical alternative.

For DAQ systems with dedicated ADCs per channel, it is important to have ADC designs that occupy as little area as possible to save on the silicon cost apart from the power. For DAQ systems with single ADC, it may be required to operate the ADC at different resolutions depending on the channel it is digitizing. In such a case, the ADC should have a feature of resolution programmability.

In DAQ systems used for neuroprosthetic applications, each electrode senses signals from multiple neurons which needs to be distinguished. Therefore, the resolution required to digitize the signal from each electrode is not uniform across all electrodes (O'Driscoll et al. 2011). In addition, the biomedical monitoring systems used to record various physiological parameters are required to process vital signals having varying bandwidth as well as dynamic range requirements. For example, for applications such as Electrocardiography (ECG) monitoring, low resolution is desirable to detect the heart rate and high resolution to observe ST pattern changes (Jeong and Yu 2006, Yip and Chandrakasan 2013). The ADCs in such systems should have the resolution and sampling rate necessary to cater to the requirements of the signal being processed. SAR ADCs with capacitive DACs are popular for biomedical signal digitization due to their low power requirements. However, conventional SAR ADCs with a fixed resolution and sampling rate are not able to adapt to multiple signals demanding different resolutions. ADCs having programmable resolution and sampling rate are appropriate for these applications.

A common fact found in the literature is that majority of the research on ADCs revolve around the conventional architectures mainly focusing on the power efficiency (PE). Area efficiency (AE) of the ADCs is typically not a prime concern. In addition, if the ADCs are designed to have the feature of resolution programmability, the design time can be significantly reduced as the same design can be reproduced for use in different channels. In addition, they also can effectively reduce the silicon real estate if reused through time multiplexing if one has a leverage on time.

Therefore, considering the above facts, this research is aimed towards the design of SAR ADCs for low and medium speed applications with AE as the parameter of focus, with multi-channel DAQ and instrumentation systems as wish targets. The main focus has been kept on the research towards proposing modifications to SAR

architecture with an intent to propose architecture having better AE and to have a resolution programmability with ease.

1.2 PRIOR WORK

A conventional SAR ADC, as shown in Figure 1.3, uses a capacitor charge redistribution DAC, introduced by McCreary and Gray (1975). As the name suggests, this architecture works on the successive approximation algorithm. The input is compared with the reference and the out bit is stored in a register. Depending upon the output, a DAC sets the reference input of the comparator for the next comparison. Since this requires a single comparator, SAR ADCs tend to occupy as small area and consume very low power. Two major limitations of traditional capacitor charge redistribution SAR ADCs are conversion speed and the bulky capacitive array. Speed of conversion is limited as it requires N-clock cycles to convert N bits. DAC capacitive array used in this architecture becomes very bulky and power hungry as the resolution of ADC increases. The bulky binary weighted capacitor arrays employed in the above architectures require large silicon area.

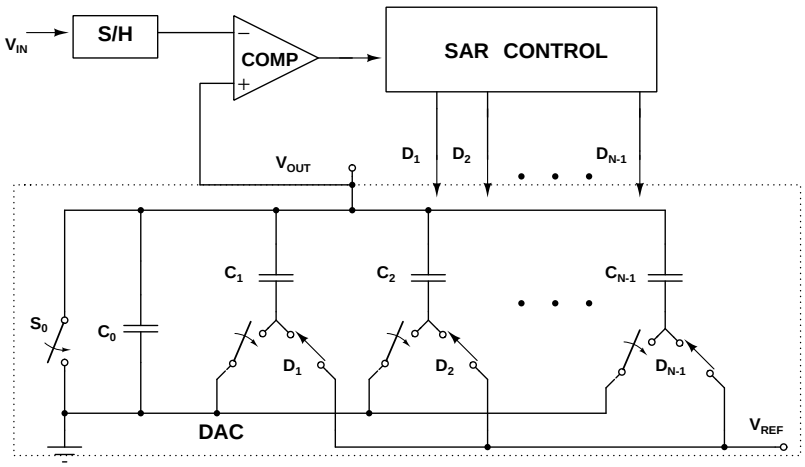

Figure 1.3: Conventional SAR ADC

In this section, a literature review of different types of SAR ADC techniques, that are found to have been designed with similar purpose, are explored. Mainly two types of SAR architectures are found in the literature. One category is SAR

with separate DAC and sample and hold (S/H) circuit. The other is SAR having capacitive DAC and inherent S/H circuit. The SAR ADC with separate DAC and S/H architecture is quite straight forward and used by many SAR ADC designs in the literature (McCreary and Gray 1975, Sauerbrey et al. 2003, Hong and Lee 2007). Even though additional power is needed for independent S/H, this architecture makes the input capacitance of the converter independent of the DAC, specially with DAC capacitor array. In the latter approach S/H is embedded into the DAC capacitor array thus making it simpler than the former approach and it also consumes lesser power. There are many designs based on this architecture that are found in the literature (Scott et al. 2003, Gambini and Rabaey 2007, Ginsburg and Chandrakasan 2007). Another advantage of this architecture is that the switching point of the comparator is independent of the input signal, hence rail to rail input common mode range for the comparator is not needed. This avoids the problem caused by the comparator offset with the input level. But the input capacitance of the ADC which is determined by the entire capacitive array is much larger than that of the former method.

The most important building block in the SAR ADC is the DAC, and it is a component which takes a major share of the power. This block determines the accuracy and conversion speed of the converter (Scott et al. 2003). The DAC required in the SAR ADC is realized in many ways; e.g.,

- Capacitor based DAC (McCreary and Gray 1975, Ginsburg and Chandrakasan 2007)
- Switched current DAC (Saul 1981, Dlugosz and Iniewski 2006)
- R-2R ladder DAC (Fayomi et al. 2001, Lin and Liu 2003)

Among these architectures capacitive DACs are preferred over resistive DACs because of their zero quiescent current, and less mismatch and tolerance than resistors in most of the earlier technologies (Saberi et al. 2011).

This thesis work mainly concentrates on the research towards proposing modifications to the SAR architecture with an intent to replace the conventional binary weighted capacitor array based DAC with a DAC that has a reduced/fixed number of unit size capacitors. Mainly there are three types of capacitor array DACs found in literature.

- Binary weighted capacitor array (BWC) DAC
- Two stage weighted capacitor array (TWC) DAC
- Split binary weighted capacitor array (SBW) DAC

The BWC DAC was first reported in 1975 (McCreary and Gray 1975). The schematic of this DAC is shown in Figure 1.4.

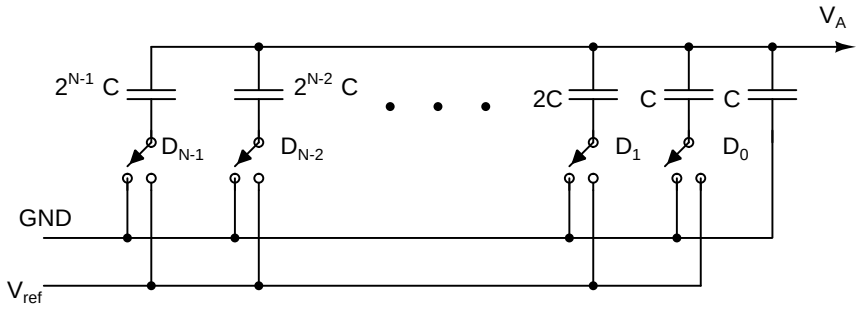

Figure 1.4: Binary weighted capacitor array DAC

Circuit operation has two modes, reset and conversion. During the reset mode, all the switches are connected to ground, allowing the bottom plate of all the capacitors in the array to discharge. During the conversion mode, the digital logic will determine which switches need to be remove from ground to V_{ref}. During conversion period the charge gets redistributed in the capacitor arrays and develop a next voltage for comparison. The binary search algorithm followed for resolving the ADC code results in the node voltage V_A to converge towards zero. The BWC DAC was adopted in Gambini and Rabaey (2006), Hong and Lee (2007). The main limitation of this architecture is that with the increase in the number of bits N, the total capacitance tends to increase exponentially. Since power consumption of the SAR ADC is directly proportional to the total capacitance of the DAC arrays, the power consumption also increases exponentially with N. Therefore the accuracy of this DAC is limited to 8 to 10 bits (Cong 2001).

Several attempts have been made to solve the problem in the BWC DAC. One of the most popular solutions is to employ an attenuating capacitor in the BWC array (Zhu et al. 2010, 2008). Here the capacitor array is split into 2 sub arrays as shown in Figure 1.5 for an 8 bit DAC, as an example. Therefore, the DAC is called TWC DAC.

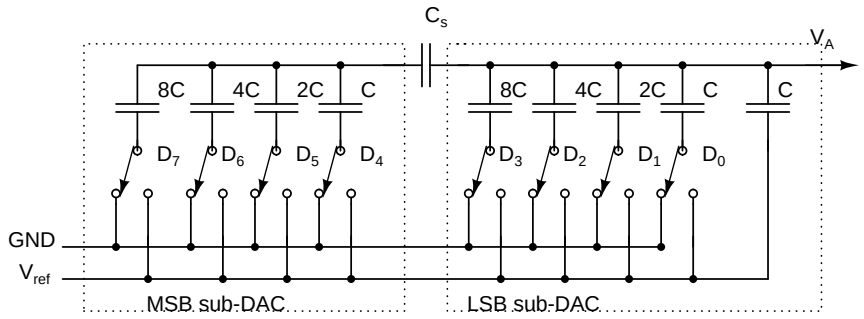

Figure 1.5: Two stage weighted capacitor array DAC

TWC DAC requires a smaller range of capacitor values over BWC DACs with improved linearity and resolution. It was introduced in Yee et al. (1979). The capacitor array is split into k most significant bit (MSB) array and m ($m = N - k$) least significant bit (LSB) array and a coupling capacitor C_S that connects these two arrays. Therefore the values of the capacitors related to MSBs are decreased by a factor of 2^m in comparison to BWC array DAC. Thus the switching losses are decreased. The value of $C_s = 2^m \cdot C/(2^m - 1)$. However, the switching sequence of the DAC is same as the BWC DAC.

The SBW DAC was first proposed in Ginsburg and Chandrakasan (2007). This DAC was proposed to save power consumption during the switching of the BWC array, especially during down transition. Figure 1.6 shows an SBW based 2 bit DAC structure. In this method, the MSB capacitor of the BWC architecture is realized as a capacitive binary weighted sub array (called as MSB sub array) exactly similar to the rest of the main array. The switching algorithm is modified as follows. In the first conversion cycle, all capacitors of the MSB sub arrays are connected to V_{ref} and other capacitors to ground. If $D_1 = 1$, this means an up transition after the comparison process after which the algorithm follows the BWC algorithm. If down transition, then half of the MSB sub array capacitors ($C_{2,1}$) are connected back to ground leaving the other capacitors of the MSB sub array connected to V_{ref} and the rest unchanged. This procedure is repeated till all the N bits are resolved. Therefore, power saving is possible with this method in every down transition (Saberi et al. 2011).

An extension of the TWC array DAC is a C-$2C$ ladder DAC, the schematic of which is shown in Figure 1.7. Compared to the BWC DAC architecture, this ladder DAC has a smaller RC time constant and hence potentially faster. Furthermore, the capacitor matching is better. It also consumes lower power because of the smaller

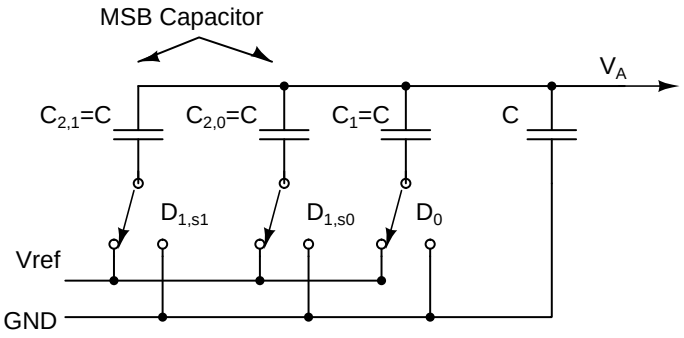

Figure 1.6: Split binary weighted capacitor array DAC, for a 2 bit case

capacitance when compared to the BWC DAC (Balasubramaniam et al. 2009). There is a linearity issue due to parasitic capacitance in the interconnecting nodes. Several attempts have been made to improve the linearity of this DAC. One such approach is a pseudo C-$2C$ ladder, which aims at compensating for the parasitic capacitance effect during the design phase itself (Cong 2001).

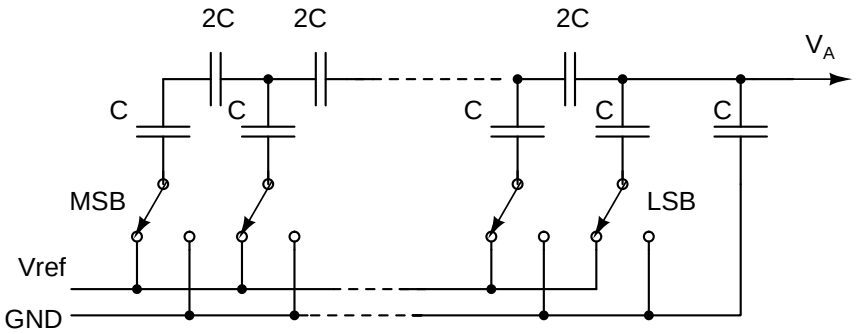

Figure 1.7: C-2C ladder DAC

All the above capacitor DACs can be used in a fully differential technique (Zhu et al. 2010, Liu et al. 2010a, Cho et al. 2010, Liu et al. 2009). Main advantage of a fully differential approach is the good noise rejection and an improvement in the dynamic range at the cost of extra power and area when compared with the single ended architecture.

1.2.1 Nonbinary weighted capacitor DAC

A set of researchers have explored realizing DACs using nonbinary weighted capacitors. In the ADC proposed by Choi and Tsui (2009) decoding of MSB bits and LSB

bits are done using two different capacitive arrays with unequal sized capacitors (non-binary) to reduce the power consumption. The energy savings have been achieved at the cost of two additional clock cycles. Moreover this layout occupies more area than the traditional approach.

A whole new DAC architecture was proposed by Kamalinejad et al. (2011) for low power and area efficient SAR ADC. The DAC employs two rail to rail low power unity gain buffers and only 4 minimum sized capacitors instead of a conventional BWC array. The architecture is highly area efficient because of it's simple structure and few capacitors. The architecture looks very promising in terms of AE. However the requirement on buffers makes it power hungry as compared to the conventional CDAC. But, this ADC can be a very good candidate for applications where area is of prime concern (since silicon real estate has a direct impact on the cost) and the power requirement is relaxed. One such application could be where there is a requirement of multiple ADCs like multi-channel DAQ with dedicated ADC per channel. Surprisingly, no research has been found subsequent to the publication of this article.

Yet another way of implementing nonbinary SAR ADC is SC integrator based ADCs. In a conventional BWC SAR ADC, for every bit increase in the DAC resolution, total DAC capacitance doubles which in turn limits the size of the unit capacitor for a given area requirement. To meet the accuracy requirement and to minimize KT/C noise, a unit capacitor should be of a reasonable size. Especially in charge redistribution SAR ADCs, DAC capacitors are used to sample the input signal as well. Hence for medium resolution applications, total input capacitance of ADC becomes appreciably large. On the other hand, nonbinary weighted DAC overcomes this problem as there are only a fixed number of unit capacitors to be used in the DAC irrespective of the resolution of the ADC. Due to reduced number of unit capacitors in the DAC, mismatch errors are greatly reduced. Also there is no need of explicit sample and hold circuit as it can be absorbed into the SC integrator. There are a few SC integrator based nonbinary ADCs reported in the literature (Seongik and Minwoong 2017, Polineni et al. 2020, **?**). It is observed that there is an opportunity for re-looking at the SC integrator based SAR ADC architecture.

The ADCs (BWC DAC and NBWC DAC) are compared with respect to their reported PE in terms of figure of merit (FOM) and AE and listed in the Table 1.1. The FOM is calculated using (1.1) (Plassche 2003).

$$FOM = \frac{\text{Power}}{2 \times f_{in} \times 2^{ENOB}} \qquad \text{(J/conv)} \tag{1.1}$$

where f_{in} is the frequency of the input. Lower FOM indicates better design. The area efficiency (AE) is computed from (1.2) (Xu et al. 2012).

$$AE = \frac{\text{CoreArea}}{2^{ENOB}} \qquad \mu\text{m}^2/\text{code} \tag{1.2}$$

Surprisingly, though ADCs with NBWC DAC are expected to have good AE as compared to BWC DAC, the reported NBWC ADCs are found to have AE which is similar to that of BWC ADC. Therefore, this research is aimed towards designing NBW ADCs with a good AE number. A detailed review of NBW ADCs found in the literature is given in Chapter 2.

Table 1.1: Comparison ADCs with respect to parameters AE and FOM

Reference	**Tech.**(nm)	**Arch.**	**FOM**(pJ/cs)	**AE**(μm^2/c)
Mortezapour and Lee (2000)	120	BWC	711.72	13564.63
Sauerbrey et al. (2003)	180	BWC	7.9	371.48
Scott et al. (2003)	250	BWC	2.63	414.06
Hong and Lee (2007)	180	BWC	19.4	390.7
Gambini and Rabaey (2007)	90	BWC	0.506	3646
Ginsburg and Chandrakasan (2007)	180	BWC	0.7209	55319.75
Yang and Van der Spiegel (2008)	250	BWC	0.576	4.465
Cao et al. (2009)	130	BWC	0.800	1855.55
Zhu et al. (2010)	90	BWC	0.0778	467.11
Wei et al. (2011)	65	BWC	0.117	282.23
Sekimoto et al. (2011)	180	BWC	0.221	752.62
Kuo and Hsieh (2011)	180	BWC	8.007	1440.82
O'Driscoll et al. (2011)	130	BWC	0.048	531.1
Yoshioka et al. (2012)	40	BWC	0.019	106.244
Yip and Chandrakasan (2013)	65	BWC	0.0224	462.62
Chaturvedi et al. (2013)	130	BWC	0.0423	787.74
Elkafrawy et al. (2015)	65	BWC	8.161	2720
Liu et al. (2016)	130	BWC	0.0442	201.35
Li et al. (2020)	130	BWC	0.0394	126.11
Kamalinejad et al. (2011)	130	NBW	0.062	-
Saisundar et al. (2012)	180	NBW	0.192	480.24
Hong et al. (2015)	45	NBW	0.080	1792.44
Seongik and Minwoong (2017)	180	NBW	256	797.62
Shi et al. (2018)	180	NBW	0.0812	480.08

1.3 RESEARCH CONTRIBUTION

From the literature survey, SAR ADC architectures employing nonbinary weighted capacitors are found to be very promising in terms of AE. Therefore, this thesis is focusing on proposing architectures for SAR ADCs using NBWC DAC. Though the power requirement is relaxed, the ADCs are designed to draw as low power as possible (few hundreds of micro watts).

The first part of this research focuses on the development of an NBWC DAC based SAR ADC architecture. The proposed architecture stands on the idea presented in Kamalinejad et al. (2011). An NBWC DAC architecture has been proposed for evaluating 2 bit/step. The SAR algorithm is also suitably modified for 2 bit/step operation. Initially an ADC is designed as a proof of concept, in 180 nm standard CMOS process for operation on a 3.3 V power supply. However, the voltage dependent nature of the parasitic capacitance posed by the switches were found to be the bottleneck in achieving a low value of AE. The solution was to have a large sized capacitors for the NBW CDAC which in turn had an adverse effect on the power. In the proof of concept ADC, unit capacitor of 2 pF has been used and the power requirement was 1.8 mW.

Subsequently, a further research in this direction culminated in an NBW CDAC architecture for SAR ADC which has a low sensitivity to the parasitic capacitances. The architecture has been verified by designing an ADC, in 90 nm CMOS process, operating on 1 V supply. The capacitance requirement on the unit capacitor of the NBWC DAC was found to be reduced by a factor of ten. In addition, there was gain on power/speed. It is also found that the proposed ADC can be easily converted to have resolution programmability and therefore, a programmable resolution ADC for resolution in the range 4-8 bits is also realized. After the layout of the ADC, it has been proven from the AE (calculated using the formula, commonly found in the literature) that the proposed ADC is one of the best among the SAR ADCs. The ADC is also found to work satisfactorily for all process, temperature and supply voltage (PVT) variations.

Another work, as part of this thesis, is exploring SC integrator based NBWC DAC based SAR ADC. The objective is to develop resolution independent, programmable resolution architecture using minimum number of NBW capacitors and switches for fully differential approach. The SAR logic of the ADC is very simple and requires

only three AND gates and a D-flip flop for serial data output. A 10 bit ADC has been designed, as a test vehicle, in 180 nm technology node using UMC foundry library models at 1.8 V supply.

1.4 ORGANIZATION OF THESIS

The thesis is organized in the following manner. Chapter 2 does a detailed literature survey of NBWC SAR ADCs. In addition 2 bit/step SAR architectures and programmable resolution SAR ADCs are reviewed.

In Chapter 3, NBWC DAC based 2 bit/step SAR ADC is proposed as a proof of concept along with the design in 180 nm CMOS process and simulation results are presented.

In Chapter 4, the 2 bit/step SAR ADC presented in Chapter 3 is modified to make the DAC operation parasitic insensitive. The modifications are justified through mathematical analysis. The chapter presents the design and simulation of the ADC designed in 90 nm CMOS process.

Chapter 5 presents a SC integrator based NBWC SAR ADC along with the design and simulation results.

The thesis concludes with Chapter 6 giving leads on possible future work and describing the pros and cons of the methods proposed and contributed as a part of this thesis work.

Chapter 2

NONBINARY WEIGHTED CAPACITOR ADCs

Among the numerous Nyquist rate ADCs, SAR ADC is found to be one of the widely used ADCs because of its simple structure and few analog components. Analog to digital conversion comprises two fundamental functions, namely, sampling and quantization. The latter can be viewed as an operation wherein an analog estimate is identified and the digital equivalent of this estimate is created. SAR ADCs use binary search algorithm to compute analog estimates that successively converge towards the input voltage. Consider the block diagram of a conventional ADC shown in Figure 1.3. Suppose that the ADC has an input range of 0 to V_{REF} and it senses an input V_{in} as shown in Figure 2.1, the binary search begins by nominating $V_{REF}/2$ as the best analog estimate. Next, since $V_{in} < V_{REF}/2$, the search identifies $V_{REF}/4$ as a better approximation and the process continues. In each cycle, the ADC compares V_{in} with the most recent analog estimate and directs the search according to the polarity of their difference. The difference is called as residue and is denoted by V_{in} - r V_{REF}, where $r = 1/2, 1/4, 1/8$ etc., in the above example. The goal of the binary search is to reduce the residue to less than 1 LSB. While simple and efficient, SAR ADC suffers from a number of issues that call for additional circuit and architectural techniques if high performance is desired.

- Limited precision by capacitor matching: The SAR ADC imposes on its DAC both high accuracy and a high resolution. Thus, high resolution SAR ADCs

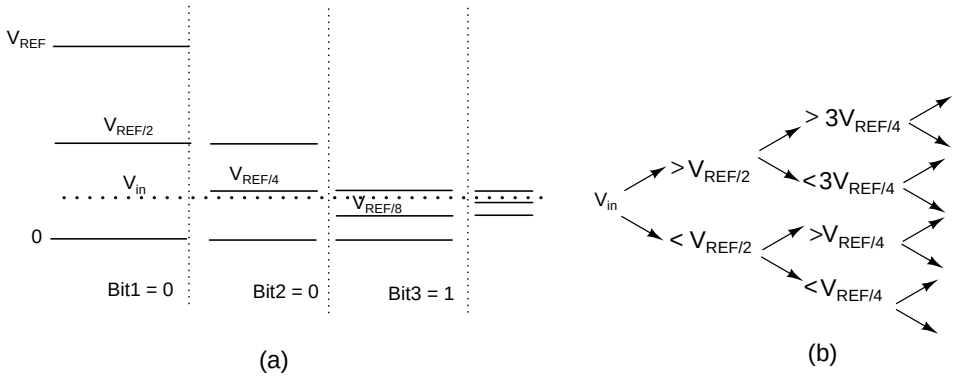

Figure 2.1: Binary search (a) Search for analog estimates (b) Decision directed binary search

tend to occupy a large area especially when the DAC unit capacitor size is dictated by matching requirements rather than by KT/C noise.

- Limited precision by comparator decision error: With binary weighted capacitor array, SNR tends to degrade due to comparator decision errors during bit decisions from MSB to LSB.

- Limited precision by comparator noise: The comparator input noise (thermal and/or $1/f$ noise) can limit the SNR of the ADC.

- Limited sampling frequency: Owing to the multiple clock cycles necessary for each conversion, the SAR architecture is typically slow.

In applications demanding multiple ADCs like in DAQ systems, silicon area occupied in System-on-Chips (SoCs) is also one of the key design constraints. Similarly, in applications like sensor nodes, unit cost of sensor node is of utmost importance which again points towards the silicon area.

In literature, it is found that majority of the research on SAR ADCs revolve around BWC DAC based architectures. However, in BWC DAC the area is predominantly decided by the capacitor array which in turn is decided based on the requirement on capacitor matching. A statistical analysis of the effect of capacitor mismatches in BWC SAR ADC presented in Wakimoto et al. (2011), shows that if a standard deviation of σ_u from the unit capacitance C_u is assumed, then the worst case standard deviation of DNL for an N bit binary weighted SAR ADC can be written as given in

(2.1).

$$\sigma_{DNL,max} = \sqrt{2^N - 1}\left(\frac{\sigma_u}{C_u}\right) \tag{2.1}$$

It is evident that the ratio of standard deviation of DNL to standard deviation of capacitor matching is decided by the unit capacitor of the array for a given N. In other words, the unit capacitance needs to be chosen for the matching requirement. With increase in N, the total capacitance of the array and hence the area requirement could be quite large. Therefore, in order to keep the unit capacitance to a sufficiently small value and still achieve the DNL performance, the designers resort to calibration techniques. Several such calibration methods have been proposed in the literature, for example, Gan and Abraham (2002), Hotta et al. (2010a), Yoshioka et al. (2010), Li et al. (2020). However, calibration methods come with the penalty of additional circuitry, increased power consumption, increased complexity and of course the silicon area.

The SBC array based SAR ADC proposed by Ginsburg and Chandrakasan (2007) is considered to be area efficient in comparison to conventional SAR ADCs. In the literature, an unconventional approach is also found where the researchers have realized the DAC of the SAR ADC by using a fixed number of unit capacitors irrespective of N (Kamalinejad et al. 2011, Seongik and Minwoong 2017, Shi et al. 2018). However, such an approach is adopted by very few researchers. These unconventional methods of realizing NBW capacitor based SAR ADCs have a great potential for achieving area efficiency, and accordingly in this thesis they are called as area efficient NBW ADCs.

-

2.1 AREA EFFICIENT NBW ADCs

A novel DAC architecture was proposed for SAR ADC by Kamalinejad et al. 2011. It uses only four unit capacitors irrespective of N. The architecture is quite interesting, the schematic of which is shown in Figure 2.2. The conventional binary search SAR algorithm is modified suitably for extracting the digital code equivalent to the analog input. This is explained with the help of the diagram shown in Figure 2.3 for the case of N=3.

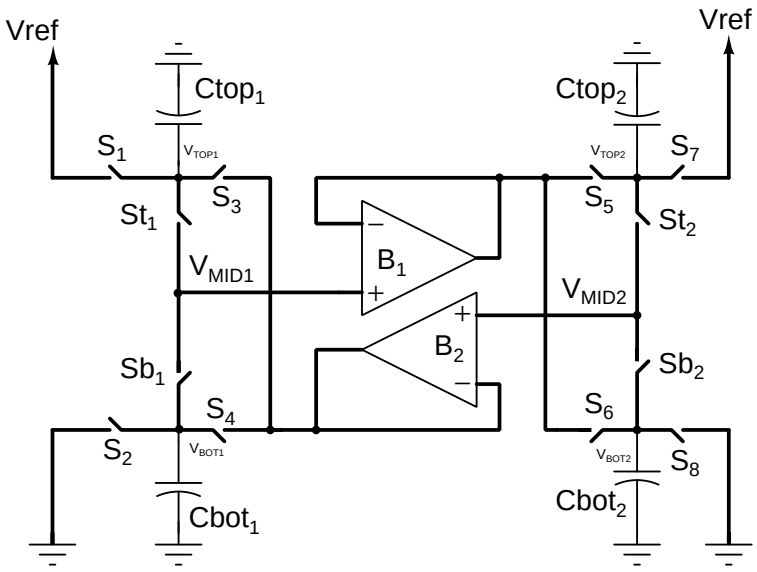

Figure 2.2: New DAC architecture as in Kamalinejad et al. (2011)

- In each clock cycle, for deciding the bit, two voltage levels V_{BOT} and V_{TOP} are defined as the lower and upper voltage bounds for that cycle.

- A mid voltage level V_{MID} is then produced from V_{BOT} and V_{TOP} by taking the average of the two as in (2.2)

$$V_{MID} = \frac{V_{TOP} + V_{BOT}}{2} \tag{2.2}$$

- For the m^{th} bit, V_{MID} generated in the corresponding cycle is compared with V_{IN} and the comparison result is the bit D_m.

- The bit D_m is then used to update the value of V_{BOT} and V_{TOP} for the next clock cycle. If $D_m = 1$, V_{TOP} maintains its old value while V_{BOT} is shifted up to V_{MID}. This is called the up transition (as shown in Figure 2.3). Conversely, if $D_m = 0$, V_{BOT} maintains its old value while V_{TOP} is shifted down to V_{MID} and is called the down transition.

- This procedure continues till all the bits are decided.

- During the conversion process V_{MID} converges towards V_{IN}.

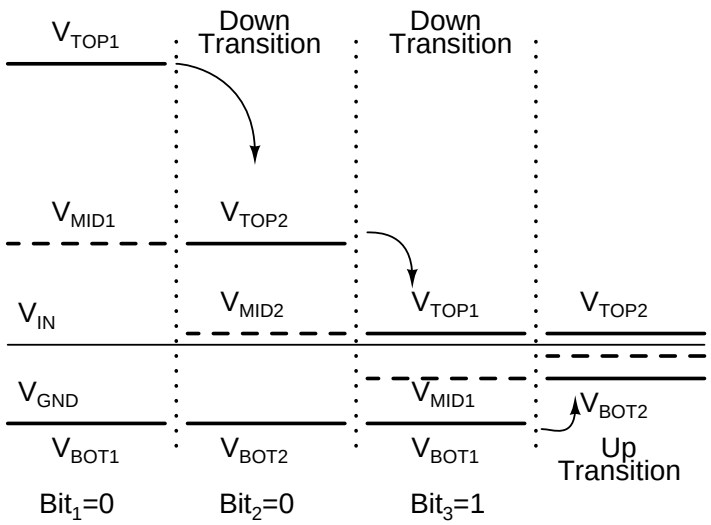

Figure 2.3: Scheme for bit decision as in Kamalinejad et al. (2011)

This 8 bit SAR ADC was designed and simulated in a 130 nm CMOS process. It was designed for a sampling frequency of 25 kHz. The schematic simulation results have shown that at Nyquist rate the achieved ENOB is 7.8. The power consumption is reported to be 350 nW achieving a FOM of 62 fJ/conversion-step. The design was operating on two power supplies, a 0.8 V analog supply and a 0.6 V digital supply.

One of the main limitations of this architecture is the requirement of two voltage buffers for recycling the voltages from one clock cycle to the next during the conversion cycle, which was not the case in conventional SAR ADCs. The buffers are power hungry units and therefore they hit hard on FOM. Interestingly, no further research has been found on this type of architecture in the literature. AE of the proposed ADC is also not ascertained since the proposal is limited to schematic design. Therefore, further exploration on this architecture to prove its candidature for area efficient ADCs is found to be a good contribution to the ADC research community. Further, the buffer settling is one of the key factors limiting the speed of the ADC. Research towards improving the speed of such ADCs can also be worthwhile. In BWC ADCs, speed enhancement is commonly achieved using one of the following techniques.

- **Extraction of multiple bits per cycle:** In this approach, the SAR ADC resolves more than 1 bit per cycle. However, compared to 1 bit/step SAR ADC,

typically threefold elements are used. Therefore, power efficiency is typically poor. A block diagram of the conventional 2 bit/step SAR ADC is shown in Figure 2.4. While the 1 bit/step generates only one reference voltage in one cycle, the 2 bit/step SAR uses three or more DACs to generate three reference voltages needed for 2 bit conversion per cycle. Three comparators compare the input with three analog estimates, providing 2 bit of information. But how the analog estimates created for consecutive cycles is of concern as each time they must be generated by the DAC.

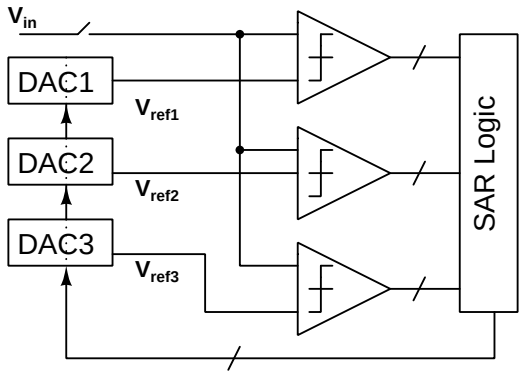

Figure 2.4: Conventional 2 bit per step SAR ADC block diagram

- **Time interleaving:** The single channel SAR ADC is not very fast because of successive bit decisions. Time interleaving is a popular method to speed up the converter among high speed ADC designs. The operating principle of time interleaving of an M channel ADC is shown in Figure 2.5. The original sampling frequency f_s can be boosted to Mf_s by the sampling delay time T between adjacent channels.

- **Pipelining:** When single capacitor array is used to resolve all N bits of ADC, capacitor array becomes large and settling time tends to be long. Conversion time can be halved if the resolution is halved into upper $N/2$ bit and lower $N/2$ bit, upper bit decision and lower bit decisions are pipelined. The Figure 2.6, shows the pipelined SAR architecture (Lee and Flynn 2010). Amplifier between the stages amplifies the residue. The required OPAMP gain is not so large as the first stage already resolves the MSB bits, amplifier gain is at LSB bits level.

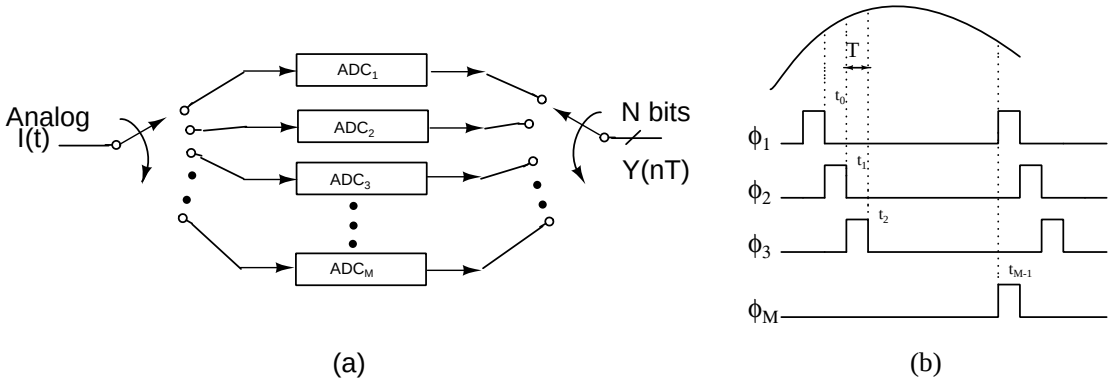

Figure 2.5: Time interleaved ADC (a) Structure (b) Signal sampling

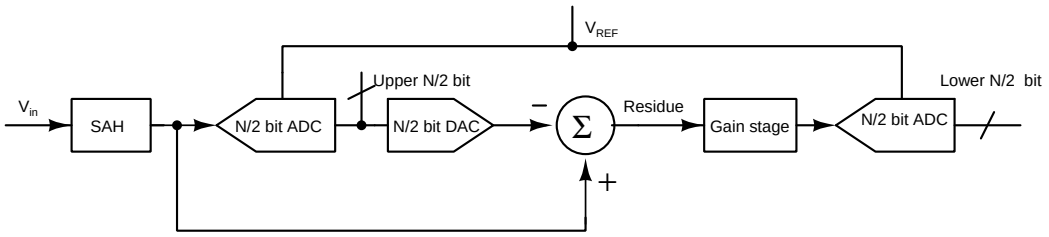

Figure 2.6: Pipelined SAR architecture

2.1.1 Two bit per cycle SAR ADCs - literature review

A design using single resistive DAC to generate multiple reference voltages has been reported (Wei et al. 2011). This paper presents an 8 bit, 400 MS/s ADC with resistive DAC based 2 bit per cycle SAR structure, which used several effective solutions at the circuit and layout level, like the interpolated sampling circuits, cross-coupled bootstrapping network and offset calibration is used to improve the accuracy. Comparing with capacitive SAR ADC, this ADC topology may lose effectiveness at high resolution level, but it extends the application range of SAR ADCs in speed. However this solution is not effective for low voltage operation because it requires more than

hundred CMOS switches whose resistance affects the overall performance. Furthermore, the DC current of the resistive DAC will dominate the power consumption at low speed losing the power scalability of the SAR ADC.

In this work (Yoshioka et al. 2012), a power and area efficient 2 bit/step method by adding threshold configurable comparator into an ordinary SAR ADC is presented. The prototype ADC achieved FoM of 19.2 fJ/conv-step with 30.7 MS/s at power supply voltage of 0.8 V. The 2 bit/step method SAR ADC is constructed only by adding V_{cm} biased current sources to dynamically configure the threshold voltage of comparator. The number of the sampling switch and the charge redistributing capacitor DAC is same as in 1 bit/step SAR ADC. However ADC occupies same area as traditional charge redistribution SAR ADC and hence area efficiency remains same as SAR ADC with similar resolution.

In this work (Hong et al. 2015), a compact 2 bit/cycle SAR ADC architecture is proposed with two different DACs, SIG-DAC and REF-DAC. Dedicated operations of sampling and residue generation utilizing the SIG-DAC eliminate the timing skew issue and reduce the input capacitance of the ADC. Since the REF-DAC operates independently of the input signal and residue, it is designed to be very compact with no control logic. A nonbinary decision scheme ensures robust performance of the ADC by correcting errors that could occur by insufficient DAC settling, varying comparator offset or kickback mismatch and reference fluctuation. In order for the capacitors in the SIG-DAC to perform nonbinary decision scheme capacitor values of $64\,C$, $32\,C$, $24\,C$, and so on are used. Therefore the total capacitance is $148\,C$, not $128\,C$, including $20\,C$ for redundancy. The REF-DAC also has additional $20\,C$ in order to match the full scale with the SIG-DAC. A prototype 7 b ADC fabricated in a 45 nm CMOS process operates at a sampling rate of 1 GS/s under a 1.25 V supply while achieving a peak SNDR of 41.6 dB and maintaining an ENOB higher than 6 up to 1.3 GHz signal frequency. The FOM under a 1.25 V supply is an 80 fJ/conversion-step with a power consumption of 7.2 mW.

A merged SAR/flash ADC that converts 6 b in three comparison cycles and one sampling/reset cycle is proposed in (Cao et al. 2009). Fabricated in a digital 0.13 μm CMOS process, each SAR ADC is clocked at 2.5 GHz, and 2 SAR ADCs are time-interleaved to sample at 1.25 GHz. Despite the structural simplicity, the 2 bit/cycle structure suffers from increased hardware overhead with three SAR ADCs.

The ADC presented in (Sugiyama et al. 2010) uses split capacitor and dual sampling technique to evaluate 2-bit per step. Due to split capacitor arrays and complex control logic, this architecture may demand for advanced process technology.

Comparison among these reported ADCs are listed in Table 2.1.

Table 2.1: Comparison with available low power, low voltage 2 bit per cycle SAR ADCs in the literature.

Reference	Song et al. (2017)	Wei et al. (2012)	Hong et al. (2013)	Hong et al. (2015)	Hotta et al. (2010b)
Technology (μm)	0.04	0.65	0.045	0.045	0.18
f_s	300 MS/s)	400 MS/s	0.9 GS/s	1 GS/s	6 MS/s
Resolution	10 b	8 b	9 b	7 b	10 b
P_{diss}	2.1 mW	4 mW	10.8 mW	7.3 mW	15 mW
FOM	19(fJ/cs)	73(fJ/cs)	40(fJ/cs)	80(fJ/cs)	13.6(pJ/cs)
Area (mm^2)	0.008	0.028	0.316	0.16	0.17
DAC structure	2 b/cycle Single DAC	2 b/cycle Resistive DAC	2xTI-2 b/cycle Nonbinary, TWC	SIG-DAC and REF-DAC(2 DAC)	2 b/cycle + redundancy

In this thesis, an attempt is made to achieve speed improvement by coming up with NBW architecture based on the DAC proposed in Kamalinejad et al. 2011 for 2 bit/step approach with as less a number of additional components as possible with an aim to keep AE to a low value.

Nonbinary search algorithm is used in some of the SAR ADCs in literature. The nonbinary weighted capacitive DAC based SAR ADCs should not be confused with one which uses nonbinary search algorithm used to enhance ENOB of ADCs. This algorithm helps to correct comparator decision error due to incomplete DAC settling. Commonly used correction methods include binary-scaled error compensation (Liu et al. 2010b, Shen et al. 2018), the nonbinary search algorithm (Kuttner 2002, Chang et al. 2013), and multiple LSB redundancy (Shen et al. 2018, Giannini et al. 2008). The binary-scaled error compensation scheme uses a greater number of binary

weighted capacitors in a typical binary weighted CDAC to obtain redundancy weights for error correction. In addition, the scheme requires an increase in the total DAC capacitance. The nonbinary search algorithm has a built-in correction mechanism to correct the erroneous decisions caused by incomplete DAC switching settling and comparator noise. Nonbinary CDACs have a higher number of redundancy weights than binary CDACs under the same search number. Therefore, nonbinary CDACs can correct a higher number of bit error decisions than binary CDACs. Furthermore, the nonbinary search architecture does not require an increase in the total DAC capacitance. The multiple LSB redundancy technique can correct bit error decisions that have occurred in the last few comparison cycles. However, for multiple LSB switching, the total DAC capacitance should be doubled.

2.1.2 SC integrator DAC based ADCs

SC integrator based architecture is found to be an another approach to realize the DAC of a SAR ADC. A few works are found in the literature.

The work in Seongik and Minwoong (2017), proposes a resolution independent SAR ADC using an SC integrator DAC. The operation of this ADC is similar to a charge redistribution based SAR ADC. But the DAC area is independent of resolution. Totally six unit capacitors are used in the DAC for a fully differential operation of a 9 bit NBW ADC designed in TSMC 180 nm CMOS high voltage technology with 5 V supply voltage. A fully differential OPAMP and a dynamic comparator are used in this ADC. The ADC has a rail to rail input full scale range. Four capacitors of value 2 pF and two integrating capacitors of 2.5 pF are used in the architecture. The ADC operates at a sampling rate of 100 kS/s. Even though the ADC architecture is resolution independent, there is enough scope to improve the sampling rate, power consumption as well and at the same time it can be made more compact for the given technology.

An 8 bit SC integrator based SAR ADC is presented in Polineni et al. (2020). The ADC designed in 90 nm CMOS process achieved a FOM of 11.39 fJ/conv-step. The design was area efficient with the design spreading over 0.00145 mm^2. For 8 bit resolution, the ADC offered a conversion speed of 0.78 MS/s. However, the ADC had a single ended architecture and required dual supply operation with a power supply

of ±350 mV. The single ended SC DAC required a total of six capacitors and had many switches. Due to the single ended architecture of the DAC and non-ideality of the switches, the SNDR is found to be degraded.

An active noise shaping SAR ADC presented in Shi et al. (2018) uses NBW capacitor architecture. It uses two equal valued capacitors as a digital to analog converter (DAC). The circuit provides first order noise shaping, which improves the ADC's linearity even for a small oversampling ratio (OSR). The proposed architecture uses a monotonic switching procedure allowing fewer conversion steps than for a conventional SAR ADCs. The ADC was fabricated in 180 nm CMOS technology. For a 2 kHz bandwidth, it achieved a 78.8 dB SNDR. It consumes 74.2 μW power from 1.5 V power supply. The two capacitors used are of value 4 pF, for better matching and small capacitance spread. The result is that the capacitor being the largest contributor for the area utilization, AE is found to be a bit poor with 480.08 μm^2/code.

The Noise shaping SAR ADC proposed in **?** uses a few unit capacitors but takes 50 percent extra time per conversion over conventional SAR ADCs.

Different nonbinary weighted capacitor array design approach (including SCI based ADCs) available in the literature with associated complexity is presented in Table 2.2.

Table 2.2: Comparison among nonbinary weighted SAR ADCs in the literature.

Reference	**DAC Approach**	**Remarks**
Choi and Tsui (2009)	MSB DAC and LSB DAC	Two extra clock cycles, more area
Cao et al. (2009)	TI, 3 SAR ADCs	Simple, more hardware
Saisundar et al. (2012)	Segmented CA and Nonbinary algorithm	Mismatch error
Hong et al. (2015)	Signal DAC and Ref. DAC, nonbinary algorithm	Power and area more
Seongik and Minwoong (2017)	SCI, Nonbinary	Power and area overhead
Shi et al. (2018)	SCI and noise shaping	Area overhead

Observing the simplicity of the architecture and the associated logic in the SC integrator based ADCs, an attempt has been made in this thesis to propose a 10 bit

SC integrator based SAR ADC with provision for programmability of resolution from 4 to 10 bits. The ADC is designed to have fully differential architecture for single supply operation on 1.8 V.

In the rest of the thesis, the outcome of the research has been discussed in detail.

Chapter 3

A CHARGE RECYCLE BASED 2 BIT PER STEP SAR ADC - PROTOTYPE

The SAR architecture presented in (Kamalinejad et al. 2011) is a compact architecture with only four unit sized capacitors in the DAC instead of a binary weighted capacitor array. The compactness coupled with the requirement of very few capacitors (nonbinary weighted) makes the architecture very attractive for applications where the form factor is of prime concern with relaxed power requirements especially for ADCs that work on a sufficiently large energy source. It is therefore felt that extending the architecture to realize 2 bit/step will be a value addition in terms of speed since implementing the algorithm would demand a careful modification of the architecture.

This chapter explains the SAR architecture modified to realize 2 bit/step. Two architectures have been proposed for nonbinary weighted SAR ADCs. First, as a proof of concept, an 8 bit SAR ADC is designed in 180 nm technology, with the proposed DAC architecture that uses minimum number of unit size capacitors and buffers.

3.1 TWO BIT PER CYCLE ADC: DAC ARCHITECTURE

The DAC in the Figure 2.2, generates the mid (average) voltage V_{MID} for the voltage segment decided by V_{TOP} and V_{BOT} in every clock cycle. Also, the V_{MID} generated in one cycle is recycled to generate V_{TOP} or V_{BOT} depending on the bit resolved. However, if the architecture is to be modified to resolve 2 bit/step it is required to generate two more voltage reference levels, say V_{TH1} and V_{TH2} (in addition to V_{MID}) in every clock cycle from V_{TOP} and V_{BOT} of that cycle. Also, provision must be made to recycle V_{MID} or V_{TH1} or V_{TH2} to V_{TOP} or V_{BOT} for the next cycle depending on the two bits resolved in the current clock cycle. The modifications are to be done in accordance with the algorithm to be followed for reference generation for resolving 2 bit/step. A pictorial representation of the algorithm is shown in Figure 3.1.

The three reference levels V_{MID}, V_{TH1} and V_{TH2} can be derived from V_{TOP} and V_{BOT} in every clock cycle using (3.1), (3.2) and (3.3).

$$V_{MID} = \frac{1}{2}(V_{TOP} + V_{BOT}) \tag{3.1}$$

$$V_{TH1} = \frac{3}{4}V_{TOP} + \frac{1}{4}V_{BOT} \tag{3.2}$$

$$V_{TH2} = \frac{1}{4}V_{TOP} + \frac{3}{4}V_{BOT} \tag{3.3}$$

A modified DAC architecture has been proposed and is shown in Figure 3.2. The buffers $B1$ and $B2$, capacitors C_{TOP1}, C_{TOP2}, C_{BOT1} and C_{BOT2}, and switches $S_{S1} - S_{S4}$ are identical to that of the basic DAC (Figure 2.2). The remaining circuitry is formed to generate V_{TH1} and V_{TH2}, and recycle them on to V_{TOP} and V_{BOT}.

The complete schematic of the ADC with the proposed DAC is shown in Figure 3.3. It has a dedicated S/H circuit, a 2 bit flash ADC for resolving 2 bits in every clock cycle, SAR logic and the proposed DAC.

The clocking scheme for the ADC is shown as a timing diagram in Figure 3.4. In the sampling phase the input is sampled on to the dedicated sampling capacitor using the S/H circuit using the clk_{sample} signal. Simultaneously, the reference voltages are also loaded on to the capacitors in the DAC.

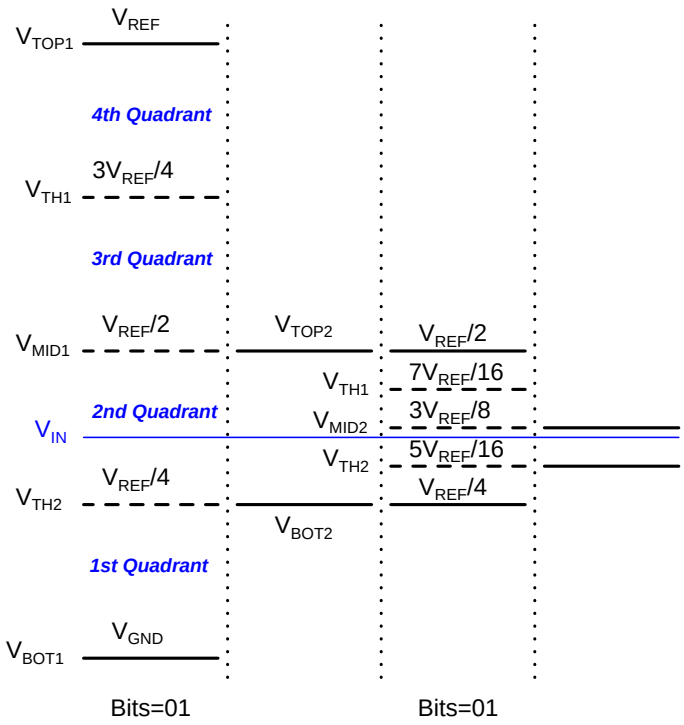

Figure 3.1: Pictorial representation of the algorithm followed in DAC for reference generation.

In the hold phase, the bits of the ADC are resolved. Every clock cycle of the hold phase is divided into two phases, comparison phase (CPh) and recycling phase (RPh). In the initial part of the CPh, the three threshold voltages V_{MID}, V_{TH1} and V_{TH2} are generated through charge sharing among the capacitors. In the other part of the CPh, two bits are resolved using the 2 bit flash. During RPh, V_{TOP} and V_{BOT} are generated for the next cycle by recycling the voltages using buffers and capacitors according to the bits generated in the current cycle.

Therefore, the main task of the proposed DAC is to generate three voltage reference levels V_{MID}, V_{TH1} and V_{TH2} for resolving the two bits. Generation of these reference levels is explained as follows.

3.1.1 V_{MID} Generation

In the proposed DAC, on either side of the buffers $B1$ and $B2$ there are two capacitors. On the left C_{TOP1} and C_{BOT1} and on the right C_{TOP2} and C_{BOT2}. These capacitors

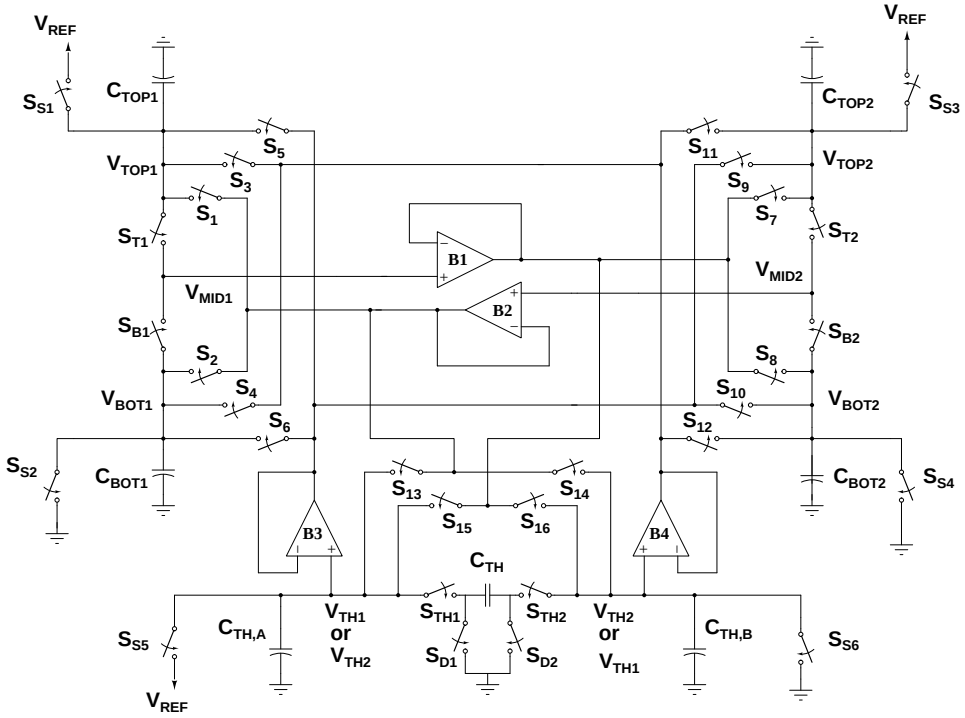

Figure 3.2: Proposed DAC architecture to evaluate 2 bit/cycle

along with the necessary switches are responsible for V_{MID} generation. The corresponding nodes on the left are V_{TOP1}, V_{BOT1} and V_{MID1}, and on the right are V_{TOP2}, V_{BOT2} and V_{MID2}.

Considering the left side of $B1$ and $B2$, V_{MID1} can be treated as the result of charge sharing due to V_{TOP1} and V_{BOT1} when the switches S_{T1} and S_{B1} are closed. Since the capacitors are equal one can write

$$V_{MID1} = \frac{1}{2}(V_{TOP1} + V_{BOT1}) \tag{3.4}$$

Similarly, for the right side one can write

$$V_{MID2} = \frac{1}{2}(V_{TOP2} + V_{BOT2}) \tag{3.5}$$

Therefore, V_{MID} can be taken either from V_{MID1} or V_{MID2}. If V_{TOP1} and V_{BOT1} are set to V_{TOP} and V_{BOT}, then $V_{MID} = V_{MID1}$. On the other hand if V_{TOP2} and

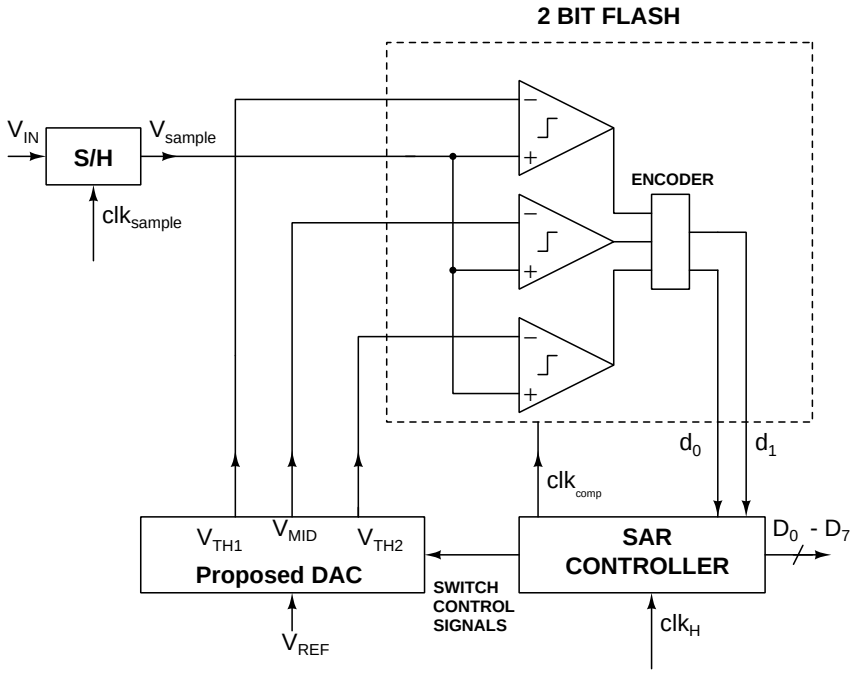

Figure 3.3: Complete ADC architecture - prototype

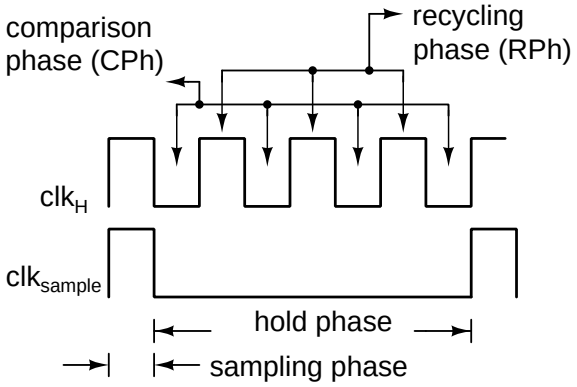

Figure 3.4: Timing diagram showing sampling phase, comparison cycle and recycling phase

V_{BOT2} are set to V_{TOP} and V_{BOT}, then $V_{MID} = V_{MID2}$. This dual facility is utilized effectively as follows. In the recycle phase of every cycle, the capacitors of either side are charged identically. However, while generating V_{MID}, left and right sides are used alternatively for charge sharing while the other side simply holds the voltages

for recycling for the next cycle.

3.1.2 V_{TH1} and V_{TH2} Generation

The voltage reference levels V_{TH1} and V_{TH2} are generated by the circuit on the bottom part of the proposed DAC shown in Figure 3.2. The circuit consisting of capacitors $C_{TH,A}$, $C_{TH,B}$ and C_{TH} and the associated switches is responsible for generating V_{TH1} and V_{TH2}. The principle can be explained as follows with the help of the simplified schematic shown in Figure 3.5.

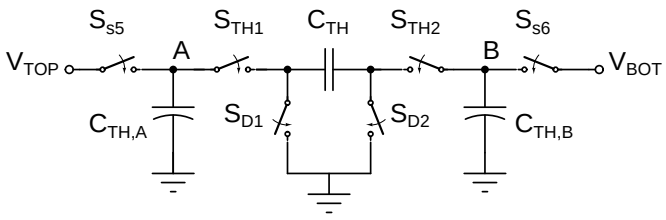

Figure 3.5: Simplified schematic of the circuit generating V_{TH1} and V_{TH2}

In one phase of the clock, the capacitors $C_{TH,A}$ and $C_{TH,B}$ are sampled with voltages V_{TOP} and V_{BOT} respectively by closing the switches S_{S5} and S_{S6}, and with the switches S_{TH1} and S_{TH2} being kept open. Capacitor C_{TH} is discharged to zero by closing S_{D1} and S_{D2}. In the second phase, S_{TH1} and S_{TH2} are closed after opening the remaining switches that were previously closed, but with a small delay.

It can be noted that the charge on nodes A and B are conserved before and after closing S_{TH1} and S_{TH2}. Equating the charge on node A before and after closing S_{TH1} and S_{TH2}, and with $C_{TH,A} = C_{TH,B} = 2C_{TH} = C$, the charge equality equation can be written as in (3.6), i.e.,

$$CV_{TOP} = CV_A + \frac{C}{2}(V_A - V_B) \tag{3.6}$$

Similarly for node B, the charge equality can be written as in (3.7).

$$CV_{BOT} = CV_B + \frac{C}{2}(V_B - V_A) \tag{3.7}$$

Solving (3.6) and (3.7) for V_A and V_B,

$$V_A = \frac{3}{4}V_{TOP} + \frac{1}{4}V_{BOT} \tag{3.8}$$

$$V_B = \frac{1}{4}V_{TOP} + \frac{3}{4}V_{BOT} \tag{3.9}$$

It can be clearly seen that (3.8) and (3.9) are identical to (3.2) and (3.3) respectively. Therefore, voltage at node A and B are the desired reference levels V_{TH1} and V_{TH2}. Another point to note here is that, if V_{TOP} and V_{BOT} are swapped, then it simply follows that V_{TH1} is available at node B and V_{TH2} at node A due to the symmetry of the circuit. This symmetry has been effectively utilized as it is necessary, many a times, for saving on clock cycles. One such case is explained as follows.

Conventionally $V_{TOP} > V_{BOT}$ and therefore, $V_{TH1} > V_{TH2}$. Consider the case when V_{TH2} (node B) and V_{BOT} obtained in one cycle have to be recycled as V_{TOP} and V_{BOT} respectively (for generating new reference levels). This would require, node A to be charged to node B potential and node B to be charged to V_{BOT} (V_{BOT} is available in one of the V_{MID} generation circuits). This calls for an additional clock cycle. This can be avoided by exploiting the symmetry of the circuit effectively, simply by retaining V_{TH2} on node B and recycling V_{BOT} on to node A. Therefore, for the next comparison, the corresponding V_{TH1} will be available on node B and V_{TH2} on node A. These voltages can be taken for comparison by suitably switching node A and B.

3.1.3 Working of the proposed ADC

In the proposed DAC, the relative values of the capacitors are taken as $C_{TOP1} = C_{TOP2} = C_{BOT1} = C_{BOT2} = C_{TH,A} = C_{TH,B} = C$ and $C_{TH} = C/2$. Out of these seven unit sized capacitors, four capacitors (C_{TOP1}, C_{TOP2}, C_{BOT1} and C_{BOT2}) are used to generate one reference voltage (V_{MID}) and the remaining three capacitors are used to generate the other two reference voltages (V_{TH1} and V_{TH2}), as already mentioned in sections 3.1.1 and 3.1.2. In this section, the working of the ADC is explained in detail with respect to Figure 3.3 and Figure 3.2.

In the sampling phase, while the input voltage is being sampled on the sampling capacitor of the ADC, switches S_{S1}-S_{S6}, S_{D1} and S_{D2} of the DAC are closed. Capac-

itors C_{TOP1}, C_{TOP2} and $C_{TH,A}$ will get charged to V_{REF} while the capacitors C_{BOT1}, C_{BOT2} and $C_{TH,B}$ are discharged to ground. At this time all other switches remain open.

3.1.3.1 The first CPh in the hold phase

In the first CPh, in the hold phase, switches S_{S1}-S_{S6}, S_{D1} and S_{D2} are open and switches S_{T1}, S_{B1}, S_{TH1} and S_{TH2} are closed.

Capacitors C_{TOP1} and C_{BOT1} share their charges among each other resulting in a voltage V_{MID1} on both of them. Note that the voltages V_{TOP1} (across C_{TOP1}) and V_{TOP2} (across C_{TOP2}) act as V_{TOP} and V_{BOT} for this cycle. Since V_{TOP} and V_{BOT} are charged to V_{REF} and zero respectively the resulting V_{MID} will be as given in (3.10).

$$V_{MID1} = \frac{1}{2}(V_{TOP1} + V_{BOT1}) = \frac{V_{REF}}{2} \tag{3.10}$$

Capacitors C_{TOP2} and C_{BOT2} retain their voltage levels acquired during the sampling phase i.e, $V_{TOP2} = V_{REF}$ and $V_{BOT2} = 0$.

Capacitors $C_{TH,A}$, $C_{TH,B}$ and C_{TH} together will generate the voltages V_{TH1} and V_{TH2} by sharing their charge as explained in section 3.1.2. The result is that node A will be charged to $\frac{3}{4}V_{REF}$ and node B will be charged to $\frac{1}{4}V_{REF}$ as per (3.8) and (3.9). Therefore, node A will act as V_{TH1} and node B as V_{TH2}.

Three reference voltages V_{MID1}, V_{TH1} and V_{TH2} generated at the end of CPh are fed to a 2 bit flash, where these voltages are compared with the input voltage V_{IN} simultaneously to resolve the most significant two bits D_7 and D_6 of the ADC. The voltages are switched to the 2 bit flash using appropriate switching scheme, the schematic of which is shown in Figure 3.6

For the example shown in Figure 3.1, V_{IN} lies in the second quadrant, in between $V_{REF}/2$ and $V_{REF}/4$, and therefore the corresponding two bits generated would be 01.

For resolving the next two significant bits, $V_{REF}/2$ (V_{MID1} of the present cycle) should be set as V_{TOP} and $V_{REF}/4$ (V_{TH2} of the present cycle) should be set as V_{BOT}. Or in other words, for the case under consideration, V_{MID1} and V_{TH2} should be recycled as V_{TOP} and V_{BOT} respectively. This is done during the first RPh.

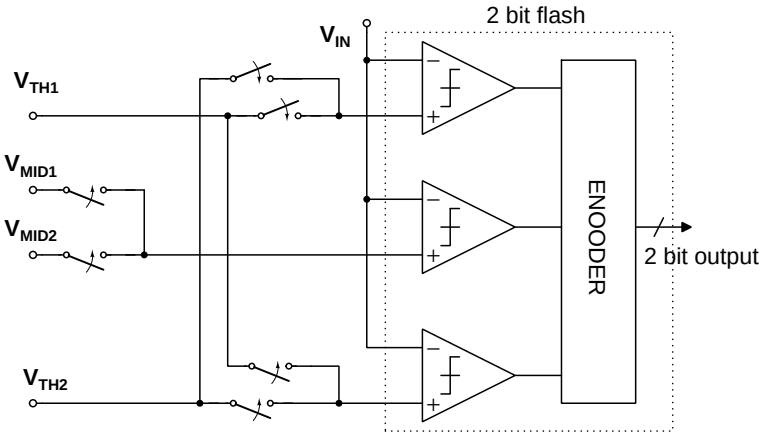

Figure 3.6: Switch configuration at input of comparators

3.1.3.2 First RPh

It can be observed that, C_{TOP1} already has the V_{TOP} required for the cycle. Also, $C_{TH,B}$ has the necessary V_{BOT}. Therefore, the recycling requires C_{TOP2} and $C_{TH,A}$ to charge to V_{MID1}, C_{BOT1} and C_{BOT2} to be charged to V_{TH2}. The SAR logic generates controls to the switches for recycling based on the two bits generated at the end of CPh. Switches S_{T1}, S_4, S_7, S_{12} and S_{15} are closed to allow recycling through buffers $B1$ and $B4$. Switches S_{D1} and S_{D2} are also closed for discharging C_{TH} to ground and make it ready for the next CPh. All other switches are open.

Therefore, for the example taken, at the end of first RPh, $V_{TOP1} = V_{TOP2} = V_A = V_{REF}/2$ and $V_{BOT1} = V_{BOT2} = V_B = V_{REF}/4$.

3.1.3.3 Second CPh

The next two significant bits are generated in the second CPh. In this phase the right part C_{TOP2}, C_{BOT2} and associated switches generate V_{MID} (through V_{MID2}). Switches S_{T2}, S_{B2}, S_{TH1} and S_{TH2} are closed so that the capacitors C_{TOP2} and C_{BOT2} will produce the voltage $V_{MID2} = (V_{TOP2} + V_{BOT2})/2 = 3V_{REF}/8$, through charge sharing.

The capacitors $C_{TH,A}$, $C_{TH,B}$ and C_{TH} together produce $7V_{REF}/16$ and $5V_{REF}/16$ as reference voltages at the nodes A and B respectively. Nodes V_{TOP1} and V_{BOT1} will simply be holding previous voltage levels $V_{REF}/2$ and $V_{REF}/4$ respectively.

The three voltage levels V_{MID}, V_{TH1} and V_{TH2} required for the 2 bit flash are now taken from V_{MID2}, V_A and V_B respectively through appropriate switches to produce the next significant two bits. For the example taken, V_{IN} is in between $3V_{REF}/8$ and $5V_{REF}/16$ and therefore, the bits generated will be 01.

3.1.3.4 Second RPh

In the next recycling period, switches S_{T2}, S_1, S_{13}, S_{12} and S_4 are closed. The nodes V_{TOP1} and node A are recycled to $3V_{REF}/8$ and the nodes V_{BOT1} and V_{BOT2} will be recycled to $5V_{REF}/16$ through buffers B_2 and B_4.

The process of recycle and comparison is continued in a similar fashion by carefully switching through the digital logic circuit (SAR). In this algorithm only two buffers out of four are turned on to charge the capacitors in a charge recycling phase.

3.1.4 Power consumption analysis

Power consumption of the reference voltage supply due to capacitor switching for an N bit DAC can be calculated as (Kamalinejad et al. 2011),

$$P_{Vref} = \frac{V_{ref}}{T_s} \cdot \sum Q_i, i = 1...N \tag{3.11}$$

where T_s is time period during which a sample is converted and Q_i is the total charge that V_{ref} supplies to the capacitive array DAC during ith clock cycle during the conversion phase.

For DAC architecture (Kamalinejad et al. 2011), during a conversion cycle, each of the two buffers contribute in the charge recycling process for at most N times. So Q_{tot} during the conversion cycle is:

$$Q_{tot} = 4 \cdot N \cdot I_b \cdot T_{CR} \tag{3.12}$$

Where N is the number of bits, Ib is the bias current for each buffer stage, T_{CR} is the charge recycling period and the factor '4' accounts for the two, two-stage amplifiers. The two factors governing I_b are the required voltage gain and speed. The voltage gain of the buffer is decided based on the settling accuracy for desired resolution.

For the proposed architecture, number of clock cycles reduced to $N/2$ (for 2 bit per cycle mode) to evaluate N bits, we can reduce Q_{tot} by half of the original and power consumption from V_{ref} can be written as, .

$$P_{Vref} = \frac{V_{ref}}{T_s} \cdot \sum Q_i, i = 1...N/2 \tag{3.13}$$

Where

$$Q_{tot} = 4 \cdot N/2 \cdot I_b \cdot T_{CR} \tag{3.14}$$

3.2 BUILDING BLOCKS OF SAR ADC

3.2.1 Sample and hold

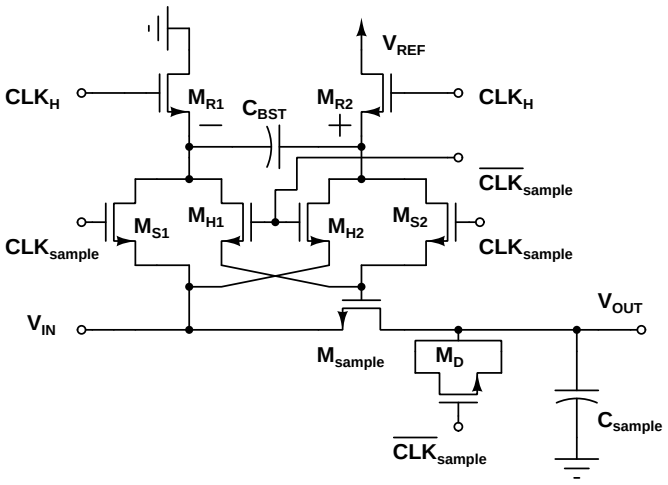

Figure 3.7: Sample and hold circuit

A switched capacitor clock boosted architecture is used for the S/H circuit due to its rail to rail capability. Schematic of S/H circuit is as shown in Figure 3.7 (Kamalinejad et al. 2011). After a few clock periods, C_{BST} is charged to V_{DD} and subsequently acts as a floating voltage source. At each sampling phase (clk_{sample}), C_{BST} connects the gate source terminals of M_{sample} in such a way that $V_{GS} = V_{DD}$.

Therefore in the sampling phase, the gate source voltage of M_{sample} will be held at V_{DD} higher than its source voltage regardless of the value of V_{IN} making the switch resistance input independent. On the other hand, in the hold phase, M_{H1} and M_{H2} turn on and M_{S1} and M_{S2} turn off, providing a negative voltage between the gate-source terminals of M_{sample}. This results in V_{GS} = -V_{DD} during the hold phase to avoid leakage problem. M_D is employed to cancel the charge injection effect. The voltage on C_{BST} may degrade due to leakage, so a high frequency clock clk_H (same as applied in DAC) is applied through transistors M_{R1} and M_{R2} to refresh it to V_{DD}.

3.2.2 Buffer

The buffer schematic is shown in Figure 3.8 (Nosratinia et al. 1991). The ADC is designed as a proof of concept, the specification on the speed of the ADC is relaxed. The buffer is designed to have a DC gain of about 80 dB so as to limit the buffer error and its accumulation to less than 25% of LSB without much emphasis on the unity gain bandwidth requirement. The circuit consists of two complementary differential stage with transistors M_1-M_5 and M_{10}-M_{14} connected in parallel. Each differential stage drives one half of the output common source push pull stage.

The transistors M_6-M_9 generate bias. In the proposed DAC architecture, only two buffers are turned on in the recycling phase. Switches S_1, S_2, S_3 and S_4 are provided in buffer Figure 3.8 to turn ON/OFF the required buffer.

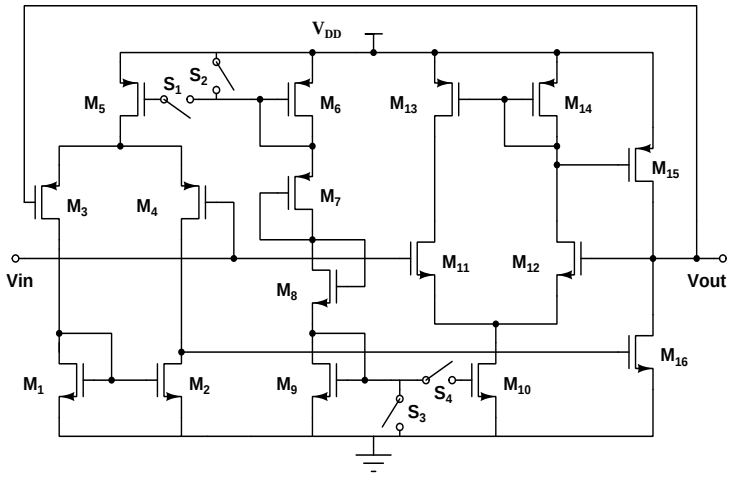

Figure 3.8: Schematic of buffer

3.2.3 Comparator

A dynamic latch based comparator (Kobayashi et al. 1993) has been used for the 2 bit flash. Schematic of the comparator is shown in Figure 3.9. The dynamic latch consists of pre-charge transistors M_9 and M_{10}, cross-coupled inverter M_{11}-M_{14}, differential pair M_7, M_8 and switch M_6 which prevent the static current flow when the signal clk_{comp} is low. When the clk_{comp} signal is low, the drain voltages of M_7 and M_8 are V_{DD}-V_T and their source voltage is V_T below the latch input common mode voltage. Therefore, once the clk_{comp} signal goes high, the NMOS transistors M_7, M_8, M_{13} and M_{14} immediately go into the active region.

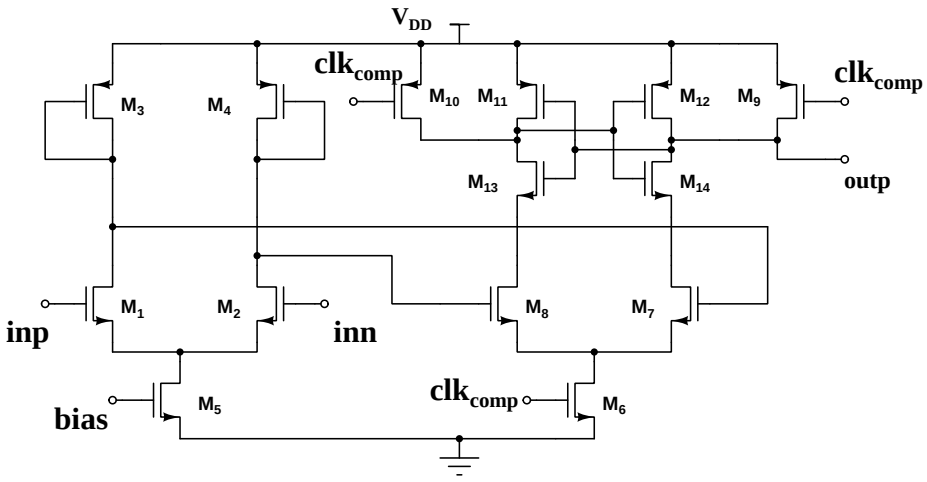

Figure 3.9: Schematic of comparator

Because one of the transistors from each cross coupled inverters is OFF in steady state, ideally there is no static power dissipation. The bias voltage generated for the buffer is also used to bias the comparator as well. Note that no offset cancellation scheme has been used. Three comparators followed by one-hot code generator and encoder are used to generate two bits from the sampled signal.

3.2.4 Control logic

The SAR controller block in Figure 3.3 performs two operations. It generates all control logic signals required to turn the switches of proposed DAC ON/OFF and also registers the two bits from the flash, generated at the end of every cycle, for generating the ADC code. In this section, the logic for generating the control signal for the DAC is explained.

One conversion cycle requires four cycles of clk_H and in each cycle two bits are resolved. As already mentioned, the V_{MID} generation is done by alternately utilizing the circuits on the left and right to the buffers $B1$ and $B2$ shown in Figure 3.2. Let us denote the two parts as $L-part$ and $R-part$. In the first clock cycle of clk_H, $L-part$ is in action and the next cycle the $R-part$ is in action. Or in other words, for odd numbered clock cycles of clk_H, $L-part$ is in action and during even numbered clock cycles, $R-part$ is in action.

The logic block for controlling the DAC switches has three inputs clk_H, the main clock and two bits $d_1 - d_0$ from the 2 bit flash. All the control signals required for the DAC are generated based on these three inputs. Few more clock signals (clk_{smpl}, clk_R, clk_C, clk_{RL}, clk_{RR}, clk_{CL}, clk_{CR}) are also required and are derived from clk_H. These clock signals are shown in Figure 3.10. The details of these clock signals are given in Table 3.1

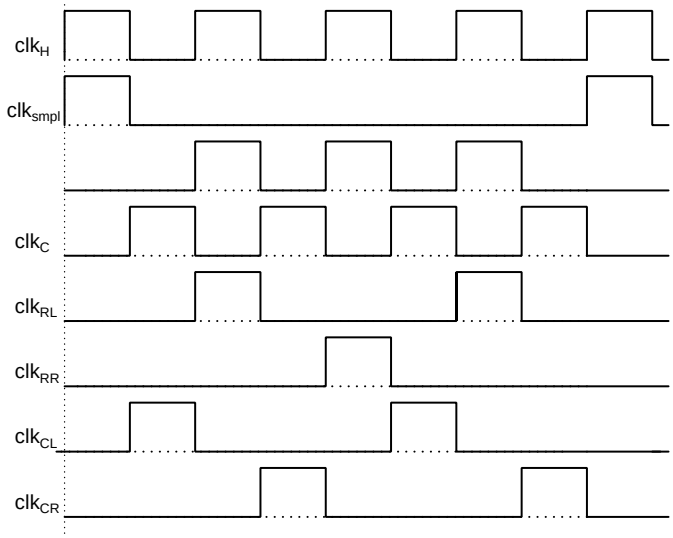

Figure 3.10: Various clock signals for the control block

Table 3.1: Various clock signals and their role

Clock	Role
clk_H	Main clock
clk_{sampl}	Sampling clock
clk_R	For charge recycling (i.e. RPh)
clk_C	For comparing V_{IN} with reference levels (i.e. CPh)
clk_{RL}	For recycling from $L-part$ to desired capacitors during RPh of second and fourth clock cycle (for setting V_{TOP} and V_{BOT} for the next cycle)
clk_{CL}	Comparing V_{MID} from $L-part$ i.e. connecting V_{MID1} to 2 bit flash for comparing (during CPh)
clk_{RR}	For recycling from $R-part$ to desired capacitors during RPh of the third clock cycle (for setting V_{TOP} and V_{BOT} for the next cycle)
clk_{CR}	Comparing V_{MID} from $R-part$ i.e. connecting V_{MID2} to 2 bit flash for comparing (during CPh)

The scheme for switching the reference levels to the comparators of the 2 bit flash is shown in Figure 3.11. clk_{CL} and clk_{CR} switches V_{MID1} and V_{MID2} appropriately to provide V_{MID} to comparator-2 ($comp_2$). S_A switches node voltages V_A/V_B to provide V_{TH1} and V_{TH2} to comparators $comp_1$ and $comp_3$ respectively.

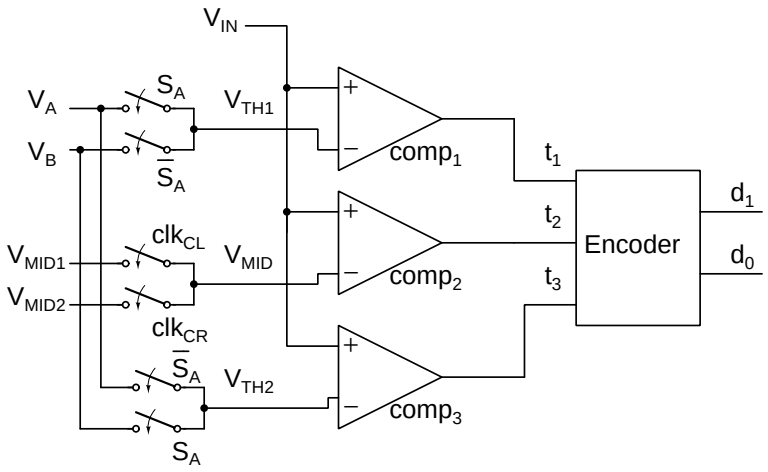

Figure 3.11: Comparators with control switches at the input for 3 bit generation

During the initialization phase (sampling phase), signal 'S_A' is initialized to logic '1' as in the first cycle it is guaranteed that $V_A > V_B$, after charge sharing, during first CPh. Therefore, $V_{TH1} = V_A$ and $V_{TH2} = V_B$. In subsequent cycles S_A takes logic values according to the bits generated.

Outputs t_1, t_2 and t_3 of the comparators at each CPh are encoded to bits d_0 (LSB bit) and d_1 (MSB bit). Based on this pair of bits, charge recycling is done by switching ON the appropriate switches.

The switches are turned ON in groups during the RPh depending upon the following cases.

- Quadrant in which the input lies during the current cycle i.e., the bits d_1-d_0 resolved in the current cycle.
- The direction in which the charge recycle has to take place from the V_{MID} generation circuit i.e., whether to recycle from $L-part$ or $R-part$.
- Whether node A takes the value of V_{TH1} or node B. Or in other words, which of the two capacitors $C_{TH,A}$ and $C_{TH,B}$ have to retain the charge.

As per the algorithm, it is found that there are a total of 8 possible combinations of switches for turning ON during RPh. The groups of switches to be turned ON along with the condition on when they are to be turned ON is given in Table 3.2.

Table 3.2: Switches to be turned ON during RPh

V_{MID} charge recycling	$V_A > V_B$ (logic 1, if TRUE)	$(d_1 d_0)$	Switches ON	Group Name
From $L-part$	1	00	$S_{B2}\ S_2\ S_{13}\ S_3\ S_{11}$	G_1
		01	$S_{T1}\ S_7\ S_{15}\ S_4\ S_{12}$	G_2
		10	$S_{B1}\ S_8\ S_{16}\ S_5\ S_9$	G_3
		11	$S_{T2}\ S_1\ S_{14}\ S_6\ S_{10}$	G_4
	0	00	$S_{B2}\ S_2\ S_{14}\ S_5\ S_9$	G_5
		01	$S_{T1}\ S_7\ S_{16}\ S_6\ S_{10}$	G_6
		10	$S_{B1}\ S_8\ S_{15}\ S_3\ S_{11}$	G_7
		11	$S_{T2}\ S_1\ S_{13}\ S_4\ S_{12}$	G_8
From $R-part$	1	00	$S_{B1}\ S_8\ S_{15}\ S_3\ S_{11}$	G_7
		01	$S_{T2}\ S_1\ S_{13}\ S_4\ S_{12}$	G_8
		10	$S_{B2}\ S_2\ S_{14}\ S_5\ S_9$	G_5
		11	$S_{T1}\ S_7\ S_{16}\ S_6\ S_{10}$	G_6
	0	00	$S_{B1}\ S_8\ S_{16}\ S_5\ S_9$	G_3
		01	$S_{T2}\ S_1\ S_{14}\ S_6\ S_{10}$	G_4
		10	$S_{B2}\ S_2\ S_{13}\ S_3\ S_{11}$	G_1
		11	$S_{T1}\ S_7\ S_{15}\ S_4\ S_{12}$	G_2

The control algorithm in the form of flow chart is as shown in Figure 3.12.

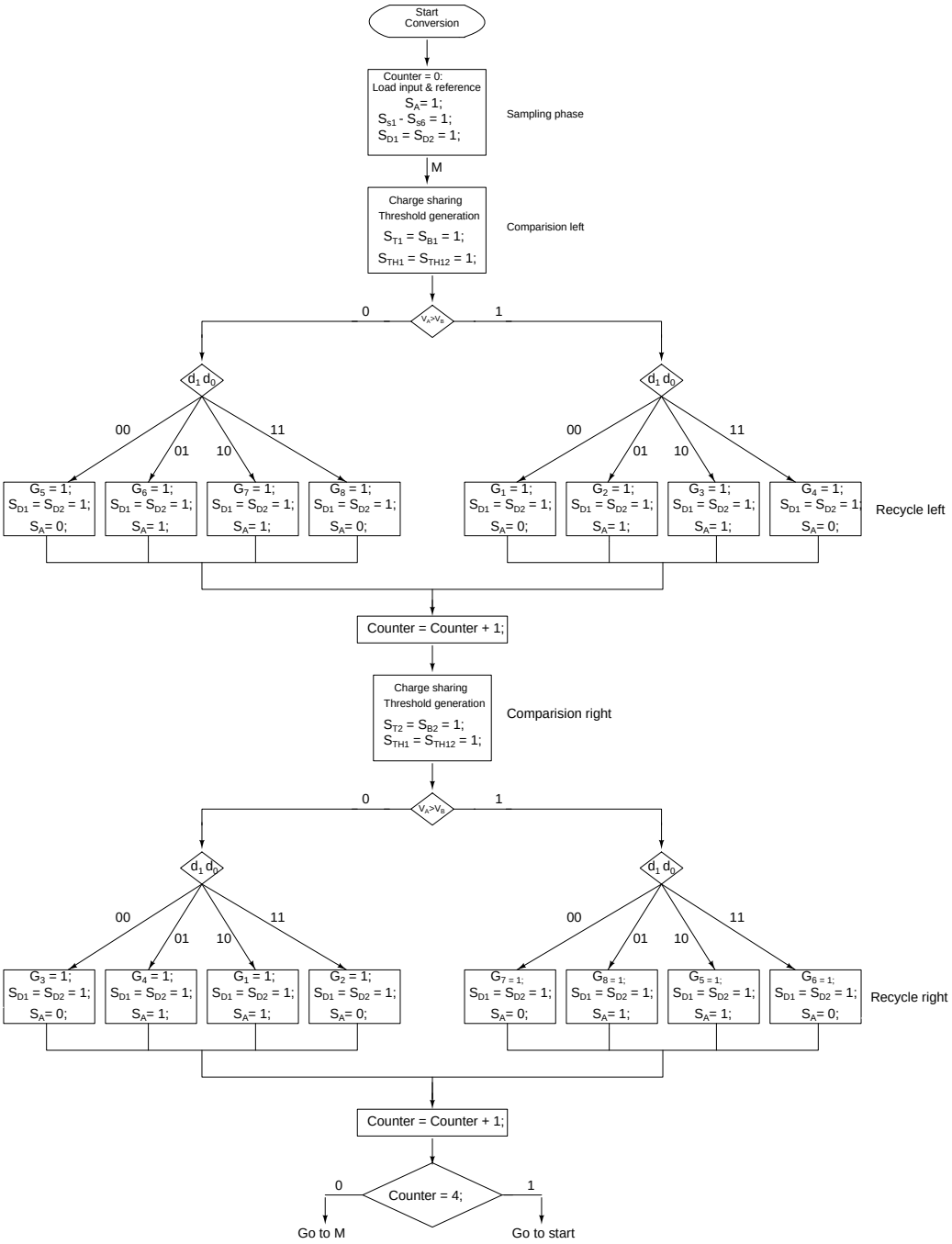

Figure 3.12: Control algorithm

The following steps explain the flow chart in detail.

- S_{s1}-$S_{s6} = clk_{smpl}$, to charge all the capacitors to their respective reference voltages, namely V_{REF} or ground.

- $S_{D1} = S_{D2}$ must be ON during each sampling phase as well as each RPh. Hence $S_{D1} = S_{D2} = clk_H$.

- Switches $S_{TH1} = S_{TH2}$ must turn ON during every CPh. Therefore they are driven by clk_C i.e., $S_{TH1} = S_{TH1} = clk_C$.

- During CPh, switches S_{T1} and S_{B1} are turned ON if V_{MID1} from $L - part$ has to be connected to the 2 bit flash. Therefore, control for these switches during CPh has been derived directly from clk_{CL}. If, V_{MID2} from $R - part$ has to be connected to the flash, S_{T2} and S_{B2} are turned ON by deriving their control directly from clk_{CR}.

Initially, VHDL code is written for the controller and simulated using Xilinx ISE simulator in order to verify the control algorithm. Later, the control logic block is developed using custom designed cells such as NOT, NAND, NOR, XOR, XNOR gates, flip flops and an encoder using 180 nm technology MOS devices. The CMOS complementary logic style is used to design gates for low power consumption. One negative edge-triggered D-flip flop with synchronous reset and set is used to store the signal 'S_A' and updated during every recycling clock.

3.3 SIMULATION RESULTS

The proposed SAR ADC is designed in 180 nm technology. The value of the capacitor C used in the DAC is 2 pF. The sampling capacitor is 800 fF.

The ADC is designed to operate on a 3.3 V supply with a full scale range of 2 V. The ADC is found to achieve a conversion speed of 500 kS/s. The simulated DNL and INL of the ADC at 500 kS/s is shown in Figure 3.13 and Figure 3.14 respectively and are found to be within ±0.5 LSB.

The spectra for an input full scale sine wave at 56.64 kHz and 232.42 kHz are as shown in Figure 3.15 and Figure 3.16 respectively. The corresponding SNDR is found to be 48.14 dB (ENOB = 7.7) and 47.03 dB (ENOB = 7.52) respectively.

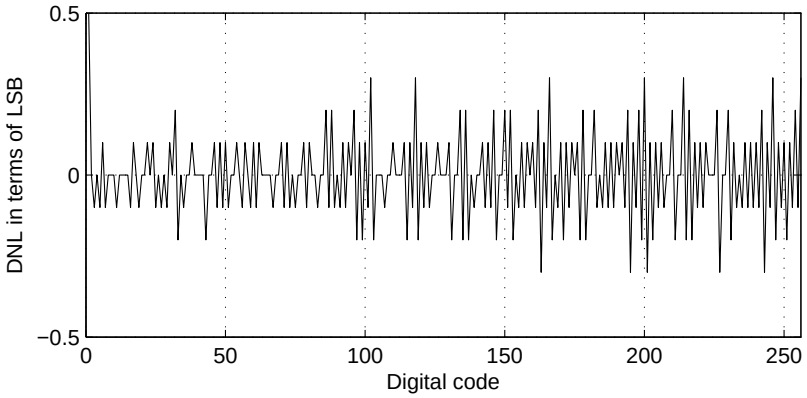

Figure 3.13: DNL plot of the ADC

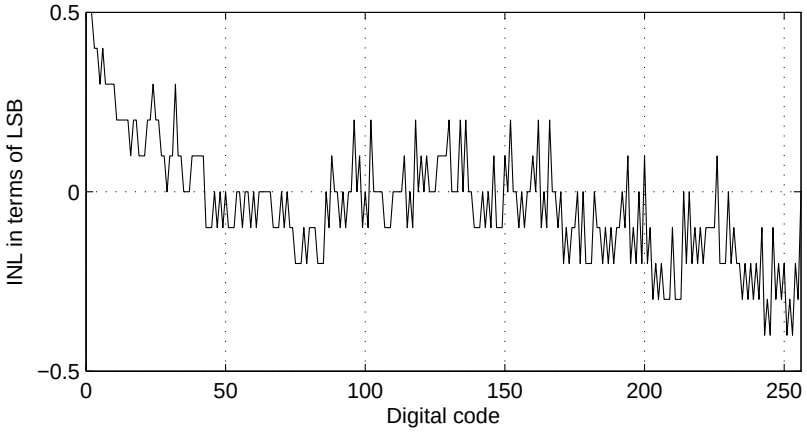

Figure 3.14: INL plot of the ADC

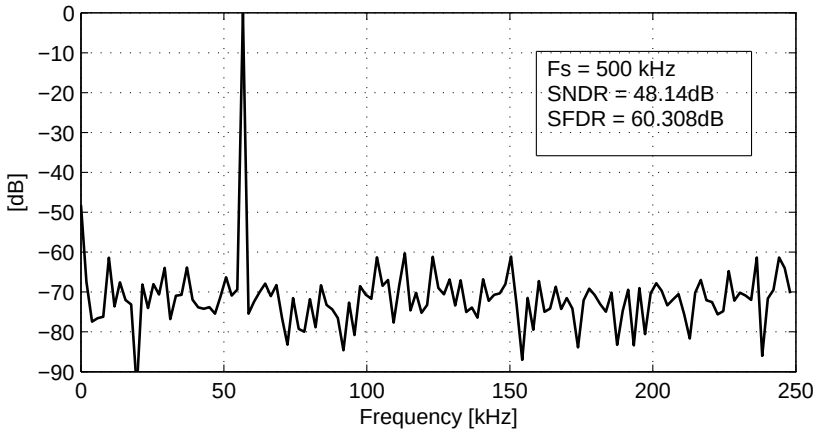

Figure 3.15: Output spectrum at input frequency 56.64 kHz

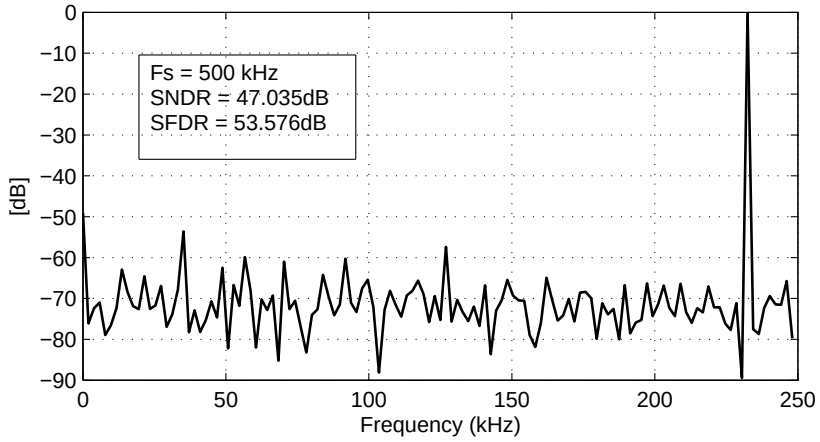

Figure 3.16: Output spectrum at input frequency 232.42 kHz

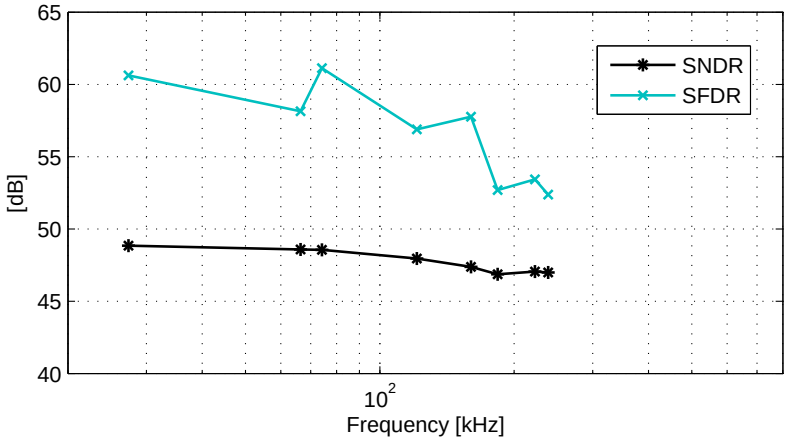

Figure 3.17: Variations in SNDR and SFDR with respect to frequency

The variation of the SNDR and SFDR with respect to the input frequency is shown in Figure 3.17. The total power consumption for 56.64 kHz and 232.42 kHz input sine wave is found to be 1.8 mW and 2.02 mW respectively.

The results of the prototype 2 bit/step SAR ADC using the proposed DAC is found to be encouraging. However, sensitivity of the DAC to parasitics from the switches and the buffer can be expected to have a significant impact on the ADC performance. To minimize the effect of parasitics, one way is to use large sized capacitors, but this calls for a larger power for the buffers in addition to the area overhead. It can be noted that the 2 pF capacitors are used for the same purpose. Therefore, to have a DAC with small capacitors (to take area advantage over BWC DAC) and at

Table 3.3: Performance summary of the ADC

Parameter	Value
Technology	0.18 μm
Supply Voltage	3.3 V
Resolution	8 bit
Sampling Frequency	500 kS/s
Input Range	2 V peak to peak
SNDR	47.03 dB @ 232.42 kHz, 48.14 dB @ 56.64 kHz
ENOB	7.52 @ 232.42 kHz, 7.7 @ 56.64 kHz
Maximum DNL, INL	0.3 LSB, 0.4 LSB
Total Power	1.8 mW

the same time to have no significant effect from the parasitics, it is necessary to have a relook into the DAC architecture for a suitable modification further. The result of the research towards this goal is a novel programmable 8 bit DAC that can also be programmed for 4-8 bit operation with ease. The design of the proposed novel DAC and the SAR ADC has been explained in the next chapter.

Chapter 4

A NOVEL, COMPACT 4 TO 8 BIT NONBINARY SAR ADC BASED ON TWO BIT PER CYCLE DAC ARCHITECTURE

The prototype ADC presented, as a proof of concept, in Chapter 3 is susceptible to parasitics when the capacitance value is not chosen high enough. The threshold references V_{MID}, V_{TH1} and V_{TH2} are generated using switched capacitor networks and buffers. The junction parasitic capacitors from the switches and buffer input capacitors are the dominant contributors to parasitics. For the same reason, the unit capacitor used is of the order of few pico farads. This demands a large power form the recycling buffers thus degrading the efficiency. With the technology scaling, this issue can aggravate, when the ADC is to be built for low voltage operation. The voltage dependent nature of their capacitances is one of the major contributors to the ADC non-linearity.

In order to overcome this issue and allow for realization of the DAC with relatively small capacitors of the order of few hundreds of femto farads and thereby reducing the power, the DAC architecture has been modified suitably. This chapter, analyzes the effect of parasitics on the DAC error in the prototype ADC, proposes suitable

modifications to generate reference voltages that are relatively insensitive to parasitics (to a large extent) and presents the design of a novel 4-8 bit programmable NBW SAR ADC using the modified DAC architecture. To realize 2 bit/step DAC and hence the SAR ADC suitable for typical DAQ systems, initial specifications were set as below:

Table 4.1: Target specification for programmable SAR ADC

Process Technology	90 nm
Power Supply	1 V
Conversion Rate	1 MS/s
Reference Voltage	0.5 V
Input Range	0.5 V
Programmable resolution	4-8 bits

4.1 EFFECT OF PARASITICS ON V_{MID} GENERATION AND ITS MITIGATION

An equivalent circuit of the V_{MID} generating circuit of the DAC presented in Chapter 3 is shown in Figure 4.1.

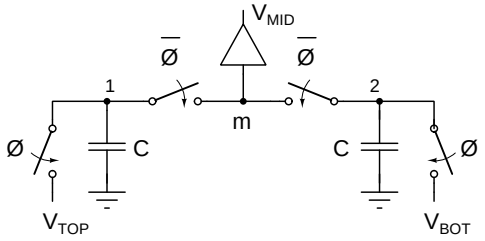

Figure 4.1: Switched capacitive network for V_{MID} generation

Let us assume that nodes 1, 2 have parasitic capacitance to ground, say C_{p1} and C_{p2} respectively, due to the switches. The node m will have a parasitic capacitance (C_{pm}) due to the switches and the buffer. During the phase ϕ, node 1 and 2 are connected to V_{TOP} and V_{BOT} respectively while node m will be at a potential equal to V_{MID} corresponding to the previous cycle. This state is shown in Figure 4.2 for the n^{th} cycle, along with the parasitic capacitance. In $\overline{\phi}$, voltages sampled at node

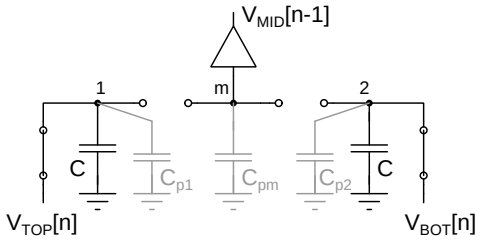

Figure 4.2: V_{MID} generation circuit in Figure 4.1 in presence of parasitics during ϕ phase.

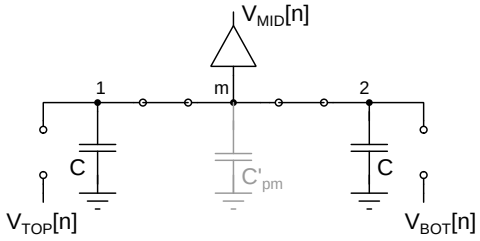

Figure 4.3: V_{MID} generation circuit in Figure 4.1 in presence of parasitics during $\overline{\phi}$ phase

1 and node 2 are shared to generate V_{MID}. This state is shown in Figure 4.3. Note that here, C'_{pm} shows the equivalent parasitic at node m. Apply charge conservation principle, the voltage at node m at the end of the n^{th} cycle can be derived and put in a form given in (4.1).

$$\begin{aligned} V_{MID}[n] &= \frac{2CV_{MID,ideal[n]}}{C_{tot}} + \frac{C_{p1}V_{TOP}[n]}{C_{tot}} \\ &\quad + \frac{C_{p2}V_{BOT}[n]}{C_{tot}} + \frac{C_{pm}V_{MID}[n-1]}{C_{tot}} \end{aligned} \tag{4.1}$$

In (4.1),

$$V_{MID,ideal}[n] = \frac{V_{TOP}[n] + V_{BOT}[n]}{2} \tag{4.2}$$

$$C_{tot} = 2C + C'_{pm} \tag{4.3}$$

It is to be noted that $V_{MID,ideal}[n]$ is the ideal voltage expected at node m during

$\overline{\phi}$. Clearly, V_{MID} generated at the end of each cycle has an error over the desired value of $V_{MID,ideal}$. In addition, the error accumulates from the previous cycle, which can seriously affect the linearity.

The error in the V_{MID} generated in the n^{th} cycle is defined as in (4.4) and can be written as in (4.5) after simplifying.

$$\Delta V[n] = V_{MID,ideal}[n] - V_{MID}[n] \tag{4.4}$$

$$\begin{aligned}\Delta V[n] = {} & \frac{V_{TOP}[n](C'_{pm} - 2C_{p1})}{2C_{tot}} + \frac{V_{BOT}[n](C'_{pm} - 2C_{p2})}{2C_{tot}} \\ & - \frac{C_{pm}V_{MID}[n-1]}{C_{tot}}\end{aligned} \tag{4.5}$$

If the circuit is symmetric and the parasitic capacitances are assumed to be voltage independent, then $C_{p1} = C_{p2}$ and $C'_{pm} = C_{p1} + C_{p2} + C_{pm}$. In such a case, $\Delta V[n]$ simplifies to

$$\Delta V[n] = \frac{C_{pm}}{C_{tot}}(V_{MID,ideal}[n] - V_{MID}[n-1]) \tag{4.6}$$

From (4.6), the worst case error occurs at the first cycle assuming $V_{MID}[n-1] = 0$ and is given by (4.7).

$$\Delta V_{max} = \frac{C_{pm}}{C_{tot}}\frac{V_{REF}}{2} \tag{4.7}$$

Minimization of this error demands for a large value of C at least of the order of few pico farads. For limiting the error to half-LSB, C_{tot} required would be 2^N times the total parasitics. For an 8 bit ADC, the presence of parasitic capacitance of 10 fF would demand the capacitors each to be of value 1.28 pF.

4.1.1 Modification to V_{MID} generation circuit

A careful look at the results given above reveal that the parasitic capacitance at node m is responsible for the error and its accumulation. A modification to the circuit in Figure 4.1 is proposed which can make the V_{MID} generation insensitive to parasitics if the parasitics are voltage independent. The proposed circuit is shown in Figure 4.4. Here, the buffer is split into two and are directly driven by node 1 and node 2 thereby eliminating node m and there by the parasitic C_{pm}. Both the nodes 1 and 2 see equal

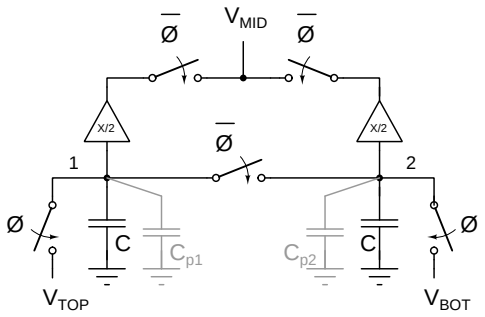

Figure 4.4: Proposed V_{MID} generation circuit

parasitics. The effect is that the error in V_{MID} generated is zero.

However, with voltage dependent parasitics, V_{MID} is bound to have an error and is given in (4.8). It can be seen that the error is proportional to the difference in parasitic capacitances between the nodes 1 and 2. The result is that the requirement on C is relaxed to a large extent. Another point to note is that the error does not accumulate.

$$\Delta V[n] = \frac{(C_{p1} - C_{p2})}{2C_{tot}}(V_{TOP} - V_{BOT}) \tag{4.8}$$

The value of unit capacitor C in $L-part/R-part$ of the DAC not only decides the error in V_{MID} generation but also the noise contribution from the DAC.
Firstly, to minimize the error in V_{MID} generation due to parasitic capacitances at charge sharing nodes of the SC circuit, the difference in parasitic capacitances at charge sharing nodes must be as low as possible as seen in (4.8). To limit this error within $0.1\,V_{LSB}$,

$$C/(C_{p1} - C_{p2}) > 640 \tag{4.9}$$

Secondly, the thermal noise due to the resistance of the switches at the charge sharing nodes at the end of N_c clock cycles is,

$$N_c\sqrt{KT/C} \tag{4.10}$$

where N_c is the number of clock cycles for N bit resolution.
To limit this noise voltage within $\beta.V_{LSB}$, where β is a fraction, then

$$C > (N_c/\beta)^2 KT/(V_{LSB})^2 \tag{4.11}$$

If β is considered as 0.1, then,

$$C > 17.36\, fF \tag{4.12}$$

To limit these errors to a safe value, a higher but reasonable capacitance value may be chosen for C. For $C = 200\,\text{fF}$, the permissible parasitic difference between the nodes 1 and 2 is found to be less than 0.312 fF.

4.2 EFFECT OF PARASITICS ON V_{TH1} AND V_{TH2} GENERATION AND ITS MITIGATION

The flash references V_{TH1} and V_{TH2} generated in the proposed prototype DAC are also prone to errors in the presence of switch and buffer parasitics. The effect of parasistics can be explained with the simplified schematic shown in Figure 4.5

In the figure it can be observed that, node A sees two parasitic capacitances C_{pA1} and C_{pA2} in a clock cycle. C_{pA1} is due to the switches and the buffer connected to node A. C_{pA2} is due to the switches connected to $C/2$. During phase ϕ, both these capacitors hold different voltages i.e., C_{pA1} charges to V_{TOP} and C_{pA2} discharges to ground. But, during the phase $\overline{\phi}$, both the capacitors will hold the same voltage as they are connected to node A through the switch. A similar case exists at node B where the parasitic capacitors are named as C_{pB1} and C_{pB2}. If the circuit is symmetric then, one can say $C_{pA1} = C_{pB1}$ and $C_{pA2} = C_{pB2}$. Please note, strictly $C_{pA2} \neq C_{pB2}$ due to presence of the bottom-plate capacitance of $C/2$ capacitor. However, they may be assumed equal if the top-plate is compensated with additional capacitance equal to the bottom-plate parasitic.

For ease of analysis, the following variables are defined.

$$\alpha_1 = \frac{C_{pA1}}{C} = \frac{C_{pB1}}{C} \tag{4.13}$$

$$\alpha_2 = \frac{C_{pA2}}{C} = \frac{C_{pB2}}{C} \tag{4.14}$$

$$\alpha = \alpha_1 + \alpha_2 \tag{4.15}$$

It can be clearly seen that the charges accumulated on node A and node B during ϕ are conserved during $\overline{\phi}$. Applying charge conservation at node A and B for the n^{th}

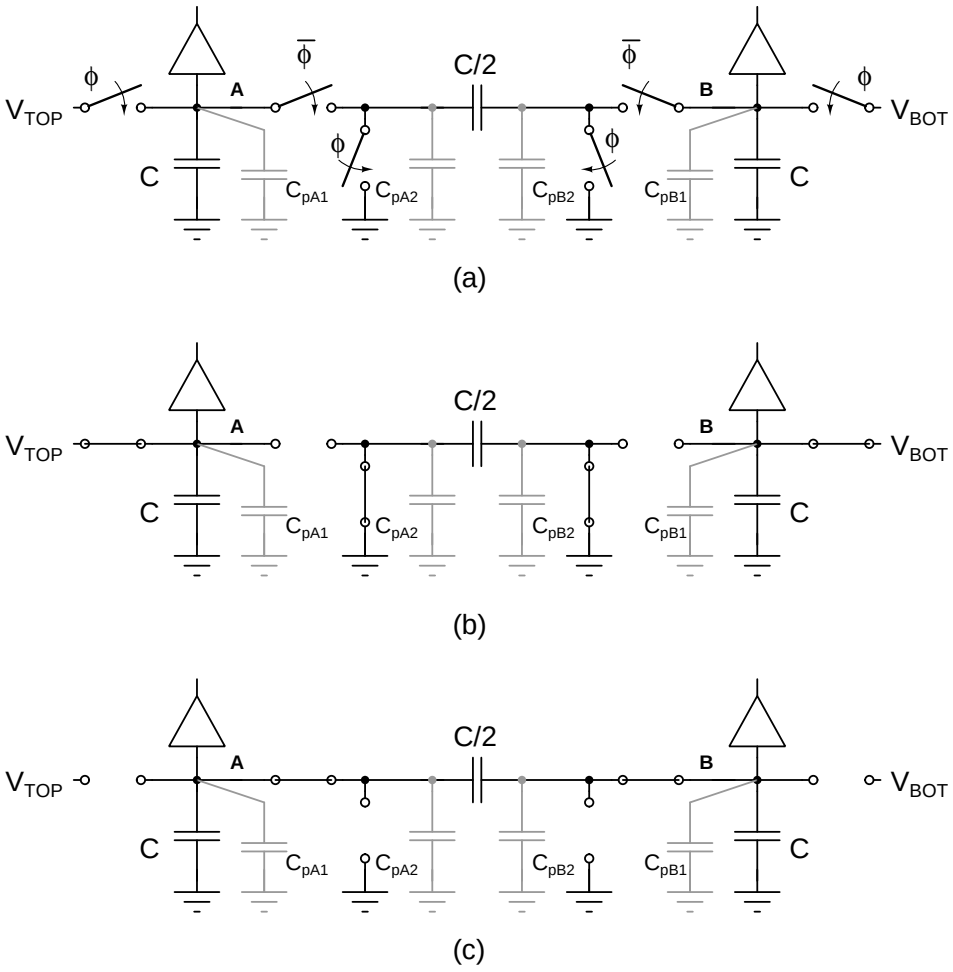

Figure 4.5: V_{TH1} and V_{TH2} generating circuit (a) Simplified schematic showing the parasitics (b) Circuit during phase ϕ (c) Circuit during phase $\overline{\phi}$

clock cycle, (4.16) and (4.17) can be written.

$$(1+\alpha_1)V_{TOP}[n] = \left(\frac{3}{2}+\alpha\right)V_A[n] - \left(\frac{1}{2}\right)V_B[n] \tag{4.16}$$

$$(1+\alpha_1)V_{BOT}[n] = -\left(\frac{1}{2}\right)V_A[n] + \left(\frac{3}{2}+\alpha\right)V_B[n] \tag{4.17}$$

Where, $V_A[n]$ and $V_B[n]$ are the threshold voltages generated due to charge sharing in the $\overline{\phi}$ phase which is fed to the 2 bit flash.

Solving (4.16) and (4.17) by neglecting higher powers of α_1 and α_2, $V_A[n]$ and

$V_B[n]$ can be approximated to (4.18) and (4.19) respectively as,

$$V_A[n] = V_{A,ideal}[n] + \left(\frac{1}{8}\alpha_1 - \frac{5}{8}\alpha_2\right) V_{TOP}[n] - \left(\frac{1}{8}\alpha_1 + \frac{3}{8}\alpha_2\right) V_{BOT}[n] \quad (4.18)$$

$$V_B[n] = V_{B,ideal}[n] + \left(\frac{1}{8}\alpha_1 + \frac{3}{8}\alpha_2\right) V_{TOP}[n] - \left(\frac{1}{8}\alpha_1 - \frac{5}{8}\alpha_2\right) V_{BOT}[n] \quad (4.19)$$

Where $V_{A,ideal}[n]$ and $V_{B,ideal}[n]$ are the ideal values expected (without parasitics) for comparison in the $\overline{\phi}$ phase of the n^{th} cycle and are defined as

$$V_{A,ideal}[n] = \frac{3}{4}V_{TOP}[n] + \frac{1}{4}V_{BOT}[n] \quad (4.20)$$

$$V_{B,ideal}[n] = \frac{1}{4}V_{TOP}[n] + \frac{3}{4}V_{BOT}[n] \quad (4.21)$$

Clearly, from (4.18) and (4.19), it can be seen that the threshold voltages generated are in error which is mainly due to the parasitics. The error also propagates to the next cycle which makes it very important to keep the error to a sufficiently low value such that the overall error is within the limit. This, again, demands for a very small ratio of parasitic to actual capacitor which can only be achieved choosing sufficiently large value of C.

4.2.1 Modification to V_{TH1} and V_{TH2} generation circuit

To mitigate the effect of parasitics, an alternative approach has been adopted. Instead of voltage division using $C/2$ and C to generate V_{TH2} from V_{TH1}, the proposed circuit generates V_{TH1} and V_{TH2} independently by using charge sharing between two capacitors of ratio 1:3. The scheme to generate V_{TH1} and V_{TH2} is shown Figure 4.6. The scheme is explained for V_{TH1} generation and the same can be extended for V_{TH2}.

In the circuit in Figure 4.6(a), for generating V_{TH1}, V_{TOP} and V_{BOT} are sampled on to the $3C$ and C respectively during the phase ϕ. During phase $\overline{\phi}$, the charges on $3C$ and C are shared by connecting them in parallel. The resulting voltage at node X (and Y) during $\overline{\phi}$ is

$$V_{X,Y} = \frac{3}{4}V_{TOP} + \frac{1}{4}V_{BOT} = V_{TH1} \quad (4.22)$$

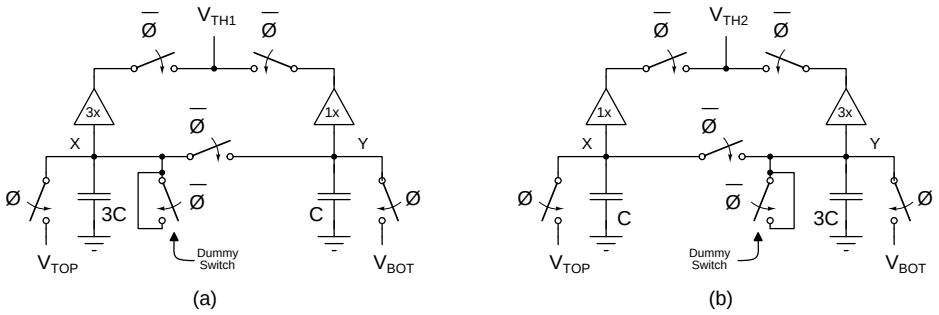

Figure 4.6: Proposed parasitic insensitive circuit to generate (a) V_{TH1} (b) V_{TH2}

The buffers for recycling V_{TH1} can be driven by either of the nodes X or Y. It is important to ensure that the parasitic capacitances across the capacitors also appear in the ratio 1:3 to minimize the effect of parasitics on the generated V_{TH1}. This is done in the following manner.

1. The voltage is taken from both nodes X and Y through the buffers and the buffers are split in the ratio 1:3 such that the ratio of parasitics introduced at the nodes remains the same (the idea presented in V_{MID} in section 4.1.1).

2. The switch connected to V_{TOP} also needs to be sized three times as compared to that connected to V_{BOT}.

3. Dummy switches have been added to balance for the parasitics offered by the charge sharing switch.

A similar arrangement can be used for generating V_{TH2}. The scheme presented above makes the threshold generation insensitive to parasitic capacitance if the parasitics are voltage independent. However, if the parasitic capacitances are considered to be voltage dependent V_{TH1} generated will be in error from the desired value. This error in V_{TH1} at the end of the n^{th} cycle can be written as in (4.23).

$$\Delta V_{TH1} = \frac{3}{4}\frac{V_{TOP}}{C_{tot,XY}}(C_{p,XY} - \frac{4}{3}C_{p,X}) + \frac{1}{4}\frac{V_{BOT}}{C_{tot,XY}}(C_{p,XY} - 4C_{p,Y}) \tag{4.23}$$

Here, V_{TOP} and V_{BOT} correspond to n^{th} cycle, $C_{p,X}$ and $C_{p,Y}$ are the parasitic capacitance at node X and Y respectively during ϕ phase, $C_{p,XY}$ is the total parasitic capacitance at nodes X and Y during $\overline{\phi}$ phase and $C_{tot,XY} = 4C + C_{p,XY}$.

With a similar analysis, voltage at node X (also at node Y) for the circuit in Figure 4.6(b) can be written as in (4.24)

$$V_{X,Y} = \frac{1}{4}V_{TOP} + \frac{3}{4}V_{BOT} = V_{TH2} \tag{4.24}$$

With the voltage dependent parasitics, the error in V_{TH2} can be written as

$$\Delta V_{TH2} = \frac{1}{4}\frac{V_{TOP}}{C_{tot,XY}}(C_{p,XY} - 4C_{p,X}) + \frac{3}{4}\frac{V_{BOT}}{C_{tot,XY}}(C_{p,XY} - \frac{4}{3}C_{p,Y}) \tag{4.25}$$

4.3 PROGRAMMABLE ADC WITH THE MODIFIED DAC

With the proposed modified V_{MID}, V_{TH1} and V_{TH2} generation circuits, a modified NBWC DAC architecture has been proposed and using the same a programmable resolution ADC is designed in 90 nm CMOS technology to operate on 1 V supply. The resolution is made programmable from 4-8 bit with 2 bit/step extraction. Note that a lower technology node with low voltage operation has been chosen to validate the candidature of the proposed methods.

The modified DAC architecture uses a fixed number of capacitors independent of the ADC resolution (in the programmablilty range of 4 to 8 bits). The proposed architecture is also made parasitic insensitive to a large extent, at-least to the first order, with the modifications suggested in the preceding sections when compared to the initial architecture discussed in Chapter 3.

A simplified block diagram of the proposed programmable resolution ADC is shown in Figure 4.7. Though the basic architecture is the same as that given in Chapter 3, the block diagram is given with signals relevant to the proposed ADC. The SAR controller controls the DAC to generate threshold voltages for the 2 bit flash. A finite state machine (FSM) generates the clocks necessary to generate control signals to turn ON/OFF the switches in the DAC as well as the switches at the inputs of the three comparators.

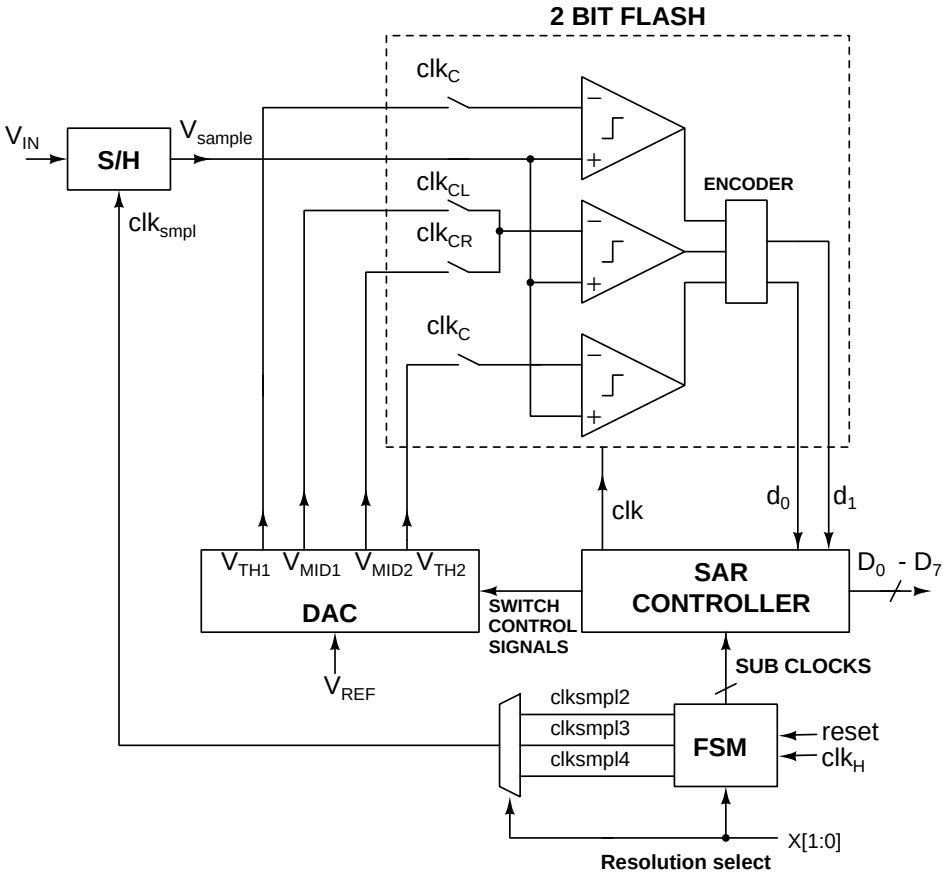

Figure 4.7: Block diagram of programmable resolution SAR ADC.

4.3.1 Algorithm

The algorithm followed for extracting 2 bits per cycle remains the same as that of the prototype ADC explained in Chapter 3. However, for the sake of continuity and completeness the algorithm has been explained with respect to Figure 4.7. A pictorial representation of the scheme followed is shown in Figure 4.8 and can be explained as follows.

- In the beginning of each clock cycle, two voltages V_{TOP} and V_{BOT} are generated based on the bits evaluated in the previous cycle.

- V_{TOP} and V_{BOT} are divided into four equal parts (quadrants), each of value (V_{TOP} - V_{BOT})/4. The resulting three levels, in between V_{TOP} and V_{BOT}, are denoted as V_{TH1}, V_{MID} and V_{TH2} (in the decreasing order of voltage).

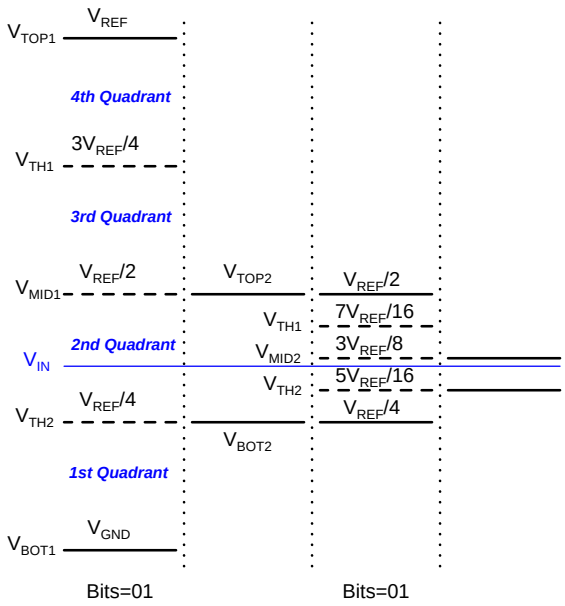

Figure 4.8: Pictorial representation of the algorithm followed in DAC for reference generation.

- These three voltage levels are compared with the input V_{IN} to evaluate the two bits in each cycle.

In the first clock cycle, V_{TOP} - V_{BOT} is equal to the full scale voltage V_{REF}. In the second cycle, V_{TOP} and V_{BOT} are updated based on the quadrant in which the input is present. This process repeats until all the bits are evaluated. As can be seen in Figure 4.8, both V_{TOP} and V_{BOT} converge towards the input. All the desired voltage levels are generated using the proposed switched capacitor circuit (DAC). Timing diagram of the conversion process is shown in Figure 4.9. Each conversion cycle has a sampling phase and a hold phase. In the sampling phase, the input is sampled and in the hold phase the conversion takes place. In the sampling phase, the input is sampled and simultaneously V_{TOP} and V_{BOT} are set such that $V_{TOP} = V_{CM} + \frac{V_{REF}}{2}$ and $V_{BOT} = V_{CM} - \frac{V_{REF}}{2}$ where V_{CM} is the common mode DC voltage. The input V_{IN} also resides on the same common mode DC. The clk_H = HIGH is the recycling phase except for the first cycle which is a sampling phase. In the recycling phase, V_{TOP} and V_{BOT} required for the bit evaluation in the current cycle are generated by recycling two voltages appropriately chosen from V_{TOP}, V_{TH1}, V_{MID}, V_{TH2} and V_{BOT} from the previous cycle based on the bits evaluated in the previous cycle. During clk_H = LOW

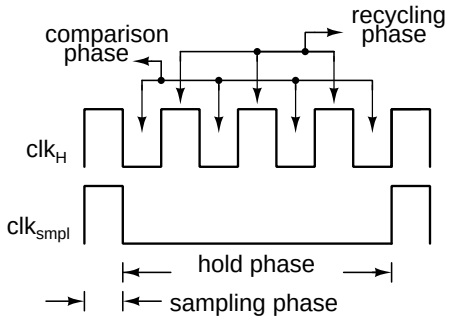

Figure 4.9: Timing details of one conversion cycle.

(comparison phase), V_{TH1}, V_{MID} and V_{TH2} are generated for the current cycle from V_{TOP} and V_{BOT}. Also, the two bits are evaluated by comparing V_{IN} with V_{TH1}, V_{MID} and V_{TH2}.

4.4 PROPOSED DAC ARCHITECTURE

The proposed (modified) DAC architecture for 2 bits per cycle evaluation for the ADC is shown in Figure 4.10. Four SC blocks are used to generate three reference voltages (V_{TH1}, V_{MID} and V_{TH2}) for the flash. They are named LEFT, RIGHT, UP and DOWN. All these blocks are derived from the proposed (modified) V_{MID}, V_{TH1} and V_{TH2} generating circuits. The SC blocks LEFT and RIGHT are identical circuits that generate V_{MID} in tandem. In one cycle LEFT generates V_{MID} and RIGHT holds the two voltages (V_{TOP}, V_{BOT}) that are being processed. These two SC blocks interchange this task in subsequent comparison cycles. UP and DOWN SC blocks are used to generate V_{TH1} and V_{TH2} respectively for every comparison cycle. Output of the comparators are encoded at each comparison phase and based on the pair of bits generated during the comparison phase, charge recycling is done by switching ON the appropriate switches in the DAC. This process continues until all pairs of bits are evaluated. DAC uses a fixed number of unit sized capacitors for reference generation which is independent of resolution.

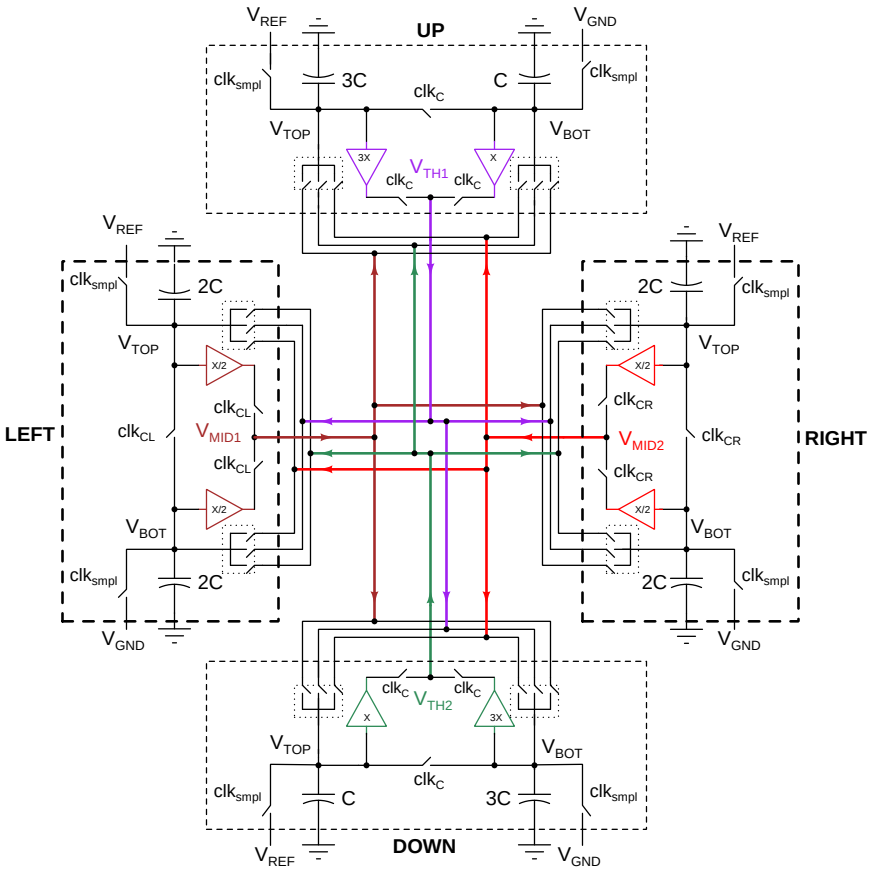

Figure 4.10: Proposed DAC architecture to evaluate 2 bit per cycle.

4.5 RESOLUTION PROGRAMMABILITY

The proposed DAC architecture supports resolution reconfigurability with ease, since the hardware used in the DAC (capacitors, switches or analog blocks) are independent of resolution. The S/H, comparator and DAC are to be designed for the accuracy demanded by the highest resolution, a requirement similar to that for the conventional approach. Since comparator resolution and buffering accuracy are designed to support ADC resolution up to 8 bits in this work, clocking scheme and control logic are modified to suit programmable resolution in the range 4-8 bits. Using FSM circuit (shown in Figure 4.7), a sampling clock is generated to sample the input signal after 2, 3 or 4 cycles of the system clock using the signals *clksmpl2, clksmpl3* and *clksmpl4* to achieve a programmability of 4 to 8 bits. Resolution is selected digitally by resolution select bits $X[1{:}0]$. Accordingly, the FSM block generates clk_{smpl} for

the S/H block. Therefore sampling rate increases as the ADC resolution decreases. Resolution is variable from 4-8 bits in 1 bit increments. In each of these resolution modes, the sampling rate can be lowered down to 60% from it's peak sampling rate. The leakage at nodes V_{TOP} and V_{BOT} in each of the SC blocks poses a lower limit on the sampling rate.

4.6 BUILDING BLOCKS OF 2 BITS PER CYCLE SAR ADC

4.6.1 Buffer

The buffers required to recycle the charges for generating 2-bit flash references are realized by connecting OTA in unity feedback configuration. To limit the buffer error to less than $\left(\frac{1}{8}\right)^{\text{th}}$ of an LSB at 8 bit resolution for a full-scale voltage of 0.5 V, it is desirable to have a gain in excess of 66 dB for the OTA. A two-stage OTA with a folded cascode first stage has been designed, the circuit of which is shown in Figure 4.11. Transistors M_1-M_9 form the first stage folded cascode amplifier and M_{13}-M_{16} form the second stage. Transistor sizes are decided to maximize the voltage gain as well as to meet the signal swing requirement. Table 4.2 shows the sizes of all the transistors of the OTA.

Approximate gain of first stage (Av_1) and the second stage (Av_2) is given by (4.26) and (4.27) respectively.

$$Av_1 \cong g_{m2}r_{o9} \tag{4.26}$$

$$Av_2 \cong g_{m13}[g_{m14}r_{o13}r_{o14} \| g_{m15}r_{o15}r_{o16}] \tag{4.27}$$

Transistors M_{10}, M_{11} and M_{12} form a part of the biasing circuit of the first and second stage of the OTA. In order to extend the input range of the amplifier and hence the DAC, the bias current through the folded cascode stage is made input voltage dependent instead of a fixed bias scheme. Here the bias current through M_6 and M_7 is made to track the variations in the current of M_3 (the tail transistor) occurring due to channel length modulation at large input signals. When used as unity gain buffer,

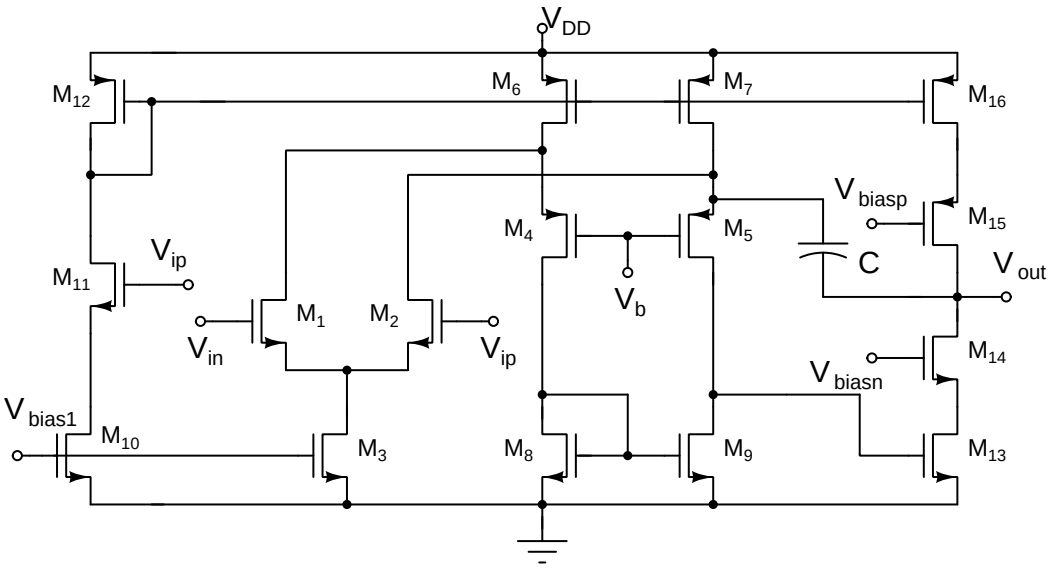

Figure 4.11: Schematic of the two stage OTA for the buffer.

Table 4.2: Transistor sizes for the OTA

Transistors	$\left(\frac{W}{L}\right)$F
M_1, M_2	$\left(\frac{1}{0.18}\right)$ 2
M_3, M_{10}	$\left(\frac{0.18}{0.18}\right)$ 2
M_4, M_5	$\left(\frac{0.36}{0.18}\right)$ 16
M_6, M_7, M_{12}	$\left(\frac{0.36}{0.18}\right)$ 8
M_8, M_9, M_{13}	$\left(\frac{0.12}{0.18}\right)$ 2
M_{11}	$\left(\frac{1}{0.18}\right)$ 4
M_{14}, M_{15}	$\left(\frac{0.72}{0.18}\right)$ 2
M_{16}	$\left(\frac{0.36}{0.18}\right)$ 4

W and L are width and length in μm.

F is the number of fingers.

this is important since for large signals, common mode rejection degrades affecting the input range (Ribner and Copeland 1984). The use of M_{11} with its gate driven by the V_{ip} input will force the current of M_{10} to follow that of M_3 thus improving the common mode rejection and the input range. The loop is compensated by adding a capacitor between the output node to the folding node. The drain to source resistance

of M_5 acts as a resistance in series with the capacitor, and thus helps in compensating for the right half plane zero appearing at $(g_{m13})/C$.

Figure 4.12 shows frequency response of the OTA. The overall DC gain obtained is 76.9 dB for typical process corner, which includes first stage gain of 28.7 dB and the second stage gain is 48.2 dB. The unity gain bandwidth of OTA is 70 MHz. The gain margin and phase margin are found to be 15 dB and 55° respectively. The maximum error in buffer output voltage for the intended input range of 0.5 V over an equal common-mode voltage is found to be less than 120 μV ($<$ 0.1 LSB). The total input referred noise of the buffer is found to be 6.17 nV^2. The response of the buffer for a

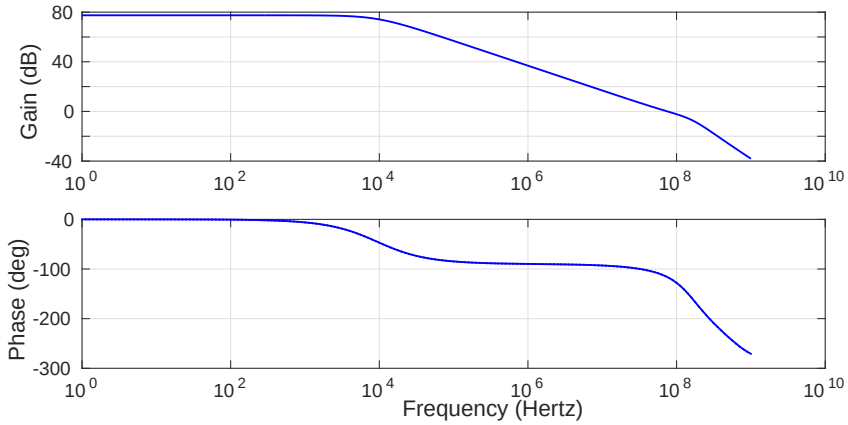

Figure 4.12: Frequency response of low power OTA

square wave input with a capacitive load of 600 fF is shown in Figure 4.13. Slew rate of 4.78 V/μs and 48.5 V/μs with settling time of 110 ns and 30 ns respectively have been achieved with this load.

Since the error in the buffer plays an important role in the DAC (and hence ADC) non-linearity, the error at the output of the buffer normalized to LSB (for $V_{REF} = 0.5$ V) is plotted for the expected input range of $(V_{CM} - V_{REF}/2) = 0.25$ V to $(V_{CM} + V_{REF}/2) = 0.75$ V and is shown in Figure 4.14. It can be seen that the maximum error is only $\left(\frac{1}{8}\right)^{\text{th}}$ LSB.

The offset correction scheme (Enz and Temes 1996) shown in Figure 4.15 has been used to minimize buffering error due to offset voltage. The offset is stored on to a capacitor C_{OS} during the sample phase ($clk_{smpl} = 1$) and correction is applied during the hold phase ($\overline{clk}_{smpl}$) by connecting in series between the output and inverting

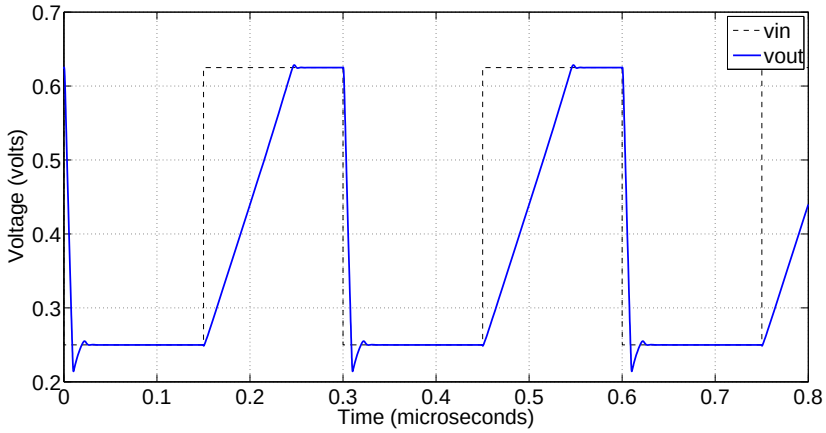

Figure 4.13: Transient response of the buffer.

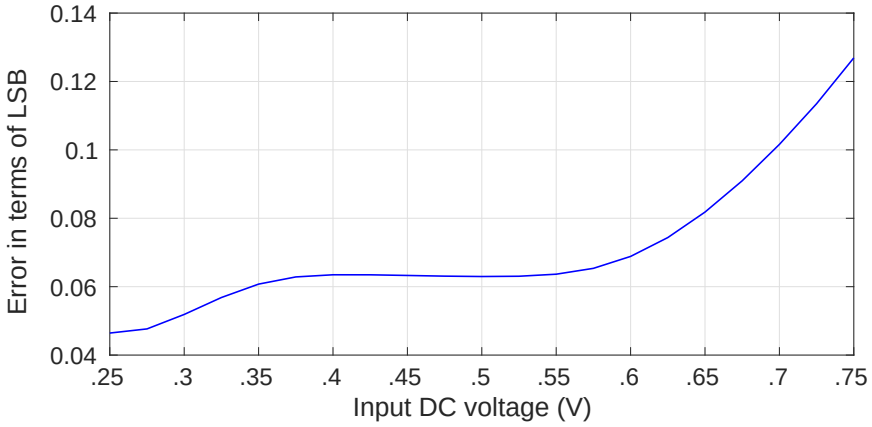

Figure 4.14: Buffer error for the entire input range, normalized to LSB.

terminal of the OPAMP. Note that ($clk_{smpl(d)}$) is delayed from (clk_{smpl}) so as to minimize charge injection effect.

Table 4.3 shows the performance summary of OTA.

4.6.2 Comparator

The comparator used for the 2 bit flash is realized by cascading two pre-amplifier stages followed by a latch. The schematic of the pre-amplifier and dynamic latch stage is shown in Figure 4.16. Pre-amplifier is realized using a simple NMOS differential amplifier with PMOS resistor loads. One of the inputs comes from input sample

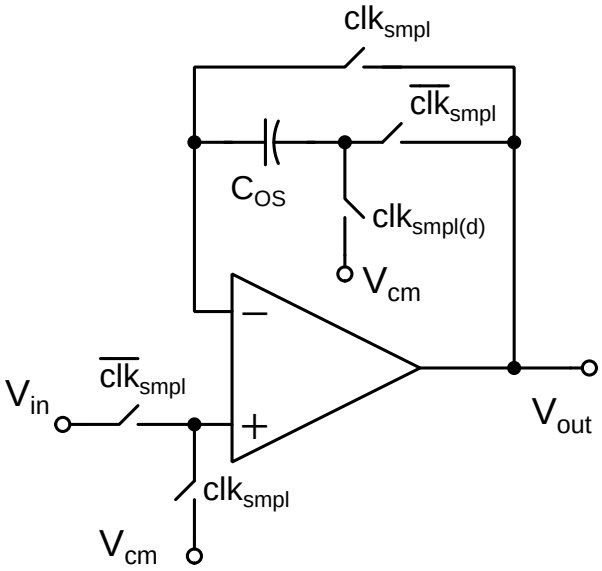

Figure 4.15: Buffer with offset correction circuit

Table 4.3: Performance summary of low power OTA at nominal process, voltage and temperature.

Performance metric	**Value**
DC Gain [dB]	76.98
UGB [MHz]	70
Gain margin [dB]	15
Phase margin [deg]	55
Power dissipation [μW]	16
Load capacitance [fF]	600
PSRR [dB]	54.7
CMRR [dB]	80

and hold circuit and the other from the DAC. Both these inputs reside on a DC of 0.5 V resulting an input common mode voltage of 0.5 V, for the pre-amplifier. Each pre-amplifier has been designed to offer a gain of 6 dB. Table 4.4 shows the size of all the transistors of the comparator.

The operation of dynamic latch is explained as follows: During *clk* low phase, nodes V_A and V_B are forced to V_{DD} by M_9 and M_{10}. When *clk* goes high, these nodes

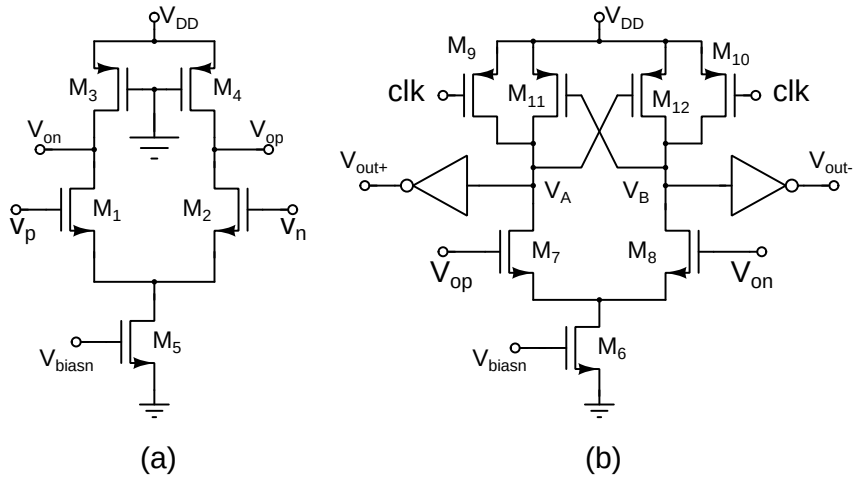

Figure 4.16: Comparator (a) Pre-amplifier stage (b) Dynamic latch stage

Table 4.4: Transistor sizes for the comparator

Transistors	$\left(\frac{W}{L}\right)$F
M_1, M_2	$\left(\frac{1}{0.18}\right)$ 2
M_3, M_4	$\left(\frac{0.12}{4.8}\right)$ 2
M_5, M_6	$\left(\frac{0.12}{0.18}\right)$ 8
M_7, M_8	$\left(\frac{0.18}{1}\right)$ 2
M_9, M_{10}	$\left(\frac{0.5}{0.1}\right)$ 6
M_{11}, M_{12}	$\left(\frac{0.5}{0.25}\right)$ 4

W and L are width and length in μm.

F is the number of fingers.

slew towards ground at unequal rates decided by the input differential voltage. When the node voltages are low enough, PMOS positive feedback load devices M_{11} and M_{12} turn on and latch the comparator. The output inverters restore the comparator outputs to logic levels. The power consumption of the comparator is $8.4\,\mu$W with a resolution of $\pm 100\,\mu$V. The pre-amplifier stage followed by latch stage not only helps in minimizing the offset of the latch stage, but it also helps to achieve overall resolution of 10 bits for the comparator. Dynamic offset voltage of the overall comparator is found to be $80\,\mu$V, which is well within $0.1\,V_{LSB}$. Careful device matching during layout as well as by slightly overdesigning the overall resolution of the comparator,

the offset calibration technique is avoided in this work.

4.6.3 Switch bootstrapping sample and hold

To improve dynamic performance of the ADC a switch bootstrapping sample and hold (Maloberti 2007), shown in Figure 4.17(a), has been used. The circuit uses a charged capacitor to sustain the gate to source voltage of M_1 during ON phase. The switch M_6 grounds the gate of the switch M_1 during OFF phase and, at the same time, switches M_3 and M_4 charge the bootstrapping capacitor to the supply voltage. Switch M_5 and transmission gate (TG) switch connect the gate and drain of M_1 during ON state with boosted gate voltage.

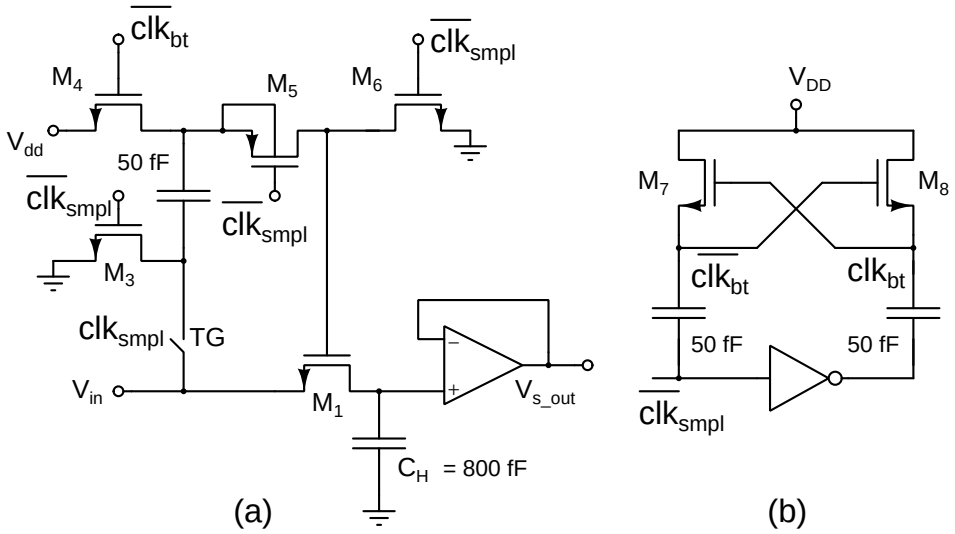

Figure 4.17: (a) Switch bootstrapping sample and hold. (b) Clock booster

Each of the switches used must have appropriate gate drive in order to ensure proper switching and suitable protection for the drains that undergo large voltage swings. Since switch M_4 is an NMOS transistor, its gate requires a voltage higher than V_{DD} for it to turn ON. Therefore a voltage doubler made by a cross coupled pair M_7-M_8 with charge pumping capacitors as shown in Figure 4.17(b) is used. The gates of M_7 and M_8 are driven by the clock and complemented clock signal. Table 4.5 shows the sizes of all the transistors of the sample and hold.

Table 4.5: Transistor sizes for sample and hold

Transistors	$\left(\frac{W}{L}\right)$F
M_1	$\left(\frac{0.12}{0.10}\right)$ 1
M_3, M_4, M_6	$\left(\frac{1}{0.1}\right)$ 1
M_5	$\left(\frac{0.4}{0.1}\right)$ 1
M_7, M_8	$\left(\frac{0.24}{0.11}\right)$ 1

W and L are width and length in μm.

F is the number of fingers.

4.7 SIMULATION RESULTS

The proposed programmable resolution 2 bit per step SAR ADC has been designed in UMC 90 nm CMOS process to operate on 1 V supply. The layout of the ADC is shown in the Figure 4.18 and the area occupied is 0.06182 mm^2 (281 μm X 220 μm). The post layout simulation results show that, ADC achieved a conversion speed of 1.2 MS/s in 7/8 bit mode and 2.4 MS/s in 4 bit mode.

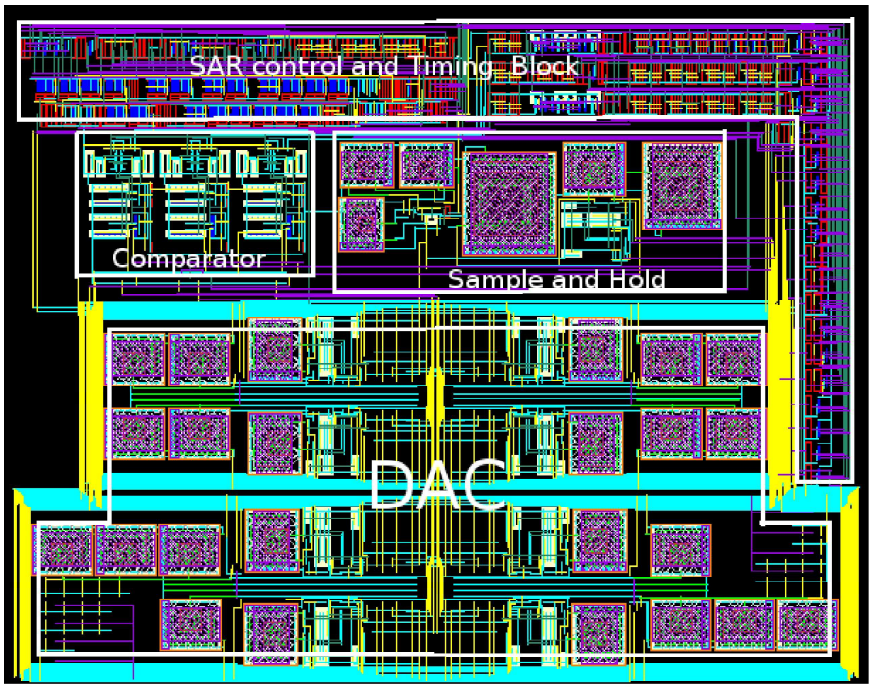

Figure 4.18: Layout of the ADC

The total capacitance used in the DAC is $16\,C$ where, C is the unit capacitor of value 100 fF. Thanks to the parasitic insensitive reference generation scheme, which otherwise would have demanded a C of at least a couple of pico farads. Also, 100 fF has been used for unit capacitors only to minimize the effect of voltage dependent parasitics. Compared to the conventional charge redistribution DAC architecture which requires $256\,C$ for an 8 bit resolution, this DAC offers large savings in terms of area, headroom on capacitor mismatch and parasitic requirements.

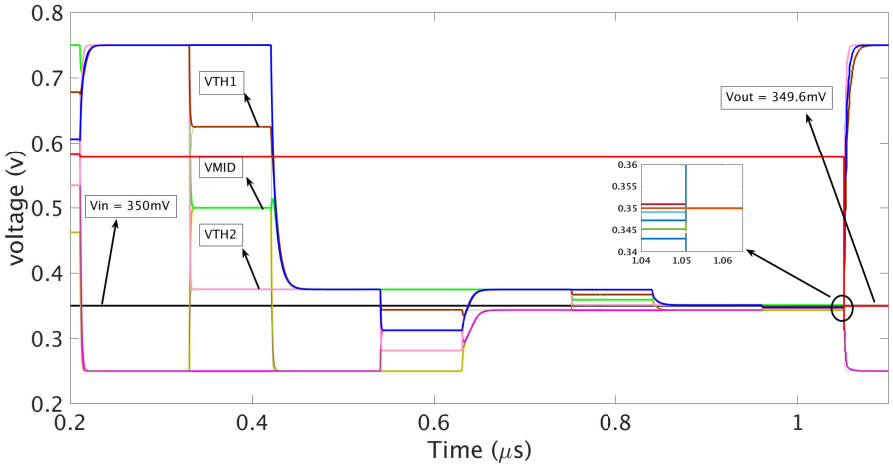

Figure 4.19: Operation of ADC for the case of $V_{IN} = 350\,\text{mV}$ (first quadrant)

Operation of the ADC is depicted in Figure 4.19 where, the transient voltages of the DAC viz-a-viz V_{TOP}, V_{BOT}, V_{MID}, V_{TH1} and V_{TH2} are shown for one conversion cycle for a case of $V_{IN} = 350\,\text{mV}$. It also shows the ADC output, as an equivalent analog voltage (ADC output fed to ideal DAC) at the end of each conversion cycle.

From static performance of ADC (code density test) in 8 bit mode, DNL and INL of the ADC at 1.2 MS/s sampling speed are found to be within 0.7 LSB/-0.5 LSB and 0.3 LSB/ -0.8 LSB respectively and is shown in Figure 4.20 and Figure 4.21 respectively.

The output spectrum of the ADC for an input full-scale sine wave at 13.95 kHz (near DC) and 525.48 kHz (at Nyquist) are shown in Figure 4.22 and Figure 4.23 respectively, for which the SNDRs of 48.57 dB (ENOB = 7.77) and 47.9 dB (ENOB = 7.66) are obtained, respectively.

The variation of the SNDR and SFDR with respect to the input frequency is shown in Figure 4.24.

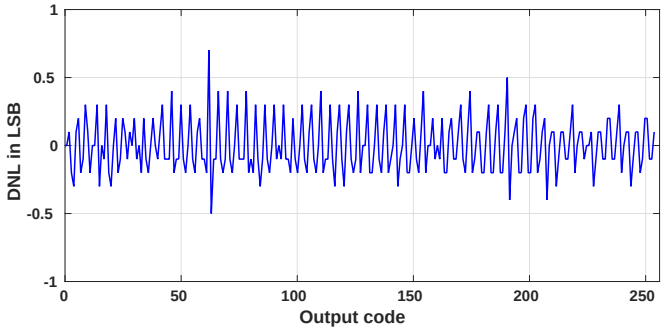

Figure 4.20: DNL error in 8 bit mode

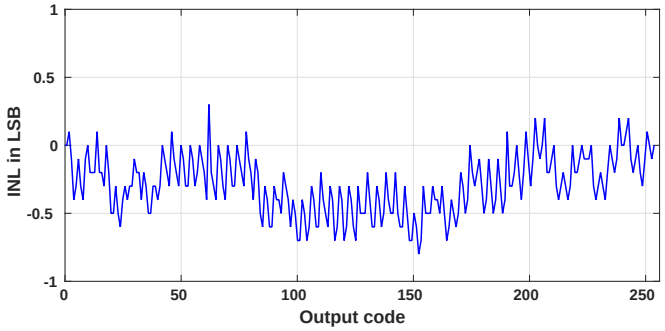

Figure 4.21: INL error in 8 bit mode

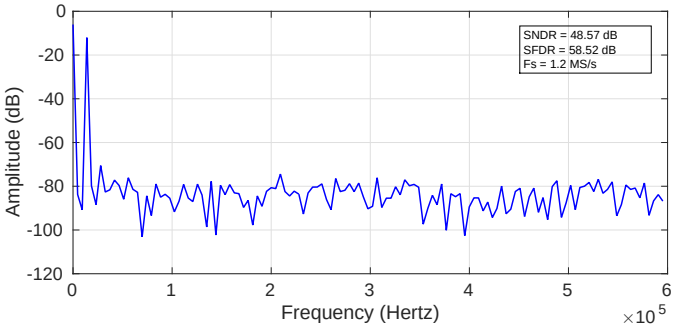

Figure 4.22: FFT spectrum of 8 bit ADC for an input frequency of 13.95 kHz

The total power consumption of the ADC is 185 μW. Further reduction in power is possible by turning the two split buffers OFF during the recycling phase. This is possible since only two of the four buffers in the DAC are used during the recycle phase. This would result in a power of 130 μW, however this was not attempted in

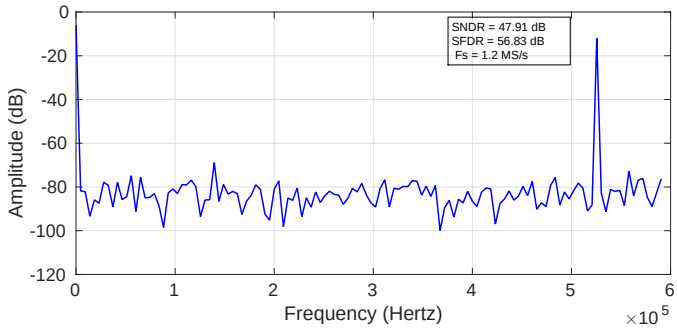

Figure 4.23: FFT spectrum of 8 bit ADC for an input frequency of 525.48 kHz

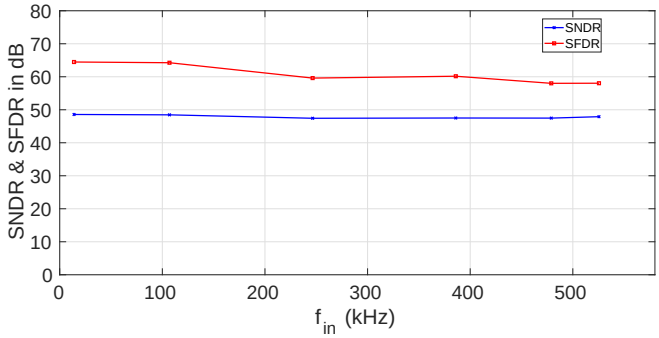

Figure 4.24: Variations in SNDR and SFDR with respect to frequency

the present ADC.

To verify the ADC performance against mismatch in buffers used in the DAC, Monte Carlo simulations of 50 runs is carried on the extracted netlist. Please note that only 50 runs are used to save on the time required for simulating the extracted netlist. Figure 4.25 shows the histogram plot of SNDR variations. The mean and sigma values of SNDR are 42.55 dB and 3.36 dB respectively. The plot shows the proposed ADC architecture is mismatch tolerated to a large extent.

The ADC performance for various process corners is given in Table 4.6. The ADC is found to offer consistent performance across corners (except at *snfp* corner) at nominal temperature and 1 V supply.

Table 4.7 shows the ADC dynamic performance and power for ±10% variation in the supply voltage over the nominal value of 1 V at nominal process and temperature. Table 4.8 presents the ADC performance for temperature variation from 0℃ - 70℃ at nominal process and supply.

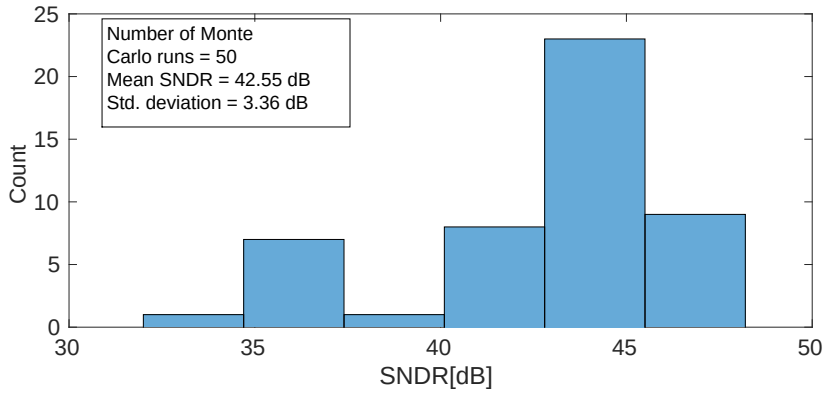

Figure 4.25: Mean and sigma SNDR against mismatch in buffers

Table 4.6: Performance of ADC over different process corners

Parameter	**tt**	**ff**	**ss**	**snfp**	**fnsp**
SNDR(dB)@DC	48.6	46.3	49.9	41.8	47.6
SNDR(dB)@Nyq.	47.9	46.0	49.3	41.3	48.6

Table 4.7: Performance of ADC over different supply voltage

Parameter	**0.9 V**	**1 V**	**1.1 V**
SNDR(dB)@DC	48.9	48.57	47.15
SNDR (dB)@Nyquist	47.43	47.9	46.89
Power(μW)	178.5	185	190.4

Table 4.8: Performance of ADC over different temperature

Parameter	**0°C**	**27°C**	**70°C**
SNDR(dB)@DC	48.82	48.57	48.14
SNDR (dB)@Nyquist	47.91	46.02	48.1

The designed programmable resolution SAR ADC performance (with resolution set to 8 bits) is compared with some of the SAR ADCs found in the literature and listed in Table 4.9 and Table 4.10. The figure of merit (FOM) used for the comparison is computed using the formula (1.1). The area efficiency (AE) is computed from (1.2).

It can be seen that the proposed SAR ADC has an FOM comparable with some

Table 4.9: Comparison with available low power 2 bit/step and variable resolution SAR ADCs in the literature.

Reference	Yip and Chandrakasan (2013)*	O'Driscoll et al. (2011)*	Chaturvedi et al. (2013)*	Cao et al. (2009)*	Hong et al. (2015)*	**This Work@**
Architecture	Prog. SAR	Prog. SAR	Prog. SAR	2 b SAR	2 b SAR	**2 b & Prog. SAR**
Technology (μm)	0.065	0.13	0.13	0.13	0.045	**0.09**
Supply Voltage (V)	0.55	1	1	1.2	1.25	**1**
f_s ((MS/s))	0.02	0.1	1	1250	1000	**1.2**
Resolution	10	8	8	6	7	**8**
ENOB (@f_{in})	8.84	7.55	7.7	5.6	6.48	**7.66**
P_{diss} (μW)	0.206	0.9	8.8	32000	7200	**185**
FOM (fJ/cs)	22.4	48	42.3	800	80.65	**762**
Area (mm^2)	0.212	0.099	0.16	0.09	0.016	**0.06**
AE (μm^2/code)	462.62	531.1	787.74	1855.55	1792.44	**296.66**
C_u (fF)	65	20	15	5	4	**100**
C_{tot} (pF)	6.24	5.12	3.84	0.24	0.6	**1.6**

* Measured results @ Simulation results

of the two bits per cycle and/or programmable resolution SAR ADCs found in the literature. A lower FOM indicates higher power efficiency. It is worth noting that

the proposed ADC has the least area and the best area efficiency (lower the better).

The performance of the ADC at different resolutions is shown in Table 4.11. The maximum sampling rate at 4 bit resolution setting is found to be 2.38 MS/s while consuming a power of 132 μW. With 4 bit setting, the FOM is expected to degrade by a factor of 16 when compared to the 8 bit setting, with the same f_s. However, at low resolution the noise and linearity requirements are relaxed due to increased LSB. Therefore, f_s can be increased to gain on the FOM. It is found that with f_s set to 2.38 MS/s the degradation in FOM is found to be only 4.7 times for 4 bit operation. Please note, this is a significant improvement over 16x degradation expected from 8 bit to 4 bit resolution scaling by truncating the bits in conventional SAR ADCs for variable resolution mode.

4.7.1 Impact of modified V_{MID}, V_{TH1} and V_{TH2} generation circuits

To assess the impact of the modified circuit for V_{MID}, where the buffers are split to minimize the effect of parasistics, the V_{MID} generation with single buffer and with split buffer are simulated. For simulation V_{TOP} is set to $V_{CM} + \frac{V_{REF}}{2}$ and V_{BOT} is set to $V_{CM} - \frac{V_{REF}}{2}$ where $V_{REF} = V_{CM} = 0.5$ V i.e. $V_{TOP} = 0.75$ V and $V_{BOT} = 0.25$ V. This setting gives the maximum error for charge sharing in presence of parasitics.

Similarly, V_{TH1} and V_{TH2} values generated by the modified scheme is compared with that generated by the scheme outlined in Chapter 3 for $V_{TOP} - V_{BOT} = V_{REF}$ setting. The results are tabulated in Table 4.12 where the errors are quoted in LSB for 8 bit resolution.

It is evident that the modified circuit outclasses the first proposed method (in the prototype). However, it is also important to see how the error varies as the conversion progresses. For this, the ADC proposed in this chapter is simulated for two cases of V_{IN}, one for V_{IN} in the first quadrant and the other for V_{IN} in the fourth quadrant.

It is also important to see the error profile of the threshold voltages (V_{MID}, V_{TH1} and V_{TH2}) in the ADC during a conversion cycle. For two cases of inputs, first, V_{IN} in the first quadrant and the other V_{IN} in the fourth quadrant, the ADC is simulated and the error in threshold voltages during the 4 clock cycles of conversion cycle is obtained and plotted. Figure 4.26 and Figure 4.27 shows the error normalized to LSB in each cycle as the conversion progresses. It can be seen that the error is limited to

Table 4.10: Comparison with available low power binary weighted SAR ADCs in the literature.

Reference	Zeng et al. (2010)	Elkafrawy et al. (2015)	Kuo and Hsieh (2011)	Liu et al. (2016)	Sekimoto et al. (2011)	**This Work*** @
Technology (μm)	0.13	0.09	0.18	0.18	0.18	**0.09**
Supply Voltage (V)	1.2	1.8	0.9	1.8	1	**1**
f_s ((MS/s))	1	50	1	10	0.82	**1.2**
Resolution	10	10	9	12	8	**8**
ENOB (@f_{in})	8.39	7.2	8.38	10.8	7.41	**7.66**
P_{diss} (μW)	150	6000	7.16	820	30.9	**185**
FOM (fJ/cs)	2213	8161	8007	44.2	221	**762**
Area (mm^2)	0.18	0.4	0.48	0.359	0.128	**0.06**
AE (μm^2/code)	536.37	2720	1440.82	201.35	752.62	**296.66**
C_u (fF)	15	15	-	17.4	-	**100**
C_{tot} (pF)	15	1.4	-	31.6	-	**1.6**

@ Simulation results

less than 0.1 LSB even with small capacitances. It is to be noted that this error is due to the combined effect of the complete DAC circuit which includes error due to buffer settling, charge injection, clock feed-through and voltage dependent parasitics.

Resolution mode	4b	6b	8b
Maximum sampling frequency [MS/s]	2.38	1.6	1.2
SNDR@dc [dB]	25.49	37.64	48.57
SFDR@dc [dB]	35.53	50.36	60.96
ENOB@dc	3.94	5.96	7.77
SNDR@Nyquist [dB]	25.58	37.5	48.2
SFDR@Nyquist [dB]	34.76	50.13	54.2
ENOB@Nyquist	3.95	5.9	7.66
Power [μW]	132	161	185
FOM[fJ/conversion-step]	3588	1685	762
FOM[Variable resolution DAC]↑	4.7x	2.2x	1x
FOM[Fixed resolution DAC] ↑	16x	4x	1x

Table 4.11: Performance summary of ADC at different resolutions

Table 4.12: Impact of modified reference generation circuits

Threshold Reference	**Error (in LSB) from Circuit in Chapter 3**	**Error (in LSB) from Modified Circuit**
V_{MID}	1.55	0.1
V_{TH1}	1.35	0.125
V_{TH2}	1.12	0.12

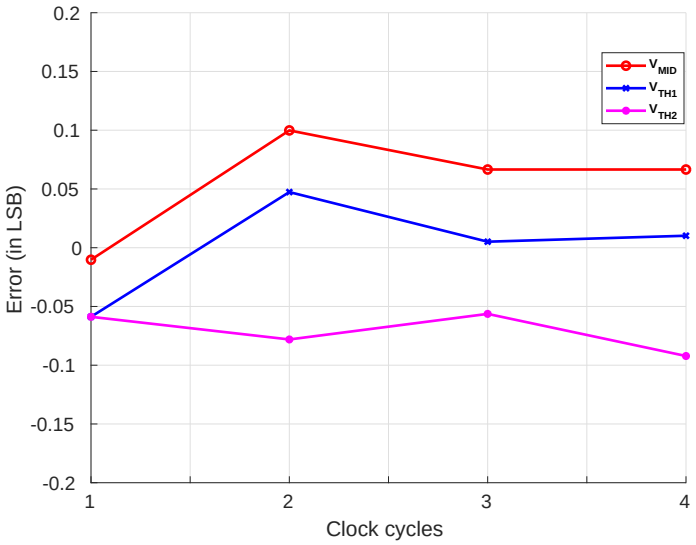

Figure 4.26: Error in threshold voltages generated in the ADC for V_{IN} in the first quadrant.

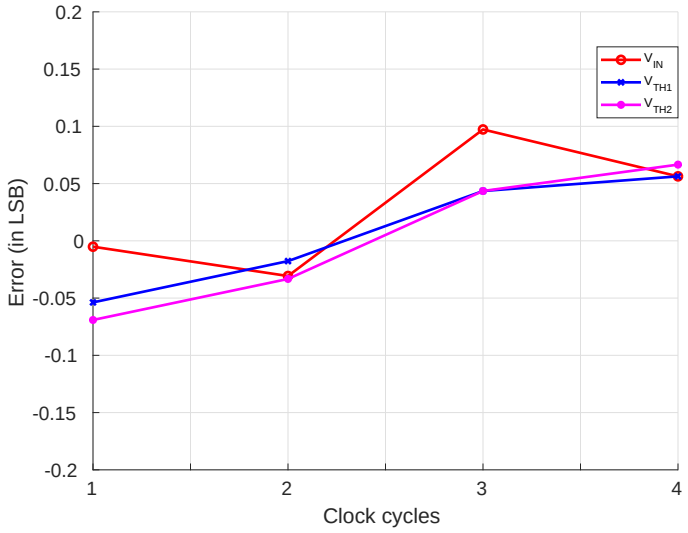

Figure 4.27: Error in threshold voltages generated in the ADC for V_{IN} in the fourth quadrant.

Chapter 5

A COMPACT 10 BIT NONBINARY WEIGHTED SWITCHED CAPACITOR INTEGRATOR BASED SAR ADC ARCHITECTURE

This Chapter proposes a SCI based approach for realizing nonbinary weighted SAR ADC. The proposed ADC has a very simple architecture for 1 bit per cycle operation requiring an OTA, a comparator and six equal sized capacitors regardless of the resolution. In addition, the digital logic requirement is very minimal with only three AND gates and a D-FF for serial output. This logic is independent of resolution since bits are taken serially.

Using the proposed method, a compact SC integrator based nonbinary weighted 10 bit SAR ADC is designed using 180 nm CMOS technology. The target specification of the proposed ADC is derived to suite typical instrumentation systems and data acquisition systems. The target specification is as follows.

Table 5.1: ADC target specification

Process Technology	180 nm
Power Supply	1.8 V
Conversion Rate	1 MS/s
Reference Voltage	1 V
Input Range	1 V
Resolution	10 bits

5.1 PROPOSED SAR ARCHITECTURE

The architecture of the proposed SAR ADC is shown in Figure 5.1. The idea is to sample the input onto a capacitor during the sampling phase and then remove/add the charges from that capacitor during the hold phase following the binary search algorithm. Therefore, in the hold phase the charge on the capacitor decreases in every cycle. Figure 5.1 shows the ADC for a differential input. The inputs V_{ip} and V_{im} are such that

$$V_{ip} = V_{CM} + \frac{v_i}{2} \tag{5.1}$$

$$V_{im} = V_{CM} - \frac{v_i}{2} \tag{5.2}$$

Where V_{CM} is the common-mode voltage and v_i is the differential input $(V_{ip} - V_{im})$.

Letting V_{refp} and V_{refm} as reference voltages as in (5.3) and (5.4) such that $V_{refp} - V_{refm} = V_{REF}$, the full scale value of the ADC.

$$V_{refp} = V_{CM} + \frac{V_{REF}}{2} \tag{5.3}$$

$$V_{refm} = V_{CM} - \frac{V_{REF}}{2} \tag{5.4}$$

The OTA along with the capacitors C_{intp}, C_{intm}, C_1, C_2, C_3 and C_4 and the associated switches form the DAC of the ADC. In the ADC designed, all capacitors are assumed to be equal. The algorithm followed is the following.

1. The conversion cycle starts with sampling and storing the inputs V_{ip} and V_{im}

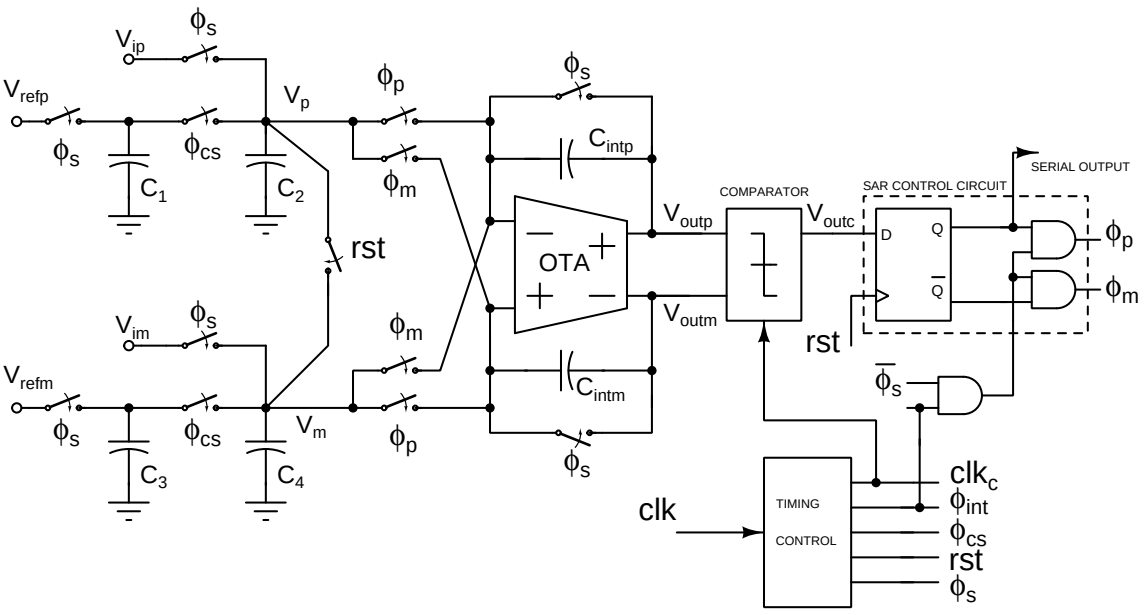

Figure 5.1: Schematic of proposed SCI based ADC

onto the integrating capacitors C_{intp} and C_{intm} respectively (note, these capacitors are equal in value). Simultaneously V_{refp} and V_{refm} are sampled on to C_1 and C_3 respectively.

2. In the subsequent cycles the binary weighted reference charges (generated by the charge sharing process between C_1, C_2 and C_3, C_4) are transferred to C_{intp} and C_{intm} with a polarity so as to continuously reduce the charge on them.

3. The comparator compares the integrated voltage and makes a decision on the bit under consideration.

4. The conversion stops when all the bits are resolved.

The SAR control logic generates the control signal for charge integration. Timing and control block generates the necessary timing signals for SCI block and SAR control logic block according to the successive approximation algorithm. The timing signals used for the ADC are shown in Figure 5.2. Details of the timing signal are given in Table 5.2

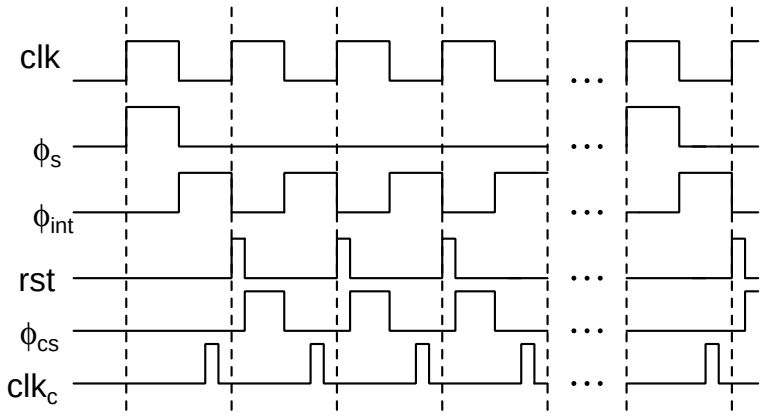

Figure 5.2: SAR timing control

Table 5.2: Details of timing control signals

Signal	Details
clk	ADC clock
ϕ_s	Sampling command
ϕ_{int}	Integration phase: During, HIGH, the charges are integrated on to the integrating capacitors.
ϕ_{cs}	Charge sharing phase : Reference charges are generated for integration during the following ϕ_{int} cycle.
rst	Resetting the charges before charge sharing.
clk_c	Command to comparator for comparing

5.2 OPERATION OF THE ADC

A step by step operation of ADC is explained as follows.

5.2.1 Sampling

Assuming all capacitors are initially discharged, ϕ_s raised to HIGH. The resulting equivalent circuit of the DAC is shown in Figure 5.3. V_{ip} and V_{im} are sampled on to C_2 and C_4 respectively. Simultaneously V_{refp} and V_{refm} are sampled on to C_1 and C_3 respectively. C_{intp} and C_{intm} are discharged to zero. The output of the integrator is $V_{outp} = V_{outm} = V_{CM}$ due to the common-mode feed back action of the OTA. The

sampling phase ends when ϕ_s goes 'LOW' (at the end of first *clk* 'HIGH' of the conversion cycle).

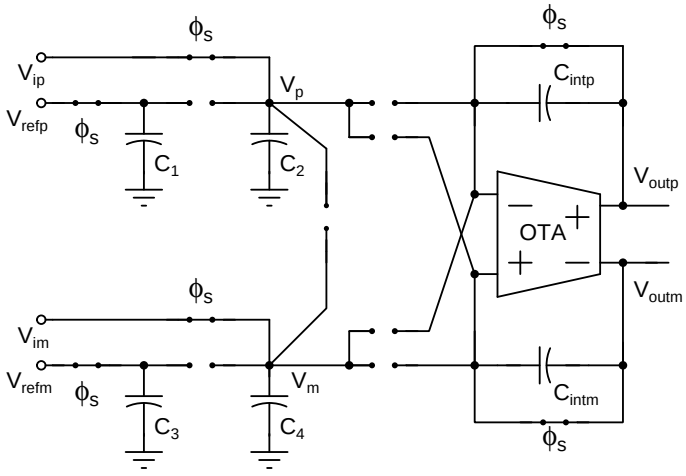

Figure 5.3: DAC equivalent circuit during the sampling phase

5.2.2 Charge integration and comparison

During the first ϕ_{int} 'HIGH' (of the conversion cycle), the SAR control logic block sets ϕ_m to '1' (since V_{outc} = logic '0' initially). The resulting equivalent circuit of the DAC is shown in Figure 5.4.

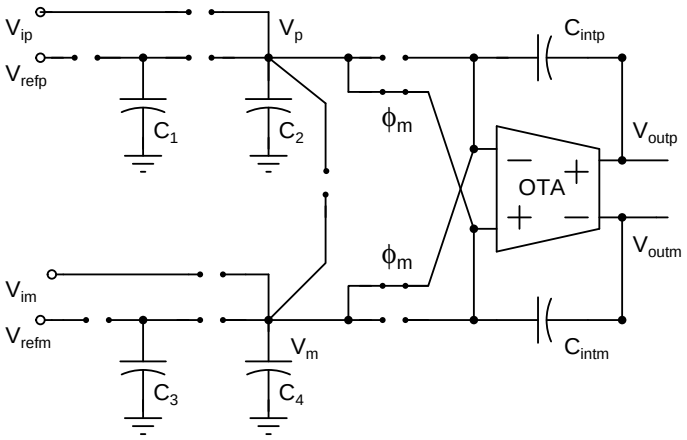

Figure 5.4: DAC equivalent circuit during the first ϕ_{int} phase

Signal component of V_{ip} and V_{im} (i.e. $+v_i/2$ and $-v_i/2$) are transferred (from C_2 and C_4) and integrated on to the respective integrated capacitors (C_{intp} and C_{intm}). Note the common-mode charge remains on C_2 and C_4.

Omitting the common-mode component in equations, for the ease of expression, and since the signal components of V_{ip} and V_{im} are 180° out of phase, it can be observed that $V_{outp} = -V_{im} = v_i/2$ and $V_{outm} = -V_{ip} = -v_i/2$. Note that integration gain is considered as unity since all capacitors are assumed equal. For a fully differential operation, one can write,

$$V_{out,diff} = (V_{outp} - V_{outm}) = v_i \tag{5.5}$$

At the end of this phase the comparator is enabled to decide upon MSB. If differential output of the integrator $V_{out,diff}$ is positive, V_{outc} becomes '1' else '0'.

5.2.3 Reset phase (rst)

This is a very short duration interval between the end of the integrating phase and before the charge sharing phase. At the end of the integrating phase, there is every chance that charges may be left over on C_2 and C_4 due to the finite gain of the OTA. These charges, if not removed, will be carried forward to the remaining cycles during the conversion, corrupting the reference voltages and degrading the ADC linearity. To mitigate this, residue charges are reset by connecting C_2 and C_4 in parallel to each other. The result is that the signal dependent charge on these capacitors are cancelled leaving behind only the common-mode charge.

5.2.4 First charge sharing phase

When ϕ_{cs} goes high, the capacitors C_1 and C_3 are put in parallel with C_2 and C_4 respectively. The charges on C_1 and C_3 are shared equally with C_2 and C_4 which had been discharged to common-mode during the rst phase. The result of the charge sharing is that $V_p = V_{REF}/4$ and $V_m = -V_{REF}/4$.

5.2.5 Second integrating phase

In the second (and in subsequent) integrating phases, V_p is either integrated on to C_{intp} or C_{intm} based on the comparator output of the previous cycle (i.e. the bit resolved during the last cycle). The same is true for the transfer of V_m also.

5.2.5.1 Case - 1: V_{outc} = '1' in the first cycle

If in the first cycle, V_{outc} = '1' (i.e. MSB = 1), it implies that $v_i > V_{REF}/2$. This means, the charge on the left plate of C_{intp} is negative and therefore should be decreased in order to decrease the voltage across C_{intp}. Similarly the opposite should happen to C_{intm}. To achieve this, positive charges are added available in C_2 i.e. V_p $(= V_{CM} + V_{REF}/4)$ is connected to the inverting terminal of the OTA. Similarly, C_4 is connected to the non-inverting terminal of the OTA for transferring its charge to C_{intm}. In other words, V_p and V_m are connected to OTA using the switches ϕ_p and the resulting equivalent circuit is as shown in Figure 5.5.

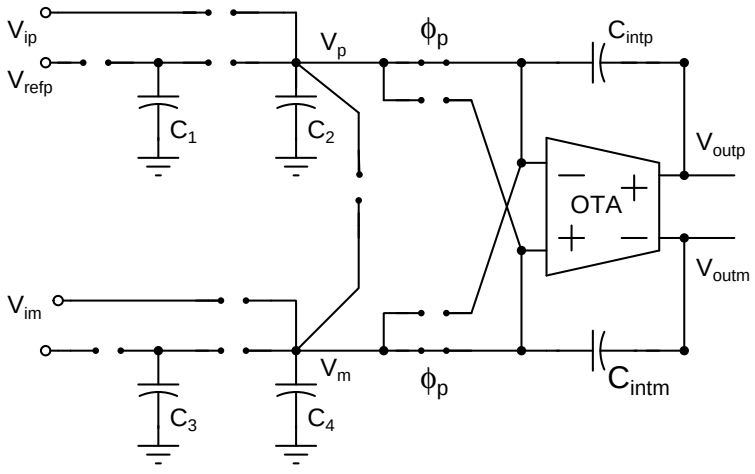

Figure 5.5: Second ϕ_{int} phase, V_{outc} = '1' (MSB)

The resulting output of the OTA are expressed in the following equations.

$$\begin{aligned} V_{outp} &= -V_{im} - V_p = -V_{im} - \frac{V_{refp}}{2} \\ &= \frac{v_i}{2} - \frac{V_{REF}}{4} \end{aligned} \tag{5.6}$$

$$\begin{aligned} V_{outm} &= -V_{ip} - V_m = -V_{ip} - \frac{V_{refm}}{2} \\ &= -\frac{v_i}{2} + \frac{V_{REF}}{4} \end{aligned} \tag{5.7}$$

Effectively the differential output of the OTA is given as

$$V_{out,diff} = v_i - \frac{V_{REF}}{2} \tag{5.8}$$

5.2.5.2 Case - 2: V_{outc} = '0' in the first cycle

If V_{outc} = '0' (i.e. MSB = 0), it implies that $v_i < V_{REF}/2$. To resolve the next bit, the charge on left plate of C_{intp}, which is positive, should be decreased in order to decrease the voltage across C_{intp}. Similarly the opposite should happen to C_{intm}. Therefore, negative charges available in C_4 are transferred to C_{intp} by connecting it to the inverting terminal of the OTA. Similarly, C_2 is connected to the non-inverting terminal of the OTA. In other words, V_p and V_m are cross connected to the OTA using the switches ϕ_m and the resulting equivalent circuit is as shown in Figure 5.4. The resulting output of the OTA are expressed in the following equations.

$$\begin{aligned} V_{outp} &= -V_{im} - V_m = -V_{im} - \frac{V_{refm}}{2} \\ &= \frac{v_i}{2} + \frac{V_{REF}}{4} \end{aligned} \tag{5.9}$$

$$\begin{aligned} V_{outm} &= -V_{ip} - V_p = -V_{ip} - \frac{V_{refp}}{2} \\ &= -\frac{v_i}{2} - \frac{V_{REF}}{4} \end{aligned} \tag{5.10}$$

Effectively the differential output of the OTA is given as in (5.11). Note that since V_{REF} is always positive and $v_i < 0$ in case - 2, $V_{out,diff}$ moves towards zero from the

value it had in the first cycle as given in (5.5).

$$V_{out,diff} = v_i + \frac{V_{REF}}{2} \tag{5.11}$$

5.2.6 Subsequent cycles

In the next comparison phase ϕ_{cs} , the next MSB is resolved. The process is continued by sharing the charges remaining in C_1, C_3 on to C_2, C_4 respectively. This process of charge sharing and integration of these charges on to the appropriate integrating capacitor happens until all bits are evaluated. $V_{out,diff}$ continuously decreases and converges towards zero at the end of conversion.

The charge sharing process is made parasitics insensitive by matching parasitic at the charge sharing nodes using dummy switches.

5.3 BUILDING BLOCKS OF SWITCHED CAPACITOR INTEGRATOR SAR ADC

5.3.1 OTA

In the proposed architecture, it can be noticed that both the input and reference voltages are transferred through identical paths i.e. $C_2(C_4)$ to C_{intp}/C_{intm}. Therefore, both the input and the references experience the same gain. Since integrating capacitors store charge corresponding to the difference in input and reference levels, the comparator has to decide whether $V_{out,diff}$ is positive or negative. Therefore, the gain error of the closed loop OTA does not have a significant impact as long as the differential path is symmetric. This relaxes the requirement on the OTA gain. However, a gain in excess of 60 dB is a good choice. But, UGB of the OTA is still an important parameter since it decides the OTA settling. The settling error of the OTA output during ϕ_{int}, considering the worst case where the output of the OTA has to swing from V_{CM} to $\pm V_{REF}/2$, can be written as

$$v_{error}(t) = \frac{V_{REF}}{2} e^{-2\pi\, t\, f_u} \tag{5.12}$$

Where f_u is the UGB of the OTA in Hz. If the permissible settling error is computed as a fraction of LSB, then for an N bit ADC, a settling time of t_{set} and error of $\left(\frac{1}{2^\beta}\right)^{\text{th}}$ of LSB the equation (5.12) can be written as

$$\frac{V_{REF}}{2^{N+\beta}} = \frac{V_{REF}}{2} e^{-2\pi\, t_{set}\, f_u} \tag{5.13}$$

Solving (5.13), the requirement on the UGB can be written as

$$f_u = \frac{1}{2\pi t_{set}}\, ln(2^{N+\beta-1}) \tag{5.14}$$

For a 10 bit operation at 1 MS/s speed, the clock period requirement is ≈100 ns, out of which ϕ_{int} is given 50 ns. The OTA has to settle before the comparator is triggered for resolving the bit. Allotting 15 ns for comparator decision, 35 ns is left for OTA settling. Out of this, 15 ns is budgeted for OTA slewing and the remaining 20 ns for settling due to bandwidth limit. With this requirement, to limit the settling error to less than $\left(\frac{1}{16}\right)^{\text{th}}$ of the LSB (i.e. $\beta = 4$), the requirement on UGB is found to be at least 66 MHz.

In order to improve the dynamic range and noise performance, a fully differential OTA is designed for SCI based ADC as shown in Figure 5.6. The two stage OTA has cascode differential amplifier as first stage and a common source second stage. Transistors M_1- M_8 form first stage differential amplifier with cascoded NMOS device and PMOS current source load. Gate bias of PMOS current source load is controlled by a common mode feedback (CMFB) circuit. PMOS common source second stage provides additional gain for the OTA. Both input and output common mode voltages of the OTA is fixed at 0.9 V. Output common mode voltage at the second stage of the OTA is compared with reference common mode voltage of 0.9 V using the error amplifier formed by M_{19}- M_{24} to obtain V_{cmfb} voltage for the first stage. A simple Miller RC compensation is used to stabilize the OTA for closed loop operation.

Table 5.3 shows the transistor sizes of the OTA. Differential operation takes care of the offset voltage due to signal independent channel charge injection. The clock phases are appropriately delayed to minimize channel-charge injection.

An autozeroing technique (Enz and Temes 1996) is employed to cancel the OTA offset, the schematic of which is shown in Figure 5.7. The circuit essentially stores the OTA offset voltage on to a capacitor C_{OS} during signal sampling phase (ϕ_s). During

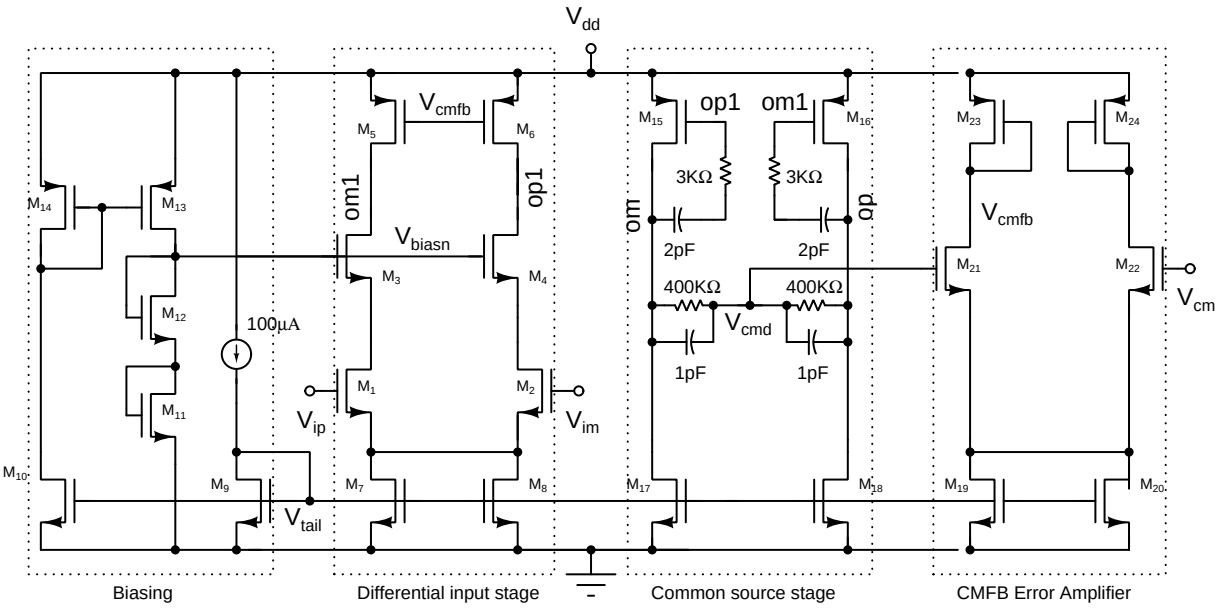

Figure 5.6: Schematic of OTA used for SCI ADC

Table 5.3: Sizes of transistors for OTA

Transistors	$\left(\frac{W}{L}\right)$F
M_1, M_2, M_3, M_4	$\left(\frac{2}{0.6}\right)$ 16
M_5, M_6, M_7, M_8, M_9, M_{10}, M_{17}, M_{18}	$\left(\frac{2}{0.6}\right)$ 32
M_{11}, M_{12}, M_{13}, M_{14}	$\left(\frac{2}{0.6}\right)$ 4
M_{15}, M_{16}	$\left(\frac{2}{0.6}\right)$ 64
M_{19}, M_{20}, M_{23}, M_{24}	$\left(\frac{2}{0.6}\right)$ 8
M_{21}, M_{22}	$\left(\frac{2}{0.6}\right)$ 4

W and L are width and length in μm.

F is the number of fingers.

the remaining part of the conversion period, C_{OS} is connected in series with the input terminals of the OTA to cancel the effect of offset.

Figure 5.8 shows the frequency response of the two stage OTA for a load capacitance of 200 fF. The overall DC gain obtained is 75.1 dB for typical process corner with unity gain bandwidth of 84 MHz. The gain margin and phase margin are found to be 5.4 dB and 63.6° respectively.

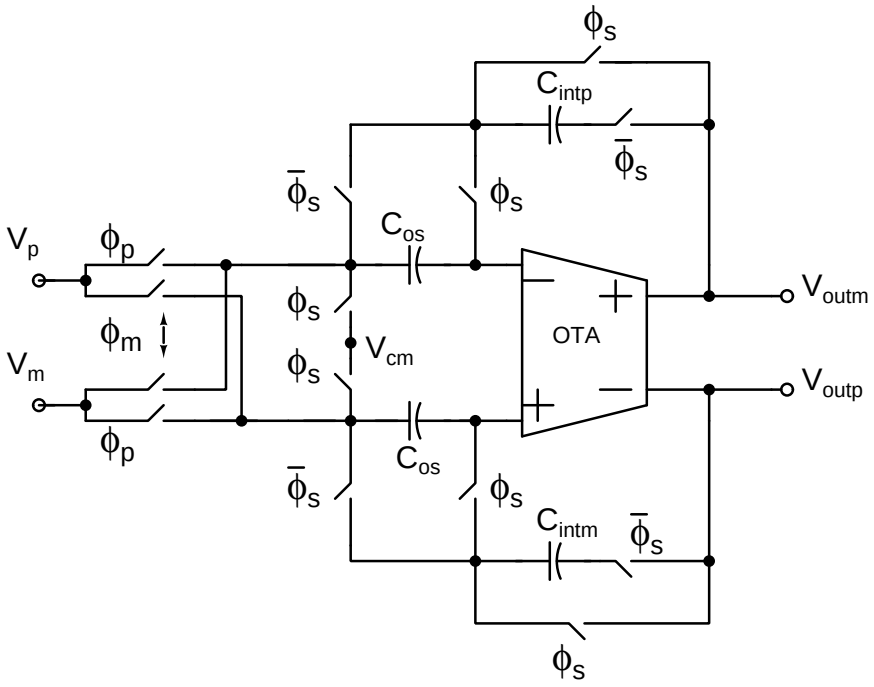

Figure 5.7: Schematic of offset correction in OTA

The overall performance parameters of OTA are listed in Table 5.4.

Table 5.4: Performance summary of low power OTA.

Performance metric	**Value**
DC Gain [dB]	75.1
UGB (MHz)	84
Gain margin [dB]	5.4
Phase margin [deg]	63.6
Power dissipation [μW]	16

5.3.2 Comparator

Schematic of the dynamic latch based comparator used in this work is shown in Figure 5.9.

The dynamic latch consists of pre-charge transistors M_9 and M_{10}, cross-coupled inverter M_5-M_8, differential pair M_1, M_2 and tail current source formed by M_3 and

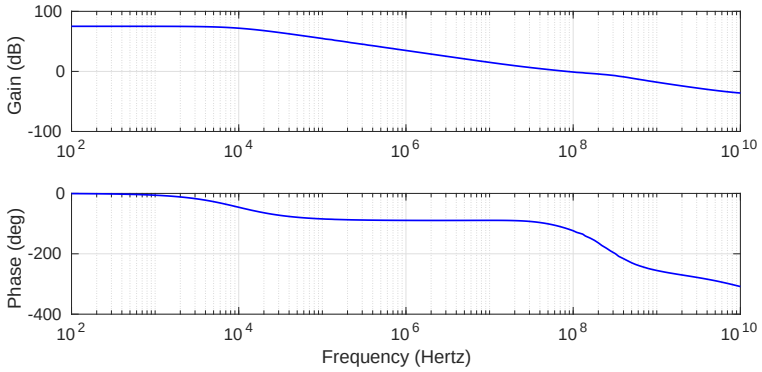

Figure 5.8: Frequency response of low power OTA with compensation.

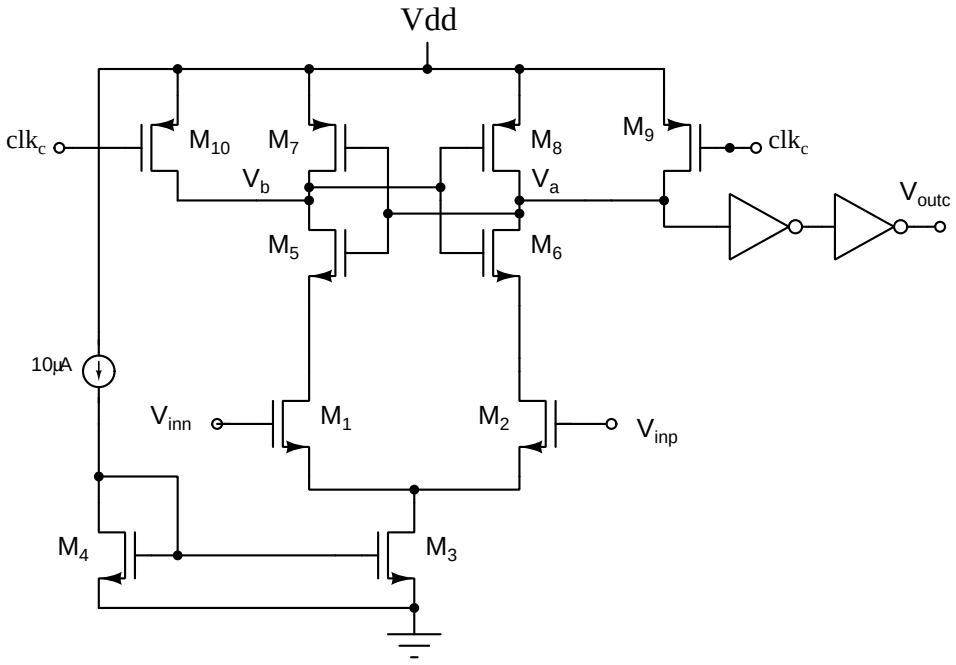

Figure 5.9: Schematic of comparator

M_4. When the clk_c signal is low, the drain voltages of M_1 and M_2 are $V_{DD} - V_T$ and their source voltage is V_T below the latch input common mode voltage. Therefore,

once clk_c goes high, the NMOS transistors M_1, M_2, M_5 and M_6 immediately go into the active region and the output nodes V_a and V_b slew towards ground at unequal rates decided by the input differential voltage. Table 5.5 shows the sizes of all the transistors of the comparator.

Table 5.5: Sizes of transistors for comparator

Transistors	$\left(\frac{W}{L}\right)$F
M_1, M_2, M_3, M_4	$\left(\frac{0.5}{0.18}\right)$ 4
M_3, M_4	$\left(\frac{2}{0.5}\right)$ 12
M_5, M_6	$\left(\frac{0.24}{0.18}\right)$ 2
M_7, M_8	$\left(\frac{1.2}{0.18}\right)$ 8
M_9, M_{10}	$\left(\frac{1.2}{0.18}\right)$ 4

W and L are width and length in μm.

F is the number of fingers.

The smallest voltage which the comparator is expected to resolve is the smallest output of the OTA which $\pm\frac{\text{LSB}}{2}$. For a 10 bit operation with V_{REF} = 1 V the LSB is ≈0.98 mV. The comparator designed in this work is capable resolving voltage less than $\pm 1\,\mu$V. The power consumption of the comparator is 11.23 μW. With a careful device matching during layout as well by a slight over design, the offset calibration is avoided.

5.3.3 SAR Control logic

The proposed ADC has a very simple SAR control logic. A D-Flip-flop (D-FF) and three AND gates are the only logic components. This is because the control logic does not require information on all the bits resolved in the previous clock cycles during the conversion. Instead, it only requires one bit which is resolved in the last clock cycle. It can be seen that only two control signals ϕ_p and ϕ_m are required to be derived from the bit generated for controlling SC-DAC during the conversion. As already explained, when V_{outc} of the comparator is '1', ϕ_p is to be asserted HIGH during ϕ_{int} and when V_{outc} is '0', ϕ_m is to be asserted HIGH. The schematic of the SAR control logic is already shown in Figure 5.1. The D-FF latches V_{outc} at the end of comparison

(negative edge of clk_c). The output Q and $\overline{Q}$ of the D-FF are used to derive ϕ_p and ϕ_m.

5.4 SIMULATION RESULTS

The proposed fully differential SCI based SAR ADC has been designed in UMC 180 nm CMOS process to operate on 1.8 V supply. The ADC has input voltage swing of 1 V peak to peak with a common mode voltage of 0.9 V. The ADC layout is shown in Figure 5.10 and area occupied is 0.05 mm^2 (267 μm X 188 μm).

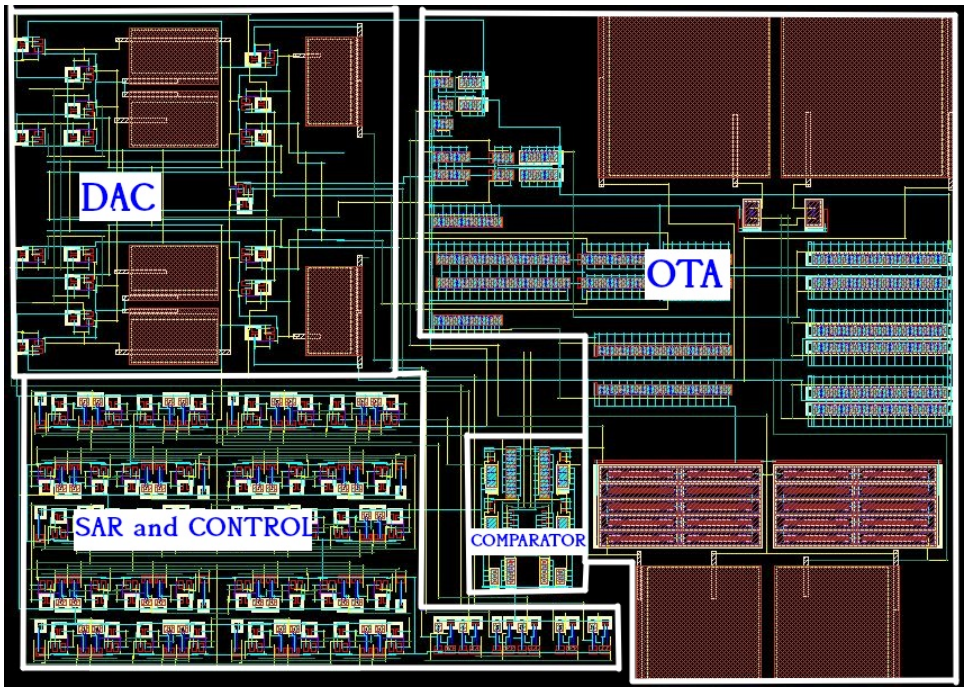

Figure 5.10: Layout diagram of SCI ADC

The simulation results shows that, the ADC achieved a conversion speed of 0.9 MS/s for 10 bit operation. The total capacitance used in the DAC is $6\,C$ where, C is the unit capacitor of value 300 fF. The unit capacitor of this order is used to limit the thermal noise at the output of the integrator. Compared to conventional charge redistribution DAC architecture which requires $1024\,C$ for 10 bit resolution, this DAC offers large savings in terms of area, headroom on capacitor mismatch and parasitic

requirements. On the other hand, in a conventional SAR ADC, if the total capacitance is taken to be 1.8 pF (i.e. 300 fF × 6), the unit capacitor required for a 10 bit operation will amounts to 1.78 fF. Note that the parasitics at a given node, in the capacitor array, itself can be comparable or more than this value.

Figure 5.11 illustrates how the output of the OTA converges towards zero during the conversion cycle. The plot is given for an analog input corresponding to an output code of 799.

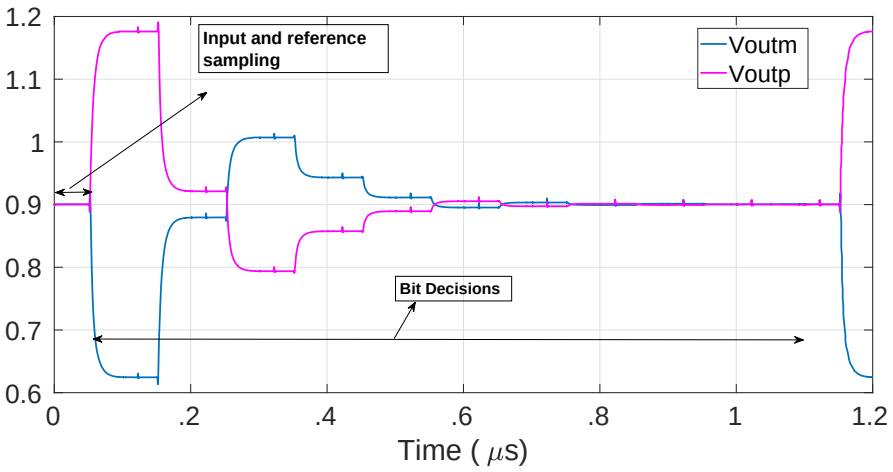

Figure 5.11: OTA output for analog input corresponding to output code of 799

From static performance of the ADC (code density test) in 10 bit, DNL and INL of the ADC at 0.9 MS/s sampling speed is found to be within 0.3 LSB/−0.6 LSB and 0.7 LSB/ −0.1 LSB respectively and is shown in Figure 5.12 & Figure 5.13 respectively.

The output spectrum of the ADC for an input full-scale sine wave at 10.65 KHz (near DC) and 450.9 KHz (at Nyquist) are shown in Figure 5.14 & Figure 5.15, for which the SNDRs of 61.7 dB (ENOB = 9.95) and 59.02 dB (ENOB = 9.5) are obtained, respectively.

The SNDR and SFDR performance of the proposed ADC for input in the range DC to Nyquist frequency at 0.9 MS/s is shown in Figure 5.16. The SNDR is found to be minimum at Nyquist rate. The ENOB is found to vary from 9.5 at Nyquist to 9.9 at near DC.

The total power consumed by the ADC is 734 μW, at 1.8 V supply. The major share of the power is taken by the OTA which is 568 μW. Comparator consumes

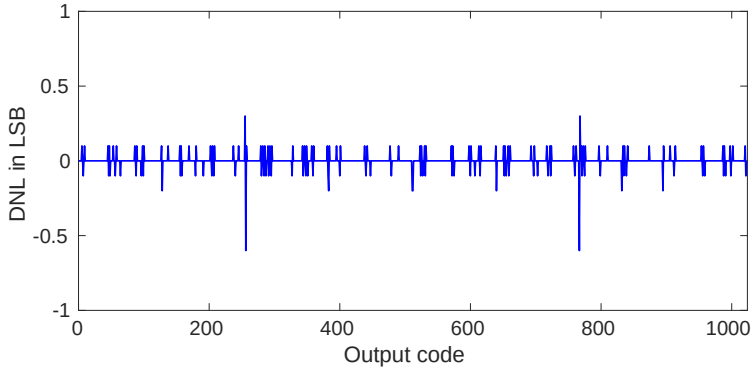

Figure 5.12: DNL error

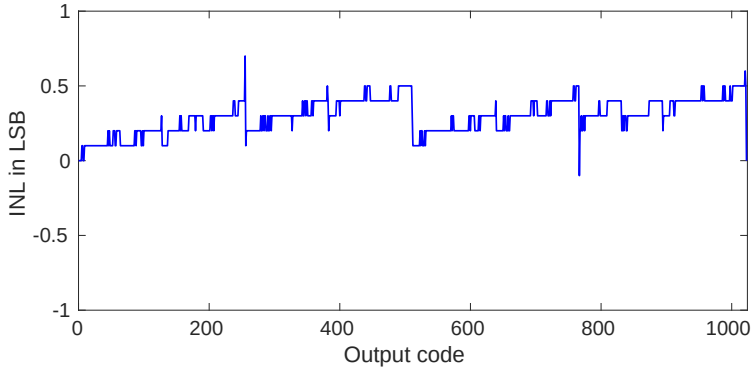

Figure 5.13: INL error

154 μW and the digital circuit consumes 12 μW. However, with a careful design, the OTA power can be reduced further. To verify ADC performance against mismatches, Monte Carlo simulations of 100 runs are carried on the extracted net list. Figure 5.17 shows the histogram plot of SNDR variations. The mean and sigma values of SNDR are 58.18 dB and 1.7 dB respectively.

ADC performance for various process corners is given in Table 5.6. The ENOB offered by the ADC is found to be 9 or above in all cases.

SNDR performance of the ADC against the supply voltage variation of $\pm 10\%$ over the nominal and temperature variation in the range $0 - 70$°C is shown in Table 5.7 and Table 5.8 respectively. The ENOB performance is found to be 9 or better.

The proposed SCI based SAR ADC performance is compared with some of the nonbinary weighted SAR ADCs in the literature and is listed in Table 5.9. The ADCs

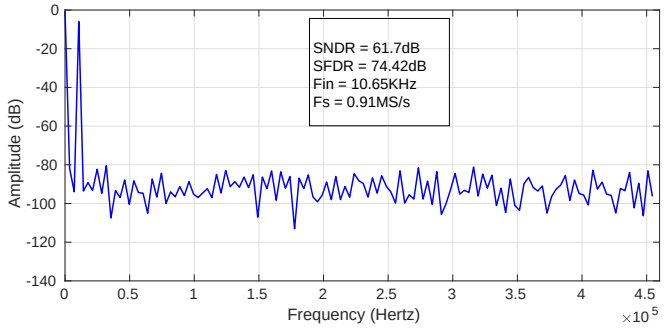

Figure 5.14: FFT spectrum of 10 bit ADC for an input frequency of 10.65 KHz

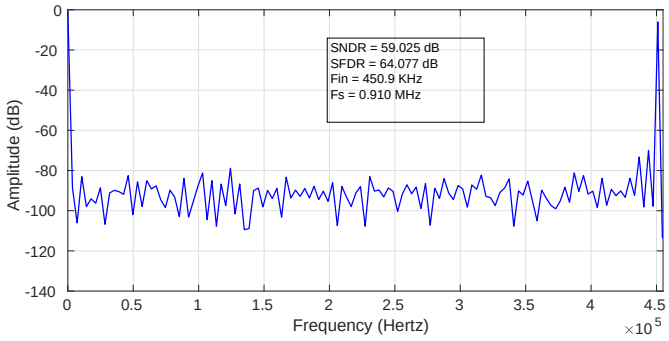

Figure 5.15: FFT spectrum of 10 bit ADC for an input frequency of 450.9 KHz

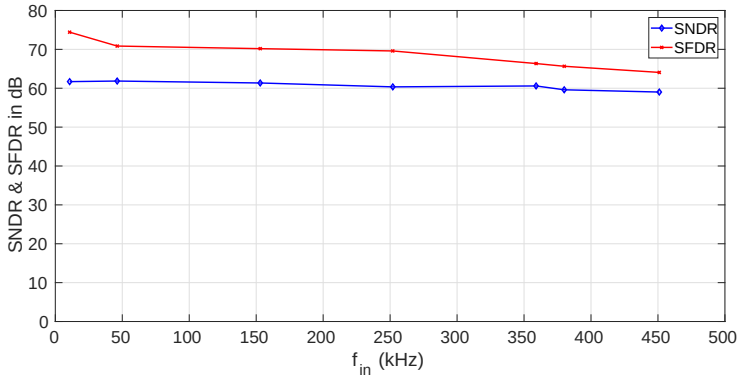

Figure 5.16: SNDR/SFDR as function of input frequency at $f_s = 0.9$ MHz

are compared using two metrics, FOM and AE. The FOM and AE are computed using the formula given in (1.1) and (1.2). It can be seen that the proposed SAR ADC has a FOM comparable with some of the state of the art SAR ADCs. A lower FOM

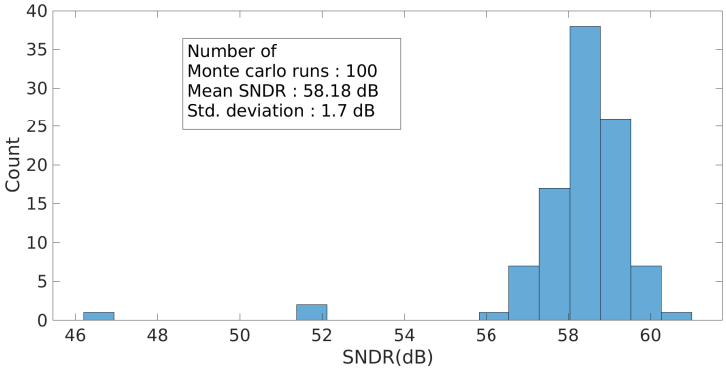

Figure 5.17: Mean and sigma SNDR against mismatch in OTA

Table 5.6: SNDR in dB of ADC over different process corners

SNDR	**tt**	**ff**	**ss**	**snfp**	**fnsp**
@DC	61.7	58.15	58.68	59.78	60.2
@Nyq.	59.02	57.22	57.1	58.59	55.75

Table 5.7: Performance of ADC over different supply voltage

Parameter	**1.62 V**	**1.8 V**	**1.98 V**
SNDR(dB)@DC	60.29	61.7	59.78
SNDR (dB)@Nyquist	55.24	59.02	58.02

Table 5.8: Performance of ADC over different temperature

Parameter	**0°C**	**27°C**	**70°C**
SNDR(dB)@DC	58.86	61.7	59.95
SNDR (dB)@Nyquist	57.83	59.02	58.79

indicates higher power efficiency. Moreover the designed ADC occupies a small area as compared to all the ADCs listed. It is worth noticing that the proposed ADC outperforms the other ADCs in terms of AE with a factor of 2.5 to 11.

Table 5.9: Comparison with available low power, low voltage nonbinary and binary weighted SAR ADCs in the literature.

Reference	Shi et al. (2018)*	Saisundar et al. (2012)*	Otfinowski et al. (2011)@!	Zeng et al. (2010)@	Seongik and Minwoong (2017)*!	Hong et al. (2015)*	Li et al. (2020)@	Polineni et al. (2020)*!	**This Work***!
Technology (μm)	0.18	0.18	0.18	0.13	0.18	0.045	0.13	0.18	**0.18**
Supply Voltage (V)	1.5	1.8	1.8	1.2	5	1.25	1.2	1.8	**1.8**
f_s (MS/s)	0.128	1	3	1	0.1	1000	30	0.002	**0.91**
Resolution	13	10	10	10	9	7	12	11	**10**
ENOB (@f_{in})	12.8	9.4	9.5	8.39	8.63	6.48	11.08	10.14	**9.5**
P_{diss} (μW)	74.2	131	465	147.6	2035	73000	2390	0.28	**734**
FOM (fJ/cs)	81.2	193	214	2170	256000	80	39.45	120	**924.7**
Area (mm^2)	0.25	0.24	0.066	0.18	0.316	0.16	0.273	0.17	**0.05**
AE (μm^2/code)	480.08	480.24	104.7	536.57	797.62	1792.4	126.11	150.66	**69.32**
C_u (fF)	4000	20	27	15	2000	5	-	-	**300**
C_{tot} (pF)	24	5.12	-	15	13	0.6	-	-	**1.8**

* Nonbinary SAR ADC @ BWC array DAC SAR ADC ! Simulation results

Chapter 6

CONCLUDING REMARKS AND FUTURE WORK

6.1 CONCLUSIONS

The research work presented in this dissertation lead to the development of a novel Nyquist rate SAR ADC architecture with two new DAC architectures and an algorithm implementation for the SAR ADC using only few unit capacitors. The power and area efficiency of both the architectures were simulated and characterized using CMOS technology. By achieving low power and lowest area utilization with reasonably good sampling rate, this ADC structure opens the door for new opportunities in various applications such as portable data acquisition systems and modern instrumentation systems.

Various ADC architectures are investigated in this work with the objective of achieving good AE and PE. At the same time SAR ADC architecture which is suitable for low power application is studied. To achieve low power with enhanced sampling rate a 2 bit per cycle SAR ADC with new area efficient DAC architecture is introduced in this work. This ADC structure trades affordable power to speed to reach better balance among speed, power, area as well as resolution and exhibits low power at a good sampling rate.

A low power 8 bit SAR ADC is implemented in 180 nm technology. The designed ADC consumes 1.8 mW power from 3.3 V supply for low frequencies. The power in-

creased to 2 mW at Nyquist frequency. Charge recycle based 2 bit per step conversion is employed to achieve 500 kS/s conversion speed. An ENOB of 7.52 was obtained when operated at Nyquist rate.

A 4-8 bit programmable resolution, 2 bit per cycle SAR ADC has been presented. The ADC uses a DAC whose architecture is resolution independent which has made the ADC programmability almost trivial. The proposed DAC architecture used a few NBW capacitors and therefore, there is an area advantage over the conventional BWC array architecture. Though the buffers required for the DAC demanded a higher power, with a careful design of buffers, the overall efficiency is maintained on par with the existing 8 bit architectures. The DAC architecture proposed is largely parasitic independent. Post layout simulation results of the ADC designed in 90 nm CMOS process operating on 1 V supply offered an ENOB of 7.77 at near DC for an 8 bit setting while it was 3.94 in 4 bit mode at DC. Degradation in FOM is only 4.7X for a resolution change from 8 bit to 4 bit when compared to 16X offered by truncating the bits. The performance of ADC is tested against PVT variations for the highest resolution mode and the ENOB is found to be satisfactory.

An area efficient 10 bit nonbinary weighted SAR ADC is presented. The ADC has SCI DAC implemented with only six unit capacitors and is area efficient over the conventional BWC architecture. Though this architecture requires OTA, resulting overall efficiency is maintained on par with the existing 10 bit architectures. The DAC architecture proposed is resolution independent and also largely parasitic insensitive. Even the ADC can be made programmable for any resolution up to 10 bits by appropriately generating reset pulse based on resolution selection. The simulation results of the ADC designed in 180 nm CMOS process operating on 1.8 V supply offered an ENOB of 9.9 at near DC and 9.5 at Nyquist frequency. The performance of ADC is tested against PVT variations and the ENOB is found to be 9 bits and above. The proposed ADCs are suitable for modern instrumentation systems and data acquisition systems.

Performance of all three ADC architectures (Chapter 3, 4, 5) are summarized in Table 6.1.

Table 6.1: Performance summary of all three ADC architectures

Parameter	**Prototype ADC**	**Progm. ADC**	**SCI ADC**
Technology (μm)	0.18	0.09	0.18
Supply Voltage (V)	3.3	1	1.8
Resolution (Bit)	8	4 to 8	10
Sampling Frequency (MS/s)	0.5	1.2	0.91
ENOB @ f_{in}	7.52	7.66	9.5
Total Power	1.8 mW	185 μW	735 μW
FOM (fJ/c-s)	-	762	924.7
Area (mm^2)	-	0.06	0.05

6.2 FUTURE WORK

- Though the two proposed DAC architectures are area efficient, PE can be improved further by careful design of individual blocks. In this work design effort is fully concentrated to develop a new DAC architecture and algorithm so that it functions most linearly. A few power saving techniques (Gambini and Rabaey 2007, Kamalinejad et al. 2011) can be incorporated to further improve PE.

  High speed comparator with associated offset calibration and with advanced nanometer CMOS technology, these ADC architectures can be more competitive when compared to other ADC topologies in terms of area, speed and resolution.

- Two bit per step evaluation concept can be extended to SCI based 10 bit SAR ADC to further improve the conversion speed. The single bit per step algorithm can be modified to evaluate two bit per step by incorporating two SCI based DACs namely signal DAC (SIG-DAC) and reference DAC (REF-DAC) (Hong et al. 2015). By adopting noise shaping concept (Shi et al. 2018, **?**), SNDR of 10 bit SCI ADC can be enhanced further.

- These designs can be used to obtain a high speed time interleaving architecture by connecting several ADCs in a parallel structure.

- Both the designs can be fabricated and tested to make sure it functions well on silicon.

Appendix I

ADC Figure of Merit

A-1 Basics of analog to digital conversion

Analog to digital conversion can be separated into two distinct operations: *sampling* and *quantization*. Sampling converts a continuous time, continuous amplitude analog signal into a discrete time, continuous amplitude signal, while quantization converts the continuous amplitude of this sampled signal into a set of discrete levels. Figure A.1 shows the principle of analog to digital conversion (Waltari and Halonen 2002).

If the ADC is able to convert the analog input into N bit digital code, then N is said to be the *resolution* of the ADC. The least voltage the ADC can resolve is given by (A.1)

$$LSB = \frac{V_{FS}}{2^N} \qquad \text{(V)} \tag{A.1}$$

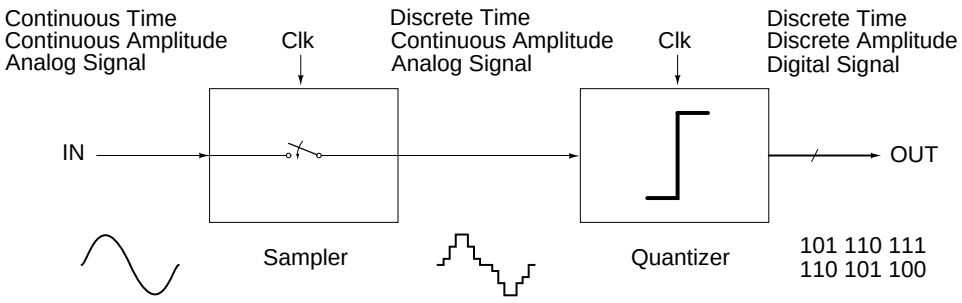

Figure A.1: Principle of analog to digital conversion.

where LSB refers to *least significant bit*, the voltage equivalent of least significant bit of digital code and V_{FS} is the full-scale voltage of the ADC.

A-2 ADC Figure of merit

The quality of an ADC is measured by both its static or DC performance and its dynamic or AC performance. Static properties are easily measured and are typically used as an indication of the dynamic performance.

An ADC might contain non-idealities like *offset error, gain error, integral non linearity (INL) and differential non linearity (DNL)*. The key to understanding the static performance of ADCs is to compare the ideal and actual transfer characteristics for DC signals. Static errors usually arise due to mismatch in circuit components and non-symmetry in the IC layout. The different forms of static error to be expected in an ADC realization are explained briefly in the following. The dynamic metrics include the likes of *signal to noise ratio (SNR), signal to quantization noise ratio (SQNR), signal to noise and distortion ratio (SNDR), spurious free dynamic range (SFDR), effective number of bits (ENOB)* etc.

The dynamic performance of an ADC is obtained by examining its AC characteristics when a spectrally pure sine wave is applied to the input. This is best done by performing an FFT on the output data and examining the spectrum for noise and distortion. The most important static and dynamic specifications are explained briefly in the following.

- *Offset error:* Offset error is the difference between the actual input and the ideal input where the output code jumps from '0' to '1'. The offset error can be positive or negative. Offset must be removed from the actual output before calculating gain error.

- *Gain error:* Gain error is the difference between the actual input and the ideal input where the output code jumps from $(2^N - 2)$ to $(2^N - 1)$ as shown in the Figure A.2.

- *Differential non linearity (DNL):* In an ideal ADC, any two adjacent output codes will be triggered by analog inputs which differ by 1 LSB. In an actual

ADC, the inputs may differ by more than 1 LSB for some adjacent codes and less than 1 LSB for some other. Any deviation from the ideal 1 LSB is called DNL of the higher code. It is important that the ADC produces no missing codes in order to guarantee monotonic behavior. This implies the maximum DNL error must always be less than ±1 LSB.

- *Integral non linearity (INL):* INL is the cumulative DNL. It is equal to the the deviation of actual input, from the ideal input trigger for that code as in Figure A.3.

  Since different ADCs work on different V_{DD} and have different resolution, these non idealities of an ADC are normalized with the LSB of that ADC.

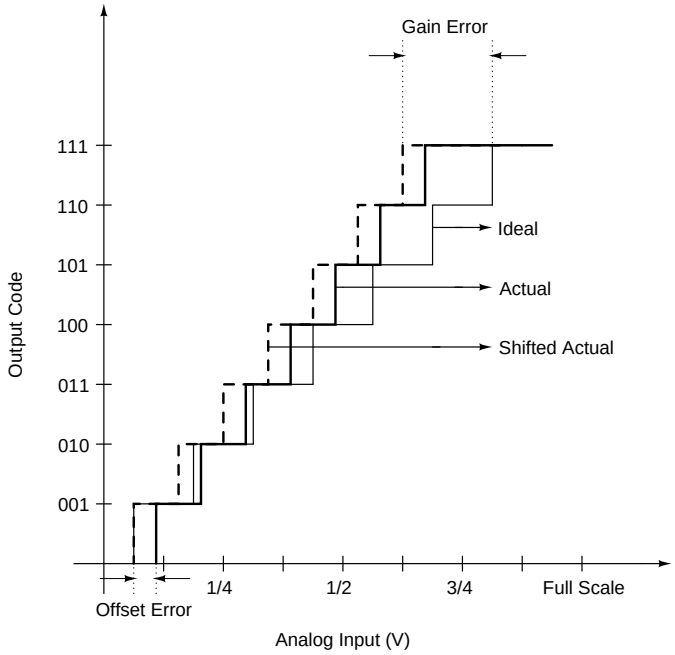

Figure A.2: Static non idealities of ADC: offset error and gain error

- *Signal to noise ratio (SNR), signal to quantization noise ratio (SQNR), signal to noise and distortion ratio (SNDR), effective number of bits (ENOB):* Whenever ADC quantizes the input voltage into discrete levels, it introduces an error called quantization error, V_q. This is the difference between the actual signal and the corresponding digital representation of that value. This error is, often, treated as noise due to its uniform amplitude distribution and flat spectral density. Because of this, there is a fundamental limit to the SNR of the ADC. When no

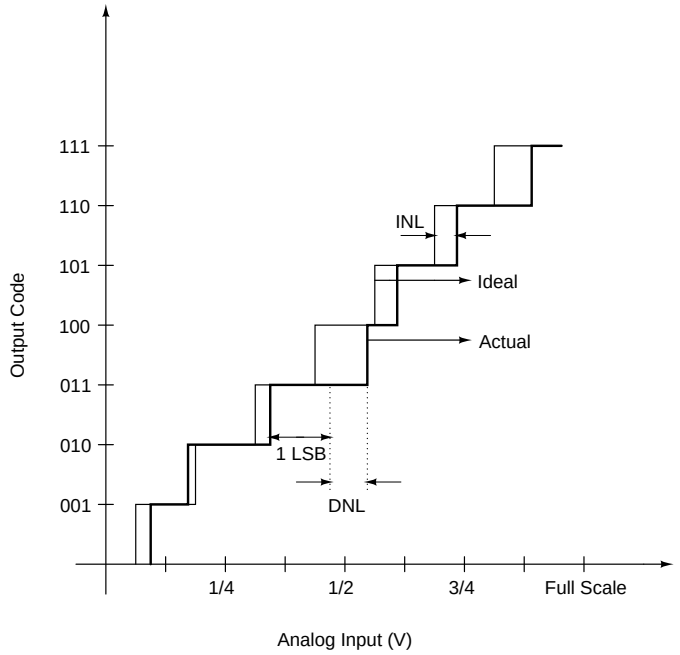

Figure A.3: Static non idealities of ADC: DNL and INL

other kind of noise exists, the maximum SQNR of an N bit ADC, for a full-scale sinusoidal input can be given as Razavi (1995),

$$SQNR = 6.02 \cdot N + 1.76 \qquad \text{(dB)} \tag{A.2}$$

In a practical environment though, there will be more distortions present due to thermal noise, disturbing signals and technology limitations. Hence, in practical ADCs, the SNDR will be less than the theoretical maximum SQNR. This means, all the output bits of the ADC may not carry any valuable information. Thus, real accuracy or resolution of ADC is specified by *effective number of bits (ENOB)*. From the equation (A.3), we can write,

$$ENOB = \frac{(SNDR - 1.76)}{6.02} \tag{A.3}$$

- *Spurious free dynamic range (SFDR):* Dynamic range of an ADC is the range between maximum input and the minimum input to which the ADC can respond. Normally, the maximum limit is limited by supply voltage and distortion, whereas the minimum limit is limited by noise. SFDR is the ratio of

the *root mean square (rms)* value of the fundamental to the rms value of the strongest spurious tone. *Full-power bandwidth (FPBW)* is the input frequency, at full-scale voltage, at which the amplitude of the output digitized result decreases by 3 dB.

- *figure of merit (FOM):* A popular *figure of merit (FOM)* used to compare different ADCs is (A.4) Plassche (2003),

$$FOM = \frac{Power}{2 \cdot f_{in} \cdot 2^{ENOB}} \qquad \text{(pJ/conv)} \tag{A.4}$$

where f_{in} is the frequency of the input. Lower FOM indicates better design. A detailed ADC glossary can be found in Maxim (2002).

- *Area efficiency (AE):* An *Area efficiency (AE)* merit of an ADC is computed as

$$AE = \frac{CoreArea}{2^{ENOB}} \qquad \text{(µm}^2\text{/code)} \tag{A.5}$$

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Publications based on the thesis

The thesis outlines the study and designs of nonbinary weighted SAR ADCs for data acquisition system applications and is a result of research carried at Department of Electronics and Communication Engineering, National Institute of Technology, Karnataka between July 2010 and August 2020. The research during this period has resulted in the following publications:

A. International Conference Proceedings:

1. Shrivastava, P., Bhat, K., Laxminidhi, T. and Bhat, M. S. (2012). "A 500 kS/s 8-bit Charge Recycle Based 2-bit Per Step SAR ADC." *Third International Conference on Emerging Applications of Information Technology (EAIT-2012)*, 462–466.

2. Bhat, Kalpana., Laxminidhi, Tonse and Bhat, M. S. (2015). "An 8-b 1.5 MS/s 2-bit Per Cycle SAR ADC with Parasitic Insensitive Single Capacitive Reference DAC." *IEEE region 10 International Conference (TENCON-2015)*, 1–6.

3. Bhat, K., Laxminidhi, T. and Bhat, M. S. (2019). "A Compact 10-bit Nonbinary Weighted Switched Capacitor Integrator Based SAR ADC Architecture." *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, 1–4.

B. Refereed International Journals

1. Bhat, K., Laxminidhi, T. and Bhat, M. S. (2019). "A Compact 4-to-8-bit Nonbinary SAR ADC Based on 2 bits per Cycle DAC Architecture." *Sadhana, Acadamy Proceedings in Engineering Sciences*, 44(6), 137–148. https://doi.org/10.1007/s12046-019-1121-1

2. Bhat, K. G., Laxminidhi, T. and Bhat, M. S. (2020). "Resolution-Independent Fully Differential SCI-Based SAR ADC Architecture Using Six Unit Capacitors." *Sadhana 45, 184*, Springer.
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