A DIGITAL HEARING AID ASIC WITH EFFICIENT 18-BAND ANSI S1.11 FILTER BANK AND DYNAMIC RANGE COMPRESSION ALGORITHMS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

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DECLARATION

I hereby ***declare*** that the research thesis entitled **A Digital Hearing Aid ASIC with Efficient 18-Band ANSI S1.11 Filter Bank and Dynamic Range Compression Algorithms** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bona fide report of the research work carried out by me***. The material contained in this research thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to certify that the research thesis entitled **A Digital Hearing Aid ASIC with Efficient 18-Band ANSI S1.11 Filter Bank and Dynamic Range Compression Algorithms**, submitted by **Deepu S. P.** (Register Number: 148050EC14FV10) as the record of the research work carried out by him, is accepted as the *research thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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Abstract

According to World Health Organization, 466 million people (more than 5 percent of the world population) have disabling hearing loss. A Digital hearing aid consists of analog front end and digital signal processing blocks along with transducers. The incoming sound signal captured by the microphone is given to an analog to digital converter (ADC). The digital output from the ADC is processed by the digital signal processor (DSP) and the processed signal is converted back to analog using a digital to analog converter (DAC) before sending it to the receiver. In this work, the design of a signal processing ASIC, which can perform the task of auditory compensation and the signal compression in a digital hearing aid is presented.

Studies on the features of current state of the art techniques suggest a requirement for further optimisation in the area of filter bank and dynamic range compression algorithms. In this work, a new filter bank architecture and new expressions addressing the effects of gain compression stage on the attack and release time decay coefficients of dynamic range compression algorithm are proposed. In dynamic range compression, by using the proposed equations for estimating the decay coefficients at the algorithm level, the errors that occur at the output with conventional method are totally removed to meet the ANSI S3.22 specifications for hearing aids. At architectural level, eight different architectures for the DRC algorithm were compared and conclusions are drawn on the selection of the features of DRC based on the hearing aid requirement. Based on the results, we propose to use an absolute level detector based DRC without smoothing stage for a low power hearing aid application. Interpolated Finite Impulse Response (IFIR) technique was used to develop the proposed 18-band ANSI S1.11 filter bank architecture. Since IFIR technique was used, the hardware implementation of the entire structure became less complex compared to other architectures. The proposed algorithm requires 50% lesser number of filter coefficients compared to other ANSI S1.11 architectures. The proposed algorithm was implemented using standard cell based design flow and the design was tested with NAL-NL2 gain prescription formula for 8 different audiograms corresponding to different hearing losses. The test results show that the maximum matching error is less than 1 dB. The major contribution of this thesis is the complete hardware implementation of 18-band ANSI S1.11

filter bank, as it is not reported in literature to best of our knowledge. The proposed filter bank combined with DRC consumes a total power of 0.39 mW for 65 nm technology. The design was verified in real-time using two FPGAs, one of them modeled as the proposed hearing aid DSP and the other as an external audio CODEC. The hearing aid chip was provided with an SPI protocol for interfacing with the external audio CODEC. The design was also ported to SCL 180 nm technology to fabricate a prototype ASIC.

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Abbreviations

Abbreviation	Expansion
ADC	Analog to Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
AM	Amplitude Modulation
AMS	Agile Mixed Signaling
ANSI	Ameraican National Standards Institute
ASIC	Application Specific Integrated Circuit
AT	Attack Time
BTE	Behind The Ear
CDAC	Centre for Development of Advanced Computing
CF	Compression Factor
CIC	Completely In Canal
CODEC	COder DECoder
CR	Compression Ratio
CT	Compression Threshold
DAC	Digital to Analog Converter
DCT	Discrete Cosine Transform
DFT	Discrete Fourier Transform
DHA	Digital Hearing Aid
DRC	Dynamic Range Compression
DSL-I/O	Desired Sensation Level-Input/Output
ECM	Electret Condenser Microphone
EDA	Electronic Design Automation
EIN	Effective Input Noise
ENT	Ear Nose Throat
FB	Filter Bank
FBC	Feed-Back Cancellation
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
FRM	Frequency Response Masking
GPIO	General Purpose Input/Output
HAC	Hearing Aid Chip
HDL	Hardware Description Language
HI	Hearing Impaired

Abbreviations

Abbreviation	Expansion
I^2S	Integrated Interchip Sound
IC	Integrated Circuit
IFIR	Interpolated Finite Impulse Response
IHAFF	Independent Hearing Aid Fitting Forum
IIC	Invisible In Canal
IIR	Infinite Impulse Response
ITE	In The Ear
LUT	Look Up Table
LSB	Least Significant Bit
MAC	Multiply and Accumulate
MBNR	Modulation Based Noise Reduction
MeitY	Ministry of Electronics and Information Technology
MEMS	Micro Electro Mechanical System
MPY	Multiplications per sample
NAL-RP	National Acoustic Laboratory - R Profound
NAL-NL	National Acoustic Laboratory - Non Linear
NR	Noise Reduction
OSPL90	Output Sound Pressure Level 90
PDK	Process Design Kit
POGO	Prescription of Gain/Output
QMF	Quadrature Mirror Filter
RIC	Receiver In Canal
RMS	Root Mean Square
RT	Release Time
RTL	Register Transfer Level
SCL	Semi-Conductor Laboratory
SNHL	Sensory Neural Hearing Loss
SNR	Signal to Noise Ratio
SPEF	Standard Parasitic Extraction File
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
TEQIP	Technical Education Quality Improvement Programme
THD	Total Harmonic Distortion
TI	Texas Instruments
UMC	United Microelectronics Corporation
VLSI	Very Large Scale Integration
WHO	World Health Organisation
WOLA	Weighted OverLap and Add

Chapter 1

Introduction

Hearing aid is a real-time system that helps people who are suffering from hearing loss. Hearing loss can be defined as partial or total inability to hear. A person having a threshold of hearing of 25 dB or more is said to have hearing loss. Based on severity level, hearing loss can be classified into mild, moderate, severe and profound. A speech banana diagram which represents the intensity and frequency of various sounds and severity of the hearing loss is shown in Figure 1.1. Different phonemes in speech, when placed in an audiogram, forms a banana-like structure. A hearing loss within speech banana can seriously affect a person's ability to perceive speech. Hearing loss can happen due to congenital and acquired reasons. Along with communication problems, the normal life of a person with hearing loss can get affected in various ways such as social, functional, emotional and economic.

According to World Health Organization (WHO), 466 million people (more than 5% of the world's population; 432 million adults and 34 million children) are suffering from disabling hearing loss (WHO (2019)). Hearing loss greater than 40 dB in the case of adults and 30 dB for children in the better hearing ear is considered as disabling hearing loss. The majority of hearing impaired (HI) live in low and middle-income countries. WHO reports also project that 900 billion teenagers and young people are at risk of hearing loss due to the unsafe use of personal audio devices including smartphones and exposure to damaging levels of sound at noisy entertainment venues. Exposure to sounds in excess of 85 dB for 8 hours and 100 dB for 15 minutes may lead to hearing impairment.

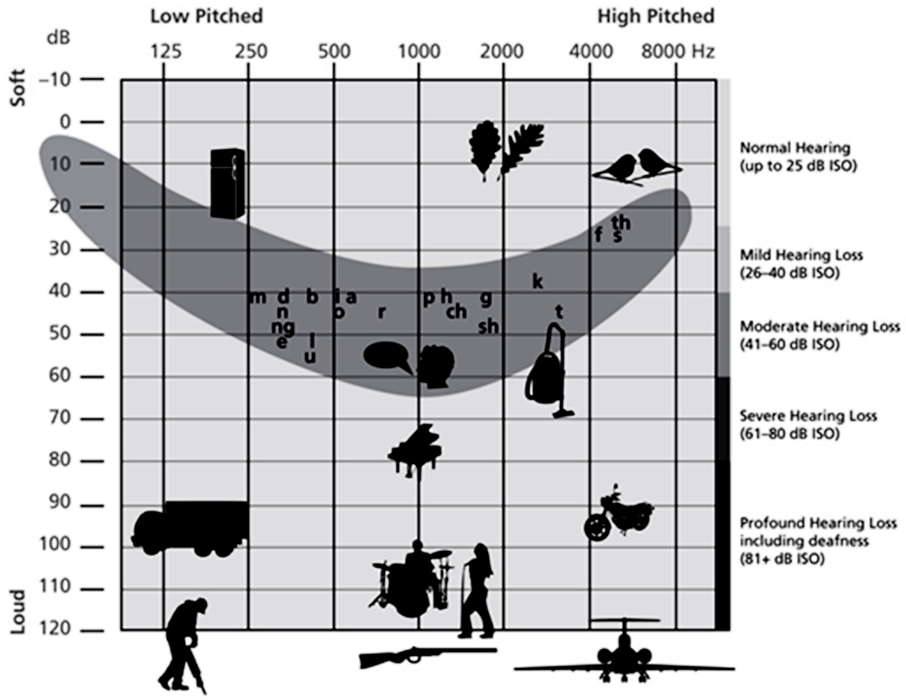


Figure 1.1: Speech banana diagram[1]

1.1 Digital Hearing Aid Block Diagram

A digital hearing aid (DHA) consists of analog front end and digital signal processing blocks along with transducers. The basic block diagram of a DHA is shown in Figure 1.2. The incoming sound signal is captured by the microphone and is given to an analog to digital converter (ADC). The digital output from the ADC is processed by the digital signal processor (DSP) and the processed signal is converted back to analog using digital to analog converter (DAC) before sending it to the receiver.

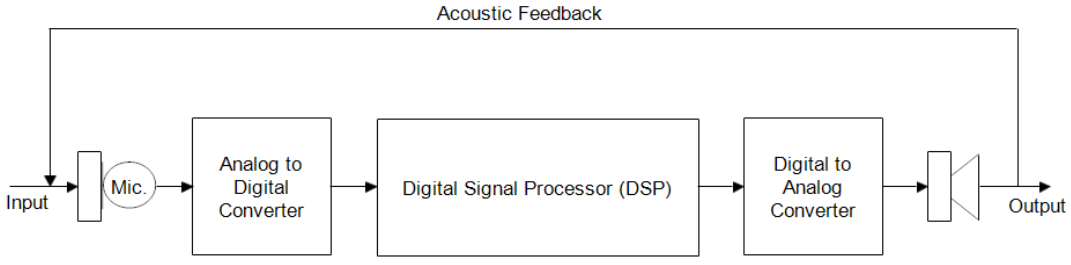


Figure 1.2: DHA block diagram

[1]source : http://www.hearinglink.org/

The microphones for hearing aids need to have low power consumption, small size and low sensitivity to vibration. A uniform frequency response over a range of 200 Hz to 5 kHz is desirable. A microphone with high sensitivity and low equivalent input noise (EIN) level has to be chosen while designing a hearing aid system. An electret condenser microphone (ECM) is most widely used in hearing aids. The MEMS microphones have started replacing ECM because of its lower power consumption, smaller size and uniform response over a wide frequency range.

Receivers also have to be small in size and free from vibrations. Advanced techniques like balanced armature technology improved the vibration performance of hearing aid receivers. The maximum output SPL of hearing aids largely depends on the capability of the receiver. The selection of receivers also depends on the hearing aid type since different styles require different size and output power.

An audio CODEC (Coder-Decoder) is composed of ADC and DAC. A CODEC can either be integrated into DSP or be used as a standalone chip. Low power consumption, small size, high dynamic range and high resolution are the main requirements of a CODEC for hearing aid application.

There is an acoustic feedback path from the receiver to the microphone. The microphone picks up the receiver output sound and causes a whistling or other audible artifacts. The presence of acoustic feedback limits the maximum gain that can be applied to a hearing aid. The effect of feedback largely depends on the type of hearing aid and the physical structure. It will be high in the case of a CIC with a vent. The feedback problem will be minimum in the case of RIC since the receiver is well isolated from the microphone.

The fundamental concept of hearing aid is to amplify the signal level in a particular frequency range where there is hearing loss as per the audiogram. In a DHA, the digital signal processing block does this function. A basic hearing aid DSP block consists of feedback cancellation (FBC), filter bank (FB), noise reduction (NR) and dynamic range compression (DRC) algorithms. The block diagram of a hearing aid DSP is shown in Figure 1.3.

Since there is a need to modify the magnitude of the frequency response according to the audiogram, a filter bank algorithm is needed to adjust the gains at various frequencies individually. The Analysis filters split the entire incoming signal into smaller bands. The insertion gain obtained from the prescription formula is applied to each band and later, fine-tuning is done manually. After processing each band, a synthesis filter bank combines each band and gives the final output.

The frequency response of the cochlea is distributed in a non-uniform manner as shown

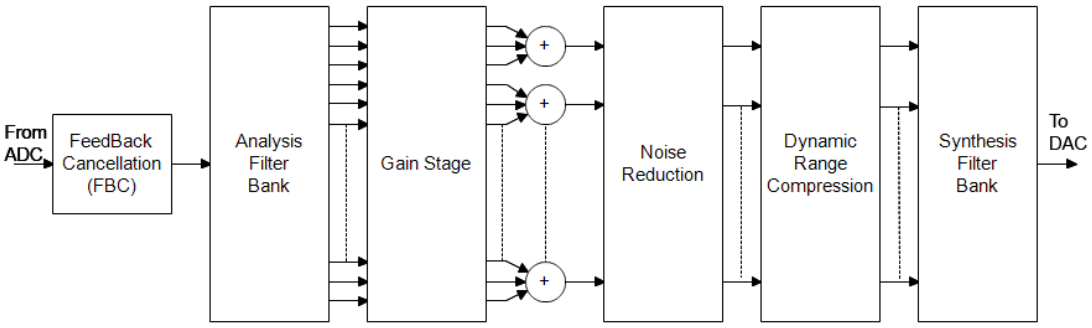


Figure 1.3: DSP block diagram

in Figure 1.4. So there are two different approaches to design filter banks for hearing aids: uniform and non-uniform. Uniform filter banks split the entire spectrum into bands of equal frequency resolution and are comparatively easy to design. In non-uniform filter banks, the auditory spectrum is divided into bands of different frequency resolutions and it gives better audiogram matching with a lesser number of bands. Hearing aid designers prefer finite impulse response (FIR) filters over infinite impulse response (IIR) filters as it provides linear phase, lower error and higher stability.

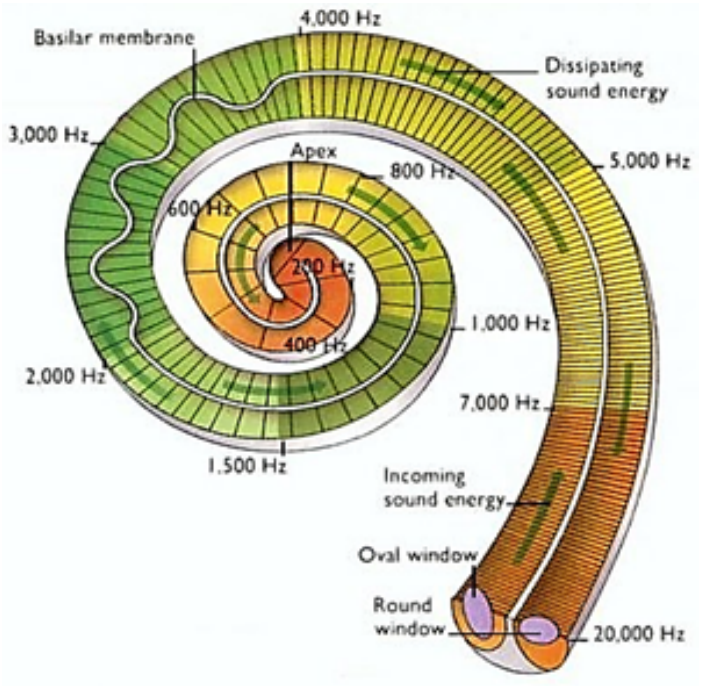


Figure 1.4: Frequency distribution inside cochlea[2]

[2]source: https://universe-review.ca/R10-16-ANS06.htm

For hearing impaired people, generally the lower threshold of hearing increases while the upper threshold remains the same. This causes a reduction in the range of audible SPL compared to normal people. So hearing impaired people may feel increased growth of loudness when SPL increases from lower value to higher value. This phenomenon is commonly called as recruitment. Because of recruitment, there is a need for compressing the wider dynamic range of input signal SPL into the residual range of hearing impaired people. This is done through a dynamic range compressor (DRC) circuit. DRC can be either single channel or multichannel. As the number of channels increases, the circuit complexity also increases, which causes higher power consumption. In most of the hearing aid algorithms, after applying the insertion gain, bands will be combined into a smaller number of channels before applying DRC.

Noise reduction algorithm is used to preprocess the signal before applying to DRC. DRC will increase the amplitude of low intensity signals more, compared to high intensity signals, which may increase the effect of noise.

Feedback cancellation algorithms are adaptive in nature. In the basic feedback cancellation algorithm, the output is multiplied by a weighting factor and the result is then subtracted from the microphone signal producing a difference signal. A self- adjustment block continuously updates the weighting factor in response to the attenuation factor (Schaub (2008)). Generally, FBC is applied before splitting the signal into different bands.

In high-end hearing aids, more sophisticated algorithms like beamforming techniques for adaptive directionality, wireless protocols for communicating with mobile phones and remote controls, classification algorithms for automatically adapting to the changing environment, localisation algorithms for binaural hearing etc., may also be included.

1.2 Motivation and Research Objectives

A considerable portion of the world population is suffering from disabling hearing loss and they can benefit from hearing aids, cochlear implants and other assistive devices, sign language and other forms of educational and social support. The current production of hearing aids meets less than 10% of global need according to WHO. One major reason why people having hearing loss are not adopting hearing aids is its value for money. According to a survey by *The Hearing Review*, the average cost of a hearing aid per ear goes above $2000 (Strom (2014)). So for a pair of hearing aids, the cost is not affordable for a person from a middle or low income group.

Following conclusions are made from the literature survey on current state of the art hearing aids. The three primary challenges for a hearing aid IC design, i.e., low power, small size and high sound quality may not change in the near future (OnSemiconductor (2014)). The IC should work well with a supply voltage as low as 1 V and the overall current consumption has to be less than or around 1 mA. Qiao et al. (2011) suggested an area constraint of 25 mm^2. Various studies suggest that delay has to be as small as possible. Bauml and Sorgel (2008) reported that even a 3 ms delay is noticeable and a 10 ms delay is significant. One major difficulty in analyzing various chip implementations is that most of the designs do not mention the delay performance of the systems in their results.

Considering the four basic signal processing algorithms required in hearing aids, FB and DRC perform the fundamental functions of loudness compensation and compression which are important, while FBC and NR are required for further signal enhancement and are optional. FBC largely depends on the final mechanical design of the hearing aid. So it is difficult to decide on the feedback cancellation algorithm to be included in the final design of the hearing aid without having a real-time measure of the actual feedback. Feedback cancellation algorithm can be avoided with a better physical design.

Most common fitting procedures NAL-NL1 and NAL-NL2 prescribe their gains in 1/3-octave bands. Therefore, most of the recent research on filter banks concentrates on 18-band 1/3-octave structure to get a perfect fitting. But 18-band structure results in large delay especially in lower frequency bands. Uniform filter banks are the most common choice in the hearing aid industry. But the problem with uniform filter bank is that it requires large number of bands to get better resolution at lower frequencies. For example, in the case of the 18-band 1/3-octave filter bank, the lowest frequency resolution is as low as 40 Hz. To get that level of resolution with a uniform filter bank, at least 200 narrow band filters are needed which will involve a large number of computations.

In DRC algorithms, according to ANSI S3.22 specifications, the attack time and release time are defined in terms of the time taken by the output signal to reach within 3 dB and 4 dB of its final value respectively. All the currently available algorithms calculate the time constants in terms of input signal level and none of them consider the effect of gain stage on the time constants. These algorithms are originally derived from general audio processing applications, where slight variations in dynamic parameters may not make much difference in the final output since the people using those applications would be having normal hearing. But in the case of hearing impaired people a precise control over time constants is preferred, because even small variations in the time constants may affect the

speech quality and intelligibility (Schaub (2008)). Because of the two stage filtering, the smoothing algorithm also affects the effective time constants adversely.

Various surveys on customer satisfaction show that low speech quality is the main reason for people not wearing their hearing aids. Especially the difficulty in speech recognition in highly non-stationary environment is still the number one problem associated with hearing aids. So there is a need for a better noise reduction algorithm which can be used for real-time processing with minimum delay and limited power consumption.

All these emphasise that there is a requirement for a high user value hearing aid affordable for middle and low income group in developing countries. Studies on current state of the art techniques suggest a need for further optimisation in the area of filter bank and dynamic range compression algorithms. Based on these factors, the following objectives have been formulated for this research work.

1) To develop a digital filter bank and dynamic range compression algorithms with low power consumption and acceptable delay for a hearing aid application, which can be programmed by any of the available nonlinear prescriptive formulas.

2) Hardware design and implementation of the developed algorithms to fabricate as a signal processing ASIC and real-time testing of the design using FPGA.

1.3 Design Approach

i) Objective 1:

FIR filters offer better stability and linear phase compared to IIR filters. Even though there is not much significance for phase response in the context of speech intelligibility, linear phase is important if any feedback cancellation algorithm needs to be included. It also helps in maintaining binaural cues which are required for acoustic directionality. So an FIR filter approach was adopted in designing the filter bank. Uniform and non-uniform FB techniques have their own advantages and disadvantages as discussed earlier. Even though uniform filter banks are predominantly used compared to non-uniform structures in practical circuits, a lot of research has been carried out in non-uniform domain in the last decade. Most of the recent research focus on the 18-band ANSI S1.11 structure to get perfect audiogram matching. Because of its high computational complexity and delay, these algorithms are yet to be considered as a practical choice in hearing aids. However, there is scope for further optimisation for the currently available architectures. Thus a non-uniform approach that satisfies the ANSI S1.11 specifications and having a reduced computational

complexity and acceptable delay performance is adopted in this work. The feasibility of the proposed design was proved by implementing the entire filter bank architecture using semi-custom design flow and analyzing the frequency matching error performance and power consumption.

Dynamic Range Compression algorithms contain two fundamental blocks: level detection and gain stage. In traditional algorithms, a single-pole low pass recursive filter has been used for level detection. The effect of the gain stage on the estimation of the time constants was studied and an algorithm which gives accurate attack and release time values as defined in ANSI S3.22 standard for hearing aid specifications was developed. A smoothing stage can be included in DRC to reduce the distortion due to word length errors. In that case, adverse effects on time constants due to two-stage filtering was eliminated by proposing new methods to estimate the decay coefficients.

ii) Objective 2:

Being a real-time device which works on low voltage and limited capacity batteries, verifying the performance of the hardware implementation of the algorithms intended for hearing aids is crucial. Hardware implementation of the proposed algorithms was carried out using standard register transfer level (RTL) techniques using Verilog Hardware Description Language (HDL). Industry-standard electronic design automation (EDA) tools are used for the design and analysis of the design at every stage. The functionality of the algorithms was verified using a software platform before doing the hardware design. To get a fair idea about the performance of the design, a technology node of 65 nm from United Microelectronics Corporation (UMC) that provides 1.2 V low power design libraries was used, which matches the battery voltage of the hearing aid. Texas Instruments has an ultra-low power audio CODEC (AIC111) designed for hearing aids. We plan to use this CODEC as the analog front end to be interfaced with our proposed ASIC. The CODEC is provided with a master SPI protocol to communicate with interfacing devices. So an SPI slave protocol is required, which is compatible with the CODEC protocol. Two Digilent ZedBoards having ZynQ-7000 FPGAs from Xilinx® were used for testing the functionality of the hardware design in real-time. The design was ported to SCL 180 nm technology also by properly following the vendor specific EDA tool flow for each stage with an intention to fabricate the chip.

1.4 Contribution of the Thesis

A digital signal processing ASIC intended to work as a processing module inside a digital hearing aid is presented in this thesis. In the proposed ASIC, modified filter bank and dynamic range compression algorithms are included, and the functionality was tested and verified in real-time using FPGA. Along with the design details about the proposed ASIC, a detailed explanation of various features, fitting procedure, and the current research trends in state of the art hearing aids are also included. The disadvantages of current hearing aids were studied and the design requirements were decided based on the literature survey given in chapter 2.

Current dynamic range compression algorithms estimate the decay coefficients erroneously. A new formula relating attack and release time parameters, envelope tracking decay coefficients and compression ratio parameters is proposed for the dynamic range compression algorithm for hearing aid application. An absolute detector based and an RMS detector based feed-forward architectures with and without smoothing stages were implemented using 4-bit and 8-bit resolution LUT based logarithm at hardware level using UMC 65 nm standard cell libraries. The approximation errors and the post-layout core power consumption analysis show that the proposed techniques give accurate expected output at required time instants while conventional methods give erroneous output values. There is no significant difference in power consumption with an increase in log table resolution, while the approximation error reduces significantly. Smoothing stages can be included if a continuous gain transition is needed with the cost of increased power consumption. These results suggest the use of an absolute level detector based DRC without the smoothing stage for lowest power consumption and overall performance, using modified decay coefficient estimation techniques for a low power hearing aid design. In applications where high quality of sound is important, a smoothing filter can be incorporated at the output stage.

A complexity-oriented architecture for ANSI S1.11 1/3 octave Class-2 filter bank for hearing aids is also proposed as part of this work. A method to define band edge frequencies of each prototype filter to get minimum orders that satisfy the required specifications is developed. Hardware implementation of the algorithm was carried out using 65 nm standard cell libraries and the output was tested with NAL-NL2 prescription for different audiograms. The maximum matching error was within the practical limit of $\pm 1.5\ dB$. The proposed architecture shows more than 50% reduction in the total number of filter coefficients required compared to other ANSI S1.11 based designs and less than 10 ms group delay with practi-

cally feasible power consumption. A complete hardware implementation and the audiogram matching results for the designed hardware of the proposed 18-band ANSI S1.11 filter bank is one of the major highlights of this thesis. Similar implementation results for an ANSI S1.11 based filter bank is not reported previously to the best of our knowledge.

Fabricating the whole chip with the proposed architectures using 65 nm technology is not viable because of the high cost for fabrication. So an ASIC with the proposed filter bank combined with the DRC architecture was implemented using 180 nm standard cell library with an intention to fabricate from the facility available at Semi-Conductor Laboratory, Chandigarh, India (SCL (2020)). Even though the area and power consumption of the chip in 180 nm technology would be higher, a working prototype will add value to the research work and it can be used in a body worn type hearing aid if all the specifications are met as per the design. The chip was designed in such a way that it is programmable externally through the serial communication protocol. The functionality of the design was tested in real-time using two FPGAs, one of them modeled as the hearing aid chip and the other as an external audio CODEC. As a whole, this research work explains the design and implementation of a programmable digital hearing aid ASIC with modifications proposed to the currently available hearing aid algorithms.

1.5 Organisation of the Thesis

Chapter 2 explains the necessary background required to understand the functionality and general features of the hearing aids. The chapter also contains a detailed literature survey on various hearing aid implementations and their characteristics, filter bank structures and dynamic range compression algorithms.

The development and implementation of the dynamic range compression algorithm are explained in chapter 3. This chapter presents two different aspects of DRC inter-related to each other. In the first part, the conventional DRC algorithm and the proposed techniques to overcome the flaws of the conventional methods are given. In the second part, implementation details and hardware-level comparison of eight different DRC architectures are described and conclusions are made based on the simulation results of different architectures to chose the appropriate design according to the specific hearing aid requirement.

The 18-band ANSI S1.11 filter bank design is described in chapter 4. The theoretical explanation of the algorithm as well as finer details of the hardware architecture are given in this chapter. It is concluded with the analysis of hardware implementation results and

audiogram matching error performance of the proposed design corresponding to different hearing losses.

The details of the implementation of proposed hearing aid ASIC using SCL-180 nm technology is given in chapter 5. The real-time testing of the proposed hearing aid algorithm using FPGAs and the design of the SPI slave protocol are also included in this chapter. Finally, the summary of the research work is given in chapter 6. This chapter also contains the scope for future research in the field of digital hearing aid, more specific to the topics covered in this thesis.

Chapter 2

Review of Digital Hearing Aids

A digital hearing aid is a complex real-time system capable of performing audio signal enhancement according to the requirements of a particular hearing loss. Every hearing aid is equipped with a wide range of features, even though the power and delay constraints are stringent. A general overview of current hearing aids is given in the first part of this chapter. Various aspects such as types of hearing loss, types of hearing aids, the way hearing aids get fitted and the common terms related to hearing aids and hearing aid research are addressed. In the second part, a detailed literature survey on hearing aids is given. It starts with a review on user satisfaction and problems with the current state of the art hearing aids followed by a survey on various hearing aid implementations and its features. Further, various filter bank algorithms and dynamic range compression algorithms available for hearing aids are explored.

2.1 Types of Hearing Loss

Hearing loss can be categorised into three types based on which part of the auditory process is affected. A cross-section of the human ear is shown in Figure 2.1.

i) Conductive hearing loss:

Conductive hearing loss happens due to the problems with the ear canal, eardrum or middle ear and its little bones. It results in a reduction in sound intensity, reaching the inner ear. So a conductive hearing loss can be mitigated by increasing the sound intensity according to the air-bone gap information that can be obtained from the audiogram. Hearing aids work well for compensating the conductive hearing loss.

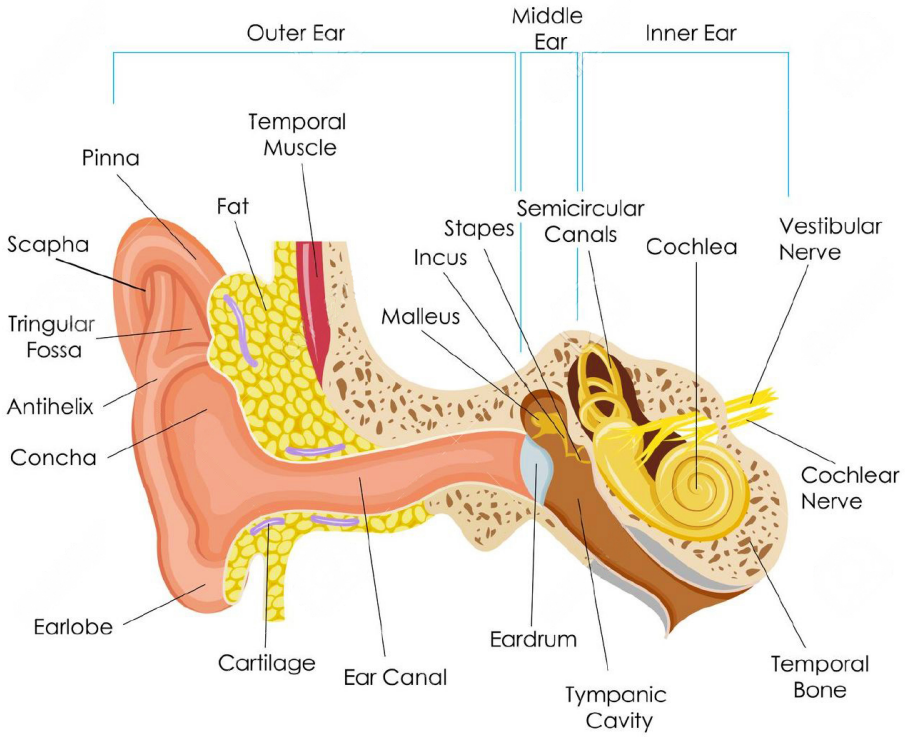


Figure 2.1: Cross-section of human ear[1]

ii) Sensorineural hearing loss (SNHL):

When hearing loss is due to the problems of the inner ear (cochlea and auditory nerve), it is called sensorineural hearing loss. The major reason for SNHL is the loss of hair cell functionality inside the cochlea. Any kind of damage to the hearing nerves also results in SNHL. It is an irreversible or permanent condition. Along with the reduction in sound intensity, it also causes distortion in perceived speech signals. Hearing aids can be used to assist people with sensorineural hearing loss by enhancing the frequencies corresponding to damaged hair cells.

iii) Mixed hearing loss:

Mixed hearing loss refers to the hearing loss due to the combination of conductive and sensorineural losses.

[1] source: http://www.123rf.com

2.2 Types of Hearing Aids

Based on the style, size and where it is worn, currently available hearing aids can be categorised into any of the following types.

i) Body worn hearing aids:

Body worn is the oldest version of hearing aids. It consists of a processing module and a receiver, which is connected to the module by a cable. Signal acquisition and processing take place in the module and the processed sound is played through the receiver. These hearing aids can provide large amplification. Poor sound quality due to ineffective sound acquisition is the major disadvantage. Since the processing element is separated from the receiver and has to be carried in a pocket, maintenance is a problem. Lower cost and higher battery capacity still help it to continue in the market.

ii) Behind The Ear (BTE):

Behind the ear hearing aids consist of a case, an earmold or dome and a connection between them. The case contains the electronics, controls, battery, microphone(s) and often the loudspeaker. Generally, the case sits behind the pinna with the connection from the case coming down the front into the ear. BTEs can be used for mild to profound hearing loss. Comparatively lower price, flexibility to use for a larger range of hearing loss and easy maintenance make it the most common style among hearing aids. Larger size compared to other types besides body worn is a disadvantage.

iii) Receiver In Canal (RIC):

Unlike BTEs, the receiver in a RIC device is housed entirely inside the ear. RICs are smaller devices worn behind the ear with a small wire running down into the ear canal attached to the receiver. Some of the advantages with this approach include improved sound quality, reduced case size, immediate patient fitting and the possibility of open-fit technology without having much feed-back problem. Small batteries with lesser capacity, higher cost and difficulty in maintenance are the major disadvantages.

iv) In The Ear (ITE):

In the ear devices fit in the outer ear bowl (called the concha). They are sometimes visible when standing face to face with someone. ITE hearing aids are custom made to fit

each individual's ear. They can be used in mild to severe hearing losses. Feed-back can be a problem in case of severe hearing loss. Earwax and moisture can easily build up and affect performance.

v) Completely In Canal (CIC)

Completely in canal aids are generally not visible unless the viewer looks directly into the wearer's ear. These aids are intended for mild to moderately severe losses. CICs are usually not recommended for people with good low-frequency hearing, as the occlusion effect is much more noticeable. Venting makes acoustic feed-back a severe problem in CIC devices.

vi) Invisible In Canal (IIC):

Invisible in canal hearing aids fit inside the ear canal completely, without leaving any visible trace of hearing aid externally. Extended wear hearing aids are hearing devices that are non-surgically placed in the ear canal by an ENT surgeon. These devices are worn for 1–3 months at a time without removal. They can be used by people with mild to moderately severe hearing loss. Higher cost, difficulty in handling and lack of flexibility are some of the disadvantages of IIC type. Different types of hearing aids are shown in Figure 2.2.

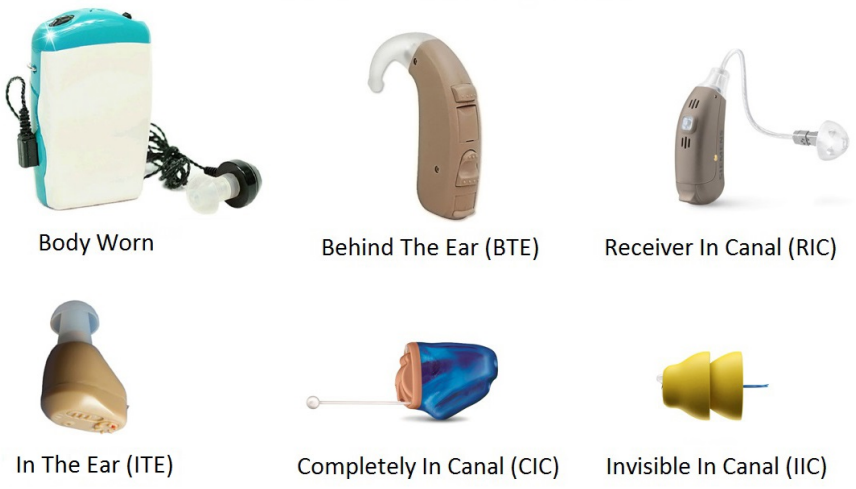


Figure 2.2: Types of hearing aids[2]

[2]source: http://www.rsfaudiology.com, http://www.medicalexpo.com/prod/phonak/product-78004-512410.html, https://www.bestsoundtechnology.com/

2.3 Hearing Aid Fitting Procedure

A patient having hearing loss has to go through a few steps before starting to use a hearing aid. An audiologist, who is a specialist in treating hearing loss will measure the degree of patient's hearing loss and decide the best possible solution after going through a set of standard procedures as explained below:

i) Hearing Test:

The first step in fitting a hearing aid is to understand the severity of the loss. A hearing test will be carried out in a soundproof room with a calibrated audiometer, which can produce sounds at different frequencies at specified levels. The audiologist plays these sounds at very low intensities through a calibrated headphone. Then the intensity level is gradually increased until the sound becomes audible. The softest sounds heard by the subject at each frequency are recorded as the thresholds. Most hearing tests analyse sounds between 125 Hz and 8 kHz and from -10 dB to 120 dB SPL. From these recorded data, SPL v/s frequency graph is plotted. The hearing test will be conducted in both the ears. An 'X' mark in the audiogram indicates the left ear and 'O' the right ear. The test using a headset is called as air conduction test. When air conduction shows a loss, a bone conduction test will be carried out to identify the conductive hearing loss. A small bone conduction vibrator will be placed on the mastoid bone directly behind the ear and sound is transmitted through the bones of the skull to the inner ear, bypassing the outer and middle ear. The audiogram will be plotted in the same way as in the air conduction test. A difference between air and bone conduction thresholds indicates a loss due to problems with the outer or middle ear, i.e., a conductive loss.

ii) Audiogram Matching:

Based on the audiogram and the patient's choice, the audiologist chooses a particular hearing aid. A hearing aid fitting software will be provided by every manufacturer, which contains all configurable options available for the particular hearing aid. One of the most important parts of the entire flow is the initial fitting. Various prescription formulas are available which give gain curves according to the audiogram. Most common methods available for hearing aid gain prescription are: NAL-RP (National Acoustic Laboratory-Revised Profound), NAL-NL1(Non-Linear 1), NAL-NL2(Non-Linear 2), DSL I/O(Desired Sensation Level Input/Output), IHAFF(Independent Hearing Aid Fitting Forum), FIG-6

and POGO-II. Hearing aid manufacturers may have their own fitting formulas as well. Still, most of them use the NAL series and DSL for initial fitting (Johnson (2012)). After the initial fitting, fine-tuning is done by adjusting the gain in each band manually, considering patient feed-back.

iii) Programming the hearing aid and testing the output:

After the initial fitting, the parameters will be loaded into the hearing aid using any of the hearing aid programming interfaces. The most common ones are Hi-Pro and NOAHlink. After loading the parameters into the hearing aid, it will be tested using a 2cc coupler by inserting inside a testing equipment. The parameters like delay, attack time, release time, frequency range, THD, OSPL90 etc., can be obtained from this test. Minimum performance requirements for a hearing aid according to WHO guidelines for designing hearing aids for developing countries is given in Table 2.1 (WHO (2004)). The entire hearing aid fitting procedure flow is shown in Figure 2.3.

Table 2.1: Minimum performance requirements of a hearing aid (WHO (2004))

Maximum $OSPL_{90}$	118 dB (± 4 dB)
$OSPL_{90}$ at 1 kHz	114 dB (± 4 dB)
Maximum full-on acoustic gain	45-55 dB (+5/0 dB)
Full-on acoustic gain at 1 kHz	42 dB (+5/0 dB)
Basic frequency response	200 Hz to 4500 Hz (200 Hz to 2000Hz ±4 dB, 2000 Hz to 4000 Hz ±6dB, on nominal frequency response curve
Total harmonic distortion at 70 dB SPL input	500 Hz < 5% 800 Hz < 5% 1600 Hz < 2%
Equivalent input noise level	< 25 dB SPL
Battery current	≤ 1 mA

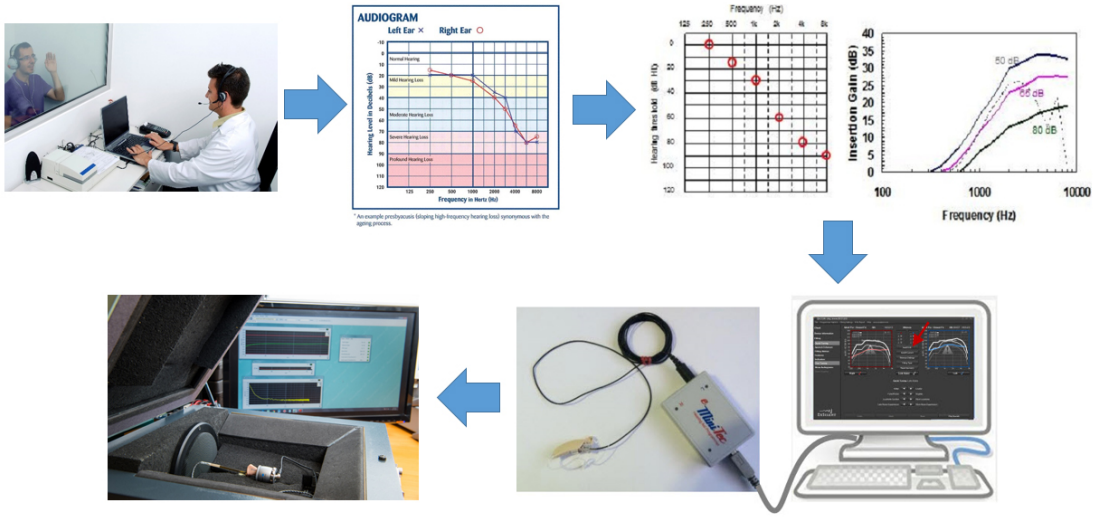


Figure 2.3: Hearing aid fitting procedure[3]

2.4 Hearing Aid Characteristics and Definitions

Definitions of some of the important terms related to digital hearing aids are given below (ANSI (2003) and Invensense (2003)):

Sound Pressure Level (SPL):

Sound pressure level is a measure of RMS value of sound expressed in decibels relative to a reference level of 20 μPa.

Output SPL for 90 dB input SPL (OSPL90):

OSPL90 is defined as the SPL developed at the output when the input SPL is 90 dB when the gain control of the hearing aid is full-on, i.e., when the volume control is set to maximum.

Full-on Acoustic Gain:

It is the result obtained at each test frequency by subtracting the input SPL from the SPL at the output of the hearing aid with the gain control set to its full-on position with an input SPL of 50 dB.

Compression Ratio (CR):

Compression ratio is the ratio of change in input SPL to change in output SPL in a compression curve.

[3] source: http://helpingmehear.com/, http://www.hearingessentials.com, http://www.audiologyonline.com, http://www.centuryhearingaids.com, http://sine.ni.com/cs/app/doc/p/id/cs-15033

Attack Time (AT):

Attack time is defined as the time between the abrupt increase from 55 to 90 dB and the point where the level has stabilised within 3 dB of the steady-state value for the 90 dB input SPL.

Release Time (RT):

Release time is defined as the interval between the abrupt drop from 90 to 55 dB and the point where the signal has stabilised to within 4 dB of the steady state value for the 55 dB input SPL

Compression Factor (CF):

Compression factor is the inverse of compression ratio, i.e., the ratio of change in output SPL to change in input SPL in a compression curve.

Compression Threshold (CT):

Compression threshold is the point at which the gain changes in a dynamic range compressor.

Sensitivity of a microphone:

The sensitivity of a microphone is defined as the electrical response at its output to a given standard input of 1 kHz sinewave at 94 dB SPL, or 1 pascal. A microphone with a higher sensitivity value has a higher level output for a fixed acoustic input.

Equivalent Input Noise (EIN) of a microphone:

Equivalent input noise is the output noise level of the microphone expressed in dB SPL, as a theoretical external noise source placed at the microphone's input. Input SPLs below the EIN level are under the noise floor of the microphone and outside the dynamic range of signals for which the microphone produces an output.

2.5 User Satisfaction and Problems with Current Hearing Aids

If a patient fitted with hearing aid feels that there is no advantage in wearing a hearing aid or if it causes any other adverse side effects, the person may stop using it. It is necessary to understand and solve the major reasons why patients stop using hearing aids. There are few studies available in the literature on why people are not using hearing aids even after spending a large amount of money and time to buy and get it fitted by an audiologist. Understanding these factors may help hearing aid designers to come up with better solu-

tions. In one of the most comprehensive studies by McCormack and Fortnum (2013), the authors have collected most of the available data on user satisfaction via a scoping study. Out of those, they have selected 10 articles reporting reasons for non-use of hearing aids and found a number of reasons including hearing aid value, fit and comfort, maintenance of the hearing aid, attitude, device factors, financial reasons, psychosocial/situational factors, healthcare professionals' attitudes, ear problems and appearance. In almost all the articles, the most important issue was the hearing aid value, i.e., the hearing aid did not provide enough benefit and comfort to the hearing impaired. Most of the people chose lack of speech clarity as the main cause of discomfort. Another important conclusion was, the stigma of wearing hearing aids had minimal impact on discontinuation.

Puder (2009), in an article on state of the art, challenges and future trends in hearing aids, claimed, reduced speech intelligibility in noisy environments as the top-ranked problem of hearing aid users and may continue as the major problem in future hearing aids too. Eric Healy, (Edwards (2015)), also noted that the difficulty of understanding speech in background noise as the number one complaint of people using a hearing aid and considered it as the "Holy Grail" in the case of hearing aid design. There are many surveys on the effectiveness of various noise reduction algorithms present in hearing aids as well. Chong and Jenstad (2018) have published one of such studies, in which the authors have comprehended the results of different single microphone noise reduction studies. In hearing aids, adding a highly advanced noise reduction algorithm is not feasible due to its power constraint and real-time requirement. According to the study, advanced noise reduction algorithms are yet to be tested on hearing aids. The paper concludes that current noise reduction algorithms are not useful for improving speech intelligibility, but may help in terms of improving listening comfort and release of cognitive load for a secondary task (i.e., dual task paradigm, such as evaluating the listening effort when a secondary visual task is carried out).

There are studies on the effectiveness of hearing aids between different languages like English and Mandarin. In one such recent studies (Wong et al. (2018)), the authors suggest that different signal enhancing algorithms may work differently on different languages. Mandarin is more vowel centric than consonant centric. So low frequency is more important for speech understanding than English. English on the other hand, is more consonant centric. So the algorithms, especially like noise reduction, work differently for tonal languages. But in some studies as by (Ho et al. (2013)), the objective parameters such as Acceptable Noise Level (ANL) are similar for Mandarin and English. So in such studies, there is no significant difference in the effectiveness of algorithms on different languages. As of now,

we could not find any such studies based on Indian languages, which are phonetic in nature. A proper study on the effectiveness of the different hearing aid algorithms for Indian languages may be helpful in developing better algorithms for hearing aids specific to Indian conditions.

There are some classic studies from earlier days using multiple hearing aids of different manufacturers (Alcántara et al. (2003), Bentler and Chiou (2006), Sarampalis et al. (2009)) on the effectiveness of hearing aids. According to Alcántara et al. (2003), the most commonly reported difficulty of people with even a mild sensorineural hearing loss is reduced speech intelligibility in environments where there is background noise or competing speech, and the hearing aids in most cases, instead of alleviating this problem, actually increases it. Even though the noise reduction algorithms may increase the apparent Signal to Noise Ratio (SNR), there is rarely any improvement in speech intelligibility.

Overall, various studies on user satisfaction and problems with current hearing aids clearly show that the majority of hearing aid wearers are not satisfied with the speech clarity, especially in disturbing noisy background conditions. Even though the presence of noise reduction algorithms improves the ease of hearing, or reduces the hearing effort, there is no proper improvement in overall speech intelligibility. Speech quality being the primary requirement for hearing aid wearers, the research should focus on improving the quality of algorithms present in hearing aids. Considering the fact that advanced and complicated algorithms are not yet tested on hearing aids due to its design constraints and showing some dependency on certain language characteristics, developing noise reduction algorithms for hearing aids is also a good and interesting area of research.

2.6 Hearing Aid Chip (HAC) Implementations

A hearing aid can be considered as one of the most challenging applications when it comes to IC design because of its real-time processing and stringent low power requirement. For hearing aid designers, there can be three primary challenges (OnSemiconductor (2014)): high performance (in terms of sound quality and computational capability), low power consumption (a battery current drain $\leq$ 1 mA) with limited supply voltage (approximately 1 V) and small physical size (depending on the style). Since all three are interrelated, it is the task of the designer to find a trade-off between these challenges. There are different options in the case of hardware platforms available for the researchers to implement the signal processing algorithms for hearing aids. For testing the algorithm in real-time during the ini-

tial stages of the design, it is a common practice to use low power general-purpose digital signal processors. Because of its size and comparatively higher power consumption, it is difficult to consider these processors for hearing aid products other than body worn type. Field Programmable Gate Arrays (FPGAs) are another option available for testing the algorithms in real-time. Application Specific Integrated Circuits (ASICs) with custom-designed dedicated architectures for the particular signal processing techniques are the best way to realise the algorithms in hardware.

Initial hearing aid systems were based entirely on analog technology. With the advancement in digital signal processing, hearing aids also started transforming from fully analog to digital platforms with an analog front end (AFE) circuitry that acts as an interface between transducers and the DSP. A literature survey was done on hardware implementations of hearing aid algorithms. Type, specifications and different signal processing algorithms included in various hearing aid system implementations available in the literature are given in Table 2.2. Some of the implementations used general-purpose signal processing kits for realizing the architectures.

In ASIC implementations, the supply voltage and power consumption decrease with the advancement in transistor technology. The performance of the hearing aids is largely limited by the currently available battery technology. Even though rechargeable batteries are available, 1.3 V zinc-air batteries are used in most of the hearing aids. Zinc-air batteries are available in different capacities and sizes. To get a reasonable battery life (at least greater than 50 hours (Qiao et al. (2011)), the current consumption should be minimum. Table 2.2 suggests that all the hearing aid ASIC implementations gave at most care to keep the power consumption in the acceptable range of around 1 mW (WHO (2004)). The power consumption also increases with the complexity of various algorithms incorporated in different implementations. Since each of the designs includes different levels of functionality and manufactured with different technology nodes, a direct comparison of power is not possible between the designs. Some of the implementations show that voltage scaling works well in reducing power consumption, (Wei et al. (2010), Qiao et al. (2011)). In (Wei et al. (2010)), the power consumption of the design got reduced from 1.09 mW to 0.314 mW when the supply voltage was reduced from 1 V to 0.6 V. The chip size depends on the complexity of the algorithm and the technology node used for fabrication. A chip area less than 25 mm^2 may be enough for BTE and ITE devices (Qiao et al. (2011)). Table 2.2 shows that the chip area reduced to less than or around 1 mm^2 as the technology advanced to deep submicron ($\leq$ 180 nm). The frequency range of the hearing aids is mainly limited by the microphone

and receiver characteristics. ANSI S3.22 standard specifies a minimum frequency range of 200 Hz to 5 kHz (ANSI (2003)). The audiogram gives information only up to 8 kHz. So a sampling frequency above 16 kHz may work well for the hearing aids. The sampling frequencies used by various implementations available in the literature are also given in Table 2.2. As the sampling frequency increases, the dynamic power consumption also increases. A sampling frequency of around 20 kHz is used in most of the practical hearing aid ICs.

For lip synchronicity, a delay less than 70 ms is sufficient (Bauml and Sorgel (2008)) which is easily attainable with the current algorithms. But the major problem with delay is the comb filter effect, which occurs when the delayed sound that comes through the hearing aid combines with the sound directly coming through the vent or bone conduction. Even a delay of 3 ms may create an echo. For a delay higher than 10 ms, this effect becomes significant and affects the intelligibility. So hearing aid delay is a major factor in the design and needs to be kept as small as possible. In most of the literature reporting chip implementations, the delay of the design is not mentioned and hence it is very difficult to compare the actual performance of different designs. Park et al. (1997) reported a delay of 10.9 ms. The other delays mentioned, 19.4 ms by Tejero et al. (1995) and 32 ms by Wei et al. (2010) are higher than the acceptable delay for a smooth output from a hearing aid.

Callias et al. (1989), Wayne et al. (1992), Bhattacharyya et al. (1996),and Serra Graells et al. (2004) are fully analog designs. In these designs, the complete processing was done only using analog circuits. The frequency decomposition was achieved mainly by tunable switched-capacitor filters (Wayne et al. (1992), Bhattacharyya et al. (1996)). The automatic gain control (AGC) circuits perform the functionality of DRC. When the designs started migrating from analog to digital, the implementations were mainly based on general-purpose DSP platforms.(Nielsen (1989), McAllister et al. (1995), Tejero et al. (1995), Stetzler et al. (1999)). Later, dedicated ASIC designs started replacing the digital hearing aid implementations. A direct comparison of these different implementations is not possible as each design depends on so many factors with its own characteristics as given in the table.

In every hearing aid design, the frequency decomposition algorithms are required to perform the auditory compensation and amplitude compression is needed to restrict the sound intensity to an acceptable loudness. The terms bands and channels are closely related to these algorithms and often used interchangeably in different implementations. For uniformity, in this thesis, the term number of bands is used to represent the number of filters used for auditory compensation, i.e., each band represents different frequency spectrum to

Table 2.2: Various hearing aid chip implementations and their features

Reference	Type	Techn-ology (um)	Power (mW)	Supply Voltage (V)	Area (mm2)	Sampling Freq. (Hz)	Delay (ms)	FB	DRC	NR	FBC
Morley et al. (1988)	Digital	1	0.002	15	10	12.5	–	Kingsbury and Rayner (1971)	Hard limiter	–	–
Callias et al. (1989)	Analog	3	1.95	1.3	35	–	–	Analog butterworth	Analog AGC	–	–
Nielsen (1989)	TMS320 C25	–	–	–	–	–	–	–	Hard limiter	Dillier (1988)	–
Wayne et al. (1992)	Analog	3	195	1.3	–	–	–	Adachi et al. (1990)	–	–	–
Svean et al. (1993)	Digital	0.8	–	–	44	–	–	–	–	–	–
Bhattacharyya et al. (1996)	Analog	3	0.73	1.1-1.5	–	–	–	–	Analog AGC	–	–
McAllister et al. (1995)	TMS320 C31-27	–	–	–	–	12.5	–	McAllister et al. (1994)	–	–	–
Tejero et al. (1995)	TMS320 C30	–	–	–	–	10.4	19.4	–	FFT based	–	–
Park et al. (1997)	Digital	0.65	–	3.3	27.5	12	10.9 for FB	8-band 128-tap FIR	Meskan (1997)	–	–
Neuteboom et al. (1997)	Digital	0.8	2	0.9-1.6	35	16	–	Saramaki et al. (1995)	–	–	–
Stetzler et al. (1999)	TMS320 C5000	–	–	–	–	16	–	1 to 50 (typically 14) band FIR	Swartz and Magotra (1994)	Magotra et al. (1998)	–
Mosch et al. (2000)	Digital	0.25	0.65	1.09	20	–	–	Nielsen and Sparso (1998)	–	–	–
Paker et al. (2001)	Digital	0.25	–	1.8	–	16	–	–	–	–	–
Gata et al. (2002)	Digital	0.6	0.297	1.1	12	40	–	Sjursen (2001)	–	–	–
Serra Graells et al. (2004)	Analog	1.2	0.3	1	–	–	–	–	–	–	–
Lee et al. (2007)	Digital	0.18	0.025	0.9	0.5	32	32	Sjursen (2001)	–	–	–
Wei et al. (2010)	Digital	0.09	1.09 at 1V and 0.314 at 0.6V	1(0.6 min)	3.13	24	–	Kuo et al. (2010)	Chang et al. (2010)	Kamath and Loizou (2002) Jia and Xu (2002)	–
Qiao et al. (2011)	Digital	0.065	0.334 at 0.8V	1(0.8 min.)	0.49	16	–	Kates (2005)	Kates (2005)	Hirsch and Ehrlicher (1995) Scalart et al. (1996)	Benesty and Huang (2003)
Ku et al. (2013)	Digital	–	0.84	0.9	–	20	–	–	–	–	–
Chang et al. (2014)	Digital	0.065	0.5	0.5	3.84	24	–	Liu et al. (2013)	Chang et al. (2010)	Chen et al. (2014)	–
Chen et al. (2015)	Digital	0.13	1.2	1	9.51	–	–	Brennan and Schneider (1998)	Kates (2008)	Kamath and Loizou (2002) Ephraim and Malah (1984) Chen et al. (2006) Ris and Dupont (2001)	Chi et al. (1999)

which the prescribed gains are to be applied and channels represent the number of different frequency spectrums to which the dynamic range compression algorithm is applied independently. It is better to have a higher number of bands so that the frequency resolution will be better for auditory compensation. That is, having a higher number of bands will improve the audiogram matching error performance. But on the other hand, various studies showing the effectiveness of the number of channels suggest that, there is no significant improvement in the intelligibility for more than four channels (Keidser and Grant (2001)).

It can be observed from Table 2.2 that, a few of the recent digital ASIC implementations have included feed-back cancellation algorithms (Qiao et al. (2011), Chang et al. (2014), Chen et al. (2015)). But the acoustic feed-back from the receiver output back to the microphone input depends significantly on the type of hearing aid and the vent present in the hearing aid (Dillon (2012)). So the requirement and the effectiveness of the feedback cancellation algorithm can be decided only after finalizing the hearing aid type and the physical structure.

From surveys on user satisfaction and problems of current hearing aids as given in section 2.5, it was evident that understanding speech in a noisy environment was having the highest priority among hearing aid wearers. Many of the recent hearing aid implementations have incorporated the noise reduction algorithm as well in their designs as seen from the table. Various studies on the effectiveness of noise reduction algorithms suggest that the presence of multiple techniques improves the performance of the system by adapting to different noisy environments (Chong and Jenstad (2018)). Multiband spectral subtraction (Kamath and Loizou (2002)), Modulation Based Noise Reduction (MBNR)(Scalart et al. (1996)), Wiener filtering (Chen et al. (2006)) and statistical methods (Ephraim and Malah (1984)) are the commonly used techniques in hearing aids. Chen et al. (2014) is a Mandarin specific noise reduction algorithm implemented on a Mandarin specific hearing aid by Chang et al. (2014). Qiao et al. (2011) have used comparatively older techniques based on wiener filtering (Hirsch and Ehrlicher (1995), Scalart et al. (1996)). Noise reduction for hearing aids is itself a vast area of research, and it is out of the scope of this thesis. It can be considered as a topic of serious interest for a future study considering the Indian scenario.

As it is already mentioned, dynamic range compression is a necessary algorithm required to protect the hearing aid wearers from further damage to their residual hearing. When it comes to the digital domain, initially hard limiters were used to restrict the output from going beyond a tolerable loudness (Morley et al. (1988), Nielsen (1989)). In hard limiters, the output was clipped if it goes beyond a particular threshold. Later, non-linear com-

pression techniques were introduced. Magotra et al. (1998) implemented the compression curve using approximation techniques like the Taylor series method in the linear domain. In the current state of the art hearing aids, the compression is applied in log domain after converting the estimated input signal to the log domain (Chang et al. (2010), Kates (2005)) so that the non-linear compression curve becomes a piece-wise linear curve.

For any hearing aid, the most power consuming part is the filter bank architecture. The ability of a hearing aid with which it can fit the prescription gain to compensate for the loss corresponding to each frequency in a patient's audiogram is decided by the frequency resolution of the filter bank. This resolution depends on the number of bands and the filter bank structure. The power consumption as well as the delay of the hearing aid are dependent on the individual filter orders, type of filtering and the number of bands present in the filter bank architecture. Table 2.2 gives information about the filtering techniques used in different hearing aid implementations.

In digital domain, uniform filter banks were used in earlier implementations (McAllister et al. (1995), Park et al. (1997)). Non-uniform structures started replacing the uniform structures in recent implementations(Kuo et al. (2010), Liu et al. (2013)). Mainly the introduction of widely accepted non-linear gain prescription formulas which give the compensation gains in an 18-band non-uniform manner (NAL-NL1, NAL-NL2 and DSL I/O) and the requirement of lesser number of bands to match that frequency distribution motivated the use of non-uniform filter banks. Even though recent implementations use these advanced non-uniform structures, detailed analysis of the delay and the feasibility of those systems(Wei et al. (2010), Qiao et al. (2011), Chang et al. (2014),Chen et al. (2015)) is not provided.

Based on the literature review on the user satisfaction, features and various algorithms present in hearing aids, we have decided to explore more on filter bank algorithms and the dynamic range compression algorithms and not on noise reduction and the feed-back cancellation algorithms as part of this research work. Detailed literature survey on the various filter bank algorithms and the development of dynamic range compression algorithm is given in sections 2.7 and 2.8 respectively.

2.7 Filter Bank Algorithm

As mentioned in previous sections, the digital filter bank can be configured as uniform or non-uniform type. Low computational complexity (which will decrease the power con-

sumption) and lower group delay are the main requirements of filter banks intended for hearing aid applications. A group delay less than 5 ms (Lunner and Hellgren (1991) Bauml and Sorgel (2008)) would be ideal to avoid comb filter effect. Audiogram matching error should be as small as possible. Lin et al. (2012) reported that the human auditory system cannot distinguish a 3 dB difference in SPL. So a matching error upto ±1.5 dB is acceptable. To achieve ±1.5 dB accuracy, the stop band attenuation has to be high and a 60 dB requirement on stop band attenuation was reported in Bauml and Sorgel (2008).

Lunner and Hellgren (1991) proposed a uniform filterbank based on Interpolated FIR (IFIR) filters. A prototype low pass FIR filter $H(z)$ of order $N-1$ was designed using the Parks-McClellan algorithm. It was interpolated with a factor of L. The interpolation factor was decided based on the number of bands required. A complementary high pass filter, $H_c(z)$, was obtained using the equation:

$$H_c(z) = z^{(-(N-1)/2)} - H(z) \tag{2.1}$$

Both the filters have to be symmetric about $\frac{\pi}{2}$. The required uniform filter bank can be obtained by combining the interpolated high pass and low pass filters. Two sub-band filters H_{s1} and H_{s2} were used to separate each individual pass bands. The filter bank was tested in real-time on TMS320E25 general-purpose DSP platform. Stop band attenuation was 40 dB. The system gave a group delay of 4.4 ms at a sampling frequency of 12 kHz. NAL was used for fitting and a maximum fitting error of ±5 dB was obtained. Various asynchronous techniques for implementing a 7-band IFIR filter bank were discussed by Nielsen and Sparso (1999). Later, Onat et al. (2000), proposed a delay optimisation technique for the IFIR filter bank by selectively removing the unused last lobe of the complementary filter. However, when the stop band attenuation was increased from 40 dB to 60 dB, the group delay also increased to 8.9 ms.

McAllister et al. (1994) used frequency sampling filters. The system was based on a comb filter which combines with a bank of 167 resonators spaced at 50 Hz intervals over the frequency range 0 to 8.3 kHz. Later Li et al. (1996) came up with a non-uniform multirate filter bank. A prototype band was designed using Johnston's 32D Quadrature Mirror Filter (QMF). In this method, lower frequency octave bands were decimated to lower sampling rates. i.e., the signal was first split into two equal sub-bands, and the lower band was decimated and given to the two-channel filter bank. The lower band was again split into two and decimated. In this way, a 7-channel filter bank was obtained with decimation factors

2,4,8,16,32 and 64. The system was implemented on TMS320C50. The prototype filter specifications and algorithm performance metrics like delay, power, fitting accuracy, etc., were not reported for analyzing the performance of the system. A frequency-domain implementation of an oversampled, Weighted Overlap-Add (WOLA) filter bank was described in Brennan and Schneider (1998). Oversampling was used to avoid aliasing. In WOLA, a single prototype filter was replicated to 32 equal bands by DFT modulation. A group delay of 12.5 ms was reported. The advantages of a multidimensional logarithmic number system for hardware implementation were utilised by Li et al. (2002) and designed an 8-channel uniform filter bank structure using Kaiser-window based parallel FIR filters. An ASIC was designed using 0.18 μm technology and a power consumption of 1.175 mW was reported. The filter chip area was 0.605 mm^2. For an 8-channel uniform filter bank structure, the power consumption reported was comparatively high considering 0.18 μm technology node used for the design.

Wei and Lian (2004) proposed Frequency Response Masking (FRM) technique and designed a 10-band non-uniform filter bank. The main difference between the architecture proposed by Li et al. (1996) and FRM technique is that in FRM, two half band prototype filters were used instead of one. The Filter Bank has higher frequency resolution at lower and higher frequency bands and low resolution at center frequencies. The design gave a 40 dB stop band attenuation and a maximum matching error of ±5 dB. Even though the system may work well for higher frequencies, the resolution is inadequate for center frequencies in the speech spectrum which is more important. The same authors enhanced the performance of the filter bank and published a work on an 8-band filter bank using the same technique (Lian and Wei (2005)). Even though the stop band attenuation was increased from 40 dB to 80 dB, the number of multipliers required was increased only to 15 from 14 reported in the previous design. The authors tested the algorithm by directly matching five different standard audiograms for different hearing losses instead of matching with gain prescribed by any prescription formula. Still, the matching error was high (nearly ±14 dB) for mid frequencies.

In the human auditory system, the frequency is distributed non-uniformly in critical bands or the Bark scale (Zwicker (1961)). Chong et al. (2006) proposed a 16-band critical-like spaced filter bank for hearing compensation. The authors followed 110 tap Linear Phase structured FIR (LPFIR) technique to design each individual filter with a stop band attenuation of 60 dB. The complexity was reduced by pre-calculating a set of intermediate signals which are common to all the filters. An ASIC was designed using 0.35 μm tech-

nology and an area of 1.62 mm^2 and power consumption of 247.5 μW were reported. The design achieved a power reduction of 47% and area reduction of 37% over a direct implementation of 16 channel logarithmic number system filter bank. However, the authors did not mention about the performance of the filter bank in terms of audiogram fitting and filter specifications. It may be difficult to get the expected frequency response due to the highly irregular distribution of the frequency bands.

Kuo et al. (2007) proposed the FIR implementation of 1/3 octave 18-band ANSI S1.11 filter bank from 157 Hz to 8 kHz. This system satisfies the class-2 specifications given in the standard (ANSI (2004)). Basically, the authors extended the technique proposed by Li et al. (1996). Three prototype filters of 1/3 octave from 4 kHz to 8 kHz along with a low pass decimation filter and an interpolation filter were designed using the Parks-McClellan algorithm. The filter orders were optimised by trial and error based iteration method to satisfy the specification. The lower order filters were derived from prototype filters by decimation and a decimation filter was used to band limit the down sampled signal. Before synthesis, an interpolation filter was used to remove the imaging frequencies generated due to up sampling. A comparison was done with traditional IIR implementations and FIR without multi-rate optimisation. An overall computation reduction of 96% was achieved over parallel structure with the same specifications. Since the common fitting procedures NAL-NL1 and NAL-NL2 also use 18-band 1/3 octave for gain prescription, authors claimed a zero fitting error. Hardware implementation of this algorithm was reported in (Kuo et al. 2010), which incorporated different low power techniques and used 0.13 μm technology. A power consumption of 178 μW was reported without clock gating and a supply voltage of 1.2 V. After applying clock gating technique, the power consumption got reduced to 155 μW and a further reduction to 122 μW was achieved when the supply voltage was reduced from 1.2 V to 0.6 V for the multiplier blocks. Later the same researchers reported that the group delay of the system is 78 ms (Liu et al. (2013)) which is not acceptable for hearing aid applications. So they reduced the delay to 10 ms by relaxing on transition band specifications at lower frequencies by keeping a fitting error of maximum 1.5 dB using an iteration algorithm. This caused an increase in algorithm complexity. Yang et al. (2014) reported the use of a poly phase matrix decomposition technique for reducing the number of multiplications. However, the delay got increased to 13.58 ms. Lai et al. (2015) designed the 18-band ANSI S1.11 filter bank by combining the two 9-band sub filter banks. The 9-band non-uniform filter bank was designed using a low pass filter and discrete cosine transform (DCT) modulation. The design reported a delay of 11.25 ms with a 72.8% reduction in

multiplication per sample compared to Liu et al. (2013).

A 33-band uniform poly phase filter bank with a channel spacing of 250 Hz and FFT length of 64 was proposed by Bauml and Sorgel (2008). The authors discussed the general requirements of filter banks for hearing aids and suggested that a uniform filter bank may be the best option considering the low computational complexity and lower delay performance. The authors focused on the design of a prototype filter based on various algorithms available in the literature and achieved a delay performance of 6.25 ms.

A 3-channel variable band IIR filter bank was proposed for hearing aid application by Deng (2010). The design was based on a variable low pass, variable band pass and variable high pass digital filters. The three filters were obtained from a Chebyshev type-1 low pass filter using frequency transformations. Only 11 multiplications and 14 additions were required for the entire system. The algorithm was tested using eight different audiograms and a maximum matching error of 3.44 dB was obtained. Along with the disadvantages of being IIR, the hardware implementation of the system may also be difficult considering the requirement of adjusting the bandwidth of each band according to each audiogram.

Wei and Liu (2011) introduced an adjustable sub-band distribution technique using FIR filters. The entire spectrum was divided into three schemes and three sections, effectively giving 27 possible combinations to choose from and can go up to a maximum of 9-bands. This was achieved by interpolation, coefficient decimation and frequency response masking applied on three prototype filters. The disadvantage of this filter structure is that in hardware implementation, it may be difficult to decide between different combinations and may not work well for all types of hearing losses.

From the literature on filter banks, it can be observed that, FIR filters are preferred over IIR for hearing aid application. Initially uniform structures were used. The research interest has changed towards non-uniform structures in recent years. Most of the the latest literature concentrates on 1/3-octave ANSI S1.11 18-band structure as it perfectly matches with the popular non-linear gain prescription procedures' frequency resolution. Even though adjustable variable band structures are recently introduced in hearing aid research, it is still in the algorithm stage.

2.8 Dynamic Range Compression (DRC)

Dynamic Range Compression was introduced in audio processing to compress the high dynamic range of original recorded signals into a highly limited range of channels in FM and

AM radio transmission. In earlier days, compression was done manually by adjusting the loudness when the signal level exceeds the maximum level of the channel. In manual compression, the response time was large. A delay of 1 second was considered fast. Blesser (1969), described the transition from manual to automatic DRC and the effect of time constants on the intelligibility of speech. Attack time should be as small as possible to avoid transients. With a long release time and short attack time, the gain decreases rapidly, but it recovers slowly. In order to prevent the effects produced by changing gain, the compressor must be designed in such a way that the transients should not dominate the shape of the envelope and the balance between different phonemes should not get affected, i.e., the compressor algorithm should not affect the spectral contrast badly. The author also identified a change in effective compression ratio, CR_e, during the attack and release phases as given below:

$$CR_e = 1 + (CR - 1)T/(k.t_r) \quad for \;\; T < k.t_r \tag{2.2}$$

where CR is the compression ratio, t_r is the release time and k is a constant. Since this change is happening only during the attack and release phases, its effect is negligible.

As the audio processing started shifting from the analog domain to the digital domain, digital techniques for DRC were also introduced. McNally (1984), described the underlying concepts of basic digital DRC for audio. Dynamic characteristics of a DRC were defined for the signal level sensing circuitry. Depending on the application, it can be of peak detecting or RMS detecting type. In both the cases, the basic structure is that of a first-order low pass recursive digital filter. The transfer function of the structure, H can be given as:

$$H(z) = \frac{a}{1 - (1 - a)z^{-1}} \tag{2.3}$$

where the filter coefficient a determines the speed of the algorithm. The static characteristics decide the amount of compression to be applied at different input levels in the log domain. The compression ratio decides whether the algorithm should act as a compressor, expander or limiter. McNally also discusses the quantisation effects that occur during hardware implementation of logarithm and antilogarithm functions using the look-up table method. A smoothing stage at the output was proposed to overcome these errors. The algorithm was tested on a BBC designed programmable audio signal processor COPAS-2. A worst-case measurement error of 0.8 dB was obtained.

Floru (1999) carried out a mathematical analysis of the analog RMS detector. The author compared the feed-back and feed-forward compressors in the linear domain and log-

domain configurations. It was proved that the transfer functions of both configurations are equivalent. The same output can be obtained with the algorithm implemented either in linear domain or in log domain with proper transformation of the compression ratio. In feed-back compression, the time constant got reduced by the compression ratio. Moreover, the dynamic range of input was also limited compared to the feed-forward compression.

A multiband DRC algorithm was implemented on a fixed point platform TMS320C54X by Magotra et al. (2000). The single pole IIR based RMS detector was used for level detection:

$$p(n) = \beta p(n-1) + (1-\beta)x^2(n) \tag{2.4}$$

where β is the smoothing constant, $x(n)$ is the input signal sample and $p(n)$ is the estimated signal power. β can be calculated approximately from:

$$n_\tau = 1/(1-\beta) \tag{2.5}$$

where n_τ is the number of samples and can be obtained as product of sampling frequency and the time constant. The gain was calculated from a compression curve having three regions of operation: linear, compression and saturation. In linear, the gain is 1 and in the saturation region, the output is constant irrespective of change in input signal power. The compression was done in linear domain using non-linear equations and implemented using Taylor series approximations. This, in turn increased the complexity and caused larger quantisation errors for higher dynamic range.

Abel and Berners (2003) described the equations for feed-back and feed-forward compression topologies in digital domain and proved that both can be implemented using same architecture with an additional factor of compression ratio in the calculation of time constants. The gain was calculated in log domain instead of in linear domain as in Magotra et al. (2000) for compression region based on the compression curve as shown in Figure 2.4. From the piecewise curve in log domain, the gain, g, can be given as the difference between output and input SPL.

$$g = l_O - l_I \tag{2.6}$$

and the output level, l_O, can be given as:

$$l_O = l_T + \frac{(l_I - l_T)}{\rho}, \quad l_I \geq l_T \tag{2.7}$$

where ρ is the compression ratio and l_T is the threshold level. Combining (2.6) and (2.7),

forward gain g_F can be obtained as:

$$g_F = (\frac{1}{\rho} - 1).(l_I - l_T), \quad l_I \geq l_T \tag{2.8}$$

After converting to linear domain, the compression gain in linear domain, $\phi_F(\lambda)$, is given as:

$$\phi_F(\lambda) = (\lambda/\lambda_T)^{(\frac{1}{\rho}-1)} \tag{2.9}$$

where λ and λ_T are the detected input level and threshold value in linear domain. For the feed-back topology, expressing (2.8) in terms of output level, the gain, g_B can be given as

$$g_B = (1 - \rho).(l_O - l_T), \quad l_I \geq l_T \tag{2.10}$$

$$\phi_B(\lambda) = (\lambda/\lambda_T)^{(1-\rho)} \tag{2.11}$$

where λ is the detected output level and $\phi_B(\lambda)$ is the compression gain in linear domain. As in the case of analog compressors, in the digital domain also the dynamic range is limited for feed-back compressors when compared to feed-forward compressors.

Cassidy (2004) proposed an equal-loudness filter to compensate for the variations in loudness perception shown by the human auditory system for different frequencies to get better performance from DRC. A typical DRC system with a recursive filter based level detector was used. The attack and release time constants were calculated by equating the unit step response of the system to the required final value according to definitions. The

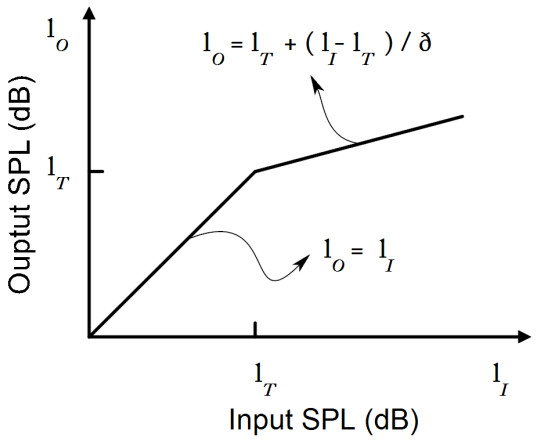


Figure 2.4: Gain compression curve (Abel and Berners (2003))

unit step response, $s_l(n)$, of the system in the digital domain was given as:

$$s_l(n) = (1 - (1 - \alpha_a)^{(n+1)})u(n) \tag{2.12}$$

where α_a is the attack time constant. Chang et al. (2010), described a complete DRC algorithm including its power optimised hardware implementations. The authors used a smoothing filter at the gain stage to remove ripples generated from the word length effects. The signal level was detected using a 4 ms time constant and which was selected in such a way that it is lesser than the short term stationary period of speech and longer than the fundamental period of sound waves. The attack and release time constants were incorporated in the smoothing stage instead of the level detection stage. The smoothing filter compared the current gain and the gain obtained in the previous step and if the difference is more than a small threshold value, the new gain was updated using a recursive filter as in level detection.

$$cg(n) = \begin{cases} \alpha.cg(n) + (1 - \alpha).tg(n - 1), & \text{if } cg(n) - tg(n - 1) > th \\ \beta.cg(n) + (1 - \beta).tg(n - 1), & \text{if } cg(n) - tg(n - 1) < th \end{cases} \tag{2.13}$$

where α and β are the attack and release time constants, th is the threshold and cg and tg are current gain and target gain respectively. The disadvantage with this technique is that the effective attack time and the release time get affected by the time constant used in the smoothing stage. Giannoulis et al. (2012), has done a study of various techniques in DRC and observed the lag in the release phase but did not propose any modification to overcome it.

2.9 Summary

The primary motivation for our research is that there is a need for the development of a high user value hearing aid for people who are suffering from hearing loss. A literature survey was done on the design requirements of a hearing aid chip and various signal processing algorithms used in a digital hearing aid. The area, power and delay requirements make the algorithm selection and development harder for a hearing aid application. Study on current filter bank algorithms suggests that a better trade-off has to be made between delay and computational complexity. Dynamic range compression algorithms follow a traditional recursive filter based method, which was originally developed for digital audio processing. An improved method for the estimation of attack time and release time is required to get

better control over these dynamic parameters. Hence, we decided to work on the design and hardware implementation of the filter bank and dynamic range compression algorithms which satisfy the requirements of a hearing aid. Customer satisfaction studies show that there is a need for a better noise reduction algorithm. A detailed subjective evaluation and performance verification before going for the hardware implementation of noise reduction algorithms would be time consuming and hence not attempted.

Chapter 3

Dynamic Range Compression Algorithm

Dynamic range compression(DRC) algorithm is used to bring down the dynamic range of normal audible sounds to the reduced range of hearing impaired persons. A pictorial representation of the DRC concept is shown in Figure 3.1. People having normal dynamic range can hear both loud and soft sounds as shown in part A in Figure 3.1. People with sensory neural hearing impairment cannot hear low-intensity sounds, whereas their upper threshold of hearing will stay unaltered (part B in Figure 3.1). When we apply the prescription gains according to the hearing loss, the signal level of too loud sounds goes beyond the

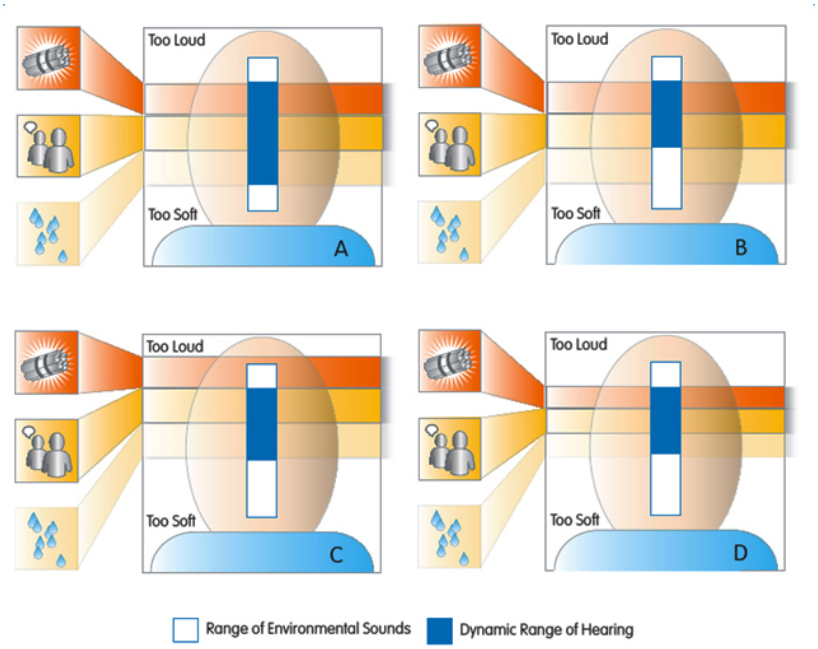


Figure 3.1: Dynamic range compression (DRC) pictorial representation (Banerjee (2011))

upper threshold of hearing as shown in part C of Figure 3.1. Dynamic range compressor protects the residual hearing of such individuals by compressing the output signal level to a reduced range as shown in part D of Figure 3.1. The rate at which the compression is to be applied and removed is decided by the time constants termed as attack and release time. Based on these time constants, the values of the envelope tracking decay coefficients are calculated. In general-purpose DRC algorithms, the coefficients are estimated based on input signal level, whereas, in hearing aid specifications, the attack and release time constants are defined in terms of output signal level (ANSI (2003)). If the input signal level based coefficient estimation method is followed, the compression applied at the gain stage alters the expected value of the time constants considerably. Hence modifications are to be made in the estimation of decay coefficients to get an accurate measure of the output signal at the expected instant of time. Novel contributions of this chapter are:

- New expressions are proposed to estimate the attack and release time decay coefficients to meet the specifications given in the ANSI S3.22 standard for hearing aids.
- Different DRC architectures for which the new parameter estimation methods are proposed, are implemented using UMC 65 nm standard cell libraries and power and error performance evaluated to choose the best one for low power hearing aid application.
- The results show that the RMS detector based DRC consumes more power, but does not provide significant improvement in error performance over the absolute detector based architecture. Inclusion of smoothing stage helps to keep the approximation error below 0.1 dB, but the power consumption increases by a significant factor.

3.1 Background

The effect of time constants on speech intelligibility has been an interesting topic among researchers for a long time. As mentioned in section 2.8, long release time and short attack time are preferred for better speech quality where, the gain can decrease rapidly, and recover slowly. At the same time, attack time should be long enough to avoid transients. Even small differences in attack time can cause damage to the spectral contrast and speech intelligibility in the case of hearing aids (Schaub (2008)). Neuman *et al.* studied the effect of release time on sound quality using different compression ratios with different background noise (Neuman et al. (1995), Neuman et al. (1998)). It has been observed that different

release times give different levels of pleasantness with different combinations of compression factors and background noises. A detailed comparison of slow-acting and fast-acting compressors based on subjective tests are given in (Stone et al. (1999)). Fast attack time is needed in the range of 1 ms to 10 ms to protect the users from intense transient sounds like a door slamming or cup falling. The discussions on the merits and demerits of fast-acting compressors or syllabic compressors, i.e., attack time in the range of 2-10 ms and release time in the range of 20-150 ms diverge. Speech in quiet situations can be understood better for a wider dynamic range using syllabic compressors. Subjective studies show that syllabic compressors, affect the intelligibility adversely in noisy environments (Stone and Moore (2004)). At the same time, some studies conclude that fast-acting multichannel compression improves speech intelligibility in noisy backgrounds having spectral and temporal dips (Moore et al. (1999)). So a better control over the time constants is important to make the hearing aid output more intelligible in different situations.

It is already mentioned in section 2.8 that the basic concepts of digital DRC algorithm was first reported in McNally (1984). The author has studied the artifacts that can be created by the quantisation errors at various stages of hardware implementation and recommends a smoothing stage to reduce it, but the impact of power overhead and the change in effective time constants due to second stage filtering were not discussed. The feed-forward topology is preferred over feed-back as it provides better stability and higher dynamic range by Abel and Berners (2003). Therefore, feed-forward topology is used for our study.

In practical DRC algorithms, the gain is applied in the log domain and there are various methods for implementing logarithms on hardware. We used a direct look-up table method (Chang et al. (2010)) since it is fast and consumes low power (Muller and Muller (2006)). A comparison of quantisation errors introduced by log tables of different resolutions is given in Chang et al. (2010). However, the authors have not given any analysis of the impact of the smoothing stage along with the log tables. Once the log resolution decreases, the quantisation error increases, and the need for the smoothing stage increases.

3.2 Basics of DRC Algorithm

Dynamic Range Compressors have two stages of processing- A level detection stage and a gain stage. There can be a smoothing stage also to reduce the unwanted wordlength error of hardware approximations (McNally (1984)). The block diagram of a feed-forward DRC topology is shown in Figure 3.2. The level detector estimates the incoming signal level.

Depending on the input signal level, the gain stage calculates the amount of compression to be applied based on an input-output(I/O) curve, which will be obtained from different gain prescription formulas corresponding to the particular audiogram of the hearing impaired person. A sample I/O curve is shown in Figure 3.3 in which the input and output SPL are specified in decibel (dB). I/O curve is defined by the static characteristics: compression threshold (CT) and compression ratio (CR). CT decides the level at which the compression is to be applied and CR is the ratio of change in input SPL to change in output SPL (ANSI (2003)). Compression factor (CF) is the reciprocal of compression ratio, i.e., change in output SPL to change in input SPL. According to ANSI S3.22 specifications for hearing aids, the attack time is defined as the time it takes to reach within 3 dB of the final value of output for an input signal changing from 55 dB to 90 dB. Release time is the time it takes to reach within 4 dB of the final value for an input changing from 90 dB to 55 dB ANSI (2003).

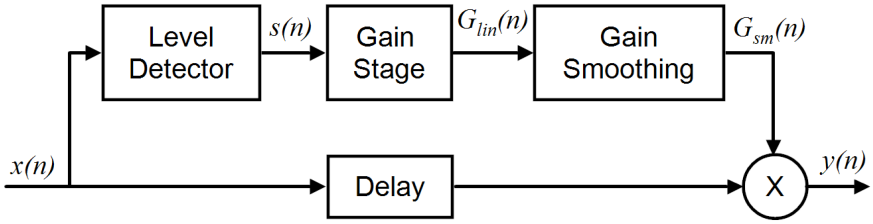


Figure 3.2: Basic block diagram of a feed-forward DRC

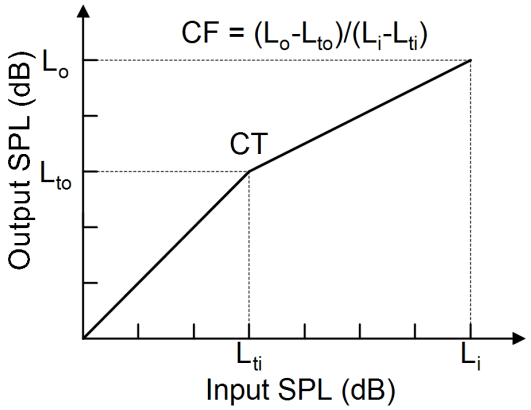


Figure 3.3: Static compression curve in the log domain

3.3 Proposed Methodology for the Estimation of Decay Coefficients

3.3.1 Level Detection

The incoming signal level can be detected based on its absolute amplitude or the Root Mean Square (RMS) value. A low pass single-pole IIR filter is used to estimate the signal, averaged over a period depending on attack or release time constants. The input to the filter can be either the instantaneous absolute value (absolute detector) or the squared value of the input signal level (RMS detector). In the case of an absolute detector (Cassidy (2004)):

$$p(n) = \begin{cases} \alpha p(n-1) + (1-\alpha)|x(n)|, & \text{if } |x(n)| \geq p(n-1) \\ \beta p(n-1) + (1-\beta)|x(n)|, & \text{if } |x(n)| < p(n-1) \end{cases} \tag{3.1}$$

For RMS detector:

$$p(n) = \begin{cases} \alpha p(n-1) + (1-\alpha)x^2(n), & \text{if } x^2(n) \geq p(n-1) \\ \beta p(n-1) + (1-\beta)x^2(n), & \text{if } x^2(n) < p(n-1) \end{cases} \tag{3.2}$$

where α and β are attack and release phase decay coefficients. $x(n)$ is the input signal amplitude at n^{th} sample instant and $p(n)$ is the corresponding input SPL in linear scale. α is obtained in conventional methods by equating the unit step response of the above filters to -3 dB (Cassidy (2004)) as specified in section 3.2.

$$1 - \alpha^{N_a+1} = 10^{-3/20} \tag{3.3}$$

If a similar method is followed, and by using the theory of transients (Valkenburg (1964)), then β can be obtained by equating the unit step response to -4 dB of the final value as:

$$\beta^{N_r+1} = (10^{((CT+4)/20)} - 10^{FV/20})/(10^{IV/20} - 10^{FV/20}) \tag{3.4}$$

It is to be noted that the system will be in the release phase, only until the estimated input SPL crosses the compression threshold, CT. IV and FV are initial and final values of input SPL in dB. Number of samples, N_a and N_r corresponding to required attack and release

time constants, t_a and t_r respectively, are obtained as,

$$N_a = f_s * t_a \tag{3.5}$$

$$N_r = f_s * t_r \tag{3.6}$$

where f_s is the sampling frequency.

In the gain stage, the compression is applied in the log domain. So the input level measured in the linear domain is converted to log domain as

$$s(n) = 20 \log_{10}(p(n)) \tag{3.7}$$

in the case of absolute detector and

$$s(n) = 10 \log_{10}(p(n)) \tag{3.8}$$

in the case of RMS detector.

3.3.2 Gain Calculation

Gain stage calculates the compression to be applied based on the input level detected in the previous stage. The gain equation is obtained from I/O curve for a feed-forward compressor as follows (Abel and Berners (2003)):

$$G_{dB}(n) = (CF - 1)(s(n) - CT) \tag{3.9}$$

$$G_{lin}(n) = 10^{(G_{dB}(n)/20)} \tag{3.10}$$

where G_{dB} and G_{lin} are the calculated gain in log and linear domains respectively. The delayed input signal is multiplied with the estimated gain to get the final output, $y(n)$.

$$y(n) = G_{lin}(n)x(n - D) \tag{3.11}$$

where D is the total processing delay of the entire DRC system.

3.3.3 Effect of Compression Factor on Decay Coefficients, α and β and Proposed Modifications to Compensate the Effect

It can be observed from equation (3.9) that the gain is related to input SPL, $s(n)$, by a factor $(CF - 1)$. This effect of CF on $s(n)$, causes the output to reach the expected value faster than the desired time constants, t_a and t_r.

Accurate estimation of the decay coefficients α and β can be obtained by the following equations:

$$1 - \alpha^{N_a+1} = 10^{(-(3+\delta_a)/20)} \tag{3.12}$$

$$\beta^{N_r+1} = (10^{((CT+4+\delta_r)/20)} - 10^{FV/20})/(10^{IV/20} - 10^{FV/20}) \tag{3.13}$$

where the values of offsets δ_a and δ_r are obtained as:

$$\delta_a = (FV - 3) - \frac{(FV * (1 - CF) - 3)}{(1 - CF)} \tag{3.14}$$

$$\delta_r = \frac{(CT * (1 - CF) + 4)}{(1 - CF)} - (CT + 4) \tag{3.15}$$

In the RMS detector, the output will reach steady-state faster since the input is squared. Accordingly, input SPL with offset should be squared in equations (3.12) and (3.13) for finding the decay coefficients for an RMS detector. The following equations will give accurate coefficients for an RMS detector.

For attack phase:

$$1 - \alpha^{N_a+1} = 10^{(-(3+\delta_a)/10)} \tag{3.16}$$

and for the release phase:

$$\beta^{N_r+1} = (10^{((CT+4+\delta_r)/20)} - 10^{FV/20})^2/(10^{IV/20} - 10^{FV/20})^2 \tag{3.17}$$

Consider the example in Figure 3.4 of a particular test signal with CT and CF set as 70 dB and 0.5 respectively. Once the instantaneous input signal crosses CT, the system goes to attack phase. Output reaches within -3 dB of its final value when the input reaches within $-(3 + \delta_a)$ of its final value, i.e., in this example, 84 dB with $\delta_a = 3$ for a CF of 0.5. The moment the instantaneous input intensity goes below the threshold value, the system goes to release phase but still under compression until $s(n)$ reaches CT. Output reaches -4 dB of its steady-state value, i.e., in this case, 51 dB when $s(n) = (CT + 4 + \delta_r)$ which is

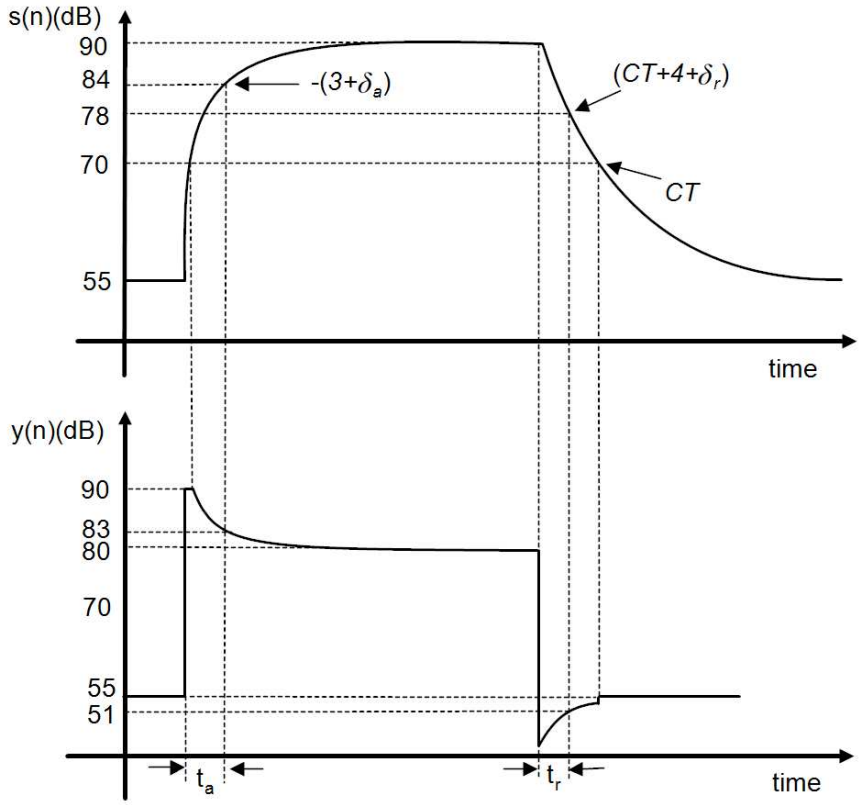


Figure 3.4: Attack and release time plot corresponding to a sample estimated input curve $s(n)$

78 dB with δ_r=4 for a compression factor of 0.5.

In the case of above example, attack and release phase decay coefficients for an RMS detector can be obtained as given below.

$$1 - \alpha^{N_a+1} = 0.2512 \tag{3.18}$$

$$\beta^{N_r+1} = 0.0564 \tag{3.19}$$

3.3.4 Smoothing

A smoothing filter can be used after converting the gain from the log domain to the linear domain to remove the approximation errors introduced at various stages of hardware implementation. The difference between smoothed gain and the actual gain is compared with an

error threshold (G_{th}) and passed through a similar first-order filter as in level detection.

$$G_{sm}(n) = \begin{cases} \alpha_{sm} G_{sm}(n-1) + (1-\alpha_{sm}) G_{lin}(n), \text{if } (G_{sm}(n-1) - G_{lin}(n)) \geq G_{th} \\ \beta_{sm} G_{sm}(n-1) + (1-\beta_{sm}) G_{lin}(n), \text{ if } (G_{sm}(n-1) - G_{lin}(n)) < G_{th} \end{cases} \tag{3.20}$$

where α_{sm} and β_{sm} are the attack and release phase decay coefficients for smoothing stage. G_{sm} is the gain at the output of smoothing filter.

Since there is a new set of coefficients introduced in the smoothing stage, the output reaches its steady-state slower than the actual expected value due to the impact of second-stage filtering. If equations (3.12) and (3.13) are used for coefficient estimation, then G_{lin} reaches within 3 dB and 4 dB points of its final values during the attack and release phases after $N_a + 1$ and $N_r + 1$ samples respectively. For example, consider a test signal as in Figure 3.4 which is sampled at 20 kHz and goes from 55 dB to 90 dB after 600 samples and from 90 dB to 55 dB after 1800 samples. Both attack and release time constants, t_a and t_r are chosen as 4 ms. Then N_a and N_r can be obtained as 80 samples from equations (3.5) and (3.6). The magnitude curve obtained from MATLAB® simulations for G_{lin} in dB is plotted in Figure 3.5. It can be observed that the gain curve reaches its 3 dB and 4 dB points (i.e., -7 dB and -4 dB corresponding to attack and release phases respectively, in the plot) after 81 samples each (i.e., at sample numbers 681 and 1881). In DRC with smoothing stage, second stage filtering is applied to this already filtered signal (G_{lin}), with a new set of coefficients (α_{sm} and β_{sm}). It will further delay the final gain curve G_{sm}. The number of samples (N_{asm} and N_{rsm}) and the smoothing stage decay coefficients (α_{sm} and β_{sm}) are also related by transient equations similar to (3.3) and (3.4) as given below:

$$(10^{(IV_{Glin}/20)} - 10^{(FV_{Glin}/20)})\alpha_{sm}^{N_{asm}+1} + 10^{(FV_{Glin}/20)} = 10^{(FV_{Glin}+3)/20} \tag{3.21}$$

$$(10^{(IV_{Glin}/20)} - 10^{(FV_{Glin}/20)})\beta_{sm}^{N_{rsm}+1} + 10^{(FV_{Glin}/20)} = 10^{(FV_{Glin}-4)/20} \tag{3.22}$$

Here, there is no effect of CF, so δ offset is not required. The total time to reach the expected output values will be $(N_a + N_{asm})$ and $(N_r + N_{rsm})$ samples in the case of DRC with the smoothing stage incorporated.

The accurate expected output for DRC with the smoothing stage can also be obtained using an empirical method as follows. If same coefficients are used for both the level detection and smoothing stages instead of using two separate decay coefficients for two phases of filtering, it is observed that the combination follows a linear relation with the required

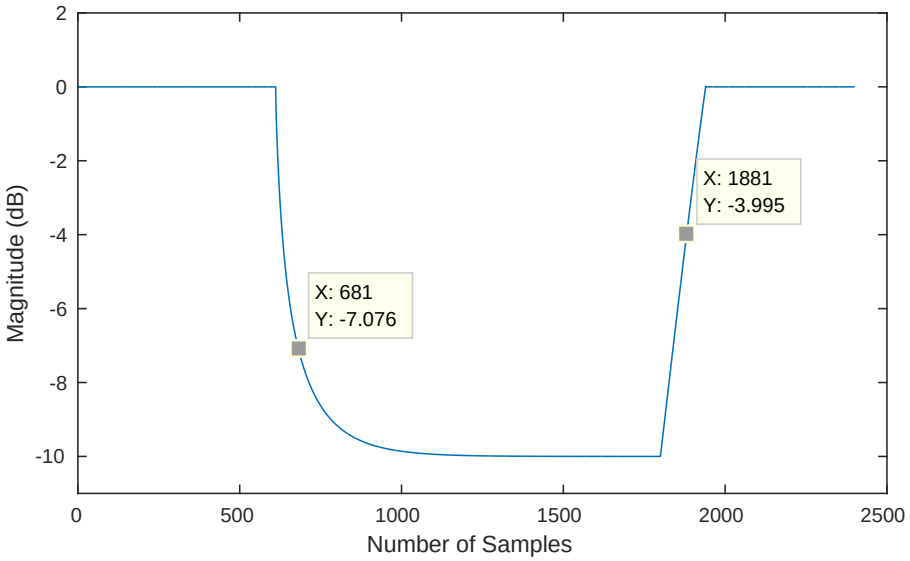


Figure 3.5: Plot of the gain curve for the test signal

single-stage time constant in both the attack and release phases in the case of the absolute detector. So new coefficients for DRC with smoothing stage incorporated can be obtained from the modified number of samples (N_{asm} for attack and N_{rsm} for release) as given below.

$$N_{asm} + 1 = 0.3039(N_a + 1) \tag{3.23}$$

$$N_{rsm} + 1 = 0.6177(N_r + 1) \tag{3.24}$$

In the case of the RMS detector, there is no squaring effect in the smoothing stage compared to level detection. So if we use equations (3.16) and (3.17) for the level detection stage and equations (3.12) and (3.13) for the smoothing stage, a linear relationship can be obtained with respect to single-stage expected decay coefficients. So for the RMS detector with smoothing stage, accurate coefficients can be obtained from a modified number of samples as given below.

$$N_{asm} + 1 = 0.2872(N_a + 1) \tag{3.25}$$

$$N_{rsm} + 1 = 0.6500(N_r + 1) \tag{3.26}$$

The linear plots to get the constants in equations (3.23) to (3.26) are obtained by varying the attack and release times from 4 ms to 10 ms, (expected number of samples from 81 to 201) as shown in Figure 3.6 for a CF of 0.5 and a sampling frequency of 20 kHz. The X-axis is the expected number of samples and Y-axis shows the number of the sample at which

the output reached the expected values using the decay coefficients derived from equations (3.12) and (3.13). The ratios of these expected and the actual number of samples are used as constants in equations (3.23) to (3.26) to get the modified number of samples N_{asm} and N_{rsm}.

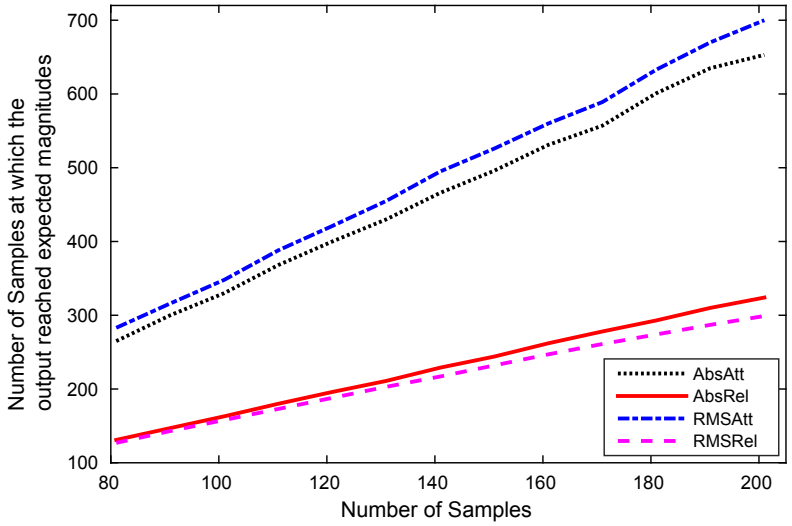


Figure 3.6: Number of samples plot for attack and release phases for finding the decay coefficients for smoothing stage. The legends can be interpreted as: *Abs*- Absolute detector based DRC; *RMS*- RMS detector based DRC; *Att*- Attack phase; *Rel*- Release phase

3.4 Hardware Implementation

The hardware architecture of the DRC algorithm with an absolute level detector is shown in Figure 3.7. The total processing latency, D added to the input is constituted by registers at different stages. All the coefficients and threshold values are stored using programmable registers. The architecture is designed in such a way that the data will be loaded and processing starts once all the programmable parameters are stored in corresponding registers. Input and all the coefficient registers are represented using 16-bit fixed-point arithmetic. In the case of absolute level detection based algorithm without the smoothing stage, five multiplications are needed including one constant multiplier. For RMS detector one extra multiplier is needed to get the squared value of the input signal.

The architectures are implemented with logarithm tables of 4-bit and 8-bit index resolution. Since the input is in 16-bit signed format, leading one's counter is used to reduce

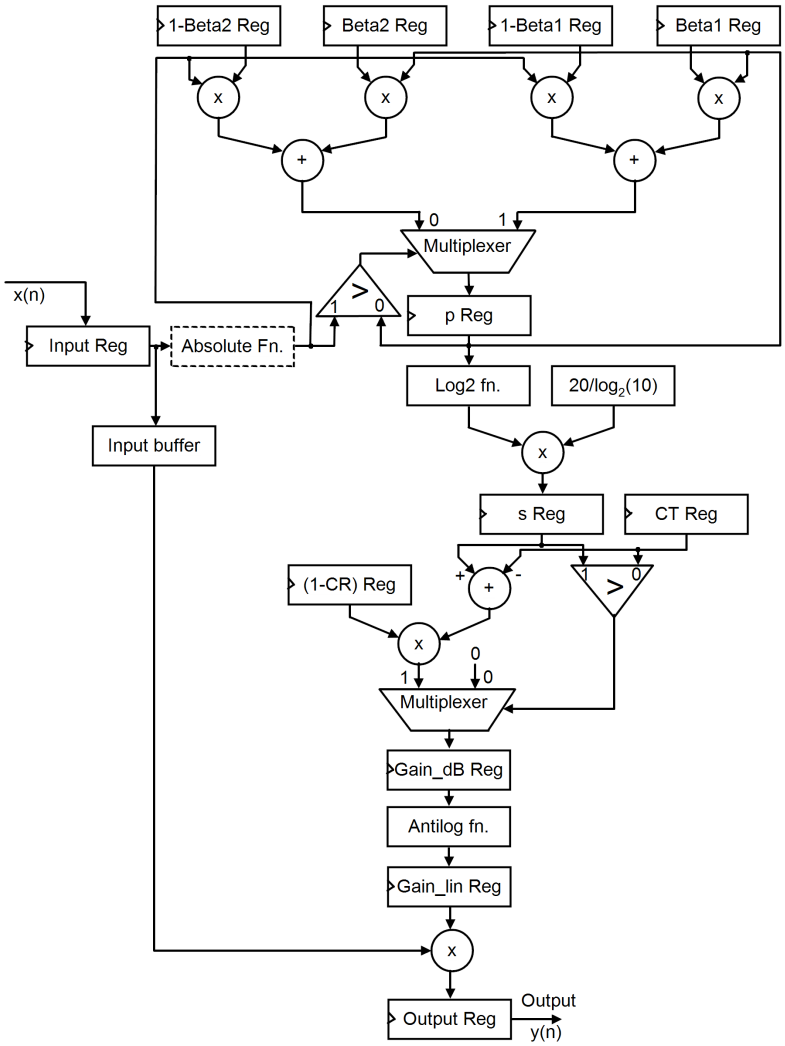


Figure 3.7: Hardware architecture of the absolute detector based DRC algorithm

the input bit width to the log table index width. The block diagram of the logarithm implementation is shown in Figure 3.8. Log table index (mantissa part of the measured input SPL) and the exponent parts are obtained from a priority encoder based address generator as shown in Figure 3.9, where w represents the width of the log table index and b represents the number of stages present in the priority encoder. In the case of 4-bit resolution table, an extra four stages are needed for leading one detector compared to 8-bit resolution table. This increase in address detection hardware, in turn nullifies the advantage of using a smaller look-up table (LUT) with lower depth and makes the power consumption for both the cases almost similar. But, as the LUT depth reduces, the quantisation error increases.

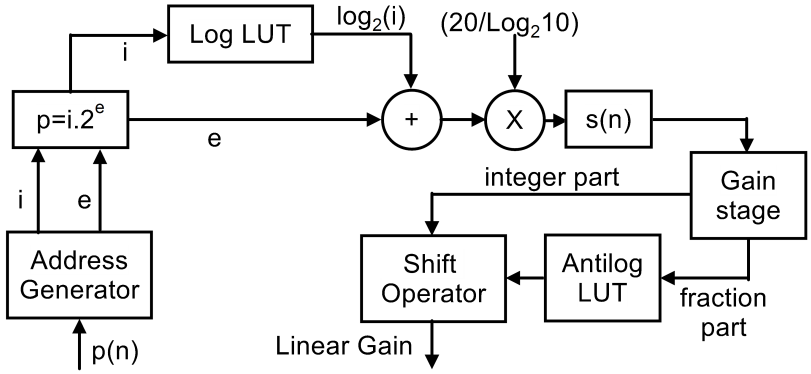


Figure 3.8: LUT based logarithm implementation

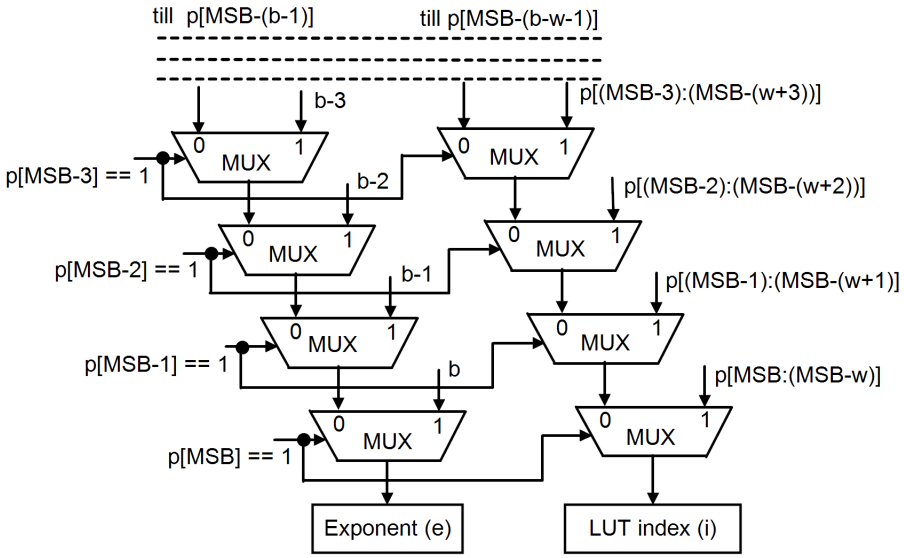


Figure 3.9: Priority encoder based address generator used for logarithm table

Hence, 8-bit resolution log table implementation gives better performance over 4-bit resolution log table considering both power and error values. In the case of RMS detector, *Absolute Fn.*, shown in the dotted box in Figure 3.7 is replaced by the squaring stage. The input range to the LUT gets scaled up from 15 bits to 30 bits due to squaring. This results in 15 extra stages in leading one's counter and an effective increase in hardware complexity. We used base-2 logarithm and antilogarithm tables as it gives more efficient hardware implementation (Muller and Muller (2006)). Base-2 log values are then converted to base-10 by the scaling factor and used in the gain stage. The antilog value of the fractional part of the gain in decibel was shifted according to the integer part to obtain the gain in the linear domain.

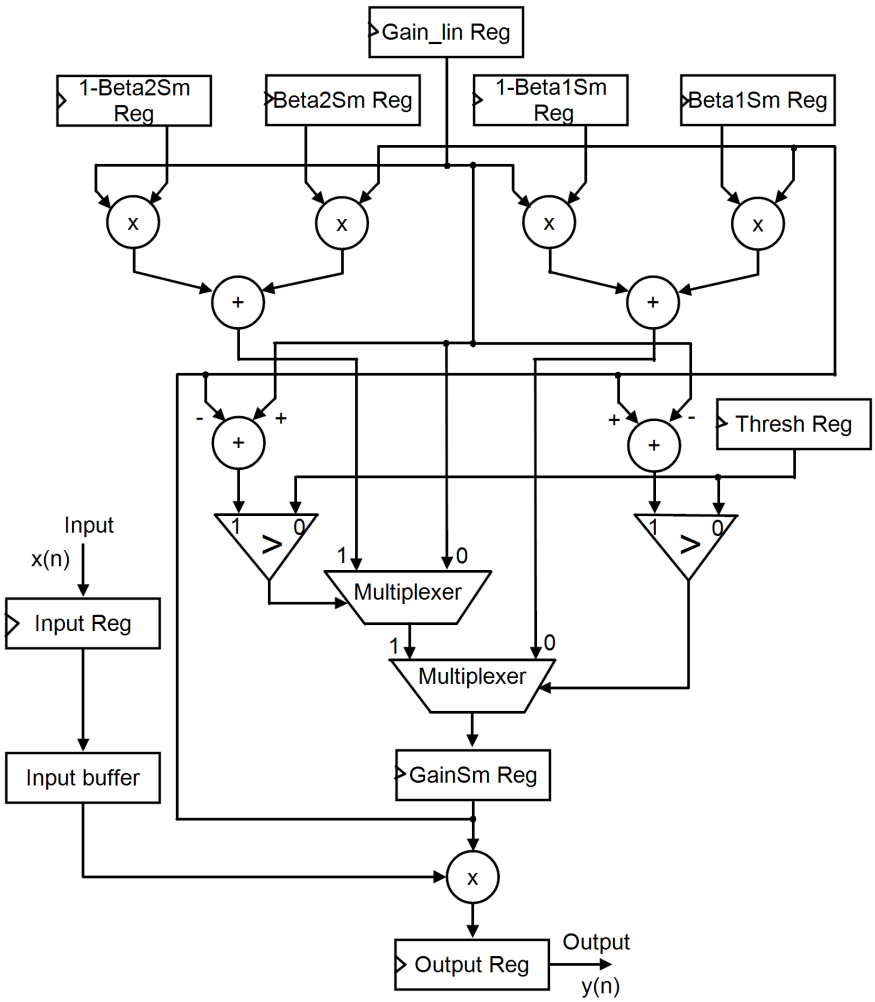


Figure 3.10: Hardware architecture of the smoothing stage

Hardware architecture of the smoothing stage is shown in Figure 3.10. In the smoothing stage, the difference between the DRC estimated gain from the gain stage (G_{lin}) and the smoothed gain (G_{sm}) is compared with a gain error threshold value, G_{th}. If the difference is greater than G_{th}, the smoothing filter is applied. $Thresh\_Reg$, the register used to store G_{th} shown in Figure 3.10 is also 16-bit wide. Since one register is used to store the smoothed gain, the input buffer stage length increases by one. In the smoothing stage, the major contribution of hardware complexity comes from two multipliers and two 16-bit subtractor based comparators along with the registers needed for storing smoothing filter coefficients, G_{th} and the final gain value.

3.5 Results and Discussion

A step signal sampled at 20 kHz was selected as a test signal according to ANSI S3.22 specifications for hearing aids. The signal changes from 55 dB to 90 dB at 600^{th} sample and comes back to 55 dB after 1800 samples, having enough time to reach steady-state during both attack and release phases. Different attack and release phase decay coefficients are estimated using both conventional (equations (3.3) and (3.4)) and proposed (equations (3.12), (3.13), (3.16), (3.17) and (3.23-3.26)) methods for an attack and release time constant of 4 ms. The estimated coefficient values are given in Table 3.1. All the simulations were carried out and proposed and conventional methods for coefficients estimation were verified using MATLAB® 2015.2. The error table with proposed and conventional methods

Table 3.1: Attack and release phase decay coefficients estimated using the modified algorithm for 4 ms transient period with a 20 kHz sampling frequency

Parameter	**Without smoothing**		**With smoothing**	
	Abs	RMS	AbsSm	RMSSm
Attack time constant	0.9914	0.9964	0.9729	0.9714& 0.9880
Release time constant	0.9824	0.9651	0.9733	0.9746& 0.9498

are given in Table 3.2. It can be observed that the proposed method gives error-free results while the conventional methods give errors as high as 3.06 dB. The output plots are shown in Figure 3.11. The figure shows that proposed methods perform as expected while conventional methods are not giving expected results during both attack and release phases for all the test cases.

Table 3.2: Output errors using conventional and proposed methods for decay coefficients estimated from output signal for the transient period of 81 samples for attack and release phases

Parameters	**Without smoothing**				**With smoothing**			
	Abs		**RMS**		**AbsSm**		**RMSSm**	
	conv	prop	conv	prop	conv	prop	conv	prop
Att. time const.	0.985	0.9914	0.985	0.9964	0.985	0.9729	0.985	0.9714&0.9880
o/p at 81^{st} sample (dB)	81.47	83	86.06	83	80.75	83	85.16	83
Error (dB)	-1.53	0	3.06	0	-2.25	0	2.16	0
Rel. time const.	0.9763	0.9824	0.9763	0.9651	0.9763	0.9733	0.9763	0.9746&0.9498
o/p at 81^{st} sample (dB)	52.548	51	49.533	51	48.96	51	47.27	51
Error (dB)	-1.548	0	1.467	0	2.04	0	3.73	0

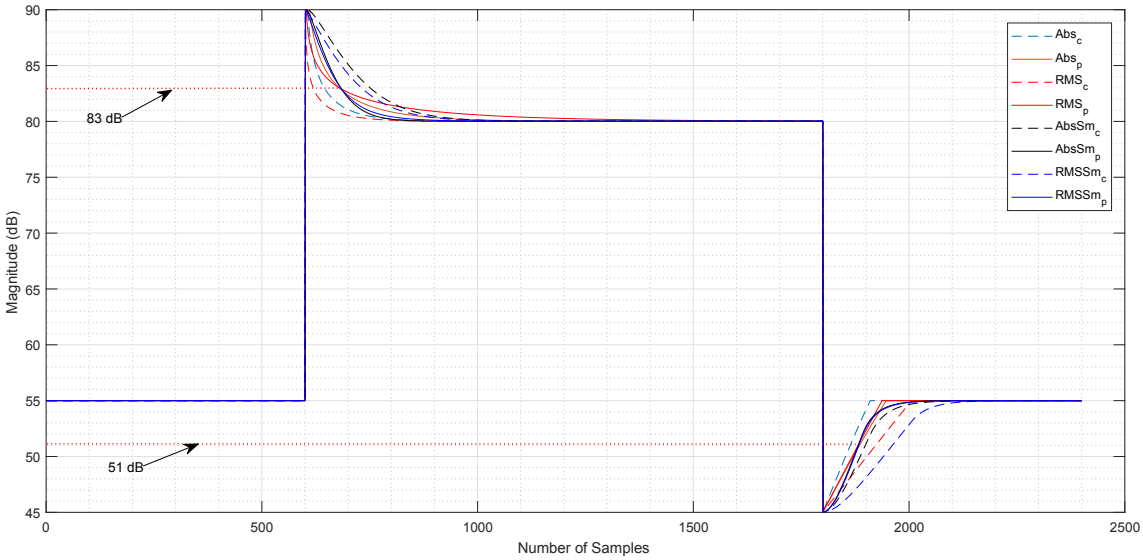


Figure 3.11: Output waveforms for proposed (solid lines) and conventional (dashed lines) methods of decay coefficients estimation. (Figure legends can be interpreted as follows: *Abs* - Absolute detector based DRC; *RMS* - RMS detector based DRC; *Sm* - DRC with smoothing stage included; $_c$ - conventional method; $_p$ - proposed method).

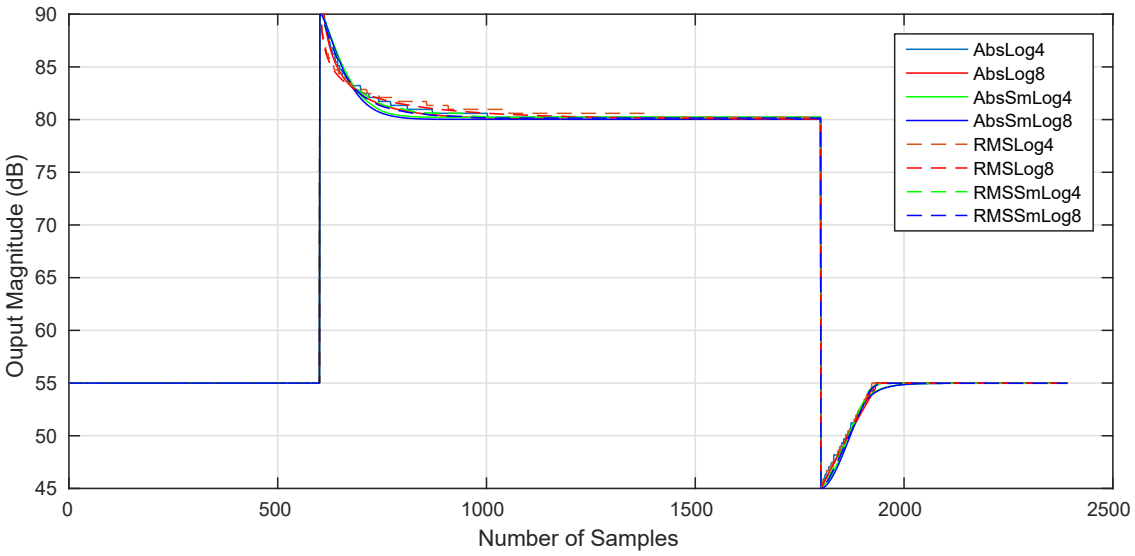


Figure 3.12: Output waveforms after post-layout simulation for different architectures

3.5.1 Hardware Implementation Results

All four architectures were described using Verilog Hardware Description Language, synthesised, placed and routed with Cadence Design tools using UMC 65 nm low power stan-

dard cell libraries. Clock frequency was chosen as 20 kHz which matches the practical sampling frequency of hearing aids. Output waveforms for a CF of 0.5 and CT of 70 dB from post-layout simulations are shown in Figure 3.12. All the outputs reach the expected value of 83 dB during the attack phase and 51 dB during the release phase in 4 ms. Post-layout core power analysis was done using Cadence Voltus^{TM} IC Power Integrity Solution with a constant switching activity and typical parasitic corner to get a uniform comparison of the architectures. All 4 architectures (i.e., DRC with absolute level detector and RMS level detector, without smoothing stage and with smoothing stage included) were compared with 4-bit and 8-bit resolution LUT based logarithm and antilogarithm implementations. Post layout power results are given in Table 3.3. From Table 3.3, it can be observed that the difference in power consumption for 4-bit and 8-bit resolution log tables is small in all the 4 cases. Since the log table is also hard-coded and synthesised inside the design module itself, the power estimate gives an overall view of the actual design. Considering the 8-bit resolution log implementation, the absolute detector based DRC with the smoothing stage consumes 58% more power compared to the one without the smoothing stage. Similarly, RMS detector based DRC with the smoothing stage consumes 21% more power compared to without the smoothing stage. Comparing the absolute detectors and RMS detectors, there is 67% increase in power consumption from absolute to RMS without smoothing stage and 28% increase when smoothing stage included. The synthesis report of the total number of standard cells for each architecture and the corresponding area are given in Table 3.4.

Table 3.3: Power consumption for different architectures

Log table resolution	**Without smoothing**		**With smoothing**	
	Abs(μW)	RMS(μW)	AbsSm(μW)	RMSSm(μW)
4 bit	2.416	4.054	3.881	5.02
8 bit	2.568	4.292	4.055	5.194

Table 3.4: Synthesised gate count and area report

	Without smoothing				**With smoothing**			
	Abs		**RMS**		**AbsSm**		**RMSSm**	
	Log4	Log8	Log4	Log8	Log4	Log8	Log4	Log8
Gate count	6054	7195	9475	10658	9035	10303	12537	13025
Area (μm^2)	19877	22269	31285	33650	29647	32088	41529	42347

3.5.2 Error Analysis

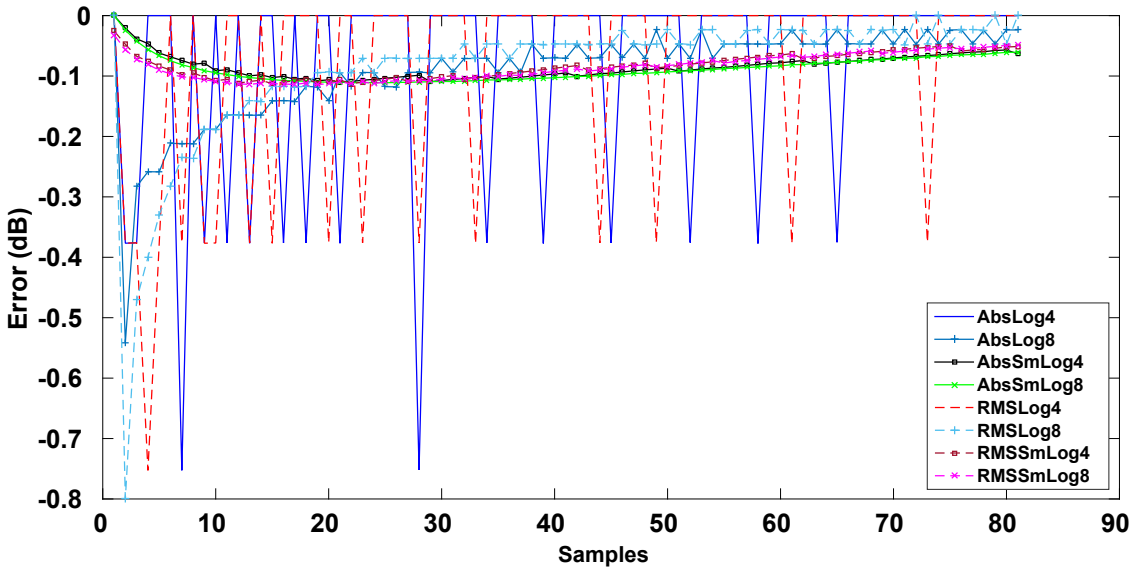
The attack and release transient periods of 81 samples are chosen for error analysis. The error plots are shown in Figure 3.13. Error below 0.2 dB is not detectable by humans (Chang et al. (2010), Zwicker and Fastl (2013)). Minimum approximation errors (during attack phase), maximum approximation errors (during release phase) and Root Mean Square Error (RMSE) for the combined transient period- attack and release phases are given in Table 3.5. After smoothing, the errors are less than 0.1 dB in all the cases. Considering the architectures without smoothing, maximum and RMSE are above 0.2 dB for 4-bit resolution log table. In the case of 8-bit resolution log table, the RMSE is around 0.1 dB and instantaneous errors go below 0.2 dB after the initial few samples, which can be observed in Figure 3.13. The layouts were not tested with different corners since we are making a relative comparison of power for different architectures and errors measured here are quantisation errors due to logarithm table resolution which are independent of corner cases.

Table 3.5: Final approximation errors estimated from the output signal for the transient period of 81 samples for attack and release phases

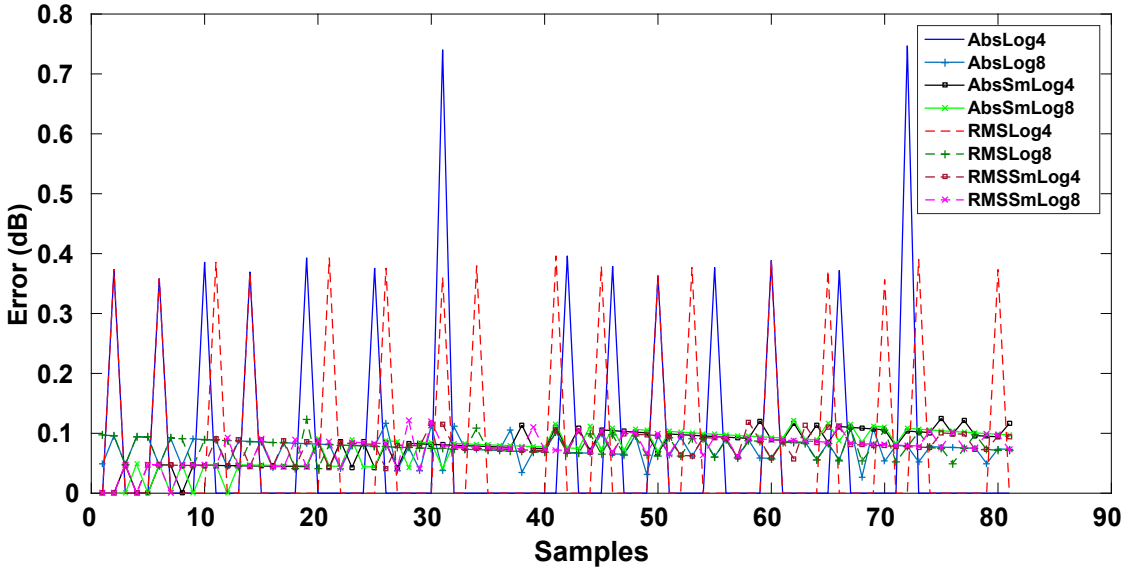
Error(*dB*)	**Without smoothing**				**With smoothing**			
	Abs		**RMS**		**AbsSm**		**RMSSm**	
	Log4	Log8	Log4	Log8	Log4	Log8	Log4	Log8
Min.(Attack phase)	-0.753	-0.541	-0.753	-0.799	-0.110	-0.111	-0.113	-0.114
Max.(Release phase)	0.747	0.117	0.396	0.124	0.125	0.122	0.119	0.122
RMSE	0.445	0.101	0.393	0.119	0.087	0.089	0.084	0.084

3.6 Summary

A new formula compensating the effect of compression ratio on the attack and release time decay coefficients for the dynamic range compression algorithm is presented in this chapter. An absolute detector based and an RMS detector based feed-forward architectures with and without smoothing stages were implemented using 4 bit and 8-bit resolution LUT based logarithm at hardware level using UMC 65 nm standard cell libraries. The approximation errors and the post-layout core power consumption were analysed for the 8 different approaches and a relative comparison was done. The results show that the proposed techniques give accurate expected output at required time instants while conventional methods give erroneous output values. Hardware comparison shows that there is no significant difference in power consumption with an increase in log table resolution, while the approximation error reduces



(a) Attack phase



(b) Release phase

Figure 3.13: Error plots during transient period for attack and release phases. (Legends for figures 11 and 12 can be interpreted as follows: *Abs* - Absolute detector based DRC; *RMS* - RMS detector based DRC; *Sm* - DRC with smoothing stage included; *Log*4 - DRC implemented with 4-bit resolution logarithm table; *Log*8 - DRC implemented with 8-bit resolution logarithm table.)

significantly. Smoothing stages can be included if a continuous gain transition is needed at the cost of increased power consumption. So we propose the use of an absolute level detector based DRC without the smoothing stage for lowest power consumption and overall performance, using modified decay coefficient estimation techniques for a low power hearing aid design. In applications where high quality of sound is important, a smoothing filter can be incorporated at the output stage.

Chapter 4

Proposed Filter Bank Algorithm and Hardware Implementation

Filter banks can be considered as the skeleton of any digital hearing aid. The quality of a hearing aid is mainly assessed by how close it fits the gain curve prescribed according to the hearing loss plotted in a patient's audiogram. For a hearing aid, the filter banks should be less complex as well as good enough to match the gain prescription provided by any of the fitting algorithms. Novel contributions of this chapter are:

- A new architecture for 1/3- octave ANSI S1.11 18-band filter bank using IFIR technique is proposed. The band edge frequencies are carefully designed by utilizing the maximum margin available to meet the ANSI specifications which reduce the prototype filter's order considerably.

- The entire filter bank is implemented using UMC 65 nm technology and the hardware design was tested using NAL-NL2 prescriptions for different audiograms.

- The filter bank combined with the proposed DRC architecture consumes 0.39 mW and the maximum matching error is within the acceptable range of 1.5 dB.

4.1 Hearing Aid Fitting and Sample Audiograms

An audiologist plots the audiogram for each hearing impaired patient to understand the severity of hearing loss. Most hearing tests analyse sounds between 125 Hz and 8 kHz and

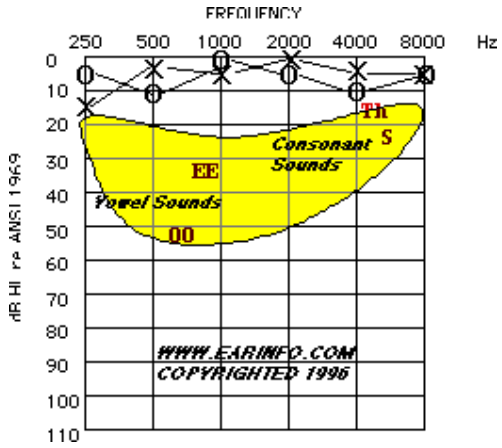
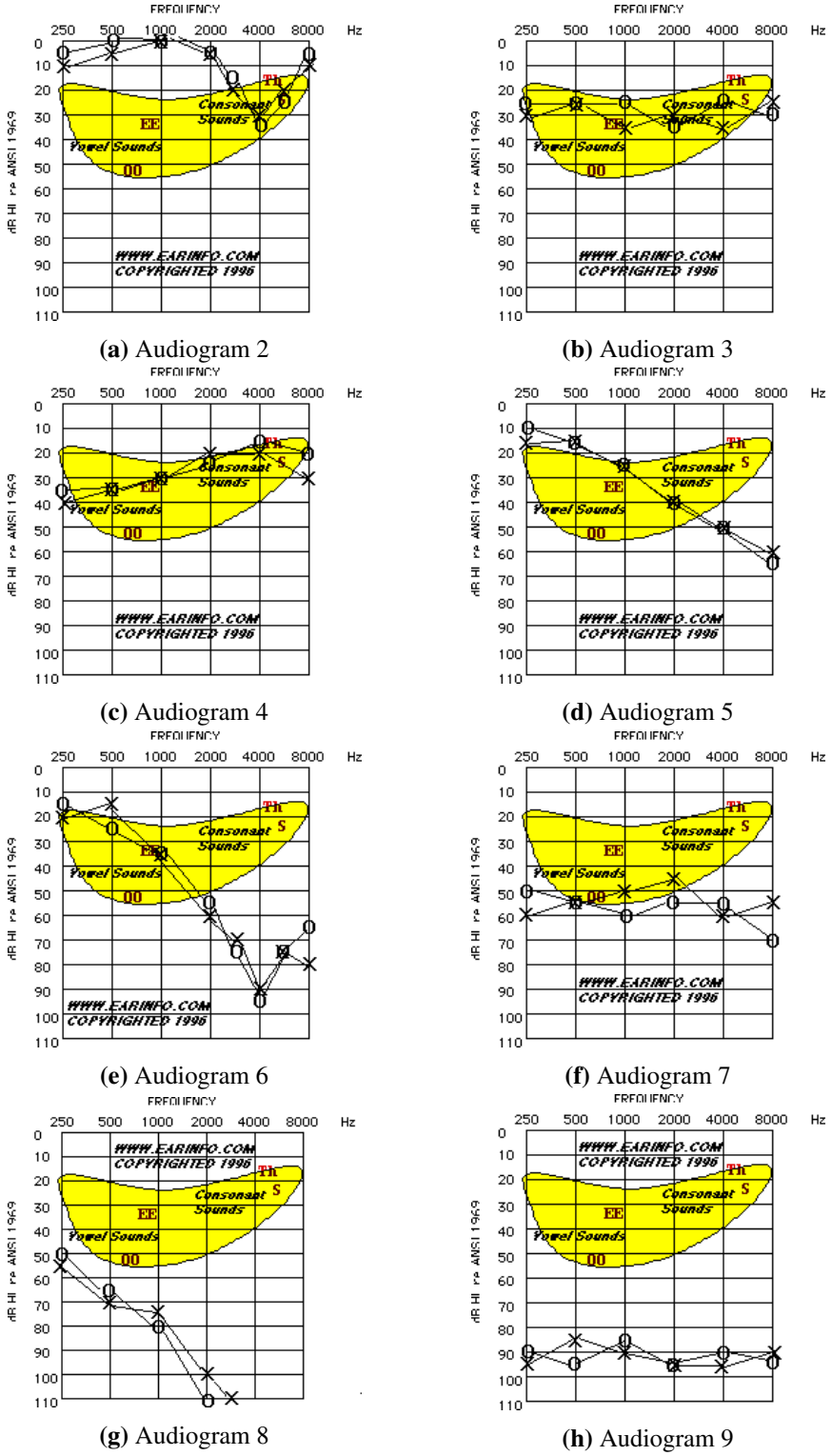


Figure 4.1: Audiogram 1 - Audiogram of normal hearing (Earinfo (2014))

from -10 dB to 120 dB Sound Pressure Level (SPL). An audiogram for a person with normal hearing is shown in Figure 4.1.

Audiograms for commonly found hearing losses are shown in Figure 4.2, (Earinfo (2014)). Audiograms 2 and 3 show mild hearing loss, whereas audiogram 4 shows mild to moderate hearing loss especially in lower frequencies. Audiogram 5 represents one of the most common types of hearing losses, increasing loss at higher frequencies. It is mainly due to aging. Audiogram 6 is very common among people working in noisy environments. Due to the severe loss at higher frequencies, it will be difficult to hear consonants which will make speech recognition difficult. Audiogram 7 shows moderate loss in all frequencies. Audiograms 8 and 9 show a severe or profound hearing loss. In such cases hearing aids will not help much unless spoken very close to the ear.

A hearing aid fitting software will be provided by every manufacturer which contains all configurable options available for the particular hearing aid. In hearing aid fitting, the insertion gains obtained from various prescription formulas are applied to different bands to fit the audiogram. An audiologist uses various prescription formulas for this purpose. Most commonly used ones are National Acoustics Laboratory-Non Linear1 (NAL-NL1) (Byrne et al. (2001)), NAL-NL2 (Keidser et al. (2011)) and Desired Sensation Level (DSL) Input/Output formula (Scollie et al. (2005)). These methods prescribe the insertion gains in terms of 1/3 octave bands from 160 Hz to 8 kHz, which closely match the spectral characteristics of the cochlea. The NAL-NL2 prescription for audiogram 6 corresponding to different input levels varying from 50 dB SPL to 80 dB SPL is shown in Figure 4.3.



(a) Audiogram 2

(b) Audiogram 3

(c) Audiogram 4

(d) Audiogram 5

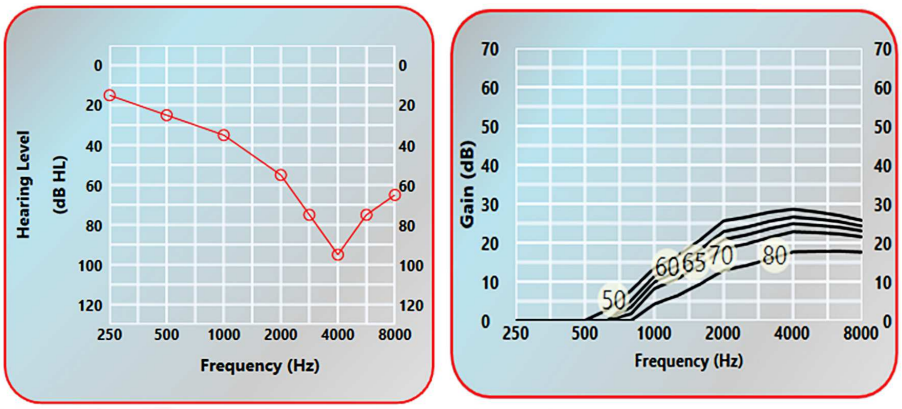
(e) Audiogram 6

(f) Audiogram 7

(g) Audiogram 8

(h) Audiogram 9

Figure 4.2: Sample audiograms showing different types of hearing losses (Earinfo (2014))



Audiogram NAL-NL2 Insertion Gain

Figure 4.3: A sample audiogram and its corresponding NAL-NL2 prescription gains

4.2 Background

Finite Impulse Response (FIR) filters are preferred over Infinite Impulse Response (IIR) filters because of their linear phase characteristics and inherent stability. Uniform or non-uniform filter bank architecture can be used and initially, uniform structures were used in hearing aids. In uniform filter banks, a large number of bands are required to get sufficient frequency resolution to match the audiograms at lower frequencies compared to non-uniform architectures. Research interest shifted to non-uniform architectures for hearing aid application in recent years.

ANSI S1.11 standard defines the specifications for 1/3-octave band pass filters from 25 Hz to 20 kHz (ANSI (2004)). A low complexity multirate ANSI S1.11 18-band filter bank was initially proposed for hearing aids by Kuo et al. (2010). The three prototype filters for the upper octave were designed using the Parks-McClellan algorithm. The remaining bands were derived from it using multirate technique. The algorithm suffers from a high group delay which is not acceptable for hearing aid application. Further modifications to multirate ANSI S1.11 18-band structure are proposed by Liu et al. (2013) and Yang et al. (2016) with reduced group delays. Both these architectures were following a relaxed version of ANSI S1.11 class-2 specifications.

The 18 bands from 157 Hz to 8 kHz are chosen from the ANSI S1.11 specifications for developing the algorithm, which covers the required audiogram frequency spectrum. The center frequency, f_{m_n}, of n^{th} band is defined as

$$f_{m\_n} = (G^{(n-30)/b})(f_r) \tag{4.1}$$

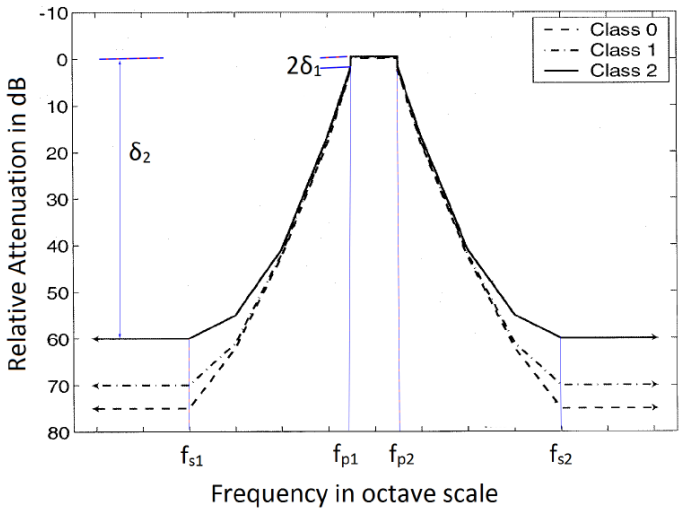


Figure 4.4: ANSI S1.11 octave band specifications (ANSI (2004))

where G is the octave ratio which is 2 for base-2 systems, n is the frequency band number and f_r is the reference frequency which is 1 kHz. For 1/3 octave b is 3. The band numbers corresponding to 157 Hz is 22 and that of 8 kHz is 39. The corresponding filter transfer functions are represented by H_{22} and H_{39} respectively. The lower and upper pass band edges of the filters are defined as

$$f_{p1\_n} = (G^{-1/(2b)})(f_{m\_n}) \tag{4.2}$$

$$f_{p2\_n} = (G^{+1/(2b)})(f_{m\_n}) \tag{4.3}$$

the pass band for each 1/3 octave is defined as $f_{p2\_n} - f_{p1\_n}$. The maximum pass band ripple (δ_1) for Class-2 filters is specified as ±0.5 dB for each band and minimum stop band attenuation (δ_2) is 60 dB. The stop band edge frequencies for 60 dB attenuation is specified as

$$f_{s1\_n} = 0.184 f_{m\_n} \tag{4.4}$$

$$f_{s2\_n} = 5.435 f_{m\_n} \tag{4.5}$$

The band specifications for ANSI S1.11 filter bank are shown in Figure. 4.4. The band edge frequencies of the 18 bands from 22 to 39 are given in Table 4.1

4.3 Proposed Methodology

The architecture of the proposed filter bank is shown in Figure 4.5. Parks-McClellan (PM) algorithm is followed for prototype filter design (Kaiser (1974)). The order of the filter in PM algorithm is given by

$$P \approx \frac{-10log_{10}(\delta_1\delta_2) - 13}{2.43B_{TW}} \tag{4.6}$$

where $B_{TW} = min(B_{TW1}, B_{TW2})$. B_{TW1} and B_{TW2} are transition bandwidths $(f_{p1} - f_{s1})$ and $(f_{s2} - f_{p2})$ respectively. Equation (4.6) shows that increasing the minimum transition bandwidth will decrease the order of the filter. According to ANSI S1.11 Class-2 specifications, the band edge frequencies for H_{22}, i.e., f_{s1_22}, f_{p1_22}, f_{p2_22} and f_{s2_22} are 29 Hz, 140 Hz, 177 Hz and 853 Hz respectively. Modifying the band edge frequencies according to the minimum of transition bandwidths, which is 111 Hz yields new specification as 29 Hz, 140 Hz, 177 Hz and 288 Hz. The direct FIR implementation for the above specification gives an order of 430, which will result in 216 multiplications per sample for band 22 alone and will cause a group delay of approximately 9 ms for a sampling frequency of 24 kHz.

Table 4.1: ANSI S1.11 band edge frequencies for the filters H_{39} to H_{22}

Band number (n)	Center frequency (f_{m_n}) (Hz)	f_{s1_n} (Hz)	f_{p1_n} (Hz)	f_{p2_n} (Hz)	f_{s2_n} (Hz)
39	8000	1472	7127	8980	43478
38	6300	1159	5612	7072	34239
37	5000	927	4490	5657	27391
36	4000	736	3563	4490	21739
35	3150	584	2829	3564	17255
34	2500	464	2245	2829	13696
33	2000	368	1782	2245	10870
32	1600	292	1414	1781	8625
31	1250	232	1122	1414	6848
30	1000	184	891	1123	5435
29	800	146	707	891	4315
28	630	116	561	707	3424
27	500	92	445	561	2717
26	400	73	354	446	2158
25	315	58	281	354	1712
24	250	46	223	281	1359
23	200	36	176	222	1076
22	160	29	140	177	856

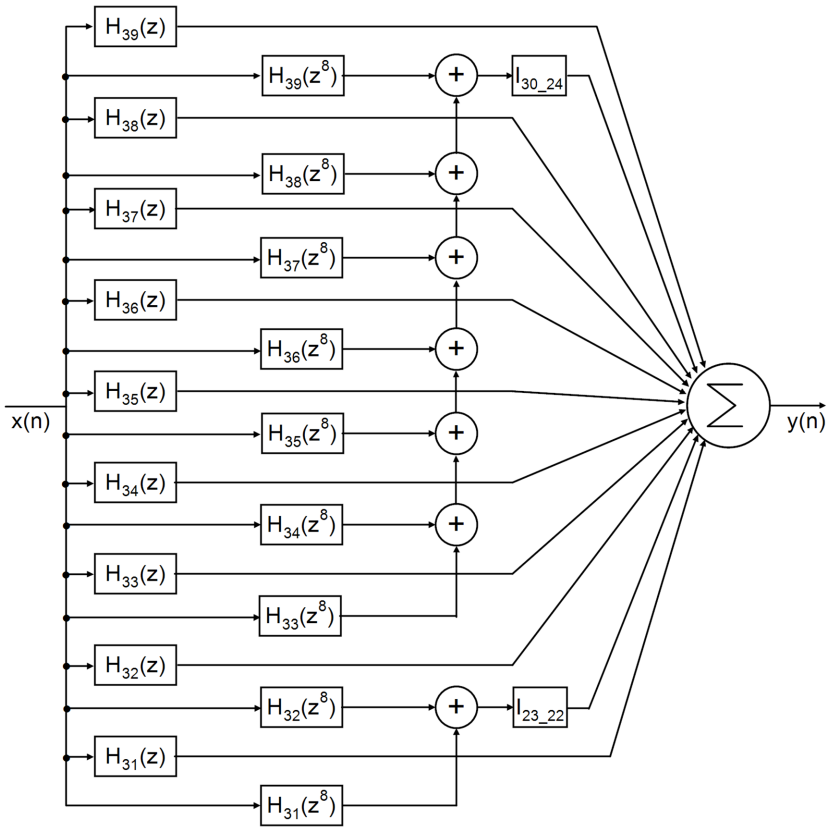


Figure 4.5: Proposed filter bank architecture

Considering the upper band, i.e., H_{39}, the ANSI S1.11 Class-2 specifications for the band edge frequencies are 1472 Hz, 7127 Hz, 8980 Hz and 43478 Hz. Taking the minimum of transition bandwidths, the band edge frequencies will get modified to 1472 Hz, 7127 Hz, 8980 Hz and 14635 Hz. To meet this specification, a sampling frequency of 29270 Hz is required to satisfy the Nyquist criteria, which is high for hearing aids. In hearing aids, the frequency spectrum is highly restricted by transducer frequency characteristics, generally in the range of 5 kHz for both microphones as well as receivers. Audiograms are recorded for a frequency spectrum of 160 Hz to 8 kHz and hence a sampling frequency greater than 16 kHz is required. We opted for a sampling frequency of 24 kHz as frequencies beyond 8 kHz are perceptually insignificant in practical hearing aids. It also facilitates a comparison of the performance of the architecture with other ANSI S1.11 based filter banks (Kuo et al. (2010), Liu et al. (2013), Lai et al. (2015), Yang et al. (2016)) which also use a sampling frequency of 24 kHz. So the specifications are modified to the maximum margin possible, i.e., 4107 Hz, 7127 Hz, 8980 Hz and 12000 Hz, which gave a filter order of 16. We opted for

critical sampling considering the fact that in practical hearing aids, the frequencies beyond 8 kHz do not matter much. This analysis shows that the lowest stop band edge is decided by the ANSI S1.11 specifications, i.e., f_{s1_22} and the highest stop band edge is decided by the sampling frequency, i.e., f_{s2_39} which is still within the required ANSI specifications.

In the proposed architecture, IFIR technique (Vaidyanathan (1993)) is used to reduce the computational complexity. The upper 9 prototype filters (H_{39} to H_{31}) were designed separately using PM algorithm and interpolated by a factor of 8 to obtain the lower 9 filters (H_{30} to H_{22}). ANSI S1.11 requirements are used to design the filter H_{31} so that it will meet the specifications for lowest band, H_{22}. Therefore, the band edge specifications for H_{31} are 229 Hz, 1123 Hz, 1414 Hz and 2308 Hz. Based on the above design criteria, the required band edge specifications for the filters H_{39}, H_{31} and H_{22} are as given in Table 4.2. It is to be noted that the band edge specifications of H_{31} is decided by the band edge specifications of H_{22} since, H_{22} has to be derived from H_{31} using interpolation by a factor of 8. H_{22} specifications in the Table 4.2 are decided by f_{s1} of H_{22}, which is obtained from equation (4.4). Whereas, H_{39} specifications in the Table 4.2 are decided by f_{s2} of H_{39}. It is decided by the chosen sampling frequency of 24 kHz, but still within the ANSI S1.11 class-2 requirements. The upper stop band edges for the filters H_{32} to H_{38} are computed using a linear interpolation between the upper stop band edges of H_{31} (f_{s2_31}) and H_{39} (f_{s2_39}) in octave scale as given below.

$$y_{s2\_n} = r(f_{m\_n} - f_{m\_39}) + y_{s2\_39} \tag{4.7}$$

where

$$r = \frac{y_{s2\_31} - y_{s2\_39}}{f_{m\_31} - f_{m\_39}} \tag{4.8}$$

$$y_{s2\_n} = G^{\frac{f_{s2\_n}}{f_{m\_n}}} \tag{4.9}$$

where f_{s2_n} is the upper stop band edge and f_{m_n} is the center frequency of n^{th} band. Calculated band edge frequencies and its corresponding orders for filters H_{39} to H_{31} are given

Table 4.2: Band edge specifications for filters H_{39}, H_{31} and H_{22} to meet the required design criteria for the 18-band structure

Filter	f_{s1} (Hz)	f_{p1} (Hz)	f_{p2} (Hz)	f_{s2} (Hz)
H_{39}	4107	7127	8980	**12000**
H_{31}	229	1123	1414	2308
H_{22}	**29**	140	177	288

in Table 4.3. The filters H_{30} to H_{22} are obtained from H_{39} to H_{31} using interpolation by a factor of 8.

Table 4.3: Prototype filter specifications

Band Number, n	**Band Edge Frequencies (Hz)** $[f_{s1}\ f_{p1}\ f_{p2}\ f_{s2}]$	**Filter Order**
39	[4107 7127 8980 12000]	16
38	[2698 5657 7127 10087]	16
37	[1805 4490 5657 8342]	18
36	[1230 3564 4490 6824]	20
35	[853 2829 3564 5540]	24
34	[600 2245 2829 4474]	28
33	[429 1782 2245 3597]	36
32	[312 1414 1782 2884]	44
31	[229 1123 1414 2308]	54

The group delay (GD) of an IFIR combination can be calculated as:

$$GD = \frac{N_a * L + N_i}{2f_s} \tag{4.10}$$

where L is the interpolation factor, N_a and N_i represents orders of analysis and interpolation filters respectively and f_s is the sampling frequency.

Since the interpolation factor is high, the constraints on image cancellation filter specification become high. Here, the transition bandwidth of the interpolation filter is decided by f_{p2_30} of H_{30} and f_{s1_22} of first image of H_{22}, which gives an order of 118 for the low pass filter. It will adversely affect the group delay as well as total multiplications per sample of the entire system. To reduce the group delay, two interpolation filters are used instead of one, which will relax the band edge requirements. For example, let the lower 9 band filters be grouped into two as H_{30_28} and H_{27_22} and two low pass filters I_{30_28} and I_{27_22} be used to cancel out the image frequencies of H_{30_28} and H_{27_22}. Then the band edge requirements of I_{30_28} is decided by f_{p2_30} of H_{30} and f_{s1_28} of first image of H_{28} which is higher than those of H_{22}, so the order of I_{30_28} is obtained as 80. Similarly, the band edge requirements of I_{27_22} is decided by f_{p2_27} of H_{27} which is lesser than that of H_{30} and f_{s1_22} of first image of H_{22} and the order of I_{27_22} is obtained as 50. Now the maximum group delay of the entire structure is decided by the maximum of group delays introduced by the combinations of (H_{30_28} & I_{30_28}) and (H_{27_22} & I_{27_22}) which is 4.67 ms and 10.04 ms respectively. Table 4.4

shows the exploration results of the orders of interpolation filters for all the combinations of the analysis filters in groups of two and their respective group delays.

Table 4.4: Interpolation filter order exploration

Pair No.	Filter Pair	Interpolation Filter Order Pair	GD Pair	#MPY
P1	H_{30} H_{29_22}	54 74	3.79 10.54	66
P2	H_{30_29} H_{28_22}	66 58	4.04 10.21	64
P3	H_{30_28} H_{27_22}	80 50	4.67 10.04	67
P4	H_{30_27} H_{26_22}	90 44	5.21 9.92	69
P5	H_{30_26} H_{25_22}	98 40	6.04 9.83	71
P6	H_{30_25} H_{24_22}	106 38	6.88 9.79	74
P7	H_{30_24} H_{23_22}	110 36	8.29 9.75	75
P8	H_{30_23} H_{22}	114 36	9.70 9.75	77
P9	H_{30_22}	118	11.46	60

It can be observed that filter pair (H_{30_24} H_{23_22}) gives the minimum group delay of 9.75 ms with a slight increase in total number of multiplications required to 75 for interpolation filters.

4.3.1 Gain Optimisation

This new band structure will distribute the inter-band interference almost uniformly among all the 18 bands since the band edges are linearly varying from H_{31} to H_{39} in a logarithmic scale and satisfy the ANSI S1.11 specifications with reduced filter order. Figure 4.6 shows the plot of inter-band interference from the first and the second neighboring bands to each filter. I_{r1} is the interference from the first neighboring band from right side, I_{r2} is the interference from second neighboring band from right side, I_{l1} is the interference from first neighboring band from the left side and I_{l2} is the interference from second neighboring band from the left side. It can be observed that the interference from the first neighboring bands is almost uniformly distributed among all the bands except for the case of interference between bands 9 and 10. Since band 10 is derived from band 18 instead of band 9, there is a comparable difference in slope in the interference plot between bands 9 and 10. Interference from second neighboring bands is less than -10 dB in most of the cases, which is negligible compared to the first neighboring band interference.

According to ANSI S1.11 Class-2 filter specifications, the pass band ripples should be within ±0.5 dB, which is important to keep the final audiogram matching error within

±1.5 dB. But the inter-band interference from adjacent bands and the ripples from the interpolation filter can adversely affect the overall pass band distortion. So a two-stage gain optimisation procedure was used as given in Yang et al. (2016) to limit the overall matching error within ±1.5 dB. During the first stage of gain optimisation, using equation (4.11), the effect of inter-band interference is canceled out and the overall ripples of the entire band are restricted to approximately within 0.5-1.5 dB.

$$\triangle P(n) = 10log(10^{0.05*g(n)} + \sum_{i} 10^{-0.05*A(n,i)} \tag{4.11}$$

where $A(n,i)$ is the magnitude measured at mid-band frequency. By making the error $\triangle P(n) = 0$, we can get the value of modified gain, $g(n)$. Since the inter-band gains are related to each other, it is not possible to get a perfect zero ripple at each center frequency. So the equation is applied multiple times to keep the overall ripple within the limit of 1.5 dB for the entire band structure. The flat band response of the proposed filter bank is shown in Figure 4.7.

In the second stage of optimisation, a similar approximation is used after applying the NAL-NL2 prescription. The flat band gain after the first stage of optimisation was added to the prescribed gain and a similar optimisation algorithm is applied during the second stage.

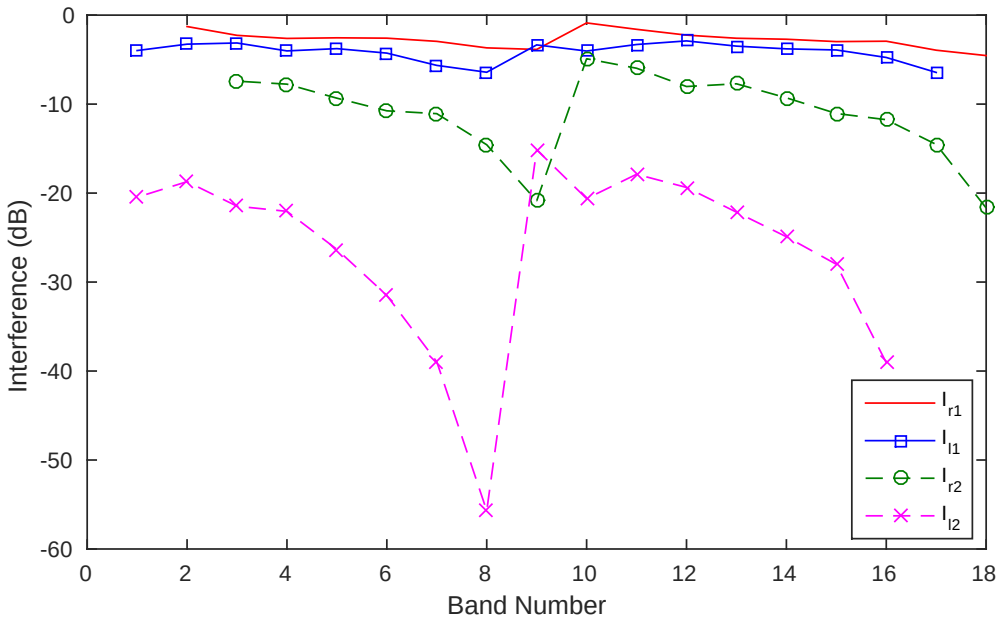


Figure 4.6: Interband interference plot from neighboring bands

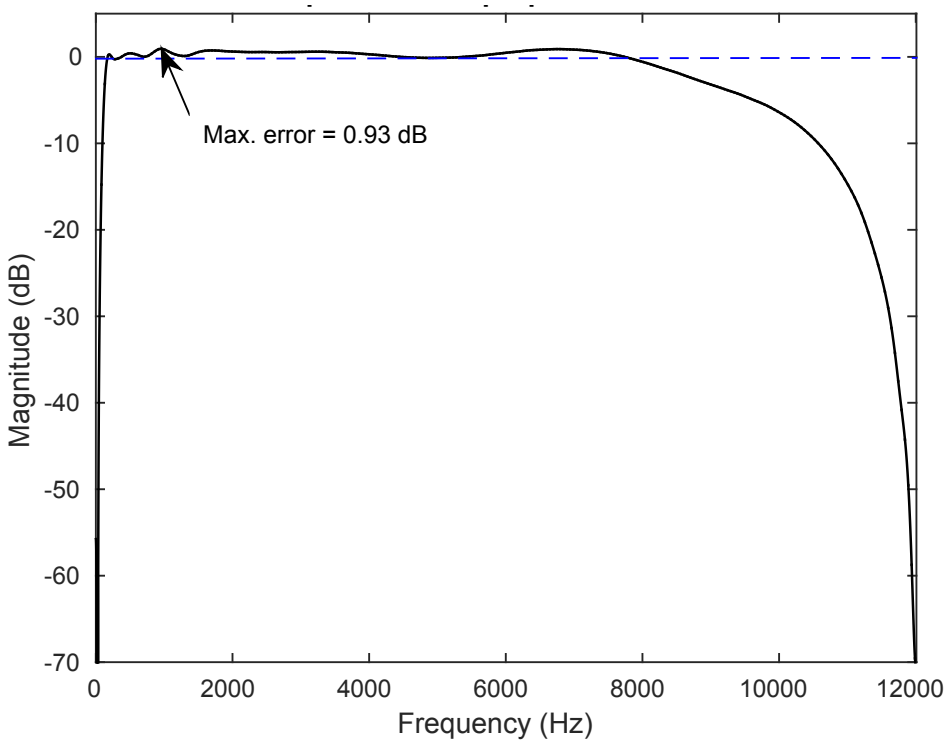


Figure 4.7: Flat band response of the filter bank

Since some audiograms vary rapidly at some frequencies, and if we apply high gains, even 1.5 dB ripple may scale to a larger value. So the following formula is applied to modify the prescribed gain for multiple iterations till the matching error comes below $\pm 1.5\ dB$ since the minimum detectable sound difference for the human ear is 3 dB (Liu et al. (2013)).

$$E(n) = 10log(\frac{1 + 10^{0.05*I(n)} + \sum_{i \neq n} 10^{0.05*(I(i) - \triangle A(n,i))}}{1 + 10^{0.1*I_g(n)}}) \tag{4.12}$$

where $I(n)$ is the final prescribed gain, $I_g(n)$ is the targeted prescribed gain from NAL-NL2 and $(I(i) - \triangle A(n,i))$ is the magnitude difference between the n^{th} and $(n + i)^{th}$ mid-band frequencies in dB.

4.4 Hardware Implementation

The hardware realisation structure of the proposed filter bank is shown in Figure 4.8. The architecture contains a total of 20 filters with odd tap length. The coefficient symmetry property of the filters is used to reduce the number of multiplications. Table 4.5 shows the

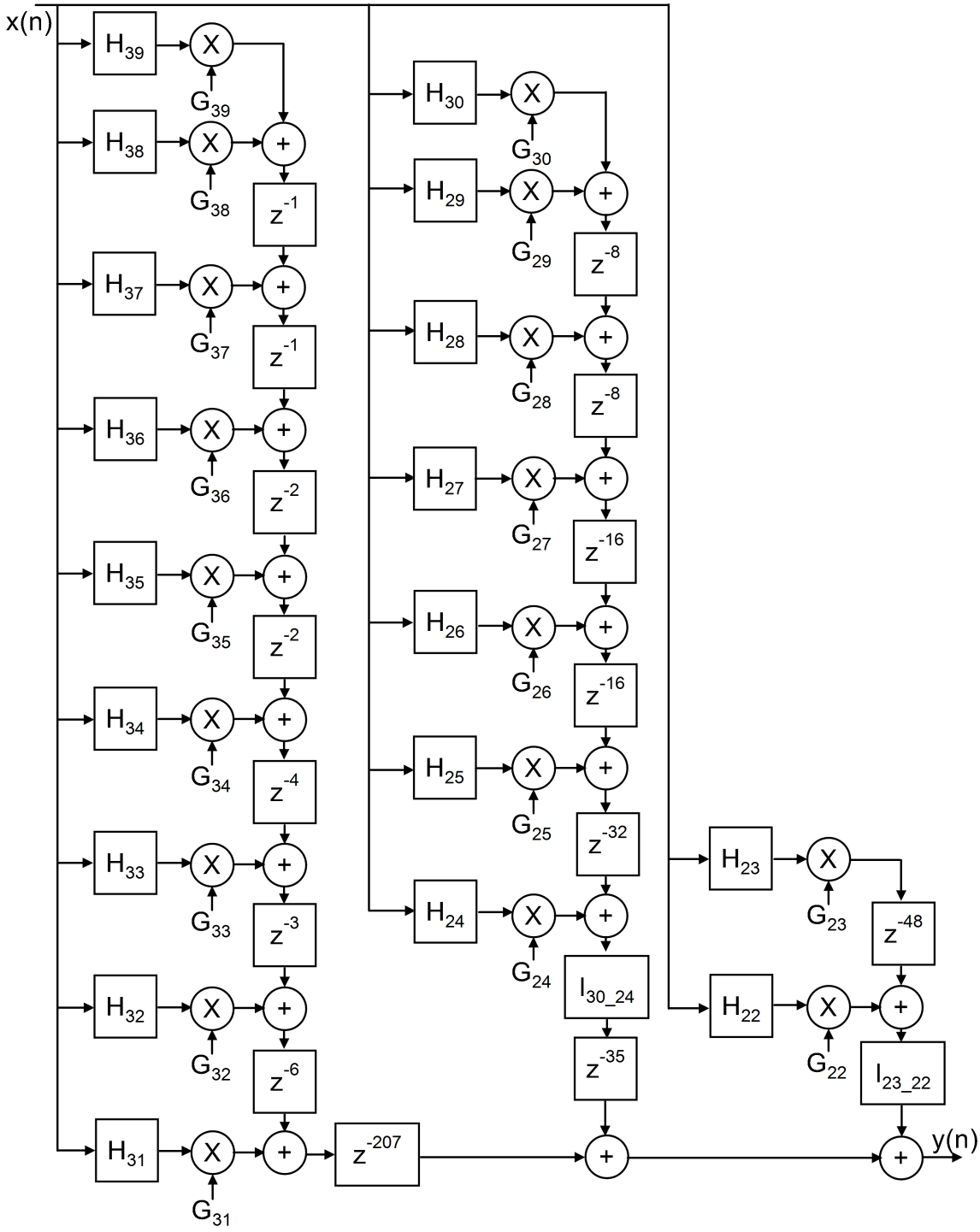


Figure 4.8: Hardware realisation structure of the proposed filter bank algorithm

Table 4.5: Filter tap lengths and number of multiplications required for each filter

Filter	H_{39}	H_{38}	H_{37}	H_{36}	H_{35}	H_{34}	H_{33}	H_{32}	H_{31}	I_{30_24}
Tap length	17	17	19	21	25	29	37	43	55	111
#Multiplications	9	9	10	11	13	15	19	22	28	56
Filter	H_{30}	H_{29}	H_{28}	H_{27}	H_{26}	H_{25}	H_{24}	H_{23}	H_{22}	I_{23_22}
Tap length	129	129	145	161	193	225	289	337	433	37
#Multiplications	9	9	10	11	13	15	19	22	28	19

filter orders and the corresponding number of multiplications required for each filter.

The entire system was implemented using 16-bit fixed point arithmetic. The prescribed gains G_{xy}, obtained from the NAL-NL2 formula, are applied to the input signal as it passes through each filter. These gains are stored in programmable registers. A 5-bit address is needed to choose between different gains. Separate input ports were provided to load the gain values and input data.

After interpolation, the tap length of filter H_{22} becomes 433, which requires the maximum number of delay registers among all 18 bands. The register array used to store the input data sequence is termed as delay line and the registers used to synchronise between multiple filters are termed as buffers. These buffers are realised as pipeline register arrays. The longest delay line required for H_{22} can be shared among the 18 analysis filters. Two separate delay lines are required for interpolation filters I_{30_24} and I_{23_22} of lengths 111 and 37 respectively, since the input data to both these filters are different. So in total, 581 registers are needed to realise the delay line structure of the proposed filter bank.

The buffers are required to maintain the linear-phase condition of FIR filters. The total number of buffers required for proper synchronisation of the entire filter bank is shown in Figure 4.9. It can be observed that a total of 19 registers are required to synchronise filters from H_{39} to H_{31}. Similarly, 80 buffer registers are needed to synchronise filters from H_{30} to H_{24} and 48 buffers are needed between filters H_{23} and H_{22}. The maximum group delay of the proposed architecture is due to the combination of filter H_{22} and the interpolation filter I_{23_22}. So 207 and 35 buffer registers are needed for upper nine bands and the output of interpolation filter I_{30_24}, respectively, to synchronise with the output of I_{23_22}. This makes a total of 389 buffer registers for the synchronisation purpose. The entire filter bank needs to be synchronised according to three delay lines as shown in Figure 4.10. That is, H_{23} and H_{22} should be synchronised according to the delay line of 433 before passing to I_{23_22}. Filters from H_{24} to H_{30} should be synchronised before passing the combined output to the delay line for I_{30_24}. Finally, the combination of filters from H_{31} to H_{39} and the output from I_{30_24}

should be synchronised with the output of I_{23_22}. So the proposed filter bank architecture requires a total of 581 data line registers and 389 synchronisation buffers to get a proper output without any phase distortion.

A multi-MAC based design was followed for the implementation of the proposed algorithm which is preferred for low power consumption (Liu et al. (2013)). Sampling frequency was chosen as 24 kHz. The entire filter bank was designed using 30 MAC units with a clock frequency of 384 kHz. Various possibilities for the number of MAC units are explored as

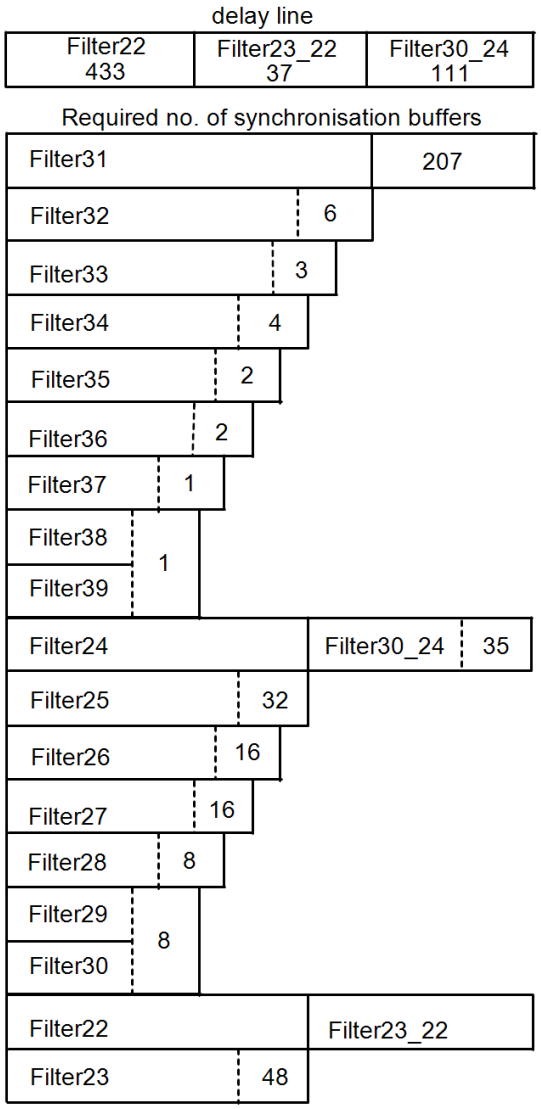


Figure 4.9: Total number of synchronisation buffer and the delay line registers required for the proposed filter bank

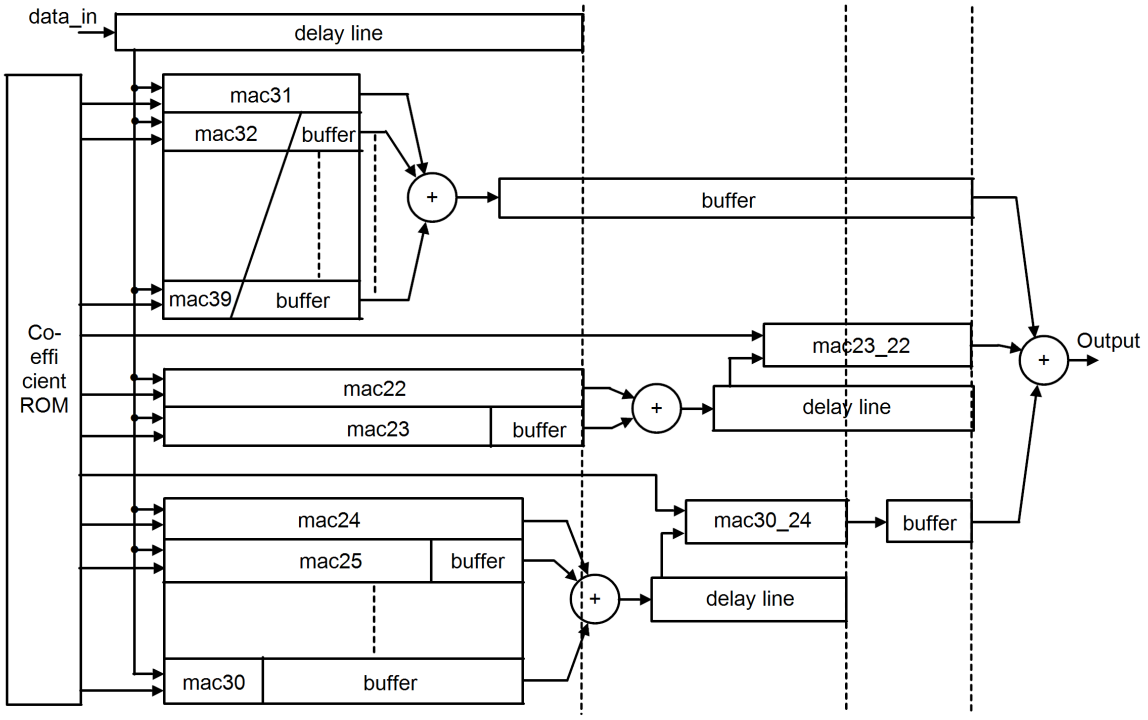


Figure 4.10: Synchronisation buffer structure of the proposed architecture

given in Table 4.6. The total number of multiplications per sample for the proposed architecture is 347. If a single MAC unit is used for performing all the multiplications, a clock frequency of 8.328 MHz will be required. Increased clock frequency will cause higher switching power dissipation. If we use two MAC units as one for 18 analysis filters and one for both the interpolation filters, then the MAC unit for 18 filters has to perform 272 multiplications per sample and the MAC unit for interpolation filters has to perform 75 multiplication per sample as given in the table. If we divide the total multiplications per sample equally between two MAC units, then it requires 174 multiplications per sample per MAC. In that case a clock frequency of 4.2 MHz is required to perform the complete filtering. If we use one MAC per filter, i.e., 20 MAC units for 20 different filters, then I_{30_24} alone requires 56 multiplications per MAC, which will require a minimum clock frequency of 1.344 MHz. After exploring the different possible options, 30 MAC units were selected with 15 multiplications per MAC, considering the number of stall cycles and the ratio of logic to sequential cells.

Using a clock frequency of 384 kHz requires ten extra MAC units to complete the entire filtering. Four MAC units are required for I_{30_24} and 2 MAC units per filter are required for I_{23_22}, H_{22}, H_{23}, H_{24}, H_{31}, H_{32} and H_{33}, since the number of multiplications needed are more

Table 4.6: Operations per MAC and the required clock frequencies

No. of MAC units	Multiplications/MAC	Min. Clock Freq.(MHz)
1	347	8.328
2	272, 75	6.528
2	174	4.2
20	56	1.344
30	15	0.384
347	1	0.048

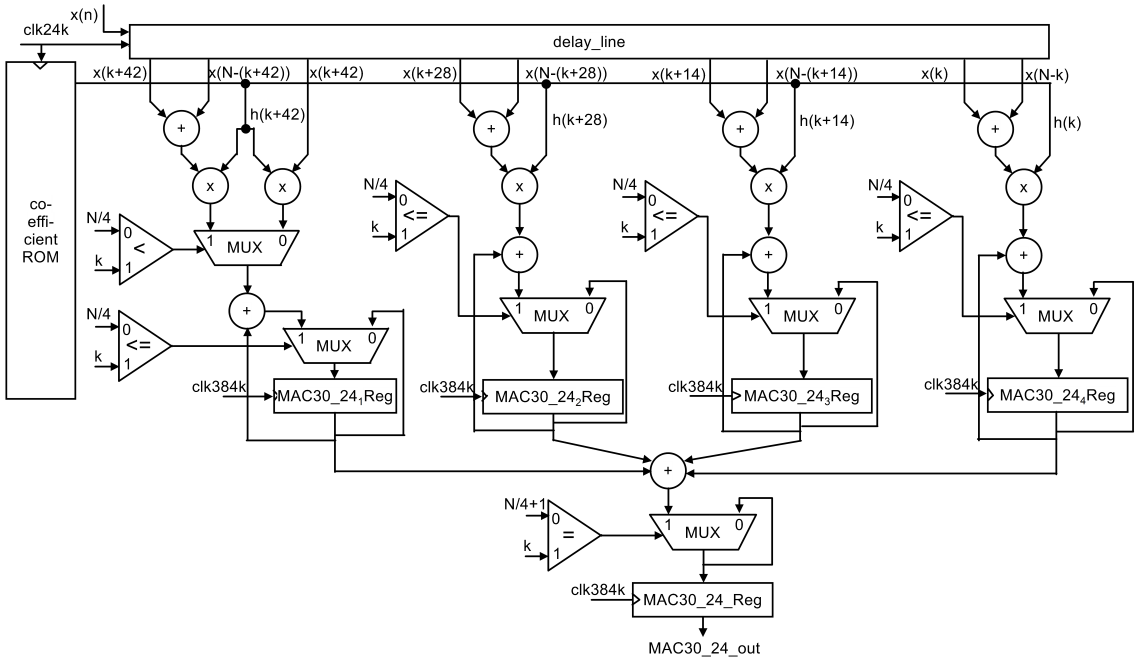


Figure 4.11: Hardware architecture of the multi MAC unit of filter I_{30_24}

than 15 in these filters. For example, the interpolating filter, I_{30_24} needs four MAC units to perform one complete convolution as shown in Figure 4.11. N represents the order of the filter and k is the count value from 0 to 15. Since I_{30_24} requires 56 multiplications per sample (MPY), 14 multiplications per MAC will be enough to complete one convolution operation which will result in one stall cycle per MAC. The outputs of all the four MAC registers ($MAC30\_24_1Reg$ to $MAC30\_24_4Reg$) are added once the count value reaches 14 and stored in the output register of the filter I_{30_24}, which is $MAC30\_24\_Reg$ as shown in the figure. So one extra cycle is needed to perform this final addition operation for the outputs of four different MAC units. In the case of filter I_{23_22}, only two accumulators are needed instead of four.

4.5 Simulation Results and Discussion

All the filter coefficients were obtained using MATLAB® 2015.2 with Signal Processing toolbox. *firpm* function was used to design the prototype filters. Filter tap lengths were adjusted to the next higher order where required, to make all the filters of Type-I, which will make the hardware implementation comparatively easier. Frequency response of the designed 18-band filter bank is shown in Figure 4.12.

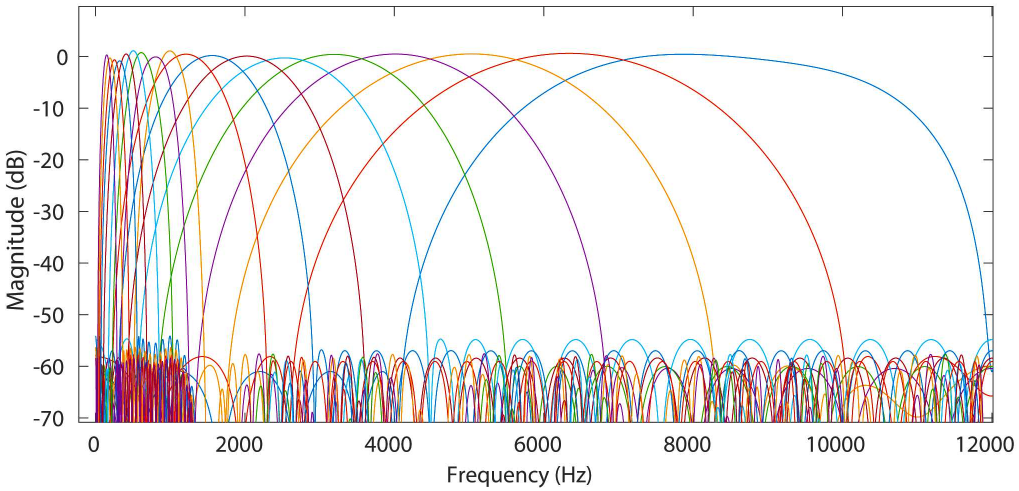


Figure 4.12: Frequency response of the filter bank

4.5.1 Comparison with other Architectures

A comparison with other architectures available in the literature is given in Table 4.7. Kuo et al. (2010) introduced the use of ANSI S1.11 specifications for fractional octave filter banks for the hearing aid application. They used multirate architecture to reduce the computational complexity. Three prototype filters were used to generate the entire filter bank along with interpolation and decimation filters. The design was satisfying the specifications with a lesser number of coefficients, but the group delay (78 ms) was high. Liu et al. (2013) modified the architecture to meet the delay constraint of 10 ms by relaxing the ANSI specifications and constricting the downsampling factor to four. They used the same design as in (Kuo et al. (2010)) for the upper three octaves and, the lower three octaves were designed with a restricted downsampling factor of 4. All the lower six filters were designed with a same order of 97, which is redundant considering the requirements for filters other than filter H_{22}. Yang et al. (2016), further modified the architecture in such a way that the 18 bands

are generated from a single prototype filter by fractional sub-sampling. This architecture is also a relaxed version of ANSI S1.11 specifications. In (Yang et al. (2016)), every band is at a different sampling rate which is difficult to implement practically as other algorithms like dynamic range compression and noise reduction are also to be implemented in hearing aids. The modifications to (Kuo et al. (2010)) in later publications were mainly focussed on lower 9 bands which were responsible for the increased complexity and delay. The upper 9 bands specifications of (Liu et al. (2013)) and (Yang et al. (2016)) were similar to (Kuo et al. (2010)).

Table 4.7: Comparison table

Reference	Type	No. of Coefficients	Delay (ms)
Kuo et al. (2010)	ANSI	91	78
Liu et al. (2013)	Quasi ANSI	506	10
Lai et al. (2014)	Quasi ANSI	451	13.58
Yang et al. (2016)	Quasi ANSI	579	10
Proposed	ANSI	212	9.75

In the proposed design, the complexity of the upper 9 bands was reduced by carefully stretching the design criteria to its maximum possible limits within ANSI S1.11 specifications and derived the lower 9 band filters from them. This approach resulted in a large reduction in filter order required for upper 9 bands and an overall reduction in the total number of filter coefficients required for the 18-band filter structure. The design requires 212 coefficients, which is less than 50% of other architectures with similar group delay. Another ANSI S1.11 architecture available in the literature is (Lai et al. (2015)), which used a non-linear structure based on frequency warping and a combination of cosine modulation and all pass transform. The algorithm was not tested after hardware implementation. Lai *et. al* also conclude that the architecture will cause phase distortion due to Infinite Impulse Response(IIR) structure used in it. The linear phase requirement is important if feedback cancellation algorithms are to be incorporated in the hearing aid.

Considering the hardware implementations available in the literature for ANSI S1.11 specifications based architectures, Kuo et al. (2010) and Liu et al. (2013) have done the implementation of only the analysis filter bank and not the synthesis filter bank. In (Kuo et al. (2010)), the authors have given the hardware results for the analysis part which requires a lesser number of storage elements, but its synthesis part requires 3432 buffer registers to meet the linear phase requirement which is large. Moreover, different octaves are running at

different sampling frequencies, which will require the generation of different clock frequencies. Handling multiple clock domains may become critical in hardware implementation when other complex signal enhancement algorithms like DRC and NR are to be added at different bands. The generation of different clock frequencies will necessitate overhead logic as well. The synthesis will become complex as buffers of different bands at different frequencies will have to be synchronised even though the architecture has a regular structure. Similar problems can arise in (Liu et al. (2013)) as well due to its multirate structure.

Compared to the above two architectures, the proposed algorithm has same sampling frequency for all the filters at the cost of a slight increase in the number of multiplications per sample. It is more practical to implement and easier to incorporate other signal enhancement algorithms without altering the sampling rate.

4.5.2 Hardware Results

The entire architecture is implemented using Verilog Hardware Description Language, and synthesised, placed and routed with Cadence design tools using UMC 65 nm standard cell libraries. Post layout core power analysis was done using Cadence Voltus^{TM} IC Power Integrity Solution with a maximum switching activity factor of one for typical parasitic corner.

Audiograms corresponding to most commonly found 8 different hearing losses available in Earinfo (2014), are widely used in research related to audiogram fitting. The prescribed insertion gains for each audiogram were obtained from the NAL-NL2 formula for an input level of 50 dB. The gains were applied to the proposed filter bank implementation and matching error for each band for all the audiograms were obtained. The quantisation error was obtained by comparing the 16-bit hardware implementation results with the MATLAB double precision implementation of the proposed architecture. The quantisation error results are given in Table 4.8. It can be observed that the maximum quantisation error is 0.122 dB. The audiogram matching results are shown in Figure 4.13. The maximum matching error for each audiogram is given in Table 4.9. The results show that the error is less than ± 1 dB in all the cases, which is less than the audible difference of 1.5 dB. Audiogram-6 has maximum matching error since it has a rapidly changing slope.

Post implementation core power results are given in Table 4.10 for a supply voltage of 1.2 V. The filter bank architecture consumes a total power of 0.37 mW. The filter bank algorithm was combined with a single channel DRC and tested with a sample audio file for flatband condition and without any compression applied. The input and reconstructed

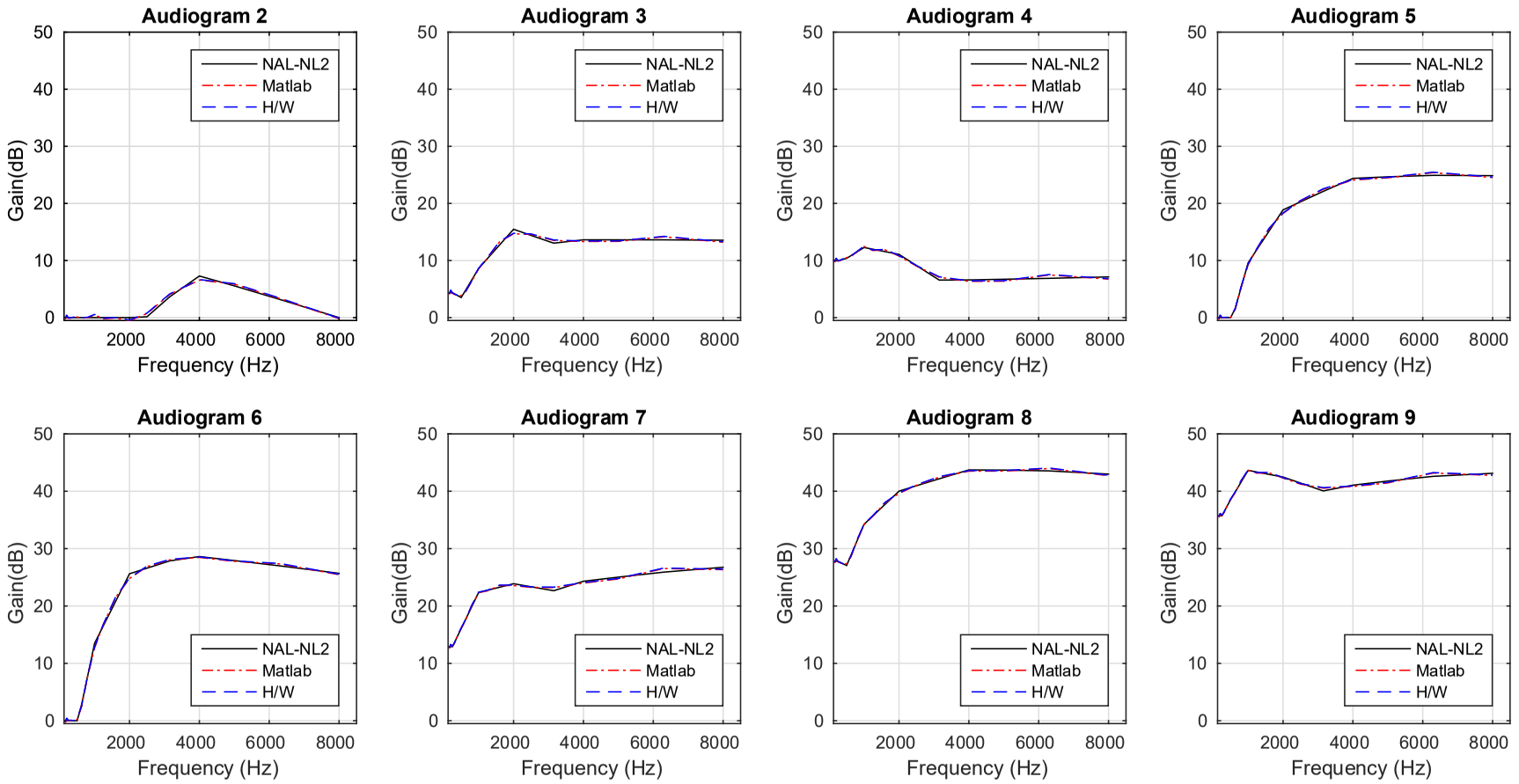


Figure 4.13: Gain matching results for NAL-NL2 prescriptions for different audiograms

Table 4.8: Quantisation error (dB) due to fixed point hardware implementation compared to floating point MATLAB implementation

Center freq. (Hz)	160	200	250	315	400	500	630	800	1000	1250	1600	2000	2500	3150	4000	5000	6300	8000
Audiogram2	0.1	0.118	0.054	0.05	0.074	0.083	0.093	0.063	0.07	0.087	0.073	0.075	0.085	0.086	0.081	0.08	0.076	0.079
Audiogram3	0.108	0.118	0.061	0.054	0.077	0.086	0.095	0.067	0.072	0.094	0.077	0.079	0.081	0.086	0.083	0.081	0.081	0.082
Audiogram4	0.104	0.115	0.057	0.054	0.076	0.087	0.089	0.071	0.076	0.093	0.077	0.078	0.076	0.088	0.088	0.085	0.079	0.082
Audiogram5	0.113	0.122	0.074	0.062	0.079	0.083	0.101	0.072	0.074	0.094	0.079	0.079	0.08	0.085	0.082	0.082	0.08	0.082
Audiogram6	0.111	0.121	0.086	0.079	0.066	0.076	0.101	0.061	0.071	0.095	0.078	0.08	0.081	0.085	0.083	0.082	0.08	0.083
Audiogram7	0.106	0.112	0.052	0.042	0.084	0.09	0.086	0.073	0.082	0.094	0.081	0.078	0.082	0.087	0.087	0.087	0.084	0.085
Audiogram8	0.109	0.119	0.066	0.062	0.078	0.089	0.093	0.073	0.08	0.097	0.082	0.082	0.083	0.089	0.086	0.085	0.083	0.086
Audiogram9	0.11	0.119	0.061	0.052	0.081	0.092	0.091	0.075	0.08	0.095	0.081	0.08	0.082	0.089	0.088	0.086	0.083	0.086

Table 4.9: Audiogram matching error

Audiogram	2	3	4	5	6	7	8	9
Max. Error (dB)	0.641	0.710	0.672	0.553	0.758	0.715	0.499	0.654

Table 4.10: Operations per MAC and the required clock frequencies

Power	**FB with DRC (mW)**	**FB without DRC (mW)**
Internal	0.1598	0.1554
Switching	0.2041	0.1930
Leakage	0.0260	0.0253
Total	0.3900	0.3737

output waveforms are shown in Figure 4.14. The filter bank with DRC consumes a power of 0.39 mW. In state of the art hearing aids, audio CODEC and transducers generally consume around 0.35 mW of power. To meet the minimum specification of less than 1 mW WHO (2004), for a digital hearing aid, the DSP part is having a power margin of around 0.65 mW in which, filter bank consumes most of the power compared to other signal enhancing algorithms. The proposed algorithm consumes only around 60% of the available power margin with a standard implementation. Power consumption can be further reduced by applying various low power design techniques. The chip is having a die area of 0.81 mm^2 and 71215 standard cells with 43.4 % of logic cells, 55.1 % sequential cells and 1.5 % of inverters. To compare the power consumption, the entire algorithm was implemented using 2 MAC units, one for all the 18 analysis bands and one for both the interpolation filters, which requires a clock frequency of 6.528 MHz and the power consumption was obtained as 5.044 mW. It shows that multi MAC architecture with lesser multiplications per single MAC unit consumes less power.

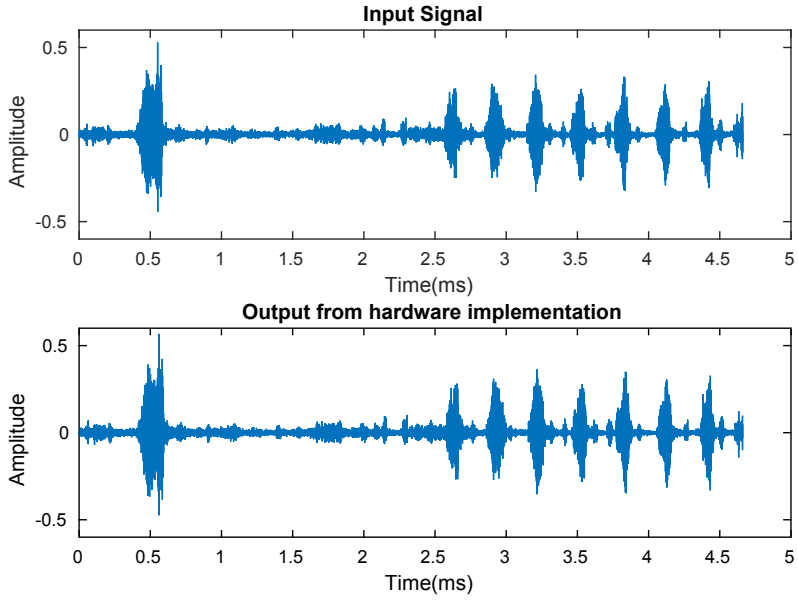


Figure 4.14: A sample audio output waveform from post layout hardware simulation

4.6 Summary

In this chapter, modifications are proposed for an 18-band ANSI S1.11 1/3 octave Class-2 filter bank. A method to define band edge frequencies of each prototype filter to get minimum order which satisfies the required specifications is presented. Hardware implementation of the algorithm was carried out using 65 nm standard cell libraries. The hardware output was tested with NAL-NL2 prescription for different audiograms and the maximum matching error was within the practical limit of $\pm 1.5\ dB$. The proposed architecture shows more than 50% reduction in the total number of filter coefficients required compared to other ANSI S1.11 based designs and less than 10 ms group delay and power consumption within practical constraints.

Chapter 5

Real-time Testing using FPGAs and ASIC Implementation

The theoretical explanation and verification of a dynamic range compression algorithm and an 18-band ANSI S1.11 filter bank are elaborated in previous chapters. Since the algorithms are developed for a practical hearing aid, the verification of the functionality of proposed algorithms on hardware is important. This chapter contains the implementation details of the real-time testing of proposed algorithms using two FPGAs. From the academic perspective, fabricating the chip using a 65 nm technology node is not feasible due to cost constraints. Semi-Conductor Laboratory (SCL) in Chandigarh is offering free fabrication of chips for academic purposes to promote the research activities in the country in the field of VLSI. The proposed hearing aid ASIC is implemented using SCL 180 nm PDK with an intention to fabricate a prototype chip. Finer details of the chip design are also presented in this chapter.

5.1 Real-time Testing using FPGAs

The hearing aid architecture with proposed filter bank and DRC algorithms was implemented and tested in real-time using two FPGA development boards as shown in Figure 5.1. Two Digilent ZedBoards™ having Xilinx® Zynq-7000 SoC were used for the experiment (ZedBoard (2014)). ZedBoard has 85000 programmable logic elements along with an ARM® Cortex-A9 dual-core processor. The available programmable logic elements were enough to meet our design requirement. The FPGA part of the board has a 100 MHz clock source and it meets our master clock requirement of 6.144 MHz. The proposed hearing aid DSP was implemented on one of the ZedBoards. The other FPGA board

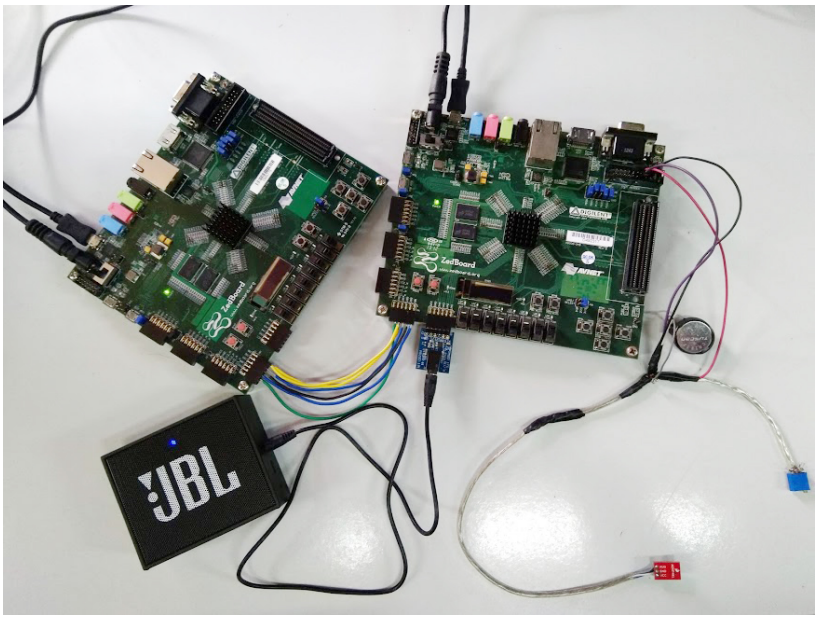


Figure 5.1: Real-time testing setup of the hearing aid system using two FPGA development boards

was modeled as an audio CODEC.

Texas Instruments (TI) has a 1.3 V micro-power voice band audio CODEC chip, AIC111, specifically designed for low power audio processing applications like hearing aids (TI (2005)). It is a single channel CODEC with delta-sigma ADC and DAC technology having a frequency response from 100 Hz to 10 kHz. The chip has a typical current drain of 350 μA. The ADC gives a 16-bit digital output and the DAC is capable of converting 16-24 bits digital data to an analog signal. AIC111 can be interfaced with external DSPs either through McBSPDSP-Codec Interface (SACI) protocol or through Serial Peripheral Interface (SPI) protocol. SACI is generally used for interfacing with TI DSPs and SPI for other devices. The slave devices need to have a compatible SPI slave protocol to communicate with AIC111. Therefore, in our hearing aid DSP, an SPI slave protocol was added to communicate with the external CODEC.

Instead of using the AIC111 breakout board to test the algorithm, a second FPGA was modeled to replicate the functionality of the audio CODEC. The top-level block diagram of the experimental setup is shown in Figure 5.2. An omni-directional MEMS microphone, ADMP401, having a flat frequency response from 100 Hz to 15 kHz was used for the experiment (Devices (2012)). The analog audio signal from the external microphone was converted to the digital domain using the XADC present in the ZedBoard. The ZedBoard

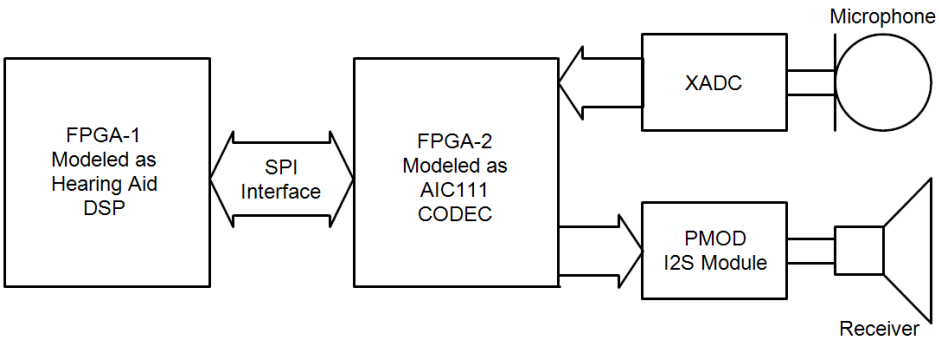


Figure 5.2: Top level block diagram of the experimental setup

has two channels of analog to digital converters embedded in it. The pinout diagram of the Agile Mixed Signaling (AMS) header of the ZedBoard is shown in Figure 5.3 (ZedBoard (2014)). From the pinout diagram, it can be observed that, ZedBoard is provided with channels 0 and 8 of the XADCs available with Xilinx 7-series FPGA kits. The XADC channel-8 is used for the experiment. The configuration details and the channel address information are available in the reference manual, Xilinx (2018). It is a 12-bit, 1-MSPS (Mega Samples Per Second) ADC with a 1 V peak to peak input level. The 12-bit data from ADC is internally converted to 16 bits by extending the LSB to extra four bits. The ADC

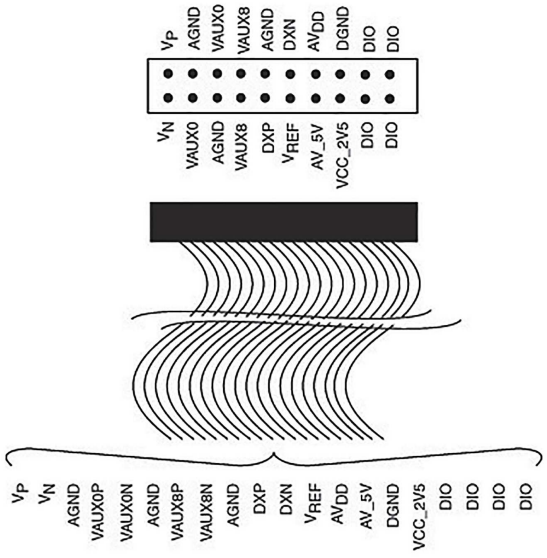


Figure 5.3: Agile Mixed Signaling (AMS) connector pinout diagram of the ZedBoard (ZedBoard (2014))

was configured in single-channel bipolar mode for our experiment.

Digilent pmod I^{2}S module having a 24-bit digital to analog converter (DAC) is used to convert the processed signal back to analog domain and play the output through the standard stereo audio port (Digilent (2016)). The DAC accepts 16-24 bit data input. It uses Integrated Interchip Sound (I^{2}S) protocol for the communication with host board GPIO ports. The module has four signals namely, Master Clock ($MCLK$), Left-right Clock ($LRCK$), Serial Clock (SCK) and Serial Data Input ($SDIN$) along with supply pins VDD and GND. $LRCK$ is used to send data to the Left and Right channels. Each channel is chosen by ON and OFF periods of the $LRCK$. Therefore $LRCK$ needs to be equivalent to the sampling frequency, which is 24 kHz. The data serializing clock, SCK, needs to run at two times of 16-bits, to send 16-bit data to one of the channels. Hence SCK is set as 768 kHz. The $MCLK/LRCK$ ratio was chosen as 256 from the datasheet according to our requirement, which gives a master clock ($MCLK$) frequency of 6.144 MHz. The timing diagram of the protocol is shown in Figure 5.4.

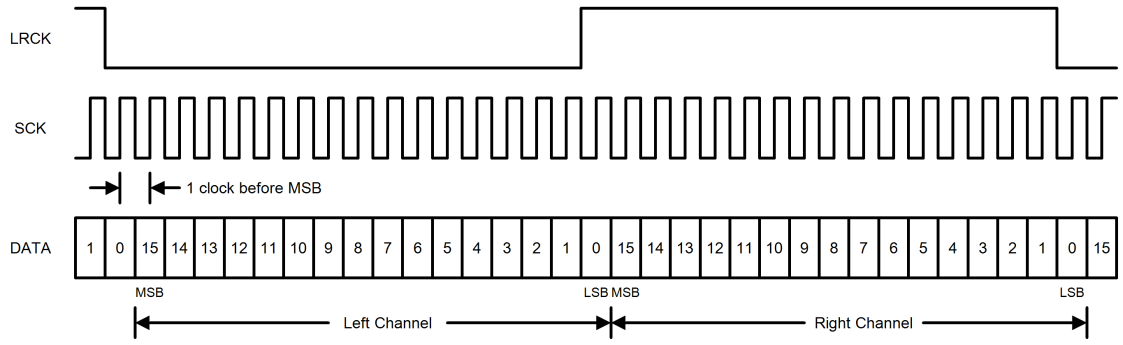


Figure 5.4: Timing diagram of I^{2}S interface

The interfacing used for communication between the two FPGAs is shown in Figure 5.5. The SPI master protocol of AIC111 was replicated in the CODEC FPGA with few modifications to make the hearing aid ASIC programmable. The hearing aid FPGA was modeled as SPI slave and the CODEC FPGA was modeled as SPI master. It has mainly four signals, data in line to the slave - *mosi* (Master Out Slave In), data out line from the slave - *miso* (Master In Slave Out), the serial clock, *sclk*, and a synchronisation signal $frame$. An extra control signal (p_d_ctrl) is added to the protocol in addition to the AIC111 SPI standard, to transfer the programmable parameters also through the same serial data in port of the interface. Generally, standard SPI protocols use a 32-bit frame size without any discontinuity in most of the applications. But in AIC111, the protocol is defined in such a way that it can

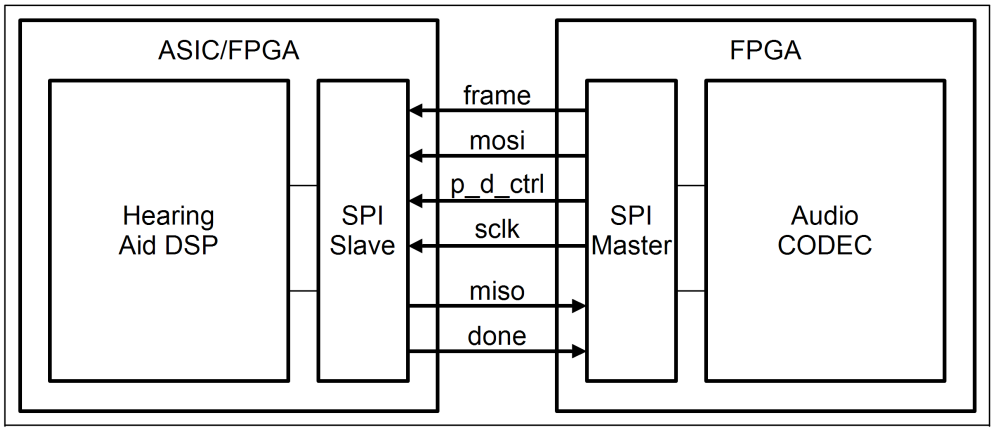


Figure 5.5: SPI interface between two FPGAs

send up to 24-bit data in a single frame. An idle period of 8 cycles is given for stable data capture. The serial clock is designed to support this 24-bit frame size with 8 extra cycles kept as idle. The control pulse *frame* is used to capture the data during the idle period of *sclk*. The timing diagram of AIC111 SPI interface is shown in Figure 5.6. Since the sampling frequency is set as 24 kHz, the serial clock is chosen as 384 kHz, i.e., 32 times the sampling frequency. A master clock, *mclk* of 6.144 MHz is used to generate the SPI signals which matches with the master clock frequency used for the PMOD I^{2}S module. An extra status signal *done* was provided, which can be used as an error detection signal.

The timing diagrams used for the SPI communication are shown in Figures 5.7 and 5.8. The hearing aid programmable parameters, i.e., prescribed gains for filter bank and the coef-

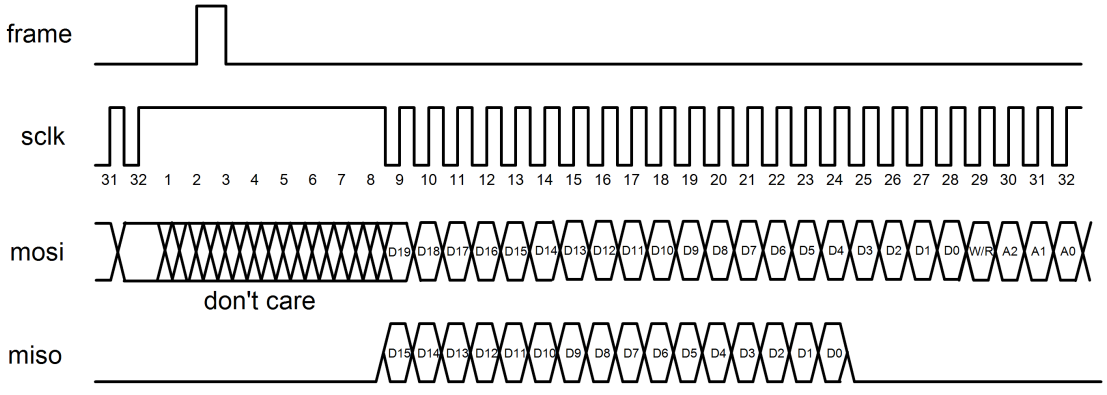


Figure 5.6: Timing diagram of AIC111 SPI protocol (TI (2005))

ficients for DRC are sent initially through the data in line by keeping *p_d_ctrl* signal *high* as shown in Figure 5.7. In the 24-bit data frame, the 16-bit parameters are followed by a 5-bit register address of each parameter. The remaining 3-bits are don't care. These parameters were stored in the block memory of CODEC FPGA. Once all the parameters are transferred, the *p_d_ctrl* signal goes *low* and audio data transfer starts as shown in Figure. 5.8. Since we are using a 16-bit data, 8-bits are not used in both *mosi* and *miso* in each frame.

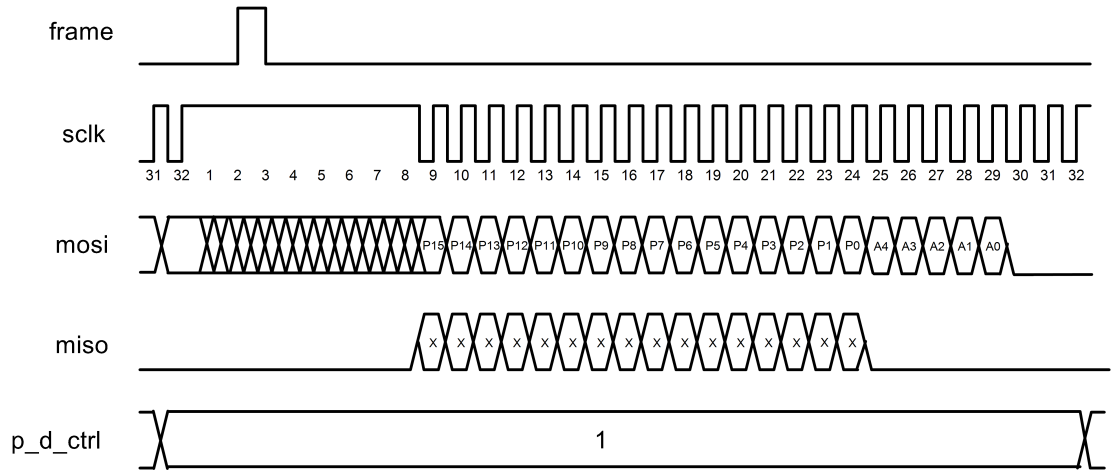


Figure 5.7: SPI protocol with *p_d_ctrl* = 1

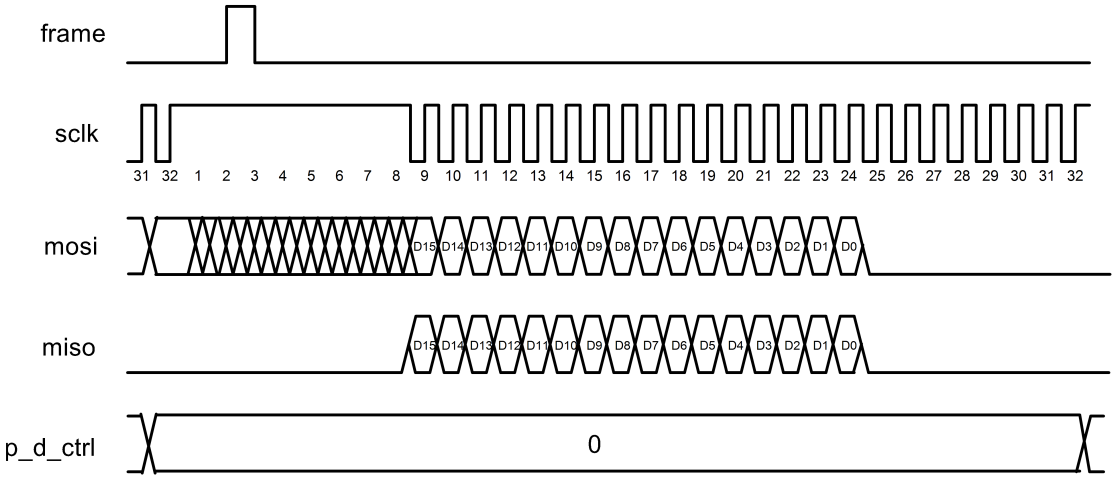


Figure 5.8: SPI protocol with *p_d_ctrl* = 0

5.2 ASIC Implementation of the Proposed Hearing Aid Architecture using SCL-180 nm Technology

The proposed hearing aid architecture was implemented using SCL 180 nm process design kit (PDK). The module hierarchy of the ASIC is shown in Figure 5.9. The top module, *top_chip_wrapper*, has 12 pins including the power supply pins *vdd*, *vss*, *vddo* and *vsso* for the core and the pads respectively. *mclk* is the master clock (6.144 MHz) pin and *rst* is the asynchronous master reset pin. The clock signals other than the SPI serial clock, *sclk* are derived from the master clock inside the *spi_slave_wrapper* module. Both the audio data as well as the control parameters, and the corresponding address for the filter bank and DRC are transferred to the hearing aid through the serial data in pin of the SPI slave, *mosi*. Before the audio data transmission starts, the control parameters and the corresponding address bits are transferred to the hearing aid by keeping *p_d_ctrl* pin *high*. This data transfer is initialised and synchronised using an extra *start* signal added to the SPI master module. The parameters, i.e., the insertion gain values for each of the 18 bands in the filter bank, and the DRC control signals such as different attack and release time coefficients, compression ratio and the compression threshold are separately stored in the programmable registers in the SPI

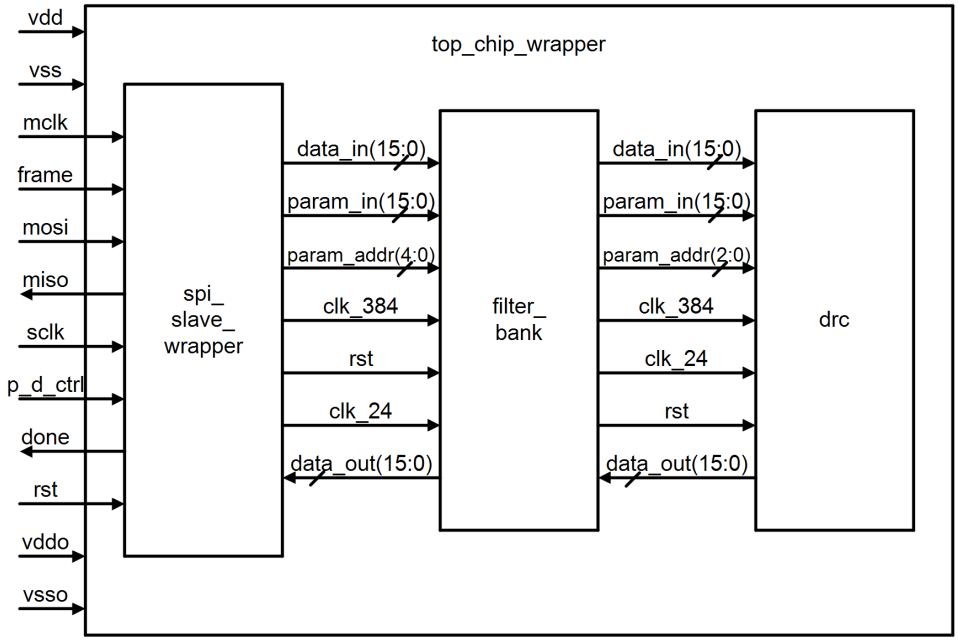


Figure 5.9: Hearing aid module hierarchy

slave wrapper module. These parameters are mapped to the filter bank and DRC modules through intermediate signal lines *param_in* and *param_addr* as shown in Figure 5.9. All the parameters are 16-bit wide. After the parameters are stored, the audio data transmission starts by keeping *p_d_ctrl* pin *low*. The *spi_slave_wrapper*, converts the serial data to 16-bit parallel data words and transfers to the filter bank module. The filter bank processes the data according to the loaded insertion gains and the gain compensated output is given to the DRC. The DRC controls the signal loudness based on the loaded compression factor, the compression threshold and the decay coefficients. Finally, the output from the DRC is converted to serial data in the SPI slave wrapper and sent to the data out pin, *miso*.

Under the Special Manpower Development Programme (SMDP) scheme of MeitY, Govt. of India, SCL offers optional die sizes of 2x2 mm and 5x5 mm. Since our design doesn't fit in 2x2 mm die size, the available option was to use 5x5 mm. In 5x5 mm, the minimum package pin count available was 48. The design requires 8 signal pins excluding power supply. Two sets of power pads, i.e., four pads for core power and ground pins (2 *vdd* and 2 *vss* pads) and one set of pads for I/O pad supply (1 *vddo* and 1 *vsso* pads) were used on all four sides. It makes a total of 24 pads for power supply. Out of the remaining 16 pins available, 8 pins were kept as dummy pins and 8 pins were assigned for controlling the functionality externally and testing the intermediate stages of the chip. The pinout diagram of the chip is shown in Figure 5.10.

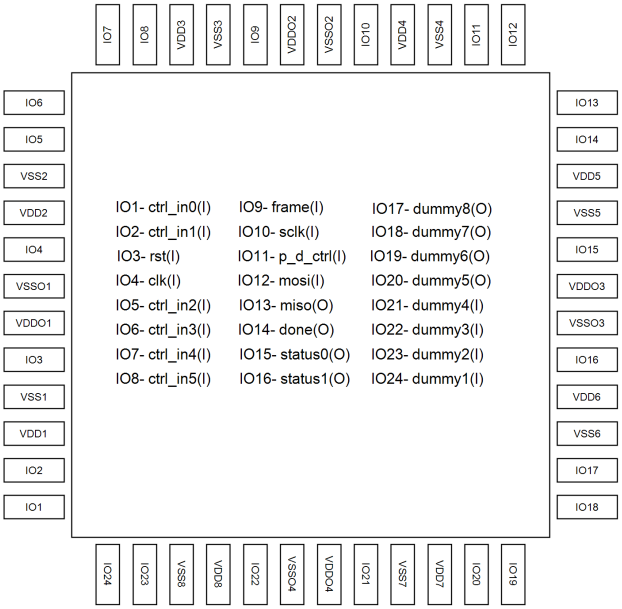


Figure 5.10: Pinout diagram of the proposed hearing aid ASIC

For the implementation of the ASIC, the SCL preferred EDA tool flow was followed except all the simulations were carried out using Cadence Incisive® simulator. The RTL of the complete design was written using Verilog HDL, after verifying the algorithm in MATLAB. The design was synthesised using Synopsys Design Compiler® with the master clock frequency of 6.144 MHz. The synthesis delay constraints were decided based on the different clock frequencies and the load information available from the datasheet of AIC111 audio CODEC since it is the targeted interface module for the proposed ASIC. After synthesis, the physical design was carried out using Synopsys IC Compiler®. After verifying the gate-level simulation (GLS), the final physical verification was done in Cadence Virtuoso and Calibre® tool from Mentor Graphics using the rule files provided by the technology vendor. After physical verification, the static timing analysis was carried out using Synopsys Prime Time tool, with the Standard Parasitic Extraction File (SPEF). The final layout of the chip with IO pads is shown in Figure 5.11.

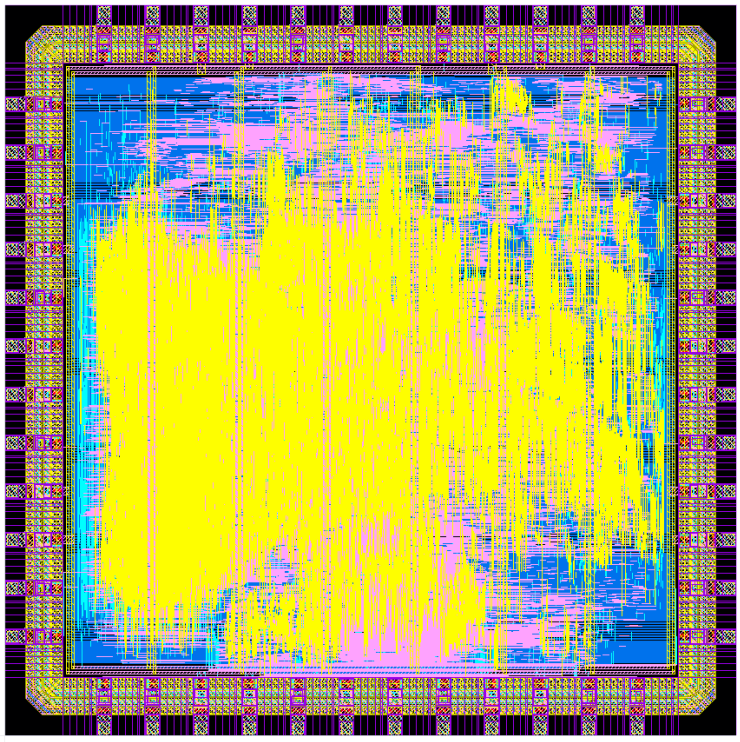


Figure 5.11: Complete hearing aid ASIC layout using SCL 180 nm

5.3 Summary

This chapter explains the real-time testing details of the proposed hearing aid DSP using FPGAs and the final ASIC design using SCL 180 nm PDK. The chip was designed in such a way that it is programmable externally through the serial data pin of the SPI interface. For FPGA testing, the external audio signal was recorded using a microphone and converted to digital using the XADC present in the CODEC FPGA. The SPI master protocol mimicking the functionality of intended external audio CODEC IC was implemented on one of the FPGAs and transferred the real-time data from the XADC to the other FPGA through the serial data line of SPI. After processing the data according to the programmed parameters, the output was transferred back to the CODEC FPGA and played through an I^2S audio interface. The chapter concludes with the explanation of the proposed hearing aid signal processing ASIC implementation using SCL 180 nm PDK. The design was completed till the final stage before tape-out using the vendor specific EDA tool flow.

Chapter 6

Conclusions and Future Scope

Hearing impaired people have to go through a series of procedures to get the hearing aid properly fitted according to the hearing loss. The effectiveness of the fitted device depends on a lot of factors ranging from, type and level of loss, type and cost of the hearing aid, features of the hearing aid, expertise of the audiologist, and quality of sound provided by the hearing aid. The quality of the sound produced by the hearing aid primarily depends on the algorithms used. A brief explanation of the working and features of current state of the art hearing aids is given in chapter 2 of this thesis. A literature survey was done on user satisfaction and problems with the current hearing aids to understand the requirements of hearing aid wearers. Further, an extensive review was done on various hearing aid implementations and the features associated with each design. Based on the features and the requirements, we decided to focus more on filter bank and dynamic range compression algorithms.

Dynamic range compression algorithms consist of a level detection stage, a gain stage and a smoothing stage. After detecting the incoming signal level, the compression gain is estimated in the gain stage. The dynamic parameters of DRC, i.e., attack and release time coefficients are important for the intelligibility of the hearing aid output. In conventional methods, the effect of the compression ratio applied at the gain stage is not considered, which generates an erroneous output. As part of this work, a new formula relating attack and release time parameters, envelope tracking decay coefficients and compression ratio parameters is proposed for the dynamic range compression algorithm. The equations are modified for an absolute detector based and an RMS detector based feed-forward architectures with and without smoothing stages. The decay coefficients estimated using the proposed set of equations give accurate expected output at required time instants while conventional

methods give erroneous output values. All the four DRC architectures were implemented using 4-bit and 8-bit resolution LUT based logarithm tables using UMC 65 nm standard cell libraries. The approximation errors and the post-layout core power consumption were analysed for the 8 different approaches and a relative comparison was done. From the hardware comparison results, the following conclusions are made:

- There is no significant difference in power consumption with an increase in log table resolution, while the approximation error reduces significantly.
- The difference in power consumption between absolute level detector based and an RMS detector based DRC architectures is noticeable. RMS detector based DRC consumes more power, but no significant improvement in error performance over the absolute detector based architecture.
- In all the cases, the inclusion of smoothing stage helps to keep the approximation error below 0.1 dB, but the power consumption increases by a significant factor, as high as 58% in some cases.

Based on these results, we propose the use of an absolute level detector based DRC without the smoothing stage for lowest power consumption and overall performance, using modified decay coefficient estimation techniques for a low power hearing aid design. Smoothing stages can be included if a continuous gain transition is needed with the cost of increased power consumption. So in applications where a high quality of sound is important, a smoothing filter can be incorporated at the output stage.

Recent research on filter bank algorithms for hearing aids is focused on the 18-band 1/3 octave non-uniform structure that follows the ANSI S1.11 Class-2 specifications. The advantage of using this structure is that the common audiogram fitting formulas also follow the same non-uniform structure for the gain prescription. The literature survey indicates that currently available architectures are struggling to find a better complexity-delay tradeoff due to the stringent specification requirement of the lower frequency bands. All the currently available algorithms concentrate on reducing only the complexity of the lower bands. In this work, the upper bands are optimised by using the maximum margin available in the ANSI S1.11 specifications and the lower bands are derived from it using the IFIR technique. This approach automatically reduces the complexity of the entire architecture. A method to define band edge frequencies of each prototype filter to get minimum order, which satisfies the required specifications is proposed. Hardware implementation of the algorithm was carried out using 65 nm standard cell libraries. The hardware output was tested

with NAL-NL2 prescription for different audiograms and the maximum matching error was within the practical limit of $\pm 1.5\ dB$. None of the other ANSI S1.11 implementations have reported hardware level audiogram matching results to the best of our knowledge. The proposed architecture shows more than 50% reduction in the total number of filter coefficients required compared to other ANSI S1.11 based designs and less than 10 ms group delay with practically applicable power consumption.

The proposed hearing aid architecture was implemented using SCL 180 nm standard cell library with an SPI slave protocol included for interfacing with the external CODEC. The chip was designed in such a way that it was programmable externally through the serial data pin of the SPI interface. The functionality of the proposed hearing aid was tested in real-time using two FPGA development boards, one of them modeled as hearing aid chip and the other as audio CODEC. The external audio signal was recorded using a microphone and converted to digital using the XADC present in the CODEC FPGA. The SPI master protocol mimicking the functionality of intended external audio CODEC IC was implemented on the CODEC FPGA and transferred the real-time data from the XADC to the hearing aid FPGA through the serial data line of SPI. After processing the data according to the programmed parameters, the output was transferred back to the CODEC FPGA and played through an I^2S audio interface. So in this thesis, modifications are proposed in the current hearing aid algorithms and the functionality of the designed ASIC was demonstrated in real-time using FPGAs.

In future, other signal enhancement algorithms like multiband noise reduction and multichannel compression algorithms can be incorporated to the proposed filter bank. Since the entire filter bank is running at the same sampling frequency, incorporating such algorithms will be easier compared to multirate architectures. The number of MAC units required may be optimised with a better design space exploration and can change depending upon the filter structure. Developing a generalised solution to find the best possible number of MAC units can also be taken as a future work. Hardware implementation was carried out by standard register transfer level procedures without incorporating any low power architectural optimisations. The overall performance of the system can be improved further by applying low power hardware implementation techniques. Hardware-level implementations of different DRC architectures are rarely explored by the research community and hence, our results can act as a basic platform for further optimisations at the hardware level.

Customer satisfaction studies show that there is a need for a better noise reduction algorithm. A detailed subjective evaluation and performance verification before going for the

hardware implementation of noise reduction algorithms would be required to understand the effectiveness of the algorithm, especially in challenging noisy environments. Developing an effective and practical noise reduction algorithm for hearing aids would be an interesting and challenging topic for exhaustive research.

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Publications based on the Thesis

Journals

1. Deepu S. P., Ramesh Kini M., Sumam David S., "Accurate estimation of decay coefficients for dynamic range compressors in hearing aids and a hardware level comparison of different architectures" *Microprocessors and Microsystems, Vol. 74, pp. 1-10, April 2020.*
   DOI: https://doi.org/10.1016/j.micpro.2019.102967 (**SCI and Scopus Indexed**)

2. Deepu S. P., Ramesh Kini M., Sumam David S., "An 18 Band ANSI S1.11 Filter Bank Based on Interpolated FIR Technique for Hearing Aids" *IET, The Journal of Engineering, April 2020.*
   DOI: https://doi.org/10.1049/joe.2019.1009 (**ESCI Indexed**)

Conferences

1. Deepu S. P., Ramesh Kini M., Sumam David S., "Estimation of Attack Time Constant for Dynamic Range Compressors in Hearing Aids" *Digital Signal Processing (DSP), 2016 IEEE International Conference on. IEEE, Beijing, China, October 2016.*
   DOI: 10.1109/ICDSP.2016.7868507

Papers Communicated

1. Deepu S. P., Ramesh Kini M., Sumam David S., "A Signal Processing ASIC Design for Digital Hearing Aids and Real-time Testing Using FPGAs", *Circuits, Systems, and Signal Processing, Springer* (Under Review).

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- Deepu S. P., Ramesh Kini M., Sumam David S., "18 band ANSI S1.11 filter bank based on interpolated finite impulse response technique for hearing aids", *IET Journal of Engineering, pp. 1-8, April 2020.*

- Deepu S. P., Sumam David, Ramesh Kini M., "Estimation of Attack Time Constant for Dynamic Range Compressors in Hearing Aids",*IEEE International Conference on Digital Signal Processing (DSP 2016), Beijing, October 2016.*

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- Hitesh Sudhakar, Lamia M. Kalam, Sripathi Muralitharan, Deepu S. P., Sumam David S., "Hardware Implementation of Dual-Tree Wavelet Transform Based Image Reconstruction", *IEEE International Symposium on Circuits and Systems (ISCAS 2020), Seville, Spain, October 2020.*

- Sathwik G.S., Barun Kumar Acharya, Bilal Ali, Deepu S.P., Sumam David S., "Real-Time Hardware Implementation of 3D Sound Synthesis", *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2020), Ha Long Bay, December 2020.*