

INVESTIGATIONS ON THREE-PHASE FRONT-END AC-DC CONVERTERS FOR POWER QUALITY IMPROVEMENT

Thesis

Submitted in partial fulfillment of the requirements for the degree of

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by

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DECLARATION

by the Ph.D. Research Scholar

I hereby declare that the Research Thesis entitled “Investigations on Three-Phase Front-End AC-DC Converters for Power Quality Improvement” which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is *a bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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ABSTRACT

The revolution in power electronics has opened an era for widespread use of power converters of different power rating from few Watts to Mega-Watts. Three-phase AC-DC converters are most widely used power converters as the distributed electric power is AC supply, while the applications based on DC supply as well as variable frequency AC supply, need conversion of AC supply into DC supply.

Large current harmonics and poor power factor in the utility interface are common problems in three-phase AC-DC converters. These AC-DC converters are used invariably at the front-end in numerous applications which may or may not be electrically isolated from the AC supply system depending on the rating and nature of the load and also the prevalent 'Standards' requirement. The applications such as electrochemical, electrometallurgical and electrical heating process, high voltage direct current systems, adjustable speed drives, battery charging, aerospace and naval equipment's, uninterrupted power supplies etc., use AC-DC conversion at the front-end. These processing industries and adjustable speed drives are the main applications wherein large amount of power is involved in AC-DC converters. These AC-DC converters are generally diode-based, thyristor-based or self-commutating device-based converters depending on applications, size and cost.

The wide spread use of AC-DC converters for various applications have resulted in power pollution leading to failure of sensitive equipment's, reduced efficiency, etc. This has led to the development of power quality standards and hence attracted attention of many researchers for improving the power quality at AC mains. This research work aims at classifying and investigating different three-phase AC-DC converters that employ diodes. The AC-DC converters are mainly classified on the basis of the circuit configuration used for power quality improvement. They are passive, active and hybrid AC-DC converters. The detailed investigation in each category is carried out based on the circuit configurations and control techniques employed. Also, it has led to the formation of

some new AC-DC converter configurations that are investigated for the power quality improvement capability.

Firstly, this research work aims at employing multi-pulse techniques for mitigating the power quality problems at the AC mains in front-end AC-DC converters. The multi-pulse technique uses autoconfigured transformer for power quality improvement and hence it is termed as passive technique. The investigations on two types of multi-pulse AC-DC converters is carried out covering a wide range of applications that use three-phase AC supply at the front-end for converting it to DC power. The two type of multi-pulse AC-DC converters are multi-phase staggering autoconfigured transformer and asymmetric multi-phase converter. The former uses delta and zig-zag autoconfigured transformer and the latter uses delta connected autotransformer for power quality improvement. The main feature of these multi-pulse AC-DC converters is its ability to reduce current harmonics distortion. In these multi-pulse AC-DC converters the number of pulses (voltage ripples at output of AC-DC converters in one cycle of AC supply voltage or steps in the current at input of AC mains) is increased by using phase staggering (or phase shifting), multi-phase (or phase multiplication) and hybrid of these techniques. Further, the unconventional pulse numbered AC-DC converters having pulse number of 20 is considered for the power quality improvement at AC mains.

Secondly, this research work aims at utilizing active front-end AC-DC converter for power quality improvement. The active topologies namely Vienna rectifier and Delta switch rectifier are chosen as front-end AC-DC converters for power quality improvement. The voltage sensorless control technique is proposed for the active front-end AC-DC converters such that the computational complexity and sensing effort have been reduced. The system results in improved power quality parameters with less engineering effort.

Finally, this research work also focuses on hybrid front-end AC-DC converter for power quality improvement. The hybrid AC-DC converter uses three-level boost converter as active modulation circuit and zig-zag transformer as passive current injection circuit. The current injection circuit along with the modulation circuit at the output stage increases the

DC-link voltage. Further, the utilised current injection circuit avoids resonance problem and also resulted in less rating. Furthermore, the modulation circuit results in reduced ripple current and device rating.

For visualizing the different advantages of the three-phase front-end AC-DC converters, the design and simulation of these converters are carried out in MATLAB/Simulink. The main emphasis of these investigations has been on compactness of configurations, simplicity and reduction in rating of components to reduce the overall cost of these front-end AC-DC converters. A laboratory prototypes of these front-end AC-DC converters are developed to validate the design. A high speed digital processor namely field programmable gate array controller, that consists of EP4CE30F484 processor is used to implement a control scheme for active and hybrid front-end AC-DC converters. The steady-state and transient-state performance of the front-end AC-DC converters are verified by changing the resistive load. These front-end AC-DC configurations and techniques have resulted in improved power quality indices with overall reduced rating and reduction in number of components.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS.....	i
ABSTRACT.....	iii
LIST OF FIGURES.....	xi
LIST OF TABLES.....	xvii
LIST OF ABBREVIATIONS.....	xviii
1 INTRODUCTION	1
1.1 GENERAL.....	1
1.2 PROBLEMS IN THREE-PHASE AC-DC CONVERTERS	2
1.3 PERFORMANCE PARAMETERS OF THREE-PHASE AC-DC CONVERTERS.....	4
1.4 OBJECTIVES AND SCOPE OF THE RESEARCH WORK.....	7
1.4.1 Analysis, design and development of three-phase front-end AC-DC converters employing passive power quality improvement technique.....	8
1.4.2 Analysis, design and development of three-phase front-end AC-DC converters employing active power quality improvement technique.....	8
1.4.3 Analysis, design and development of three-phase front-end AC-DC converters employing hybrid power quality improvement technique.....	8
1.5 OUTLINE OF CHAPTERS.....	9
2 LITERATURE REVIEW.....	13
2.1 GENERAL.....	13
2.2 SIGNIFICANT DEVELOPMENTS IN THREE-PHASE FRONT-END AC-DC CONVERTERS.....	13
2.2.1 Brief classifications of three-phase front-end AC-DC converters..	14
2.2.1.1 Boost converters.....	15
2.2.1.2 Buck converters.....	16
2.2.1.3 Buck–boost converters.....	16

2.2.1.4	Multi-pulse converters.....	17
2.2.1.5	Multi-level converters.....	17
2.2.2	Power quality improvement using three-phase front-end AC-DC converters.....	17
2.3	LITERATURE REVIEW ON THREE-PHASE FRONT-END AC-DC CONVERTERS.....	20
2.3.1	Passive AC-DC converters.....	20
2.3.2	Active AC-DC converters.....	22
2.3.2.1	Vienna type AC-DC converter.....	22
2.3.2.2	Delta type AC-DC converter.....	23
2.3.3	Hybrid AC-DC converters.....	24
2.4	IDENTIFIED RESEARCH AREAS.....	26
2.5	CONCLUSION.....	27
3	POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING PASSIVE TECHNIQUE.....	29
3.1	INTRODUCTION.....	29
3.2	PROBLEM FORMULATION.....	29
3.3	ASYMMETRIC NON-ISOLATED 20-PULSE MSAT CONFIGURATION.....	30
3.3.1	Design and analysis of the asymmetric MSAT configuration.....	33
3.3.1.1	Design of asymmetric MSAT configuration.....	33
3.3.1.2	Performance parameters of the asymmetric MSAT configuration.....	39
3.3.2	Results and discussion.....	42
3.4	A 20-PULSE AMPC CONFIGURATION SYNTHESIS.....	48
3.4.1	Design and analysis of non-isolated AMPC configuration.....	50
3.4.1.1	Design of non-isolated autoconfigured transformer.....	50
3.4.1.2	Performance parameters of the non-isolated autoconfigured transformer.....	55
3.4.2	Results and discussion.....	56
3.5	COMPARATIVE STUDY.....	62

3.6	CONCLUSION.....	65
4	POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING ACTIVE TECHNIQUE.....	67
4.1	INTRODUCTION.....	67
4.2	PROBLEM FORMULATION.....	67
4.3	THREE-PHASE THREE-SWITCH BOOST TYPE VIENNA CONVERTER.....	68
4.3.1	Design, analysis and control technique of the Vienna type front-end AC-DC converter.....	68
4.3.1.1	Analysis and design of the Vienna type front-end AC-DC converter.....	68
4.3.1.2	Voltage sensorless control, modulation technique and efficiency calculation.....	74
4.3.2	Results and discussion.....	83
4.4	THREE-PHASE BOOST TYPE DELTA CONNECTED AC-DC CONVERTER.....	89
4.4.1	Design, analysis and control technique of the Delta type front-end AC-DC converter.....	90
4.4.1.1	Analysis and design of the Delta type front-end AC-DC converter.....	90
4.4.1.2	Voltage sensorless control and component stresses calculation.....	95
4.4.2	Results and discussion.....	100
4.5	COMPARATIVE STUDY.....	106
4.6	CONCLUSION.....	109
5	POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING HYBRID TECHNIQUE.....	111
5.1	INTRODUCTION.....	111
5.2	PROBLEM FORMULATION.....	111
5.3	THREE-PHASE HYBRID FRONT-END AC-DC CONVERTER.....	112

5.3.1	Analysis and design of three-phase front-end AC-DC converter using hybrid technique.....	113
5.3.1.1	Analysis of front-end DBR with passive injection circuit.....	113
5.3.1.2	Analysis of three-level boost type modulation circuit...	120
5.4	CONTROL TECHNIQUE FOR THE HYBRID FRONT-END AC-DC CONVERTER.....	127
5.5	RESULTS AND DISCUSSION.....	128
5.6	COMPARATIVE STUDY.....	134
5.6	CONCLUSION.....	137
6	MAIN CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK...	139
6.1	GENERAL.....	139
6.2	MAIN CONCLUSIONS.....	139
6.3	SUGGESTIONS FOR FUTURE WORK.....	142
APPENDIX A.....		145
	SPECIFICATION OF THE THREE-PHASE FRONT-END AC-DC CONVERTERS USING PASSIVE TECHNIQUE.....	145
A.1	MSAT.....	145
A.2	AMPC.....	146
APPENDIX B.....		147
	DESCRIPTION OF EXPERIMENTAL PLATFORM FOR THE THREE-PHASE FRONT-END AC-DC CONVERTERS USING ACTIVE TECHNIQUE.....	147
B.1	OVERVIEW OF THE EXPERIMENTAL PLATFORM FOR VIENNA TYPE AC-DC CONVERTER.....	147
B.2	FPGA CONTROL BOARD.....	148
B.3	GATING SIGNAL ISOLATION AND AMPLIFICATION CIRCUIT...	151
B.4	VOLTAGE AND CURRENT SENSOR CIRCUIT.....	152
B.5	IGBT BASED CONVERTER.....	153

B.6	CONVERTER SPECIFICATION OF VIENNA TYPE AC-DC CONVERTER.....	154
B.7	CONVERTER SPECIFICATION OF DELTA TYPE AC-DC CONVERTER.....	154
APPENDIX C		156
	SPECIFICATION OF THE THREE-PHASE FRONT-END AC-DC CONVERTER USING HYBRID TECHNIQUE.....	156
BIBLIOGRAPHY		157
	PUBLICATIONS BASED ON THE THESIS	169
BIO-DATA		171

LIST OF FIGURES

Figure 1.1	The outline of the thesis.....	10
Figure 2.1	Brief classification of three-phase front-end AC-DC converters...	15
Figure 2.2	Detailed classification of three-phase front-end AC-DC converters	19
Figure 2.3	Classification of various types of multi-pulse AC-DC converters...	21
Figure 3.1	Schematic diagram of the 20-pulse asymmetric MSAT fed high power DC load.....	31
Figure 3.2	(a) Winding and (b) Resultant phasor diagrams of the asymmetric MSAT representing the phase-staggered angle positions of different phasors.....	32
Figure 3.3	Phase currents $i_{ab2,rms}$ & $i_{ca2,rms}$ and input line current $i_{A,rms}$ of the asymmetric MSAT.....	37
Figure 3.4	Theoretical waveforms of voltage and current of PNDBC A with respect to supply voltage, and DC-link voltage of PNDBC A and PNDBC B for the non-isolated asymmetric MSAT.	40
Figure 3.5	Simulated results of input voltage and current for the asymmetric MSAT at (a) FL condition. (b) LL condition.....	43
Figure 3.6	Simulated results of the asymmetric MSAT (a) Input voltage and current of PNDBC A. (b) Input voltage and current of PNDBC B...	43
Figure 3.7	Simulated results of the asymmetric MSAT at FL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.....	43
Figure 3.8	Simulated results of the asymmetric MSAT at LL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.....	44
Figure 3.9	Simulated results of the asymmetric MSAT (a) Output voltage and current of PNDBC A. (b) Output voltage and current of PNDBC B.....	44
Figure 3.10	Simulated results of the asymmetric MSAT (a) Voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to source voltage (v_A). (b) Currents of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to input current (i_A).....	44
Figure 3.11	Annotated photograph of the laboratory prototype.....	45

Figure 3.12	Experimental results of input voltage and current for the asymmetric MSAT at (a) FL condition. (b) LL condition.....	46
Figure 3.13	Experimental results of the asymmetric MSAT (a) Input voltage and current of PNDBC A. (b) Input voltage and current of PNDBC B.....	46
Figure 3.14	Experimental results of the asymmetric MSAT at FL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum..	46
Figure 3.15	Experimental results of the asymmetric MSAT at LL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum..	47
Figure 3.16	Experimental results of the asymmetric MSAT (a) Output voltage and current of PNDBC A. (b) Output voltage and current of PNDBC B.....	47
Figure 3.17	Experimental results of the asymmetric MSAT (a) Voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to source voltage (v_A). (b) Currents of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to input current (i_A).....	47
Figure 3.18	Schematic diagram of the 20-pulse non-isolated AMPC.....	49
Figure 3.19	Schematic diagram of the non-isolated AMPC representing (a) Winding diagram and (b) Resultant phasor diagrams of the phase-staggered angle positions of various phasors.....	49
Figure 3.20	Winding current analysis of the non-isolated AMPC supplying constant DC load current.....	52
Figure 3.21	PNDBC phase currents ($i_{bc9,rms}$, $i_{bc10,rms}$, $i_{bc11,rms}$, $i_{ab5,rms}$, $i_{ab6,rms}$, $i_{bc8,rms}$, $i_{bc7,rms}$, $i_{bc6,rms}$, $i_{ca5,rms}$, $i_{ca6,rms}$), winding currents ($i_{ab1,rms}$ & $i_{ca4,rms}$) and input line current ($i_{A,rms}$) of the non-isolated AMPC.....	53
Figure 3.22	Simulated waveforms of three-phase input voltage (v_A, v_B, v_C), input current (i_A, i_B, i_C), phase shifted voltage (v_{A1}, v_A, v_{B1}), PNDBC input currents (I_{A1}, I_{B1}), DC-link voltage (V_{dc}) and DC-link current (I_{dc}) of the non-isolated AMPC.....	57
Figure 3.23	Experimental results of (a) Input source voltage (v_A)/current (i_A) under LL condition, (b) Current THD under LL condition, (c) Input source voltage (v_A)/current (i_A) under FL condition, (d) Current THD under FL condition, (e) Input phase current (i_A), PNDBC input currents (I_{A1}, I_{B1}) with output DC-link voltages (V_{d1}, V_{d2}) and	

	(f) Phase shifted voltage (v_{A1}, v_A, v_{B1}) with input phase current (i_A) for the non-isolated AMPC.....	59
Figure 3.24	Simulated and experimental results of (a) Winding voltage ($v_{ab1,rms}$)/current ($i_{ab1,rms}$) waveforms (b) Winding voltage ($v_{ca4,rms}$)/current ($i_{ca4,rms}$) waveforms and (c) Input phase voltage ($v_{A,rms}$)/current ($i_{A,rms}$) of the non-isolated AMPC.....	60
Figure 3.25	Variations of (a) Input source current %THD with varying % leakage reactance and (c) PF with varying % leakage reactance for the non-isolated AMPC.....	61
Figure 4.1	Schematic diagram of the Vienna type front-end PFC rectifier.....	69
Figure 4.2	(a) Single phase equivalent circuit of the Vienna type front-end converter and its operating modes when (b) positive input cycle, (c) negative input cycle.....	74
Figure 4.3	(a) Equivalent circuit of the input stage of front-end unity PF rectifier incorporating voltage sensorless control. (b) Block diagram of control technique for input voltage evaluation.....	76
Figure 4.4	Modulation scheme for the Vienna type front-end PFC rectifier...	78
Figure 4.5	Conduction states for the converter when (a) Switching state (011), (b) Switching state (010), (c) Switching state (000), (d) Switching state (100).....	79
Figure 4.6	(a) Loss distribution of different MT and (b) Calculated efficiency of the Vienna type front-end AC-DC converter.....	80
Figure 4.7	Control scheme for the Vienna type front-end PFC rectifier.....	81
Figure 4.8	Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the Vienna type front-end PFC rectifier under load variations.....	84
Figure 4.9	Simulation results of the input AC mains current (i_a) along with its frequency spectrum for the Vienna type front-end PFC rectifier at (a) FL and (b) LL conditions.....	84
Figure 4.10	Comparison of power quality indices under varying load conditions of an active PFC rectifier with 6-pulse rectifier (a) Variation of THD of input current with load and (b) Variation of PF of input current with load.....	85

Figure 4.11	Hardware demonstrator of an active three-phase front-end AC-DC converter.....	86
Figure 4.12	Hardware results of (a) Input line-to-line AC voltages (v_{L-L}), (b) Input phase currents, (c) Input voltage and current, (d) DC-link voltage, (e) Input voltage frequency spectrum and (f) Input current frequency spectrum for the Vienna type front-end PFC rectifier under steady state conditions.....	87
Figure 4.13	Hardware results of (a) Input three-phase currents with DC-link voltage, (b) Input phase voltage (v_a), phase current (i_a) with DC-link voltages (c) Input voltage frequency spectrum and (d) Input current frequency spectrum for the Vienna type front-end PFC rectifier under dynamic load conditions.....	88
Figure 4.14	Schematic diagram of front-end Delta switch rectifier as PFC rectifier.....	89
Figure 4.15	Schematic diagram of front-end Delta switch AC-DC converter with detailed circuit configuration.....	90
Figure 4.16	Equivalent circuit of (a) AC side part of Delta rectifier. (b) Delta switch rectifier being equivalent to star network. (c) Delta switch rectifier for calculating zero-sequence component i_0	92
Figure 4.17	Theoretical waveform for the construction of the input current, $i_{N,a}$ (a) Converter output current, I_{dc} . (b) Third harmonic circulating current, i_0 . (c) Input current of DBR phase leg a, $i_{a,DBR}$. (d) Input phase current, $i_{N,a}$	94
Figure 4.18	Control scheme for the Delta type front-end AC-DC converter.....	95
Figure 4.19	(a) Generation of switching functions for the phase ‘a’ of Delta switch rectifier. (b) Combinational logic circuit used to generate the PWM pulse.....	96
Figure 4.20	Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the Delta type front-end converter under load variations.....	101
Figure 4.21	Frequency spectrum of input line current $i_{N,a}$ at (a) LL condition (20%). (b) FL condition (100%).....	102
Figure 4.22	Comparison of power quality indices with varying load of front-end AC-DC converter with conventional 6-pulse DBR.	

	(a) Variation of THD of input current with load and (b) Variation of PF of input current with load.....	102
Figure 4.23	Hardware results of the Delta type AC-DC converter (a) Input voltage, $v_{N,a}$ and current, $i_{N,a}$ (b) Harmonic spectrum of input current, $i_{N,a}$ (c) Output DC-link voltages, V_{dc} (d) Injected voltage. (e) Injected voltage and current.....	104
Figure 4.24	Hardware results of the Delta type AC-DC converter under varying load conditions (a) Input current $i_{N,a}$ (10 A/div) and voltage $v_{N,a}$ (100 V/div) with DC-link voltage V_{dc} (100 V/div); Time scale (20 ms/div). (b) Input three-phase currents (10 A/div) with output DC-link voltage V_{dc} (100 V/div); Time scale (20 ms/div). (c) Input current $i_{N,a}$ (10 A/div) and output DC-link voltage V_{dc} (100 V/div); Time scale (10 ms/div). (d) Input current $i_{N,a}$ (10 A/div) and voltage $v_{N,a}$ (100 V/div) with DC-link voltage V_{dc} (100 V/div); Time scale (10 ms/div).....	105
Figure 5.1	Schematic diagram of three-phase front-end hybrid AC-DC converter.....	112
Figure 5.2	Equivalent circuit indicating the circulating third harmonic current for (a) The analysis of input line current (b) Conduction of D_5 and D_6 (c) Conduction of D_6 and D_1 (d) Conduction of D_1 and D_2 (e) Conduction of D_2 and D_3 (f) Conduction of D_3 and D_4 (g) Conduction of D_4 and D_5	116
Figure 5.3	Theoretical waveforms for the construction of the input current, i_{as} (a) Converter output current, i_{dc} . (b) Converter output voltage (v_{d+} , v_{d-}) with injected voltage, v_{mn} . (c) Injected current, i_{zN} . (d) DBR input current i_{DBR} . (e) Input current, i_{as}	118
Figure 5.4	Waveforms of three-level boost converter switching cycle and inductor current when (a) $v_d < v_{dc}/2$ and (b) $v_d > v_{dc}/2$	122
Figure 5.5	Operating modes of three-level boost converter (a) Mode 1, (b) Mode 2, (c) Mode 3 and (d) Mode 4.....	123
Figure 5.6	Inductors ripple current waveform of three-level boost converter...	125
Figure 5.7	Control scheme for the hybrid front-end AC-DC converter.....	127
Figure 5.8	Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the hybrid front-end converter under load variations.....	128

Figure 5.9	Frequency spectrum of input line current i_{as} at (a) LL condition (20%) (b) FL condition (100%).....	129
Figure 5.10	Comparison of power quality indices with varying load of front-end AC-DC converter with conventional DBR (a) Variation of THD of input current with load and (b) Variation of PF of input current with load.....	129
Figure 5.11	Hardware results of the hybrid front-end AC-DC converter (a) Input phase voltage, v_{as} and phase current, i_{as} (b) Harmonic spectrum of input current, i_{as} (c) Output DC-link voltages, v_{c+} , v_{c-} (d) Injected neutral voltage of zig-zag transformer, v_{mN} . (e) Injected neutral voltage, v_{mN} and current, i_{zN} of zig-zag transformer.....	131
Figure 5.12	Hardware results of the hybrid front-end AC-DC converter (a) Switching pulses for S_+ (5V/div) and S_- (5V/div); Time scale (50ms/div) (b) Input phase current i_{as} (5A/div) and phase voltage v_{as} (20V/div) with DC-link voltages v_{c+} (200V/div), v_{c-} (200V/div); Time scale (10ms/div) under varying load conditions. (c) Input three-phase currents (2A/div) with output DC-link voltage v_{dc} (500V/div); Time scale (10ms/div) under varying load conditions. (d) Input phase current i_{as} (5A/div), output DC-link voltage v_{dc} (400V/div) with load currents i_+ (5A/div), i_- (5A/div); Time scale (20ms/div) under varying load conditions.....	132
Figure B.1	Schematic diagram of hardware implementation of three-phase active front-end AC-DC converter using FPGA controller.....	148
Figure B.2	Digital card of FPGA controller board.....	149
Figure B.3	Isolation and amplification circuit diagram for PWM pulses.....	151
Figure B.4	Connection diagram for voltage sensor.....	153
Figure B.5	Connection diagram for current sensor.....	153

LIST OF TABLES

Table 3.1	Winding voltages and currents of the asymmetric MSAT and its VA rating.....	38
Table 3.2	Winding voltages and currents of the non-isolated AMPC transformer and its VA rating.....	54
Table 3.3	Comparison of simulation results of MSAT and AMPC autoconfigured transformers with other multi-pulse autoconnected transformers for various power quality indices.....	63
Table 3.4	Comparison of MSAT and AMPC autoconfigured transformers with other multi-pulse autoconnected transformers.....	64
Table 4.1	Switching states and respective voltage/current with respect to mid-point (M).....	75
Table 4.2	Different MTs for the Vienna type front-end AC-DC converter.....	77
Table 4.3	Power quality indices for the Vienna type front-end PFC rectifier under varying load conditions.....	85
Table 4.4	Power quality indices for the Delta type front-end AC-DC converter under varying load conditions.....	106
Table 4.5	Comparison of the three-phase front-end AC-DC converters with some of the available systems in the literature	108
Table 5.1	Diode conducting sequence and currents of the hybrid front-end converter.....	115
Table 5.2	Power quality indices for the hybrid front-end AC-DC converter under varying load conditions.....	131
Table 5.3	Comparison of simulation and hardware results of harmonic contents in the input line current.....	132
Table 5.4	Comparison of the hybrid AC-DC converter with some of the available systems in the literature.....	134

LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
AMPC	Asymmetric multi-phase converter
CCM	Continuous conduction mode
CF	Crest factor
CIC	Current injection circuit
CSI	Current source inverter
DAC	Digital-to-analog converter
DBR	Diode bridge rectifier
DC	Direct current
DCM	Discontinuous conduction mode
DF	Distortion factor
DPF	Displacement power factor
DSP	Digital signal processor
FF	Form factor
FL	Full load
FPGA	Field programmable gate array
HPF	High pass filter
HVDC	High voltage direct current
LL	Light load
MCM	Mixed conduction mode
MT	Modulation technique
MSAT	Multi-phase staggering autoconfigured transformer
PCC	Point of common coupling
PF	Power factor
PFC	Power factor correction
PI	Proportional and integral
PNDBC	Prime numbered diode bridge converter

PST	Phase shifting transformer
PWM	Pulse width modulation
RF	Ripple factor
RMS	Root mean square
SWG	Standard wire gauge
TDD	Total demand distortion
THD	Total harmonic distortion
TUF	Transformer utilization factor
UPS	Uninterrupted power supplies
VSI	Voltage source inverter
ZSBT	Zero sequence blocking transformer

CHAPTER 1

INTRODUCTION

1.1 GENERAL

Three-phase front-end AC-DC converters are developed with improved power quality for reducing harmonics in AC mains and ripples in DC output. Since, these converters are observed as one of the strong means for power quality improvements in number of applications, therefore, the detailed investigations on these converters are considered as main objectives of this research work. In view of these main objectives, this chapter deals with the introduction to AC-DC converters, the state of art, power quality aspects and standards, performance parameters, objective and scope of this research work. At the end, outline of chapters of this thesis is briefly given for quick reference. This research work is targeted to provide a broad perspective on three-phase front-end AC-DC converters technology for power quality improvement.

Solid state AC-DC converters are widely used in number of applications such as adjustable speed drives, high voltage direct current (HVDC) transmission, electro-chemical processes such as electroplating, telecommunication power supplies, battery charging, uninterruptible power supplies (UPS), high capacity magnet power supplies, high power induction heating equipment's, aircraft converter systems, plasma power supplies, and converters for renewable energy conversion systems. These converters, which are also known as rectifiers, are generally fed from three-phase AC supply of power rating above few kW and have the problem of power quality in terms of harmonic injection, power factor (PF), AC voltage distortion and rippled DC outputs. Because of these problems in AC-DC conversion, several standards and guidelines are laid down, which are followed by designers, manufacturers and users. Therefore, various methods are used to mitigate these problems in AC-DC converters. Normally, filters are recommended in already existing installations, which may be passive, active or hybrid types depending upon the rating and

economic considerations. These filters are developed from small power to large power ratings to reduce the power quality problems of AC-DC converters. However, in some cases, the ratings of these filters are observed close to the converter rating, which not only increase the cost but also increases the losses and component count, resulting in reduced reliability of the system. In future installations, it is preferred to modify the converter structure at design stage using passive (magnetic), active or hybrid techniques. The passive wave shaping technique is normally based on magnetics in three-phase AC systems and corresponding developed systems are known as multi-pulse AC-DC converters. Active technique of AC-DC converters is widely used in number of applications. Hybrid technique of AC-DC converters is also widely used in medium and high-power applications. Therefore, a need is felt to carry out comprehensive study on front-end AC-DC converters and to investigate them for the engineers designing AC-DC converters having improved power quality performance.

1.2 PROBLEMS IN THREE-PHASE AC-DC CONVERTERS

The major problems in AC-DC converters are injection of harmonics at input AC mains and output DC loads. The degree to which harmonics can be tolerated is determined by the susceptibility of the load (or power source) to them. Traditionally, AC-DC power conversion has been dominated by diode or phase-controlled rectifiers, which act as non-linear loads on the power distribution systems and draw harmonic rich currents. These also cause poor supply PF, thus creating the power quality problems in the utility lines. The other associated problems with these AC-DC converters include:

1. Non-linearity, discontinuity and harmonics at the input and output voltages and currents.
2. Poor PF at the input AC mains.
3. Harmonics cause dielectric, thermal or voltage stress, which cause premature ageing of electrical insulation.
4. Voltage distortion at the point of common coupling (PCC) takes place due to the voltage drop of harmonic currents flowing through system impedances.

5. Slow varying rippled DC output at load end.
6. Capacitor banks getting overloading due to system resonance.
7. Interference on telephone and communication lines due to noise induced from the power conductors carrying harmonic currents.
8. Low efficiency and requires large size AC and DC capacitors.

Mitigation of power quality is often seen as synonym to reduction of harmonic voltage or current distortion. However, improving the immunity of the equipment can also mitigate the problem, although it may not be the most economical solution. The techniques for harmonic reduction include:

1. Use of filters: Hybrid of shunt passive and active filter.
2. Harmonic compensation or injection: Harmonic currents can be eliminated by inducing harmonic fluxes in the core of transformer with 180° phase shift from the harmonic fluxes induced by the current flowing in the transformer secondary.
3. Phase multiplication: It is the most effective technique for an installation which cause equal sized converters having equal loading and phase retard are used.

In view of these above-mentioned problems, regulatory agencies have issued several strict standards such as IEEE-519, IEC-1000, and IEC 61000-3-2, etc., are being enforced on the consumers. IEEE-519-2014 Standard namely “Recommended Practices and Requirements for Harmonic control in Electrical Power Systems” provide the guidelines of acceptable limits of harmonics and other aberrations in the waveform (Committee et al. 2014). To meet these standards and improve the power quality, use of passive, active and hybrid techniques have been made along with conventional rectifiers, especially in high power rating, in already existing installations. Fixed compensation, bulkiness of the components, series and parallel resonance phenomena in passive filters and large rating, and complexity of active power filters are the greatest drawbacks with these compensation techniques.

To overcome these drawbacks, improved power quality AC-DC converters are included as an inherent part of the AC-DC conversion system which produces higher efficiency, reduced size, and well-regulated DC output. The output voltage in these converters is regulated even under the fluctuations of the input voltage and changes in the load. Since the converter output voltage remains constant even under the supply voltage fluctuations, the power quality improvement converters can solve the supply brownout problem. These new breeds of rectifiers have made possible mainly because of the use of modern solid-state, self-commutating power semiconducting devices such as power MOSFETs, IGBTs, GTOs, etc., and are specifically known as switched mode rectifiers, power factor corrections (PFCs), high PFCs and pulse width modulation (PWM) rectifiers. The single-phase power quality improvement converters are already in common use and the industrial applications of three-phase converters have also emerged. It can be said that for medium to high power applications, the input rectifier is fed from a three-phase AC source.

1.3 PERFORMANCE PARAMETERS OF THREE-PHASE AC-DC CONVERTERS

The output voltage of AC-DC converters is DC but it normally contains ripples. An AC-DC converter should give a DC output voltage with a minimum amount of ripple contents. At the same time, it should maintain the input current as close to sinusoidal as possible and in-phase with the input voltage so that the PF is near unity. The power quality at the input and output of an AC-DC converter requires the determination of harmonic contents of the input current, the output voltage, and the output current. There are different types of AC-DC converter circuits and the performances are normally evaluated in terms of the following parameters.

Considering the average value of the output (load) voltage as V_{dc} , and average value of the output (load) current as I_{dc} , the output DC power can be given as,

$$P_{dc} = V_{dc} I_{dc} \quad (1.1)$$

Considering the root mean square (rms) value of the output voltage having ripples as V_{rms} , and the rms value of the output current as I_{rms} , the output AC power can be given as,

$$P_{ac} = V_{rms} I_{rms} \quad (1.2)$$

The output voltage can be considered as composed of two components: (i) the DC value, and (ii) the AC component or ripple.

The effective (rms) value of the AC component of the output voltage, V_{ac} as,

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \quad (1.3)$$

The form factor (FF), which is a measure of the shape of the output voltage, is given as,

$$FF = \frac{V_{rms}}{V_{dc}} \quad (1.4)$$

The ripple factor (RF), which is a measure of the ripple content, is defined as,

$$RF = \frac{V_{ac}}{V_{dc}} = \left\{ \left(\frac{V_{rms}}{V_{dc}} \right)^2 - 1 \right\}^{\frac{1}{2}} = (FF^2 - 1)^{\frac{1}{2}} \quad (1.5)$$

Generally, the voltage may be considered sinusoidal at the input of an AC-DC converter but the current is highly non-sinusoidal and not in-phase with the supply voltage. Let the V_s be rms value of sinusoidal input voltage, I_s is the rms input current, and I_{s1} is its fundamental component. If ϕ_1 is the angle between the fundamental components of the input current and voltage, ϕ_1 is called the displacement angle and the displacement power factor (DPF) or fundamental PF is defined as,

$$DPF = \cos \phi_1 \quad (1.6)$$

The measurement of distortion of a waveform compared to sinusoidal waveform is expressed by distortion factor (DF) that is defined as ratio of rms value of fundamental component I_{s1} to the rms value of distorted current waveform I_s .

Total harmonic distortion (THD) is a measure of the distortion of any waveform and is also known as harmonic factor. This is the most important power quality index and synonymous to power quality itself. The THD of the input current is defined as,

$$THD = \left\{ \left(\frac{I_s}{I_{s1}} \right)^2 - 1 \right\}^{\frac{1}{2}} \quad (1.7)$$

where I_{s1} is the rms value of fundamental component of the input current and I_s is rms value of total input AC current.

In the case, when the input current is purely sinusoidal, $I_{s1}=I_s$ and the PF equals the DPF. However, input current in AC-DC converters is not sinusoidal and so fundamental component of input current decides the PF. The displacement angle φ_1 becomes the impedance angle $\theta_1 = \tan^{-1}(\omega L / R)$ for an equivalent RL load. The input PF is defined as,

$$PF = \frac{V_s I_{s1}}{V_s I_s} \cos \varphi_1 = \frac{I_{s1}}{I_s} \cos \varphi_1 = DF \cdot DPF \quad (1.8)$$

The crest factor (CF), which is a measure of the peak input current $I_{s(peak)}$ as compared with its rms value I_s , is often of interest to specify the peak current ratings of devices and components. The CF of the input current is defined as,

$$CF = \frac{I_{s(peak)}}{I_s} \quad (1.9)$$

The efficiency of a converter, which is a figure of merit and compares the effectiveness is defined as,

$$\eta = \frac{P_{dc}}{P_{ac}} \quad (1.10)$$

The AC-DC converters use transformers in various constructions and the utilization of their winding varies with their configuration and pulse number of the AC-DC converter. The transformer utilization factor (TUF) is defined as,

$$TUF = \frac{P_{dc}}{V_{sec} I_{sec}} \quad (1.11)$$

where, V_{sec} and I_{sec} are rms voltage and rms current of the transformer secondary, respectively.

The TUF is defined on the basis of V_{sec} , I_{sec} and DC load power, P_{DC} . However, a number of transformer are there which have different primary winding arrangement and their utilization also affects TUF. The power rating (VA rating) of transformers that is based on rms voltage and current of each winding is an important parameter to compare their utilization. The VA rating of these transformers is calculated as,

$$VA \text{ rating} = 0.5 \sum (V_{winding} I_{winding}) \quad (1.12)$$

where, $V_{winding}$ is rms winding voltage and $I_{winding}$ is rms winding current of the transformer.

An ideal converter should have $V_{ac}=0$, $RF=0$, $TUF=1$, $THD=0$, $PF=DPF=1$ and $\eta=100\%$.

1.4 OBJECTIVES AND SCOPE OF THE RESEARCH WORK

The AC-DC converter interface to the electric utility in various applications exhibits non-linear characteristics, which deteriorates the power quality at the AC mains. The present work aims at eliminating the harmonics in the input AC mains of three-phase front-end AC-DC converters using various techniques and hence improving the power quality.

In this work, various techniques of power quality improvement at input AC mains for medium and high-power applications are investigated. The AC-DC converters with improved three-phase PFC rectifiers are used to improve the power quality indices at AC mains. The following research areas are identified for investigation in this research work and the same is simulated and implemented in hardware.

1.4.1 Analysis, design and development of three-phase front-end AC-DC converters employing passive power quality improvement technique

It is well known that increasing the pulse number in AC-DC converters results in improving the power quality indices at AC mains. In this research work, the technique of phase staggering and multi-phase techniques are investigated in detail. Two different configurations of 20-pulse autoconfigured transformer-based AC-DC converters are designed, modeled, simulated and developed for improving power quality at AC mains. The main emphasis is kept on reducing the magnetic rating, simplifying the configurations and reducing the number of components besides improving power quality at AC mains. These converters are designed, developed and tested with resistive load.

1.4.2 Analysis, design and development of three-phase front-end AC-DC converters employing active power quality improvement technique

Active three-phase front-end AC-DC converters are popular for medium and high-power applications. These active power quality improved AC-DC converters are designed and developed for the selected topologies namely Vienna rectifier and Delta switch rectifier. Further, voltage sensorless control technique is applied for the selected topologies which results in reduced number of sensors requirement. Both the topologies are designed, modeled and simulated to study their performance. The prototypes of these converters are developed and extensive tests are conducted to validate their design.

1.4.3 Analysis, design and development of three-phase front-end AC-DC converters employing hybrid power quality improvement technique

It has been observed that the injection of harmonic current on AC side results in reduction in different harmonic components of supply current, thus leading to the improvement in power quality indices. Based on this principle, current injection technique is applied in existing 6-pulse AC-DC converter to improve power quality indices. This hybrid power quality improvement technique is employed in the AC-DC converter using active modulation circuit and passive current injection circuit. The detailed analysis is made to

realize the hybrid AC-DC converter and the prototype of these converter is developed to validate the simulated results.

On the basis of the scope of research work, the present thesis embodies results of a detailed investigation on different three-phase front-end AC-DC converters. The work reported in this thesis are summarized below in the form of brief outlines of chapters.

1.5 OUTLINE OF CHAPTERS

There are six chapters and three appendices in this thesis document. The outline of this thesis is highlighted in Figure 1.1.

Chapter 1: This chapter introduces the front-end AC-DC converters. It presents the state of art on three-phase AC-DC converters in relation to the power quality improvement techniques. It covers power quality aspects, standards and performance parameters pertaining to three-phase AC-DC converters. Moreover, it includes main objectives and scope of the research work. At the end, outline of chapters are given in brief.

Chapter 2: This chapter includes an exhaustive literature review on various AC-DC converters based on different techniques employed for power quality improvements. The significant developments in three-phase front-end AC-DC converters are reviewed and detailed classification of the three-phase front-end AC-DC converters are discussed. Based on the review, research areas are identified for the proposed investigations.

Chapter 3: This chapter presents the design, modeling, simulation and development of two types of three-phase 20-pulse AC-DC converters. These converters are studied in terms of power quality parameters. New configurations of 20-pulse AC-DC converters based on zig-zag and delta connection of autotransformers are designed and developed, which results in reduction of size of magnets and improved power quality performances. Further, the detailed comparison in terms of power quality indices and performance parameters are presented.

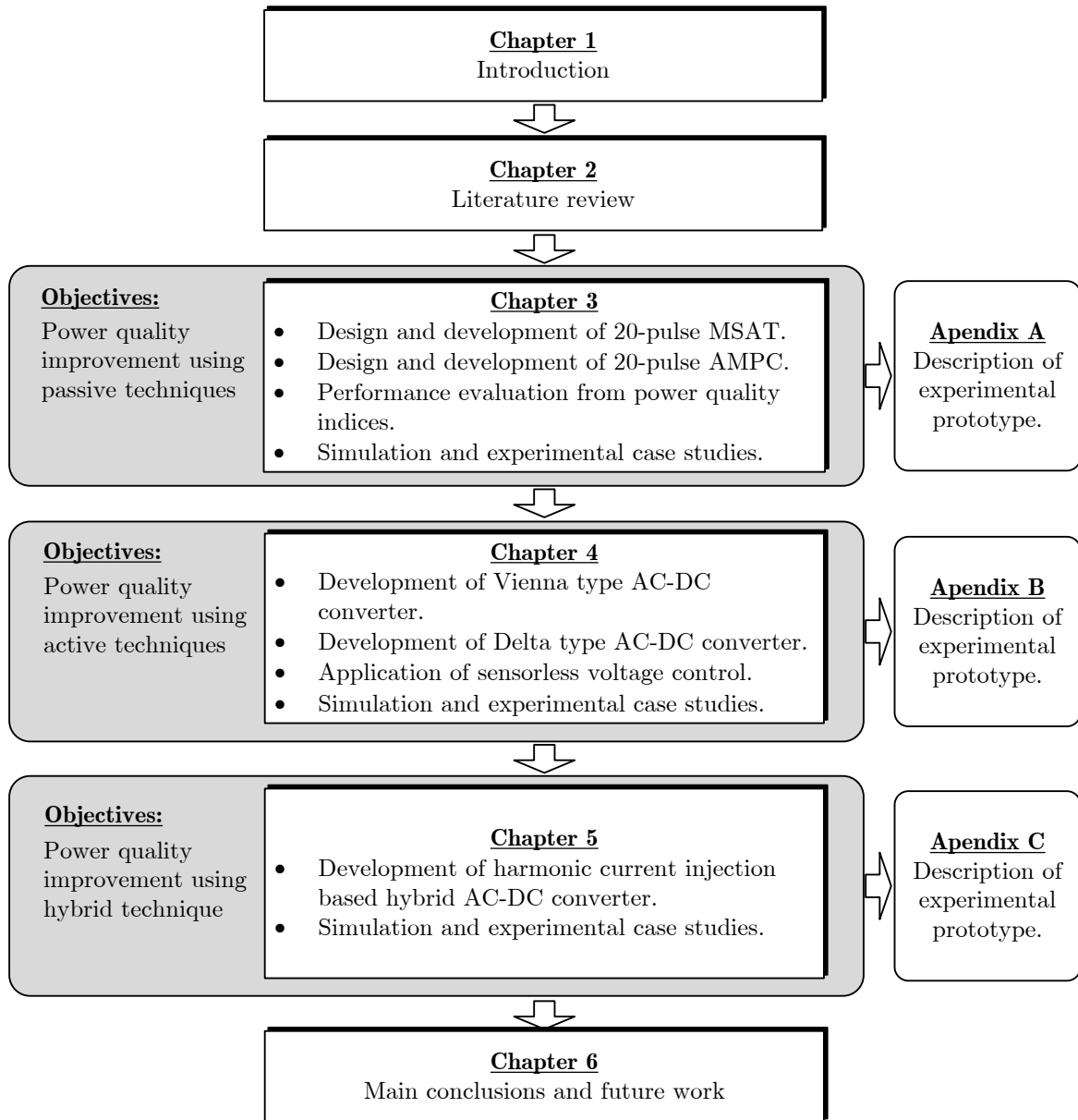


Figure 1.1: The outline of the thesis.

Chapter 4: In this chapter, the analysis, design, simulation and development of three-phase AC-DC converters using active power quality improvement techniques are carried out for the configurations based on Vienna and Delta type converter. These three-phase front-end AC-DC converters are employed with proposed voltage sensorless control for power quality improvement. Finally, a comprehensive comparative study with other converters are included.

Chapter 5: This chapter deals with design, modeling, simulation and development of three-phase front-end AC-DC converter based on hybrid power quality improvement technique. This three-phase front-end AC-DC converter is employed with harmonic current injection technique for power quality improvement wherein active modulation and passive current injection networks are used. At the end, the detailed comparative study is performed to highlight the performance of hybrid front-end AC-DC converter.

Chapter 6: This chapter summarizes the important findings emerging out of this research work and significant conclusions drawn from the work are presented in this thesis. It also enlists the scope of further work in power quality improvement techniques associated with three-phase front-end AC-DC converters.

CHAPTER 2

LITERATURE REVIEW

2.1 GENERAL

This chapter deals with a comprehensive review of classifications, significant developments of three-phase front-end AC-DC converter configurations and identified research areas. Extensive research work has been reported in the area of power quality improvement and also in control techniques for front-end AC-DC converters. The implementation of various international standards has given further motivation to innovate new configurations of improved power quality converters to adhere to these standard limits. The motivation for developing new configurations have been focused mainly to reduce the magnetic ratings, to simplify the control circuitry, to improve the efficiency of the system and finally to bring down the cost of the complete system. In active AC-DC converter system, the main focus of research has been on reduction of number of sensors required to reduce the cost and simultaneously to enhance the reliability of the converter system. An exhaustive literature review is carried out on different techniques used for power quality improvement in three-phase front-end AC-DC converters.

2.2 SIGNIFICANT DEVELOPMENTS IN THREE-PHASE FRONT-END AC-DC CONVERTERS

Three-phase front-end AC-DC converters are gaining widespread use at various power levels due to their improved performance and better power quality. They are able to achieve nearly unity input PF, negligible input AC line-current THD and regulated, reduced-ripple DC output voltage. There are new developments in the PFC technology for further improvement in their performance. The concepts of interleaved and multi-level/multi-pulse converters are being experimented in three-phase PFCs. It further improves their performance and eliminates the use of passive filters. Increased emphasis is laid on the

development of single-stage, three-phase PFCs which further reduces the size and increases the efficiency and reliability of three-phase PFC circuits.

Progress in the direction of solid-state device technology in terms of low conduction losses, higher permissible switching frequency, ease in gating process, and low voltage drop will further give a boost to the ever-growing technology of three-phase front-end AC-DC converters. Parallel with other developments, sensors reduction or elimination techniques have also been attempted and successfully implemented for many three-phase front-end AC-DC converter systems which have helped to further reduce the cost and increase the reliability of systems. High-speed microcontrollers, dedicated digital signal processors (DSPs) and field programmable gate array (FPGA) controllers have added a new dimension in this technology and very complex control algorithms can be implemented with least effort and high processing speed in these processors.

2.2.1 Brief classifications of three-phase front-end AC-DC converters

Three-phase front-end AC-DC converters can be classified based on:

1. Converter topology as boost, buck, buck–boost and multi-pulse/multi-level converters with unidirectional and bi-directional power flow.
2. Type of converter used as unidirectional and bi-directional converters.

Three-phase unidirectional PFCs are realized using a three-phase diode bridge followed by step-down chopper, step-up chopper, step-down/up chopper, isolated, forward, fly-back, push-pull, half-bridge, full-bridge, SEPIC, Cuk, Zeta and multi-level converters. These converters are implemented using single-stage conversion which reduces the size, weight, volume, losses and cost. A high-frequency isolation transformer offers reduced size, weight, cost, appropriate voltage matching and isolation. On the other hand, three-phase bi-directional PFCs consist of basic converters such as push-pull, half-bridge, voltage source inverter (VSI) topology or current source inverter (CSI) topology. Four-

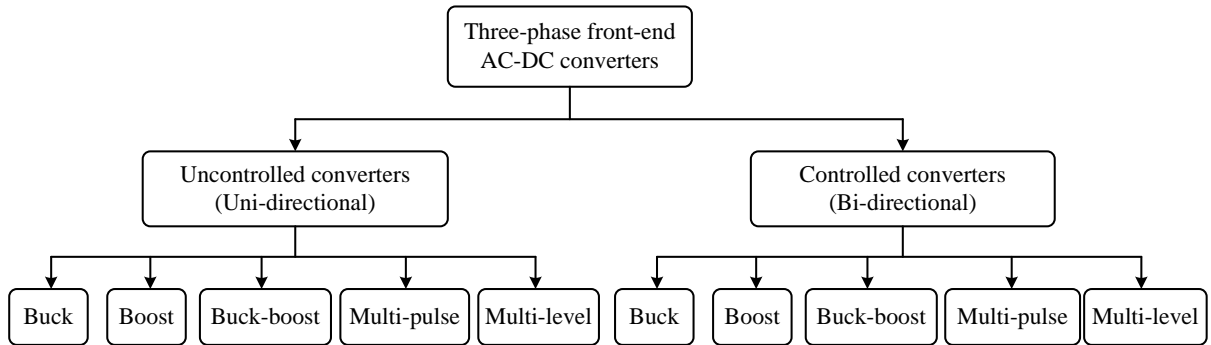


Figure 2.1: Brief classification of three-phase front-end AC-DC converters.

quadrant three-phase AC-DC power converters can be implemented using matrix converters.

Moreover, as per various standards limiting the voltage harmonics at PCC and requirements of reduction of voltage levels, the need of galvanic isolation becomes a must. In applications like welding, power supplies for telecommunication tower, DC arc-furnaces and some electro-chemical process working on low voltage/high current, it is absolutely essential to have an isolation. The above discussion leads to the classification of three-phase front-end AC-DC converters with reduced harmonics as shown in Figure 2.1. The applications of the converters as per classification are described as follows:

2.2.1.1 Boost converters

In case of three-phase boost converters the output voltage is greater than the peak input voltage. Unlike a single-phase boost converter, the voltage across the output capacitor does not have low-frequency ripple in balanced condition. Thus, a wide bandwidth voltage feedback loop can be used resulting in fast voltage control without distorting the input current references. The three-phase PFC are now in the stage of being developed using single-stage power conversion for transformer-coupled DC power supplies as the applications for three-phase systems are likely to increase, particularly in areas where high-performance and/or high-power density are critical, like the telecommunications industry or in autonomous system such as aerospace and marine. Moreover, in order to increase the

power handling capability of the system, single-switch boost converter stages can be connected in parallel, thus giving rise to interleaved parallel-stage circuits which improves the line currents, reduces the L, C input filter, output capacitor volume and reduces the current stress of the switching devices with interleaved switching topology. Three-phase, unidirectional boost converters are widely used nowadays as a replacement of conventional diode rectifiers to provide unity input PF, reduced THD at AC mains and constant, regulated DC output voltage even under fluctuations of AC voltage and DC load.

2.2.1.2 Buck converters

Three-phase, buck converters produce output voltages less than the converter input voltage. They have some attractive features compared to boost rectifiers such as meeting the requirement of varying controllable output DC voltage, inherent short-circuit protection, and easy inrush current. Their input currents can be controlled in the open loop and much wider voltage loop bandwidth can be achieved. Actually, the input current in such converters is distorted because the buck converter can work only under the condition that the input voltage is larger than the output voltage. For a higher voltage gain of the converter, the input current THD becomes unacceptably large. Therefore, three-phase unidirectional buck converter is not a good candidate for discontinuous conduction mode (DCM) input PFC. Further, three-phase buck derived forward converter contains the third winding to demagnetize the transformer. However, the demagnetizing current is blocked by the rectifier diodes. Therefore, three-phase forward converter is not suitable for PFC purpose. An unidirectional buck converter is a replacement of the thyristor semi-converter with improved power quality at AC mains and also at DC output.

2.2.1.3 Buck–boost converters

It is not possible to achieve output voltages lower than input in boost converters and higher than input in buck converters. The three-phase buck–boost type AC-DC converters have step-up or step-down output voltage characteristics and also have the capability of limiting the inrush and DC short circuit currents. Therefore, this type of converter is convenient for

several power supplies and is highly suitable for input PFC. These converters have either isolated or non-isolated DC output from input AC mains. These converters are also realized by combination of three-phase diode bridge with filter and buck–boost DC-DC converters such as Cuk, SEPIC, flyback, etc. For an isolated DC output, a high-frequency transformer of reduced size in conjunction with flyback, isolated Cuk, Zeta or SEPIC converters is used along with the rectifier at the front-end. A three-phase flyback converter has all the advantages of buck–boost converter without any limitation. These advantages make flyback converter more preferable for PFC with DCM input technique.

2.2.1.4 Multi-pulse converters

In high-power applications, AC-DC converters based on the concept of multi-pulse, namely, 12, 18, 24, 30, 36, 48 ... pulses are used to reduce the harmonics in AC supply currents. They use either a diode bridge or thyristor bridge and a special arrangement of magnetics through transformers and tapped inductors. Therefore, the last category is multi-pulse converters with unidirectional and bi-directional power flow.

2.2.1.5 Multi-level converters

Apart from multi-pulse converters, multi-level converters are also used effectively for reducing harmonics at the PCC. An AC-DC converter with the number of levels is effective in reducing the harmonics and switching loss in the converter through operating the switching devices at low switching frequency.

2.2.2 Power quality improvement using three-phase front-end AC-DC converters

Three-phase front-end AC-DC converters are used in various fields such as in industries, electric utility, aircraft and for commercial applications. Selection of suitable improved power quality three-phase front-end AC-DC converters for a particular application is an important and critical decision to be taken by an application engineer and involves a deep knowledge of the subject and experience in the field. Some important factors to be taken into consideration for selection of the right converter configuration for a specific

applications are permitted THD, input PF, required level of power quality in DC output (voltage-ripple, voltage regulation, sag, swell), type of output DC voltage (constant, variable), nature of DC output (isolated, non-isolated), requirement of DC output (buck, boost, and buck–boost), power flow (unidirectional, bi-directional), number of quadrants (one, two, or four), voltage rating (low, medium, high), power rating (low, medium, high), efficiency, size and weight, reliability and cost of converter system. These factors act as guiding factors for the proper selection of a converter for a specific application. The three-phase PFC converters are more suitable for utility-based application, since the input power quality can be improved and therefore the overall system will achieve higher efficiency and reliability.

The state of art on three-phase front-end AC-DC converters indicates that a number of converter configurations have been proposed by different researchers. The detailed classification of uncontrolled three-phase AC-DC converters are shown in Figure 2.2. The power quality improvement techniques in the front-end AC-DC system is broadly classified into passive, active and hybrid techniques. Further, the front-end AC-DC converter system consists of only DBR and not thyristor circuits, there is no possibility of output voltage regulation. The passive techniques use multi-pulse AC-DC converter for power quality improvement. The major breakthrough in the multi-pulse technology of AC-DC converters is due to phase shifting process through transformers to convert original three-phase AC supply to multi-phase AC supply that result in higher number of pulses in DC output for reducing ripple content and high number of steps in AC mains current to make it close to sinusoidal with reduced and acceptable THD. Further, the power quality improvement is achieved by various transformer configurations and also increased pulse number AC-DC converters. The optimum value of DC-link inductor and leakage reactance of input transformer drastically reduce the values of THD of AC mains currents thus resulting in improved power quality.

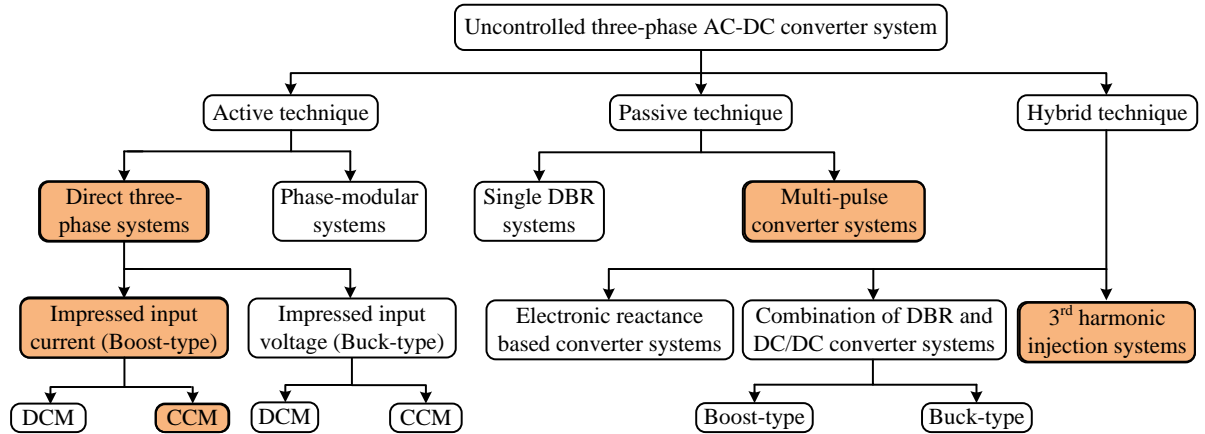


Figure 2.2: Detailed classification of three-phase front-end AC-DC converters.

Further, the sinusoidal control of the AC mains currents and output DC voltage regulation are achieved using active techniques. Here, high frequency PWM converters are normally used and thereby results in increased power density. Various improved control techniques are available in the literature for power quality improvement in active type AC-DC converters. Depending on the applications and output voltage range, either buck or boost-type topologies are chosen for the power quality improvement.

Third harmonic injection concepts are more popular and it is a major group of hybrid AC-DC converter circuits. The current injection is carried out either by active or passive injection network. The input current waveforms are shaped into sinusoidal currents and thereby improves the power quality of the AC-DC converters. Here, three-phase diode bridge rectifier (DBR) is employed at the front-end for AC-DC conversion. In the DC side, an active network used for current modulation, injection and voltage regulation for power quality improvement. The resultant topology is simple in construction and require less complex control technique.

2.3 LITERATURE REVIEW ON THREE-PHASE FRONT-END AC-DC CONVERTERS

AC-DC converters are developed in vast varying configurations to fulfil the exact requirements of wide range of applications. Accordingly, the review of the literature follows, that has given direction to the investigations on development of new configurations of AC-DC converters.

2.3.1 Passive AC-DC converters

A conventional three-phase AC-DC converter fed power electronic systems exhibit a THD of more than 10%. This leads to reduced input PF, increased voltage distortion, overloading of the capacitor banks, heating of equipment and other power quality issues. At present, AC-DC converters used in power electronic systems are expected to draw sinusoidal input current at unity PF from the utility (Yun et al. 2012). Hence, power electronic systems are supposed to comply to IEEE-519 (Committee et al. 2014) and IEC 61000-3-2 standards (IEC 1998). Phase shifting transformer (PST) based multi-pulse AC-DC converters is a well-established method to reduce harmonic distortion (Paice 1999). Currently, use of 6 or 12-pulse PSTs based multi-pulse AC-DC converter for power electronic system is popular and has resulted in high THD and low PF. Further, PST based multi-pulse AC-DC converters are classified into isolated and non-isolated type with symmetric/asymmetric configuration as shown in Figure 2.3. It is established that the symmetric autoconnected transformer-based converters produce harmonic content greater than 5% and requires higher magnetic rating (Kalpana et al. 2010; Meng et al. 2013, 2015a). Use of high-pass filter (HPF) in conjunction with PST for further reduction in harmonic distortion is suggested in (Kalpana et al. 2010). In addition, application of filters at the input and output side of the PST to smooth out the ripples is demonstrated in (Blanchery 2011; Feng et al. 2014). Increasing the pulse number intending to reduce harmonic distortion with superior waveform quality has been addressed in (Bhim. Singh et al. 2006; Yang et al. 2015). However, increase in pulse number profoundly impacts the magnetic rating of the PST configuration (Kalpana et al. 2013; Singh et al. 2010).

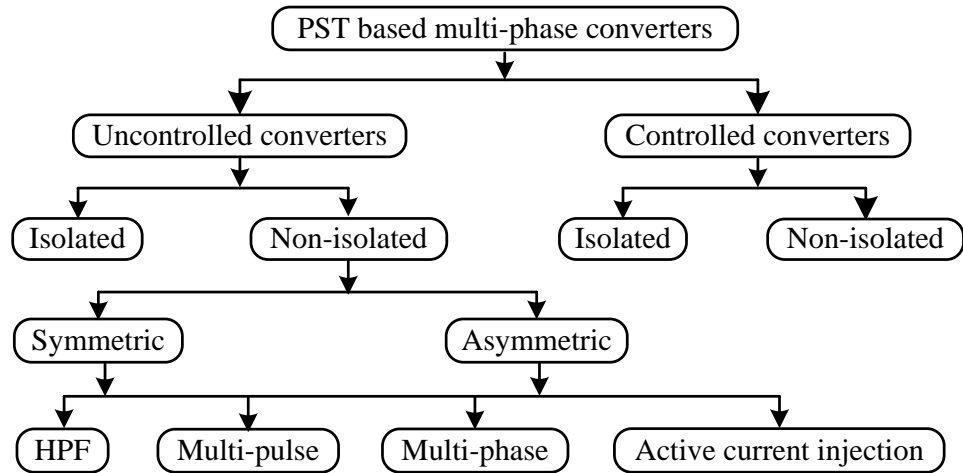


Figure 2.3: Classification of various types of multi-pulse AC-DC converters.

Another method to negate the detriment of increased harmonic distortion is by increasing the number of phases (Derek Albert Paice 2009; P et al. 2018). However, this necessitates additional diode bridges connected at the output of PST. This in turn increases cost and complexity of the system. In addition, for the satisfactory and independent operation of diode bridges connected in parallel, zero sequence blocking transformer (ZSBT) is inevitable. Recently the advent of pulse doubling method using an inter-phase transformer has gained a lot of attention, as it requires a PST with lesser magnetic rating (Abdollahi and Gharehpetian 2016; Rohollah Abdollahi 2013; Singh and Gairola 2008) when compared to the magnetic rating of PST without pulse doubling technique.

Furthermore, efforts have also been made to develop active current injection techniques for low and medium power applications to draw near sinusoidal currents from the utility in combination with PST (Biela et al. 2011; Sewan Choi et al. 1996). Application of a chopper switch to enhance the voltage and frequency regulation while the use of two-stage auxiliary circuit at the rectifier end for power quality improvement has been presented in (Meng et al. 2015b; Sheelvant et al. 2017; Singh et al. 2008). Further, state of the art PST based rectifiers and their modeling are detailed in (Chiniforoosh et al. 2016; Solanki et al. 2015) respectively. The drawbacks associated with these active current injection techniques are

increased control complexity, feedback sensors, and difficulty in sustaining PF. This eventually leads to higher financial implications and reduced reliability.

2.3.2 Active AC-DC converters

2.3.2.1 Vienna type AC-DC converter

The conventional front-end 6-pulse diode rectifier with capacitive DC-link voltage, results in distortion of mains voltage and current thereby leading to power quality problems. One of the methods to improve input power quality using multi-pulse converter based front-end AC-DC converter system (Kalpana et al. 2010; Meng et al. 2013, 2015a; P et al. 2018; Prakash et al. 2015). Also, current injection in DC side through active devices are commonly employed in low and medium power applications to draw near sinusoidal currents from the utility along with the multi-pulse transformer (Biela et al. 2011; Sewan Choi et al. 1996; Sheelvant et al. 2017; Swamy 2015). In addition, connecting Vienna rectifier in parallel with multi-pulse rectifier for active filtering is proposed in (Izadinia and Karshenas 2018). The advancement of the multi-pulse technique leads to the betterment of input power quality even though, the main issues with these techniques are increased magnetic rating, weight, and volume of the system.

Another method to improve power quality at input mains with reactive power compensation using Vienna rectifier is demonstrated in (Kedjar et al. 2014). Furthermore, efforts have also been made to develop efficient control methods using space vector modulation and carrier-based modulation (Hang et al. 2014). To simplify the control complexity, one cycle control strategy is proposed in (Chongming Qiao and Keyue Ma Smedley 2003) and modified one cycle control strategy is presented in (Gong et al. 2014), which improves the DC-link voltage utilization and neutral balancing. On one hand, a sensorless voltage control is introduced for easy control (Kastha and Mukherjee 2015) and on the other hand, a sensorless current control is proposed in (Wang et al. 2007). These sensorless techniques are proposed for reducing the cost and also the complexity in control. Hybrid control scheme is described in (Li et al. 2018) for regulating DC-link voltage, controlling input current and maintain neutral point voltage in balanced condition.

In addition, the analysis is extended to mixed conduction mode (MCM), a state in which transition between DCM and continuous conduction mode (CCM) have taken place. A feedforward compensator is proposed for MCM by considering input inductance value, switching frequency and system power level (Hang et al. 2013). The interleaved Vienna rectifier with high efficiency and its switching frequency circulation current reduction technique is developed in (Wang et al. 2018), which discusses the loss calculations in detail. In order to reduce the losses associated with the rectifier, output ripples and operating with unity PF, the most advantages modulation techniques are presented in (Baumann and Kolar 2005). The comparative evaluation of modulation methods and its advantages are investigated in (Baumann et al. 2008; Nussbaumer et al. 2008). Higher device stress, low frequency distortion, difficulties in neutral point balancing, less efficient utilization of DC-link voltage, increased control complexity and cost, limited dynamic performance during transients/low PF are the associated drawbacks of the existing control techniques.

2.3.2.2 Delta type AC-DC converter

Grid connected AC-DC converters are mostly employed with PFC circuit for its better power quality performance such as high input PF, low harmonic distortion of input current and high efficiency. In addition, it should have smaller size and weight, low conducted and radiated emissions, better load sharing, and easily serviceable under working conditions (Yun et al. 2012). But depending upon the requirements the size may vary in medium and high-power applications. Many promising PFC techniques have been reported for AC-DC converters (Singh et al. 2003b). Some of them are using passive techniques, active techniques, soft switching techniques, active filters etc. The main objective of the above-said techniques is to comply with the power quality indices required by the load. The PFC based on harmonic current injection technique is more popular and it has been discussed in (Itoh and Ashida 2008; Kanaan and Al-Haddad 2012; Kolar and Friedli 2013; Vazquez et al. 2009). In general, the front-end power quality improvement is achieved by passive, active or hybrid techniques.

The star connected injection circuit is more popular and well know structure available in the literature (Chongming Qiao and Smedley 2002a; b; Kanaan et al. 2004; Minibock and Kolar 2005). Efforts have been made to develop efficient control techniques using various methods that are studied in the literature. Moreover, the star connected injection circuit with center-tapped DC-link and spilt output capacitors experience reduced voltage stress across the active switches, that is ideally half DC-link voltage, but requires full current rating capability. In addition, the possibility of shoot-through of a bridge-leg due to short-circuit across the DC-bus is more predominant. These issues associated with star connected injection circuit does not exists in Delta connected circuits. Hence, three-phase three wire system widely uses an injection circuit as Delta connected configuration (Collier et al. 2014; Collier and Heldwein 2013; Greul et al. 2006; Hartmann et al. 2009, 2012; Noor et al. 2007; Soeiro et al. 2011, 2015; Soeiro and Kolar 2013). Many modulation schemes are reported in the literature (Collier et al. 2014; Collier and Heldwein 2013; Noor et al. 2007) for different Delta rectifier applications. Additionally, the Delta connection is extended to hybrid rectifiers (Soeiro and Kolar 2013) and multi-level rectifier applications (Soeiro et al. 2011, 2015) wherein the number of switches have increased and its associated control techniques gets more complicated. Hence, Delta switch rectifier with less complex modulation or control technique is of greater importance.

2.3.3 Hybrid AC-DC converters

There are variety of concepts available in the literature for PFC in the industrial applications (Singh et al. 2003a). Some of them are passive components, active elements, soft switching techniques, active filters etc. The PFC based on harmonic current injection technique is more popular, and it has been discussed in (Itoh and Ashida 2008; Kanaan and Al-Haddad 2012; Vazquez et al. 2009). In general, the input side power quality improvement can be achieved by passive, active or hybrid techniques. Passive techniques involve the multi-pulse transformer-based methods (P et al. 2018), active techniques

involve the switch-based topologies (Prakash P et al. 2018) and hybrid technique involves both of the above-said techniques (Sheelvant et al. 2017).

The harmonic mitigation in three-phase AC-DC converters have also been done by current injection techniques that have modulation and current injection circuits (Nishida et al. 2014). The modulation and current injection circuits are either passive or active components (Abi Rached et al. 2010; Jankovic et al. 2012; Kanaan et al. 2004, 2012; Li and Chen 2007; Naik et al. 1995; Norhisam et al. 2010; Pejovic and Janda 1998, 1999; Sikyung Kim et al. 1994; Vazquez et al. 2009; Vreljakovic et al. n.d.; Xiaoqing Li and Guozhu Chen 2007; Zynal and Younis 2013). Depending upon the topology, the circuit has its own merits and demerits. Primarily, the modulation circuit consists of passive elements which are designed to extract the particular harmonic current (Kanaan et al. 2012; Li and Chen 2007; Pejovic and Janda 1999; Sikyung Kim et al. 1994; Xiaoqing Li and Guozhu Chen 2007; Zynal and Younis 2013). The main drawback of this method is the requirement of large space due to its passive nature, poor dynamic response, resonance problem and less efficiency. The other type of modulation circuit is made up of active elements (Abi Rached et al. 2010; Chongming Qiao and Smedley 2002a; b; Collier et al. 2014; Collier and Heldwein 2013; Greul et al. 2006; Hartmann et al. 2009, 2012; Kanaan et al. 2004; Minibock 2001; Minibock and Kolar 2005; Naik et al. 1992; Noor et al. 2007; Norhisam et al. 2010; Pejovic and Janda 1998; Saravana Prakash P and Kalpana 2016; Soeiro et al. 2011, 2015; Soeiro and Kolar 2013). These topologies have better dynamic response and efficiency but requires complex control structure. Various advanced control techniques are adopted for improving the efficiency and reducing the component size.

The current injection circuit is either made up of passive or active components. The passive components can be either transformers or passive elements (Abi Rached et al. 2010; Itoh and Ashida 2008; Kanaan et al. 2012; Li and Chen 2007; Naik et al. 1992; Pejovic and Janda 1998; Sikyung Kim et al. 1994; Vreljakovic et al. n.d.; Xiaoqing Li and Guozhu Chen 2007) which has its own merits and demerits. It is mainly designed for a particular system specification, and hence it is more sensitive to system parameter variations. Similarly, the active components are switch-based topologies (Abi Rached et

al. 2010; Jankovic et al. 2012; Kanaan et al. 2004; Zynal and Younis 2013) which has its own advantages and disadvantages. These techniques require accurate current control derived from the input voltage information wherein accurate magnitude and phase angle extraction is the challenging task. Further, the current injection circuit is realized using L-C branches, tuned for third harmonic frequency. The main drawback of this injection circuit is, it draws excessive fundamental current and susceptibility to resonance, and also the system performance is sensitive to the variation of parameters (Sikyung Kim et al. 1994). The main objective of the modulation and current injection techniques are to maintain the power quality indices well within IEEE and IEC standards (Committee et al. 2014; IEC 1998).

2.4 IDENTIFIED RESEARCH AREAS

On the basis of an exhaustive literature survey on various three-phase front-end AC-DC converters, the following research areas have been identified in this research work.

1. To develop new configurations of multi-pulse AC-DC converters using autoconfigured transformer for power quality improvement.
2. To analyze the performance of new configurations of multi-pulse AC-DC converters and examine the possibility of reducing magnetic rating of the multi-pulse transformer.
3. Design of three-phase front-end AC-DC converters employing active power quality improvement techniques.
4. Development of voltage sensorless control technique for the active front-end AC-DC converters.
5. Design of three-phase front-end AC-DC converter utilizing hybrid power quality improvement technique.
6. Verification of some of the best topologies of three-phase front-end AC-DC converters using MATLAB/Simulink and hardware prototype.

2.5 CONCLUSION

A comprehensive review of AC-DC converters has been presented to explore a wide variety of configurations of three-phase front-end AC-DC converters. The three-phase front-end AC-DC converters have been investigated by number of researchers for various applications and the need is felt to investigate further using modern tools and techniques to evolve new configurations of these AC-DC converters. The classification of three-phase front-end AC-DC converter (based on the literature survey) has also highlighted the fact that the possibility of power quality improvement techniques must be investigated in detail.

CHAPTER 3

POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING PASSIVE TECHNIQUE

3.1 INTRODUCTION

This chapter introduces two new 20-pulse autotransformer configurations for power quality improvement in medium and high-power applications. First, the design and development details of the proposed 20-pulse multi-phase staggering autoconfigured transformer (MSAT) configurations are described in detail. Secondly, an improved version of the 20-pulse asymmetric multi-phase converter (AMPC) transformer configuration is introduced with reduced magnetic rating wherein the design and development details are also explained. Further, the power quality performance of both the configurations are analysed in terms of standard power quality indices. Finally, the simulation and experimental results pertaining to both the circuits are provided with a detailed comparative evaluation.

3.2 PROBLEM FORMULATION

The availability of multi-pulse AC-DC converters results in the various industrial applications (Singh et al. 2004) wherein the power quality indices are maintained within the standard limits. From the literature, applications urging harmonic free source current fed from multi-pulse non-isolated transformer-based techniques increases the complexity and magnetic rating of transformer configuration. So, a trade-off has to be made between pulse number and complexity of transformer configuration. Hence, with this motivation autoconfigured transformer with less complexity and reduced magnetic rating for power quality improvement at input AC mains is presented in this chapter.

3.3 ASYMMETRIC NON-ISOLATED 20-PULSE MSAT CONFIGURATION

The 20-pulse MSAT is realized by combining the delta and zig-zag transformers. Contrary to the prior art multi-pulse autoconnected transformer, the configuration requires a magnetic rating of only 40% of the load rating with improved power quality indices. Moreover, an additional advantage is the creation of neutral point ascribed to inbuilt zig-zag windings available in the autoconfigured transformer. Therefore, with this suggested configuration, the performance of zig-zag transformer can be achieved within the autoconfigured transformer.

Figure 3.1 shows the schematic diagram of the proposed 20-pulse asymmetric non-isolated MSAT. It comprises of front-end asymmetric MSAT with inherent power quality improvement capability and two prime numbered diode bridge converter (PNDBC) at the output. The proposed asymmetric non-isolated MSAT is capable of generating a set of prime numbered phases from the available three-phase input AC source. These set of prime numbered phases can be 5-phase, 7-phase, 11-phase, 13-phase and so on. With the increase in number of prime numbered phases, the design of autoconfigured transformer gets more complicated. So, in this research work, number of prime numbered phases are limited to 5. The set of prime numbered phases created by an asymmetric MSAT are fed to the PNDBC. The total number of output pulses generated by the PNDBC is double the prime numbered output phases, i.e., for 5-phase, the number of output pulses generated are 10-pulse which can be generalized as (3.1),

$$\begin{aligned} &\text{Total number of output pulses from a PNDBC } (P) = 2 \\ &\times \text{Number of prime numbered output phases } (N). \end{aligned} \quad (3.1)$$

In MSAT, the required phase angle between two adjacent phases (φ) is obtained as (3.2),

$$\begin{aligned} &\text{Adjacent phase displacement angle } (\varphi) = 360^\circ / \\ &\text{Total output prime numbered phases.} \end{aligned} \quad (3.2)$$

In phase-staggered approach, the required phase staggering angle among the PNDBC (Ψ) is obtained as (3.3),

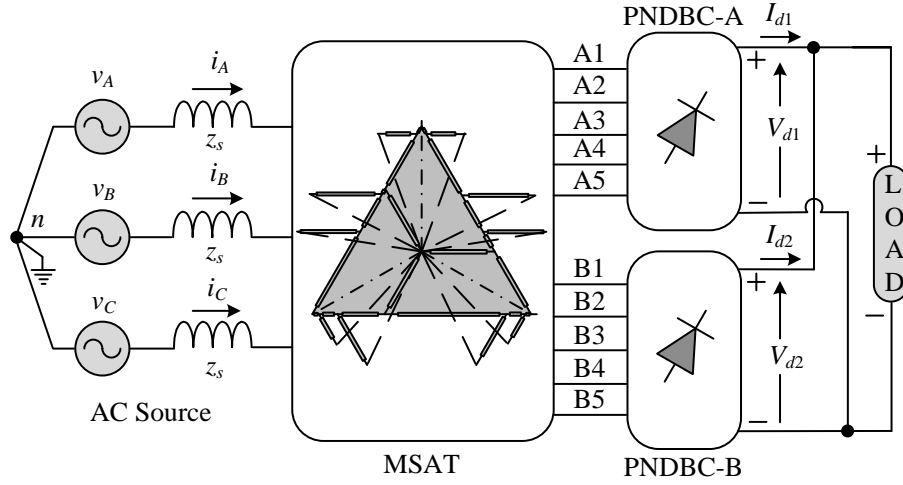


Figure 3.1: Schematic diagram of the 20-pulse asymmetric MSAT fed high power DC load.

$$\text{Phase-staggered angle } (\Psi) = 360^\circ /$$

$$\text{Total number of output pulses.} \quad (3.3)$$

The elimination of harmonics in a multi-phase system is achieved by displacing adjacent phases at an equivalent angle of φ . The number of output pulses for a 5-phase system is 10, therefore input source current waveform is made up of 20 steps that nearing a sinusoidal waveform. Hence, using the proposed asymmetric non-isolated MSAT, higher number of steps in the input source current can be achieved by lower order of prime numbered phases.

The front-end asymmetric non-isolated MSAT configuration discussed herein creates two sets of prime numbered 5-phase supply ($N=5$) that feeds two PNDDBC ($P=10$). Thus, the total number of output pulses from the two converters is $2P$. Each PNDDBC A and B are fed by two 5-prime numbered sets of phase-staggered voltages A1, A2, A3, A4, A5 and B1, B2, B3, B4, B5 respectively, generated by the asymmetric MSAT. The winding diagram of proposed asymmetric MSAT is shown in Figure 3.2(a). The 10 phase-staggered voltages are at an angle of $\pm\Psi$ and their magnitudes are essentially identical. Therefore, the phase angle between (A1, B1) is $\pm\Psi/2$ with respect to the supply voltage v_A . Similarly, the phase angle for other phase staggered voltages between (A2, B2), (A3, B3), (A4, B4) and (A5, B5) is $\pm\Psi$ as shown in Figure 3.2(b). To create phase-staggered voltages of $\pm\Psi$, the

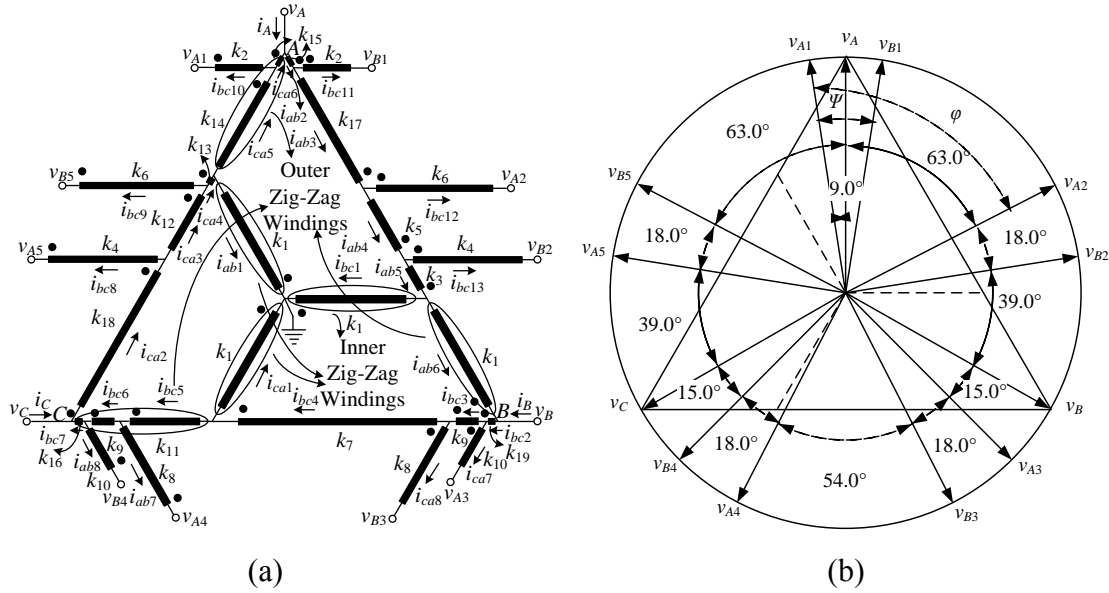


Figure 3.2: (a) Winding and (b) Resultant phasor diagrams of the asymmetric MSAT representing the phase-staggered angle positions of different phasors.

asymmetric MSAT is designed by estimating the approximate turns value for various windings.

The asymmetric MSAT has 29 windings in total with combined delta and zig-zag transformer configuration as shown in Figure 3.2(a). The key advantage of the asymmetric MSAT is its ability to create an effective neutral point. Due to this neutral point, the system remains in balanced condition in case of single-phasing and also, the harmonic currents generated by the non-linear loads are circulated within the system thereby, avoiding the injection of harmonic currents into the input AC mains. Further, the zig-zag transformer formed by connecting inner windings at $1/3^{\text{rd}}$ of phases of autoconfigured transformer and part of autoconfigured transformer windings for creating the outer phases of zig-zag transformer, reduces the overall magnetic rating of the autoconfigured transformer by 26% of load rating. With this uncomplicated modification suggested, the performance of zig-zag transformer is achieved within the autoconfigured transformer. Therefore, the total VA rating of the inner zig-zag winding is only a small fraction of the load rating.

3.3.1 Design and analysis of the asymmetric MSAT configuration

Figure 3.2(a) and (b) depicts the various windings and phasor representation pertaining to the proposed autoconfigured transformer respectively.

3.3.1.1 Design of asymmetric MSAT configuration

Constants K_1 - K_{19} decides the winding turns value. A typical value of three-phase and prime numbered 5-phase voltages of AC source are chosen to determine the number of turns. The three-phase voltages are expressed as (3.4),

$$\begin{aligned} v_A &= v_R \sin \omega t \\ v_B &= v_R \sin(\omega t - 120^\circ) \\ v_C &= v_R \sin(\omega t + 120^\circ) \end{aligned} \quad (3.4)$$

v_R – amplitude of phase voltage. The phase angle between the phase staggered voltages and input phase voltage corresponding to PNDBC A are given in (3.5),

$$\begin{aligned} v_{A1} &= v_R \angle 9^\circ \\ v_{A2} &= v_R \angle -63^\circ \\ v_{A3} &= v_R \angle -135^\circ \\ v_{A4} &= v_R \angle 153^\circ \\ v_{A5} &= v_R \angle 81^\circ \end{aligned} \quad (3.5)$$

Similarly, the phase angle between phase staggered voltages and input phase voltage corresponding to PNDBC B are given in (3.6),

$$\begin{aligned} v_{B1} &= v_R \angle -9^\circ \\ v_{B2} &= v_R \angle -81^\circ \\ v_{B3} &= v_R \angle -153^\circ \\ v_{B4} &= v_R \angle 135^\circ \\ v_{B5} &= v_R \angle 63^\circ \end{aligned} \quad (3.6)$$

The resultant phase staggered voltages corresponding to PNDBC A obtained from Figure 3.2(b) are expressed as follows,

$$\begin{aligned} v_{A1} &= k_1 v_{AB} - k_{14} v_{CA} - k_2 v_{BC} \\ v_{A2} &= k_1 v_{BC} + (k_3 + k_5) v_{AB} + k_6 v_{BC} \\ v_{A3} &= k_1 v_{CA} + (k_7 + k_9) v_{BC} + k_{10} v_{CA} \\ v_{A4} &= k_1 v_{CA} - k_{11} v_{BC} - k_8 v_{AB} \\ v_{A5} &= k_1 v_{AB} + (k_{12} + k_{13}) v_{CA} - k_4 v_{BC} \end{aligned} \quad (3.7)$$

Similarly, the resultant phase staggered voltage of PNDDB B are expressed as follows,

$$\begin{aligned}
v_{B1} &= k_1 v_{AB} - k_1 v_{CA} + k_2 v_{BC} \\
v_{B2} &= k_1 v_{BC} + k_3 v_{AB} + k_4 v_{BC} \\
v_{B3} &= k_1 v_{CA} + k_7 v_{BC} + k_8 v_{CA} \\
v_{B4} &= k_1 v_{CA} - (k_{11} + k_9) v_{BC} - k_{10} v_{AB} \\
v_{B5} &= k_1 v_{AB} + k_{13} v_{CA} - k_6 v_{BC}
\end{aligned} \tag{3.8}$$

Thus, the constants obtained from the above equations are: $k_1=0.3295$, $k_2=0.0903$, $k_3=0.1042$, $k_4=0.2928$, $k_5=0.1985$, $k_6=0.3117$, $k_7=0.5593$, $k_8=0.2645$, $k_9=0.0848$, $k_{10}=0.119$, $k_{11}=0.2296$, $k_{12}=0.1986$, $k_{13}=0.0269$, $k_{14}=0.3289$, $k_{15}=0.0006$, $k_{16}=0.0208$, $k_{17}=0.3678$, $k_{18}=0.445$, $k_{19}=0.0207$. Considering one volt per turn, the number of turns or voltage across each winding of the asymmetric MSAT is decided by the winding turns value K_1 - K_{19} .

A. Winding voltages of the asymmetric autoconfigured transformer:

The asymmetric MSAT is designed by considering three single-phase transformers T_A , T_B and T_C . The rms voltages across each winding are calculated by considering the line-to-line rms voltage and their corresponding winding constants. The equations pertaining to winding voltages (rms) of transformer T_A are given by (3.9),

$$\begin{aligned}
v_{ab2,rms} &= v_{ca6,rms} = \left\{ \frac{2}{3} - (k_{17} + k_5 + k_3) \right\} v_{LL,rms} \\
v_{ab3,rms} &= \left\{ \frac{2}{3} - (k_{15} + k_5 + k_3) \right\} v_{LL,rms} \\
v_{ab4,rms} &= \left\{ \frac{2}{3} - (k_{15} + k_{17} + k_3) \right\} v_{LL,rms} \\
v_{ab5,rms} &= \left\{ \frac{2}{3} - (k_{15} + k_{17} + k_5) \right\} v_{LL,rms}
\end{aligned} \tag{3.9}$$

The equations pertaining to winding voltages (rms) of transformer T_B are given in (3.10),

$$\begin{aligned}
v_{bc2,rms} &= \left\{ \frac{2}{3} - (k_9 + k_7) \right\} v_{LL,rms} \\
v_{bc3,rms} &= v_{bc6,rms} = \left\{ \frac{2}{3} - (k_9 + k_7) \right\} v_{LL,rms} \\
v_{bc4,rms} &= \left\{ \frac{2}{3} - (k_{19} + k_9) \right\} v_{LL,rms} \\
v_{bc5,rms} &= \left\{ \frac{1}{3} - (k_{16} + k_9) \right\} v_{LL,rms} \\
v_{bc7,rms} &= \left\{ \frac{1}{3} - (k_{11} + k_9) \right\} v_{LL,rms} \\
v_{bc8,rms} &= v_{bc13,rms} = k_4 v_{LL,rms} \\
v_{bc9,rms} &= v_{bc12,rms} = k_6 v_{LL,rms} \\
v_{bc10,rms} &= v_{bc11,rms} = k_2 v_{LL,rms}
\end{aligned} \tag{3.10}$$

Similarly, the equations pertaining to winding voltages (rms) of transformer T_C are given in (3.11),

$$\begin{aligned}
v_{ca2,rms} &= \left\{ \frac{2}{3} - (k_{13} + k_{12}) \right\} v_{LL,rms} \\
v_{ca3,rms} &= \left\{ \frac{2}{3} - (k_{18} + k_{13}) \right\} v_{LL,rms} \\
v_{ca4,rms} &= \left\{ \frac{2}{3} - (k_{18} + k_{12}) \right\} v_{LL,rms} \\
v_{ca5,rms} &= \left\{ \frac{1}{3} - k_{15} \right\} v_{LL,rms}
\end{aligned} \tag{3.11}$$

A few winding voltages (rms) of transformer T_A, T_B and T_C are identical, and is expressed in (3.12),

$$\begin{aligned}
v_{ab1,rms} &= v_{bc1,rms} = v_{ca1,rms} = v_{ab6,rms} = \frac{1}{3} k_1 v_{LL,rms} \\
v_{ab7,rms} &= v_{ca8,rms} = k_8 v_{LL,rms} \\
v_{ab8,rms} &= v_{ca7,rms} = k_{10} v_{LL,rms}
\end{aligned} \tag{3.12}$$

Thus, the theoretical rms voltage across each winding are considered for calculating the VA rating of the proposed asymmetric MSAT.

B. Winding currents of the asymmetric autoconfigured transformer:

In Figure 3.2(a), applying KCL at node ‘A’ the input line current rms, $i_{A,rms}$ can be obtained as (3.13),

$$i_{A,rms} = i_{ab2,rms} - i_{ca6,rms} \tag{3.13}$$

To calculate the input rms line current, it is required to determine the rms winding currents of phase AB ($i_{ab2,rms}$) and CA ($i_{ca2,rms}$). The rms winding currents are calculated by considering the zero-net ampere turns of the asymmetric autoconfigured transformer, that is, $\sum AT = 0$. For phase AB, the zero-net ampere turns is expressed in (3.14),

$$\begin{aligned}
i_{ab2,rms} k_{15} + i_{ab3,rms} k_{17} + i_{ab4,rms} k_5 + i_{ab5,rms} k_3 + i_{ab6,rms} k_1 \\
+ i_{ab7,rms} k_8 + i_{ab8,rms} k_{10} = 0
\end{aligned} \tag{3.14}$$

and the associated winding currents are given in (3.15),

$$\begin{aligned}
i_{ab2,rms} &= i_{ab3,rms} + i_{bc11,rms}; \quad i_{ab3,rms} = i_{ab4,rms} + i_{bc12,rms} \\
i_{ab4,rms} &= i_{ab5,rms} + i_{bc13,rms}; \quad i_{ab5,rms} = i_{ab6,rms}
\end{aligned} \tag{3.15}$$

By substituting (3.15) in (3.14), the resultant winding current $i_{ab2,rms}$ is obtained as,

$$\begin{aligned}
i_{ab2,rms} &= \left[\frac{1}{(k_{17} + k_{15} + k_5 + k_3 + k_1)} \right] \\
&\quad \left\{ i_{bc11,rms} (k_{17} + k_5 + k_3 + k_1) + i_{bc12,rms} (k_5 + k_3 + k_1) \right\} \\
&\quad \left\{ + i_{bc13,rms} (k_3 + k_1) - i_{ab7,rms} k_8 - i_{ab8,rms} k_{10} \right\}
\end{aligned} \tag{3.16}$$

Similarly, for phase CA, the zero-net ampere turns is expressed in (3.17),

$$\begin{aligned} i_{ca6,rms}k_{15} + i_{ca5,rms}k_{14} + i_{ca4,rms}k_{13} + i_{ca3,rms}k_{12} + i_{ca2,rms}k_{18} \\ + i_{ca7,rms}k_{10} + i_{ca8,rms}k_8 = 0 \end{aligned} \quad (3.17)$$

and the associated winding currents are given in (3.18),

$$\begin{aligned} i_{ca6,rms} = i_{ca5,rms} - i_{bc10,rms}; \quad i_{ca5,rms} = i_{ca4,rms} = i_{ca3,rms} - i_{bc9,rms} \\ i_{ca3,rms} = i_{ca2,rms} - i_{bc8,rms} \end{aligned} \quad (3.18)$$

By substituting (3.18) in (3.17), the resultant winding current $i_{ca6,rms}$ is obtained as,

$$\begin{aligned} i_{ca6,rms} = [1/(k_{18} + k_{15} + k_{14} + k_{13} + k_{12})] \\ \left\{ \begin{aligned} & -i_{bc10,rms}(k_{18} + k_{14} + k_{13} + k_{12}) - i_{bc9,rms}(k_{18} + k_{12}) \\ & -i_{bc8,rms}k_{18} - i_{ca7,rms}k_{10} - i_{ca8,rms}k_8 \end{aligned} \right\} \end{aligned} \quad (3.19)$$

For calculating the rms phase currents for phase AB ($i_{ab2,rms}$) and CA ($i_{ca6,rms}$), the magnitude of rms winding currents through the windings of asymmetric MSAT are considered from the simulation.

By substituting (3.16) and (3.19) in (3.13), the input line current rms, $i_{A,rms}$ is obtained. Figure 3.3 shows the phase currents $i_{ab2,rms}$ & $i_{ca6,rms}$ and input line current $i_{A,rms}$. The waveforms in the Figure 3.3 are obtained by considering the autoconfigured transformer with negligible value of leakage reactance. Similarly, the rms value of other input line currents, $i_{B,rms}$ and $i_{C,rms}$ are calculated by the same procedure as discussed.

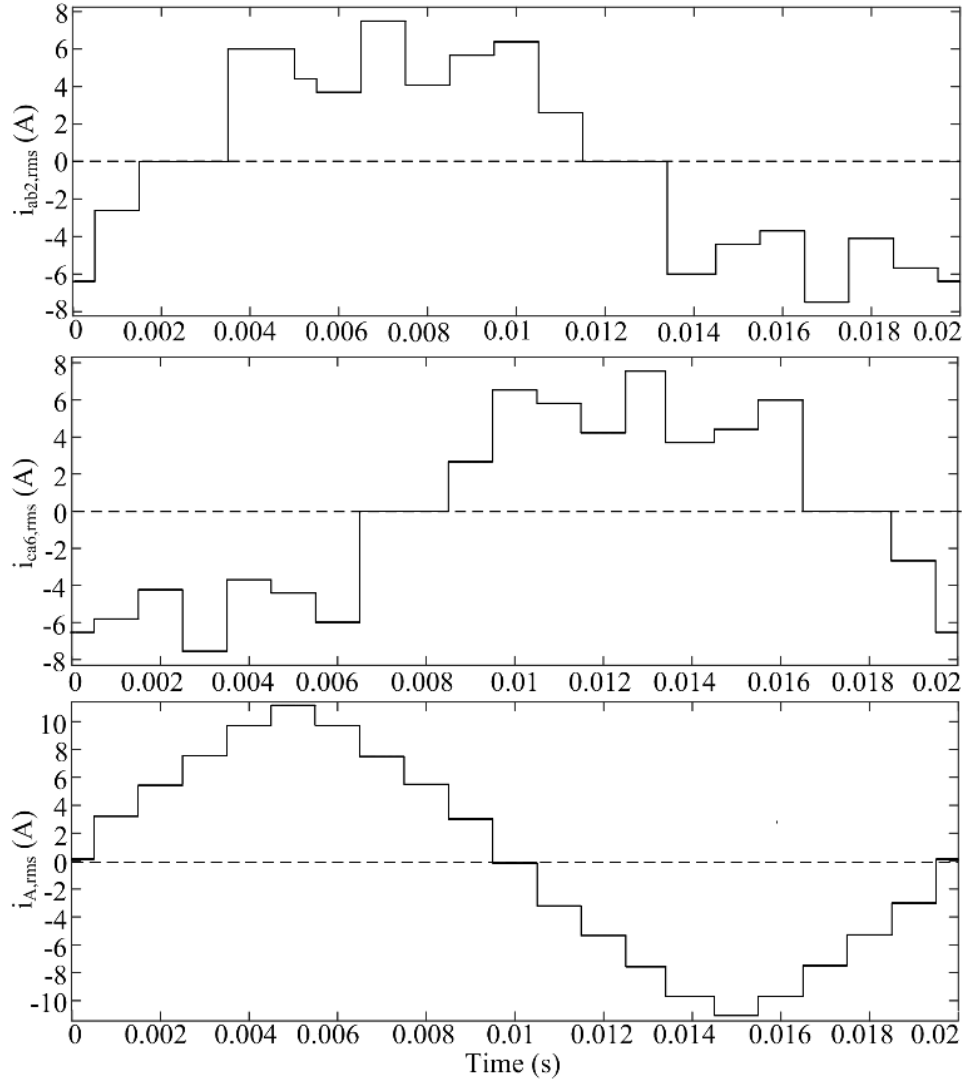


Figure 3.3: Phase currents $i_{ab2,rms}$ & $i_{ca2,rms}$ and input line current $i_{A,rms}$ of the asymmetric MSAT.

C. Magnetic rating of the proposed autoconfigured transformer:

Table 3.1 shows the corresponding winding voltages and currents of the three single-phase transformers, which are considered for calculating VA rating of the asymmetric MSAT for a load rating of 12 kW. The VA rating (Paice 1999) is calculated as, $S_{rating} = 0.5(\sum v_{rms} i_{rms}) = 4832.73 \text{ VA}$ and the magnetic rating as a fraction of load rating is

Table 3.1: Winding voltages and currents of the asymmetric MSAT and its VA rating

Transformer	rms values	w ₁	w ₂	w ₃	w ₄	w ₅	w ₆	w ₇	w ₈	w ₉	w ₁₀	w ₁₁	w ₁₂	w ₁₃	VA rating
T _A	$v_{rms}(V)$	45.58	1.590	150.7	80.53	41.40	45.58	109.8	49.38						1056.09
	$i_{rms}(A)$	12.52	0.007	1.116	4.668	10.25	12.52	0.003	0.007						
T _B	$v_{rms}(V)$	45.58	9.360	35.96	238.9	94.50	35.96	7.850	121.5	129.3	37.47	37.47	129.3	121.5	2679.55
	$i_{rms}(A)$	12.25	4.404	4.393	4.387	12.10	4.393	16.15	5.585	5.785	0.004	0.004	5.750	5.585	
T _C	$v_{rms}(V)$	45.58	183.1	80.82	9.570	138.1	1.590	49.38	109.8						1097.09
	$i_{rms}(A)$	12.52	2.699	8.490	10.01	2.509	0.006	0.006	0.003						

calculated as, $S_{rating} = \frac{4832.73}{12000} = 40.27\%$. Thus, the magnetic rating of the asymmetric autoconfigured transformer is found to be 40.27% of the load rating. This shows that the asymmetric autoconfigured transformer has lower magnetic rating and hence there is a significant reduction in overall size and cost of the system.

3.3.1.2 Performance parameters of the asymmetric MSAT configuration

In this sub-section, the performance parameters such as power quality indices and efficiency of the asymmetric autoconfigured transformer are evaluated.

A. Power quality indices:

From Figure 3.4, the average value of the PNDBC current can be derived as follows,

$$I_d = \frac{1}{2\pi} \left[\int_{\frac{3\pi}{10}}^{\frac{7\pi}{10}} I_d d(\omega t) + \int_{\frac{13\pi}{10}}^{\frac{17\pi}{10}} I_d d(\omega t) \right] = \frac{2I_d}{5} \quad (3.20)$$

and the rms value of the PNDBC current is given by (3.21),

$$I_{d,rms} = \left\{ \frac{1}{2\pi} \left[\int_{\frac{3\pi}{10}}^{\frac{7\pi}{10}} I_d^2 d(\omega t) + \int_{\frac{13\pi}{10}}^{\frac{17\pi}{10}} I_d^2 d(\omega t) \right] \right\}^{\frac{1}{2}} = \sqrt{\frac{2}{5}} I_d \quad (3.21)$$

The average value of the PNDBC output voltage can be written as (3.22),

$$V_d = \frac{5}{\pi} \int_{-\frac{\pi}{10}}^{\frac{\pi}{10}} \sqrt{3} v_m \cos \omega t d(\omega t) = 1.7036 v_m \quad (3.22)$$

where v_m is the peak phase voltage and the rms value of PNDBC output voltage is given in (3.23),

$$V_{d,rms} = \left[\frac{5}{\pi} \int_{-\frac{\pi}{10}}^{\frac{\pi}{10}} 3 v_m^2 \cos^2(\omega t) d(\omega t) \right]^{\frac{1}{2}} = 1.704 v_m \quad (3.23)$$

The RF, which is measure of the ripple content, is found from the equation (3.24),

$$RF = \left[\left(\frac{V_{d,rms}}{V_d} \right)^2 - 1 \right]^{\frac{1}{2}} = 0.0153 \quad (3.24)$$

So, the amount of AC component present in the DC output of PNDBC is only 1.53 %.

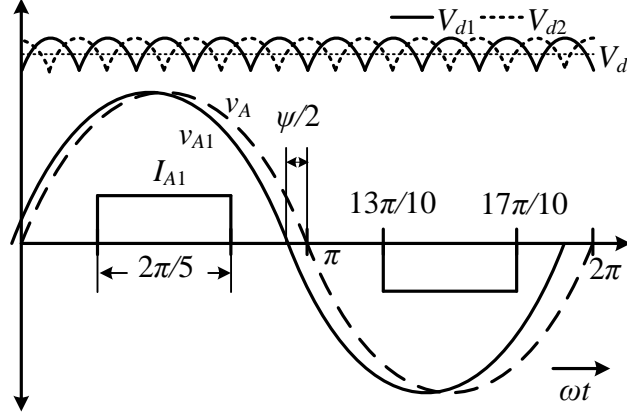


Figure 3.4: Theoretical waveforms of voltage and current of PNDBC A with respect to supply voltage, and DC-link voltage of PNDBC A and PNDBC B for the non-isolated asymmetric MSAT.

The input source current THD is computed by using the relation between the rms and fundamental frequency component of the input line current. From the waveform shown in Figure 3.3, the rms value of input line current is calculated using (3.25),

$$I_{A,rms}^2 = \frac{2}{\pi} \int_0^{\frac{\pi}{2}} i_A^2(t) d(\omega t) \quad (3.25)$$

The maximum and rms value of the fundamental component of the input line current are calculated by (3.26),

$$I_{1A,max} = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} i_A \sin(\omega t) d(\omega t)$$

and its rms value is, $I_{1A,rms} = \frac{I_{1A,max}}{\sqrt{2}}$ (3.26)

The theoretical value of input line current THD is obtained as,

$$\% i_{A,THD} = \frac{\sqrt{I_{A,rms}^2 - I_{1A,rms}^2}}{I_{1A,rms}} \times 100 = 7.39\% \quad (3.27)$$

and its corresponding DF is,

$$DF = \frac{1}{\sqrt{1 + i_{A,THD}^2}} = 0.9972 \quad (3.28)$$

It is found that the theoretical value of the % $i_{A,THD}$ and DF for the asymmetric autoconfigured transformer is 7.39% and 0.9972 respectively.

B. Efficiency of the overall system:

The efficiency of the overall system is determined by accounting the individual losses in the system. The total loss of the system comprises of,

$$P_T = P_{MSAT} + P_{PNDBC} \quad (3.29)$$

a) Losses in MSAT (P_{MSAT}): There are mainly two kinds of losses in an autoconfigured transformer, namely core loss and ohmic loss. Core loss consists of hysteresis loss (P_h) and eddy current loss (P_e). Hysteresis and eddy current loss are given by (3.30),

$$\begin{aligned} P_h &= K_h f B_m^{1.6} \\ P_e &= K_e f^2 B_m^2 \end{aligned} \quad (3.30)$$

where K_h is a proportionality constant which depends on the volume and quality of the core material used, K_e is a proportionality constant which depends on the volume and resistivity of the core material used, B_m is the maximum flux density and f is the frequency of the alternating flux. In a conventional model, the values of the coefficients K_h and K_e are assumed to be constants, which are invariable with frequency f and magnetic flux density B_m . From the data sheet, the values of K_h and K_e are found to be 0.0118 and 0.03 respectively. Thus, the estimated core loss is found to be 48.41W. With $R = 0.06 \Omega$ and winding currents being chosen from Table 3.1, the ohmic loss (I^2R) computed is 93.25 W. Thus, the total losses in the autoconfigured transformer is,

$$P_{MSAT} = 48.41 + 93.25 = 141.66 \text{ W} \quad (3.31)$$

b) Losses in PNDBC (P_{PNDBC}): The power loss components (neglecting the turn-OFF losses) of the PNDBC's are calculated by considering voltage drop of diode $V_f = 0.7 \text{ V}$, internal resistance of the diode $R_d = 1 \text{ m}\Omega$, and $I_d = 10 \text{ A}$ and is given by (3.32),

$$P_{PNDBC} = \frac{1}{\pi} \int_0^{\pi} (V_f I_d + I_d^2 R_d) dt = V_f I_d + I_d^2 R_d = 7.1 \text{ W} \quad (3.32)$$

So, the total power loss for the two in number 5-phase PNDBC is $2 \times 10 \times 7.1 \text{ W} = 142 \text{ W}$.

Therefore, the total power losses (P_T) associated with the system is 283.66 W and thus, the efficiency of the overall system at full load is found to be 97.69%.

3.3.2 Results and discussion

The asymmetric non-isolated MSAT feeding a DC load of 12 kW is simulated by using MATLAB/Simulink environment and the corresponding simulation parameters are listed in Appendix A. Figure 3.5(a) and (b) shows the input source voltage/current of the asymmetric MSAT under full load (FL) and light load (LL) conditions respectively. Figure 3.6(a) and (b) shows the input voltage/current of the PNDBC A and PNDBC B respectively. Figure 3.7(a) and (b) shows the harmonic spectrum of input source voltage and current respectively under FL. It is observed from Figure 3.7(a) and (b) that, the % input voltage and current THD are 1.84% and 3.04% respectively with unity PF. Similarly, Figure 3.8(a) and (b) shows the harmonic spectrum of input source voltage and current respectively under LL conditions with % input voltage and current THD are 2.36% and 4.2% respectively. From the current harmonic spectrum of Figures 3.7(b) and 3.8(b), it is inferred that the asymmetric MSAT eliminates the harmonic order less than 19. Figure 3.9(a) and (b) shows the output DC-link voltage/current for the PNDBC A and PNDBC B respectively. Figure 3.10(a) shows the voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to the source voltage (v_A). From Figure 3.10(a), the phase shift between source voltage and PNDBC voltages is observed to be $\pm 9^\circ$. Similarly, Figure 3.10(b) shows the current of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to source current (i_A). It can also be inferred from the Figure 3.10(b) that, the phase shift of 18° is confirmed between the currents of PNDBC A and PNDBC B.

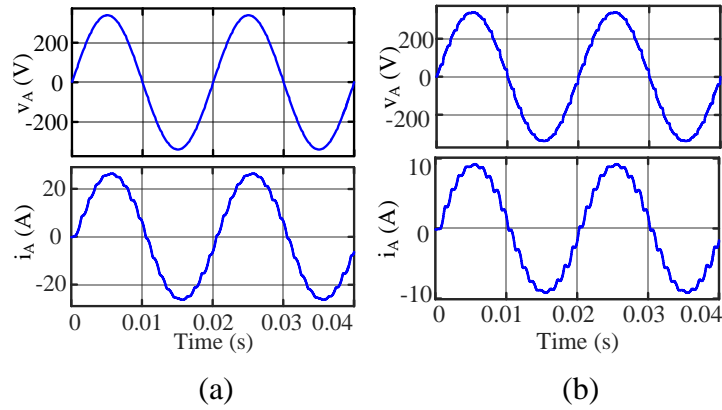


Figure 3.5: Simulated results of input voltage and current for the asymmetric MSAT at (a) FL condition. (b) LL condition.

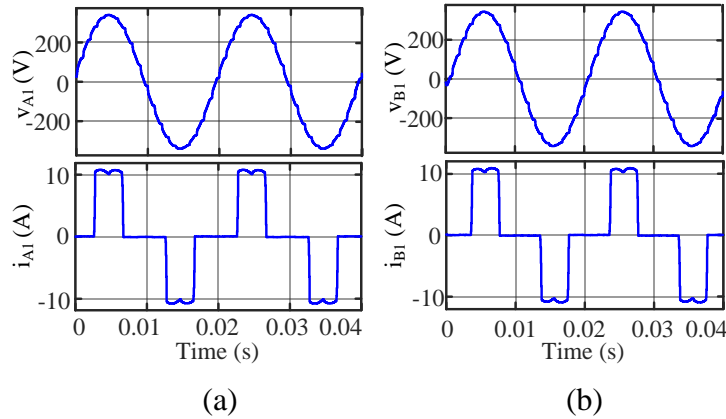


Figure 3.6: Simulated results of the asymmetric MSAT (a) Input voltage and current of PNDBC A. (b) Input voltage and current of PNDBC B.

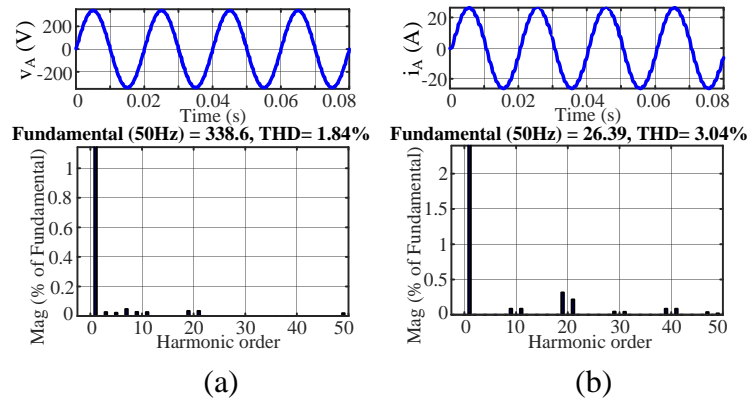


Figure 3.7: Simulated results of the asymmetric MSAT at FL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.

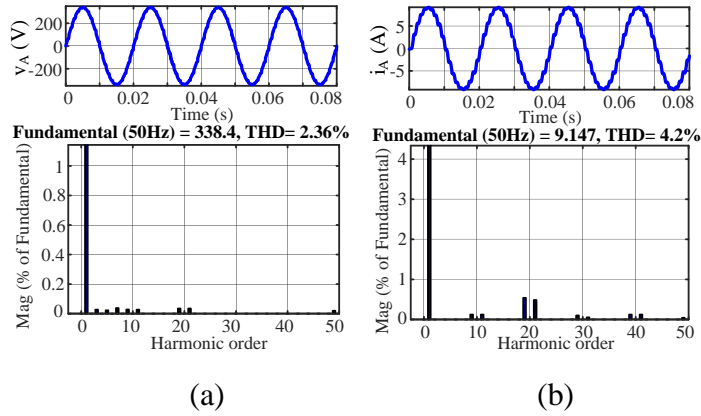


Figure 3.8: Simulated results of the asymmetric MSAT at LL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.

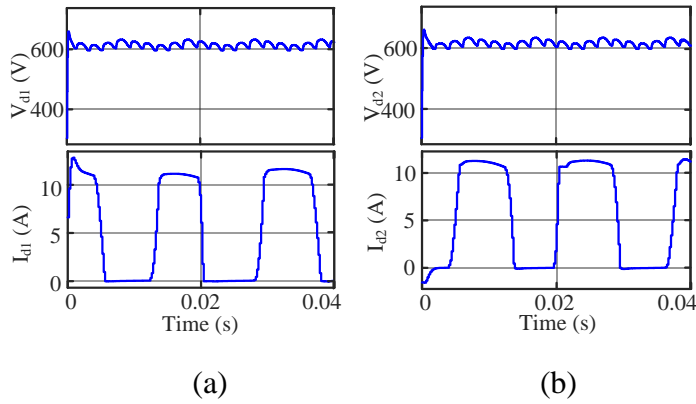


Figure 3.9: Simulated results of the asymmetric MSAT (a) Output voltage and current of PNDBC A. (b) Output voltage and current of PNDBC B.

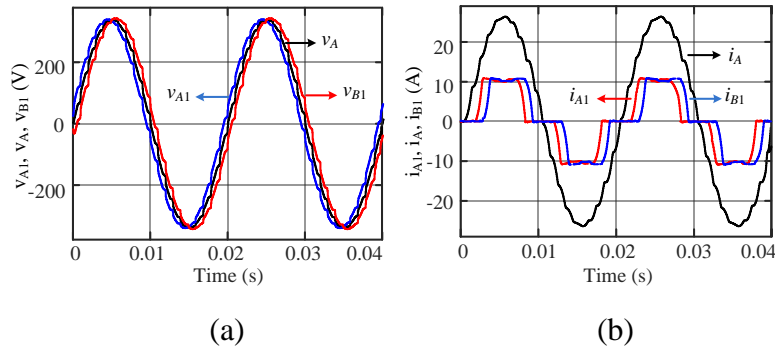


Figure 3.10: Simulated results of the asymmetric MSAT (a) Voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to source voltage (v_A). (b) Currents of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to input current (i_A).

To validate the aforementioned theoretical analysis and numerical simulation, the experimental set up was built in the laboratory as shown in Figure 3.11. Extensive tests have been conducted on the developed prototype fed from a reduced source voltage of magnitude 110 V (rms) and the results are shown in the Figures 3.12 to 3.17. Figure 3.12(a) and (b) shows the input source voltage/current of the asymmetric MSAT under FL and LL conditions respectively. Figure 3.13(a) and (b) shows the input voltage/current of the PNDBC A and PNDBC B respectively. Figure 3.14 and 3.15 shows the harmonic spectrum of input source voltage/current under FL and LL conditions respectively. It is observed from Figure 3.14 that, the % input voltage and current THD are 2.8% and 3.7% respectively with unity PF. Similarly, it can also be observed from Figure 3.15 that, the % input voltage and current THD are 2.1% and 5.6% with unity PF respectively. Figure 3.16(a) and (b) shows the output DC-link voltage/current for the PNDBC A and PNDBC B respectively. Figure 3.17(a) shows the voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to the source voltage (v_A). Similarly, Figure 3.17(b) shows the current of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to source current (i_A). From the above results a clear agreement between the simulation and experimental results confirms the correctness of the developed design procedure and simulation model of the asymmetric MSAT.

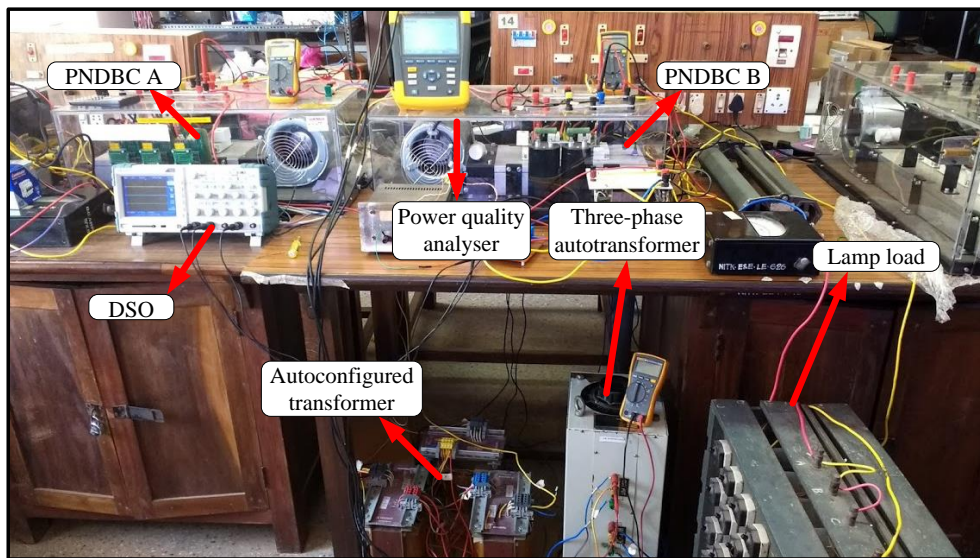
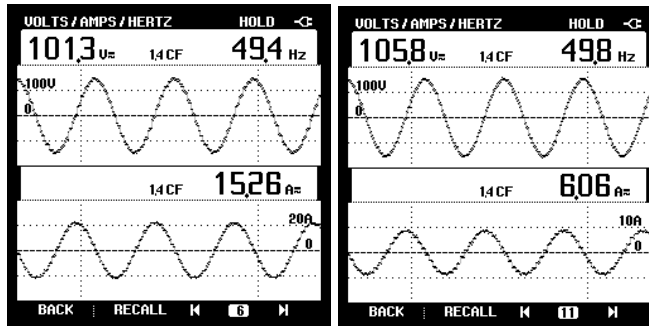


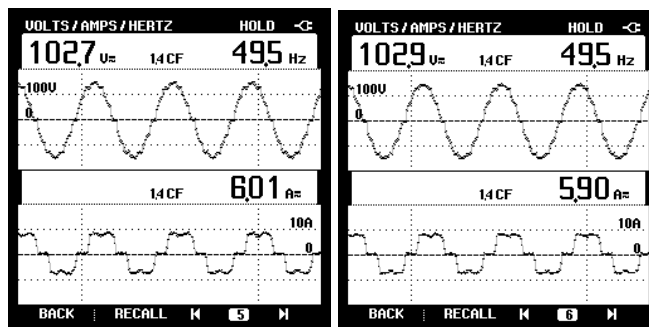
Figure 3.11: Annotated photograph of the laboratory prototype.



(a)

(b)

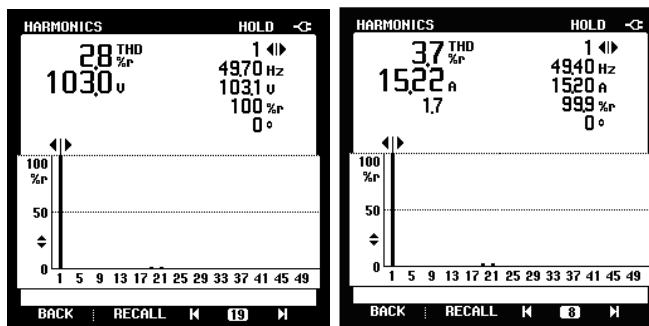
Figure 3.12: Experimental results of input voltage and current for the asymmetric MSAT at (a) FL condition. (b) LL condition.



(a)

(b)

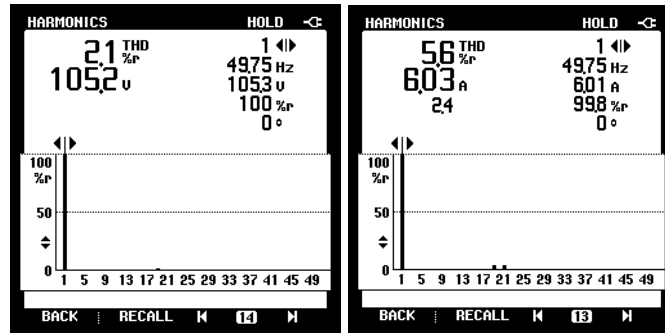
Figure 3.13: Experimental results of the asymmetric MSAT (a) Input voltage and current of PNDBC A. (b) Input voltage and current of PNDBC B.



(a)

(b)

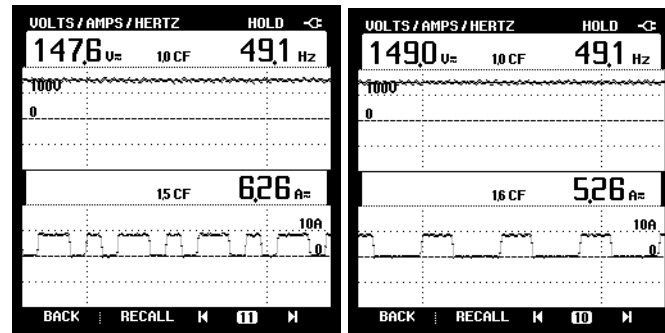
Figure 3.14: Experimental results of the asymmetric MSAT at FL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.



(a)

(b)

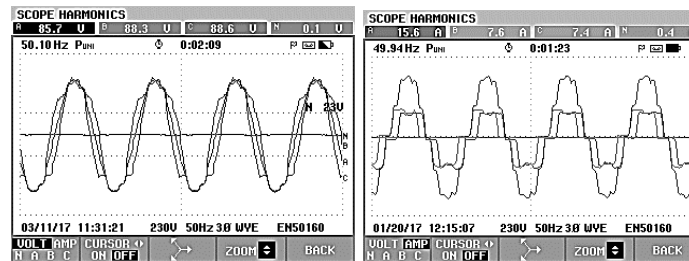
Figure 3.15: Experimental results of the asymmetric MSAT at LL (a) Input voltage harmonic spectrum. (b) Input current harmonic spectrum.



(a)

(b)

Figure 3.16: Experimental results of the asymmetric MSAT (a) Output voltage and current of PNDBC A. (b) Output voltage and current of PNDBC B.



(a)

(b)

Figure 3.17: Experimental results of the asymmetric MSAT (a) Voltages of PNDBC A (v_{A1}) and PNDBC B (v_{B1}) with respect to source voltage (v_A). (b) Currents of PNDBC A (i_{A1}) and PNDBC B (i_{B1}) with respect to input current (i_A).

The notable contribution of this configuration is the design of an asymmetrical MSAT for converting three-phase input AC source voltage to prime numbered phase-staggered voltages that are not multiples of factor three. The asymmetric MSAT is a combination of multi-pulse/multi-phase and phase-staggering approach with inherent PF correction performing comparable to a higher pulse numbered AC-DC converter. Also, the autoconfigured transformer eliminates the ZSBT and thereby further reduces the magnetic rating of the overall system.

3.4 A 20-PULSE AMPC CONFIGURATION SYNTHESIS

With the underlying principle of the asymmetric 20-pulse MSAT configuration, an opportunity for a further reduction in the magnetic rating is explored in the present section. Figure 3.18 shows the schematic diagram of the 20-pulse non-isolated AMPC. The system comprises of a utility interfaced non-isolated AMPC transformer and multi-phase PND BCs feeding the load. The winding and phasor diagram of non-isolated AMPC is shown in Figure 3.19(a) and (b). The non-isolated AMPC transformer has 23 windings catering to delta connected transformer as shown in Figure 3.19(a). The uncomplicated construction of prime numbered output phases leads to a reduced harmonic content in the input side with lesser VA rating of transformer. The construction of prime numbered multi-phases is same as that of MSAT configuration discussed section 3.3.

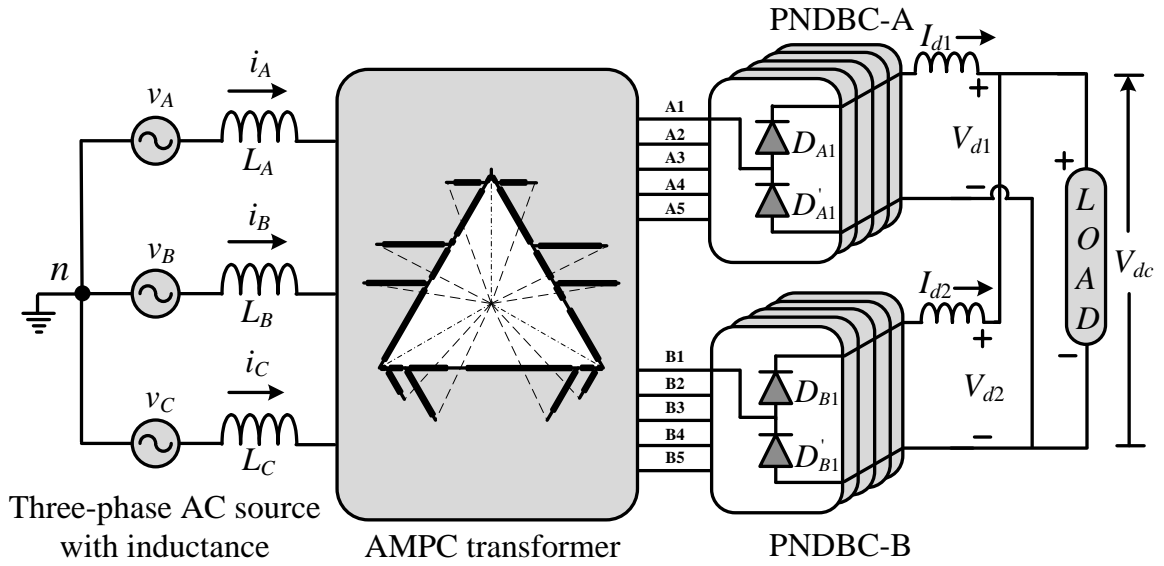


Figure 3.18: Schematic diagram of the 20-pulse non-isolated AMPC.

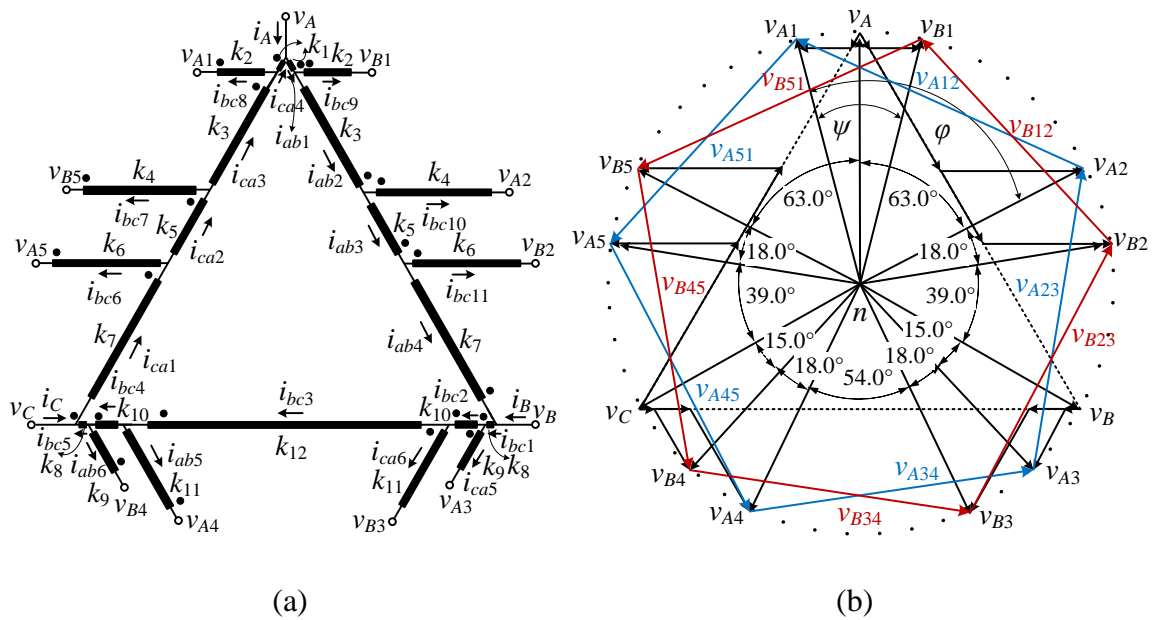


Figure 3.19: Schematic diagram of the non-isolated AMPC representing (a) Winding diagram and (b) Resultant phasor diagrams of the phase-staggered angle positions of various phasors.

3.4.1 Design and analysis of non-isolated AMPC configuration

The design and analysis of non-isolated AMPC configuration is discussed in this section. Figure 3.19(a) and (b) depicts the corresponding windings and the resultant phasor representation of the autoconfigured transformer respectively.

3.4.1.1 Design of non-isolated autoconfigured transformer

Constants k_1 - k_{12} decides the number of turns. The voltage across the various windings is determined by the product of the number of turns and its corresponding phase voltage. The phase angle between phase staggered voltages and input phase voltages are given in (3.33),

$$\begin{aligned} v_A &= v_R \sin \omega t; v_B = v_R \sin(\omega t - 120^\circ); v_C = v_R \sin(\omega t + 120^\circ) \\ v_{A1} &= v_R \angle 9^\circ; v_{A2} = v_R \angle -63^\circ; v_{A3} = v_R \angle -135^\circ; v_{A4} = v_R \angle 153^\circ; v_{A5} = v_R \angle 81^\circ \\ v_{B1} &= v_R \angle -9^\circ; v_{B2} = v_R \angle -81^\circ; v_{B3} = v_R \angle -153^\circ; v_{B4} = v_R \angle 135^\circ; v_{B5} = v_R \angle 63^\circ \end{aligned} \quad (3.33)$$

v_R – amplitude of phase voltage.

The phase staggered voltage equations for PNDBC A and B are as follows,

$$\begin{aligned} v_{A1} &= v_A - k_1 v_{CA} + k_2 v_{BC}; & v_{B1} &= v_A + k_1 v_{AB} - k_2 v_{BC} \\ v_{A2} &= v_A + (k_1 + k_3) v_{AB} - k_4 v_{BC}; & v_{B2} &= v_A + (k_1 + k_3 + k_5) v_{AB} - k_6 v_{BC} \\ v_{A3} &= v_B + k_8 v_{BC} - k_9 v_{CA}; & v_{B3} &= v_B + (k_9 + k_{10}) v_{BC} - k_{11} v_{CA} \\ v_{A4} &= v_C - (k_8 + k_{10}) v_{BC} + k_{11} v_{AB}; & v_{B4} &= v_C - k_8 v_{BC} + k_9 v_{AB} \\ v_{A5} &= v_C + k_7 v_{CA} + k_6 v_{BC}; & v_{B5} &= v_C + (k_5 + k_7) v_{CA} + k_4 v_{BC} \end{aligned} \quad (3.34)$$

Thus, the value of the constants obtained from the above equations are: $k_1=0.0082$, $k_2=0.0862$, $k_3=0.3557$, $k_4=0.3324$, $k_5=0.1983$, $k_6=0.2890$, $k_7=0.4376$, $k_8=0.0227$, $k_9=0.1380$, $k_{10}=0.0848$, $k_{11}=0.2606$, $k_{12}=0.7849$. Considering the volt per turn ratio as one, the voltage value across each winding is derived.

A. Winding voltages of the non-isolated autoconfigured transformer:

The rms voltage across each winding are calculated by considering the input line-to-line rms voltage and their corresponding winding constants. The equations pertaining to the rms value of the winding voltages are given in (3.35),

$$\begin{aligned}
v_{ab1,rms} &= v_{ca4,rms} = k_1 v_{LL,rms}; v_{ab2,rms} = v_{ca3,rms} = \{1 - (k_1 + k_5 + k_7)\} v_{LL,rms} \\
v_{ab3,rms} &= v_{ca2,rms} = \{1 - (k_1 + k_3 + k_7)\} v_{LL,rms}; v_{ab5,rms} = v_{ca6,rms} = k_{11} v_{LL,rms} \\
v_{ab4,rms} &= v_{ca1,rms} = \{1 - (k_1 + k_3 + k_5)\} v_{LL,rms}; v_{ab6,rms} = v_{ca5,rms} = k_9 v_{LL,rms} \\
v_{bc1,rms} &= v_{bc5,rms} = 2k_8 v_{LL,rms}; v_{bc2,rms} = v_{bc4,rms} = \{1 - (2k_8 + k_{12})\} v_{LL,rms} \\
v_{bc3,rms} &= \{1 - (2k_8 + 2k_{10})\} v_{LL,rms}; v_{bc6,rms} = v_{bc11,rms} = k_6 v_{LL,rms} \\
v_{bc7,rms} &= v_{bc10,rms} = k_4 v_{LL,rms}; v_{bc8,rms} = v_{bc9,rms} = k_2 v_{LL,rms}
\end{aligned} \tag{3.35}$$

The VA rating of the non-isolated AMPC is computed with the aid of the above derived theoretical rms voltages.

B. Winding currents of the non-isolated autoconfigured transformer:

Figure 3.20 shows the schematic diagram of non-isolated AMPC under study. The PNDBC A and PNDBC B are assumed to deliver an output current of magnitude $I_d/2$. Applying KCL at node A the input line current rms, $i_{A,rms}$ can be obtained as (3.36),

$$\begin{aligned}
i_{A,rms} &= i_{ab1,rms} - i_{ca4,rms}; i_{B,rms} = i_{bc1,rms} - i_{ab4,rms} \\
i_{C,rms} &= i_{ca1,rms} - i_{bc5,rms}
\end{aligned} \tag{3.36}$$

The rms value of the input line current, $i_{A,rms}$ is obtained using the rms value of the winding currents of phase AB ($i_{ab1,rms}$) and CA ($i_{ca2,rms}$). Using the zero-net ampere turns relation ($\sum AT=0$), the rms value of winding currents are deduced. Applying this principle to phase AB leads to (3.37),

$$\begin{aligned}
i_{ab1,rms} k_1 + i_{ab2,rms} k_3 + i_{ab3,rms} k_5 + i_{ab4,rms} k_7 \\
+ i_{ab5,rms} k_{11} + i_{ab6,rms} k_9 = 0
\end{aligned} \tag{3.37}$$

and the associated winding currents are given by (3.38),

$$\begin{aligned}
i_{ab4,rms} &= i_{ab3,rms} - i_{bc11,rms} \\
i_{ab3,rms} &= i_{ab2,rms} - i_{bc10,rms} \\
i_{ab2,rms} &= i_{ab1,rms} - i_{bc9,rms}
\end{aligned} \tag{3.38}$$

Substituting (3.38) in (3.37), the resultant winding current $i_{ab1,rms}$ is obtained as (3.39),

$$i_{ab1,rms} = (1/(k_1 + k_3 + k_5 + k_7)) \left\{ \begin{aligned} &i_{bc9,rms} (k_3 + k_5 + k_7) + i_{bc10,rms} (k_5 + k_7) \\ &+ i_{bc11,rms} k_7 - i_{ab5,rms} k_{11} - i_{ab6,rms} k_9 \end{aligned} \right\} \tag{3.39}$$

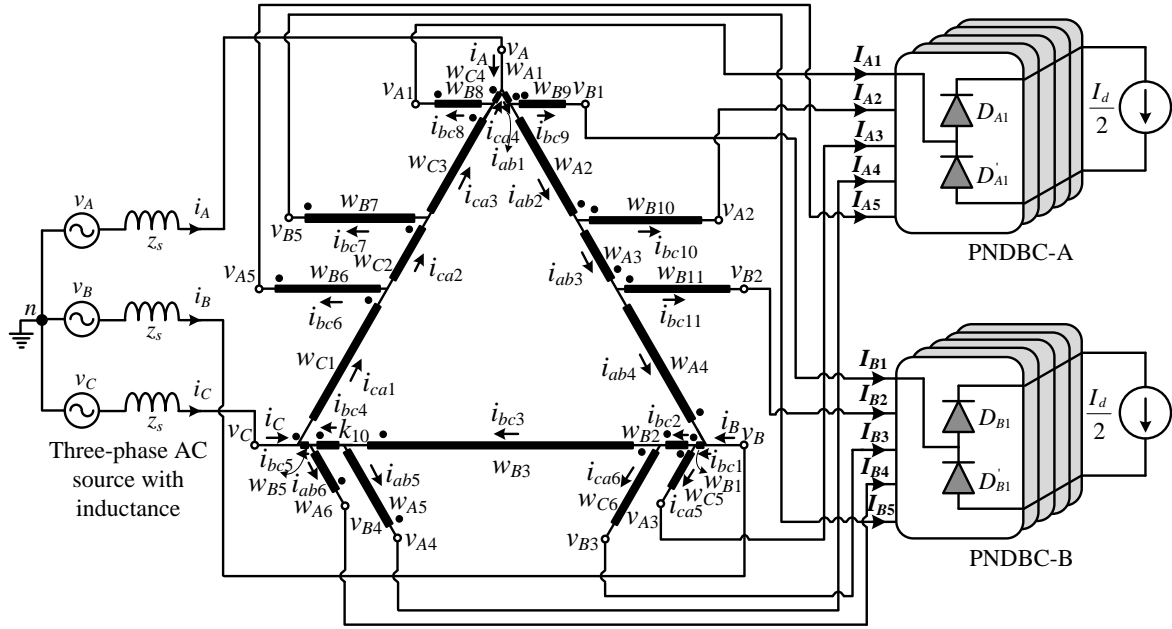


Figure 3.20: Winding current analysis of the non-isolated AMPC supplying constant DC load current.

Similarly, for phase CA, the zero-net ampere turns is given by (3.40),

$$i_{ca4,rms}k_1 + i_{ca3,rms}k_3 + i_{ca2,rms}k_5 + i_{ca1,rms}k_7 + i_{ca5,rms}k_9 + i_{ca6,rms}k_{11} = 0 \quad (3.40)$$

and the associated winding currents are given by (3.41),

$$\begin{aligned} i_{ca1,rms} &= i_{ca2,rms} + i_{bc6,rms} \\ i_{ca2,rms} &= i_{ca3,rms} + i_{bc7,rms} \\ i_{ca3,rms} &= i_{ca4,rms} + i_{bc8,rms} \end{aligned} \quad (3.41)$$

Substituting (3.41) in (3.40), the resultant winding current $i_{ca4,rms}$ is obtained as (3.42),

$$i_{ca4,rms} = (1/(k_1 + k_3 + k_5 + k_7)) \left\{ \begin{aligned} & -i_{bc8,rms}(k_3 + k_5 + k_7) - i_{bc7,rms}(k_5 + k_7) \\ & -i_{bc6,rms}k_7 - i_{ca5,rms}k_9 - i_{ca6,rms}k_{11} \end{aligned} \right\} \quad (3.42)$$

The additional rms values of the winding currents required for computation of (3.39) and (3.42) are obtained through the simulation. The rms value of the phase A current is obtained by substituting (3.39) and (3.42) in (3.36). Figure 3.21 shows the phase currents ($i_{bc9,rms}$, $i_{bc10,rms}$, $i_{bc11,rms}$, $i_{ab5,rms}$, $i_{ab6,rms}$, $i_{bc8,rms}$, $i_{bc7,rms}$, $i_{bc6,rms}$, $i_{ca5,rms}$, $i_{ca6,rms}$), winding currents ($i_{ab1,rms}$, $i_{ca4,rms}$) and input line current ($i_{A,rms}$). The required PNDDBC currents for

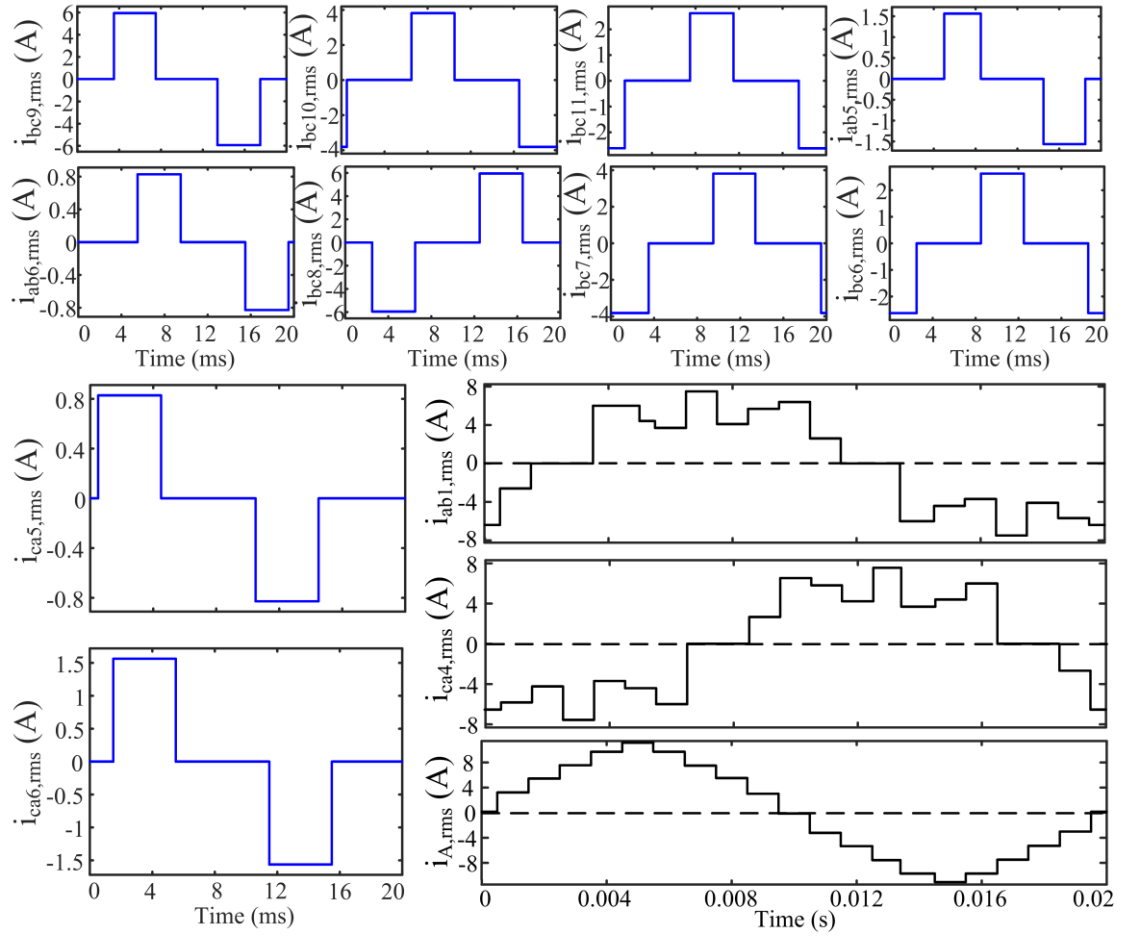


Figure 3.21: PNDBC phase currents ($i_{bc9,rms}$, $i_{bc10,rms}$, $i_{bc11,rms}$, $i_{ab5,rms}$, $i_{ab6,rms}$, $i_{bc8,rms}$, $i_{bc7,rms}$, $i_{bc6,rms}$, $i_{ca5,rms}$, $i_{ca6,rms}$), winding currents ($i_{ab1,rms}$ & $i_{ca4,rms}$) and input line current ($i_{A,rms}$) of the non-isolated AMPC.

the computation of phase currents $i_{ab1,rms}$ & $i_{ca4,rms}$ and input line current $i_{A,rms}$ obtained by considering the negligible value of autoconfigured transformer's leakage reactance is depicted in Figure 3.21. However, the same procedure can be followed and repeated for deriving other phase currents.

C. Magnetic rating of the non-isolated autoconfigured transformer:

The non-isolated AMPC transformer is realized using three single-phase transformers namely T_A , T_B , and T_C . The corresponding winding voltages and currents of T_A , T_B , and

Table 3.2: Winding voltages and currents of the non-isolated AMPC transformer and its VA rating

Transformer	rms values	w ₁	w ₂	w ₃	w ₄	w ₅	w ₆	w ₇	w ₈	w ₉	w ₁₀	w ₁₁	VA rating
T _A	v_{rms} (V)	3.403	147.7	82.58	181.9	108.1	57.27						1737.80
	i_{rms} (A)	6.14	4.092	1.440	2.430	3.332	3.342						
T _B	v_{rms} (V)	18.84	70.42	325.8	70.42	18.84	119.9	137.9	35.77	35.77	137.9	119.9	3826.15
	i_{rms} (A)	7.884	4.982	3.120	4.918	7.810	3.256	3.172	1.260	3.328	3.130	3.280	
T _C	v_{rms} (V)	181.9	82.58	147.7	3.403	57.27	108.1						1665.95
	i_{rms} (A)	2.256	1.260	3.952	6.024	3.328	3.300						

T_C are listed in Table 3.2. Following assumptions were made while evaluating the VA rating of the proposed non-isolated AMPC:

1. Input AC voltages are balanced.
2. Current shared among the PNDBC's is equal and ripple free.

The VA rating is calculated using $S_{rating} = 0.5(\sum v_{rms} i_{rms}) = 3614.95$ VA suggested in (Paice 1999) and the magnetic rating as a fraction of load rating (12 kW) is obtained as, $S_{rating} = \frac{3614.95}{12000} = 30.12\%$. Thus, the magnetic rating of the non-isolated AMPC transformer is found to be 30.12% of the nominal load, which proves that the non-isolated AMPC transformer has a lower magnetic rating and hence there is a significant reduction in overall size and cost of the system.

3.4.1.2 Performance parameters of the non-isolated autoconfigured transformer

The performance parameters namely power quality indices and efficiency are discussed in the following section.

A. Power quality indices:

The power quality performance of the AMPC autoconfigured transformer have been same as that of MSAT configuration discussed in section 3.3.1.2 A.

B. Efficiency of the overall system:

The efficiency of the overall system is evaluated by considering the individual loss components of the system. Overall losses in the system corresponding to losses in the AMPC and PNDBC's, is given by (3.43),

$$P_T = P_{AMPC} + P_{PNDBC} \quad (3.43)$$

a) *Losses in AMPC (P_{AMPC}):* There are mainly two kinds of losses in an autoconfigured transformer, namely core loss and ohmic loss. Core loss consists of hysteresis loss (P_h) and eddy current loss (P_e) and it is given by (3.30). Thus, the core loss estimated is found to be 48.41 W. With $R = 0.06 \Omega$ and winding currents being chosen from Table 3.2, the ohmic

loss (I^2R) computed is 24.05 W. Thus, the total loss in the autoconfigured transformer is, $P_{AMPC} = 48.41 + 24.05 = 72.46$ W.

b) Losses in PNDBC (P_{PNDBC}): The power loss components of the PNDBC's are calculated (Alishah et al. 2017; Shalchi Alishah et al. 2015) by considering the following: voltage drop of diode ($V_f = 1$ V), internal resistance of the diode ($R_d = 3.5$ m Ω), and PNDBC current ($I_d = 10$ A) is given by (3.44),

$$P_{PNDBC} = \frac{1}{\pi} \int_0^{\pi} (V_f I_d + I_d^2 R_d) d(\omega t) = V_f I_d + I_d^2 R_d = 10.3 \text{ W} \quad (3.44)$$

Hence, the total power loss of the two 5-phase PNDBCs is $2 \times 10 \times 10.3 \text{ W} = 206 \text{ W}$. Therefore, the total power losses associated with the proposed system is $P_T = 278.46$ W, and overall efficiency so obtained at full load is % Efficiency = $\frac{12000}{12278.46} = 97.73$ %.

3.4.2 Results and discussion

The 20-pulse non-isolated AMPC fed DC load rated for 12 kW (600 V, 20 A) is simulated using MATLAB/Simulink. The simulation parameters are listed in Appendix A. It can be inferred from Figure 3.22 that the conduction period of a diode is 72° which provides a smooth current transition from one pair to other, the DC-link voltage of the non-isolated AMPC consists of 20-pulses and input phase current almost sinusoidal which confirms the unity PF operation.

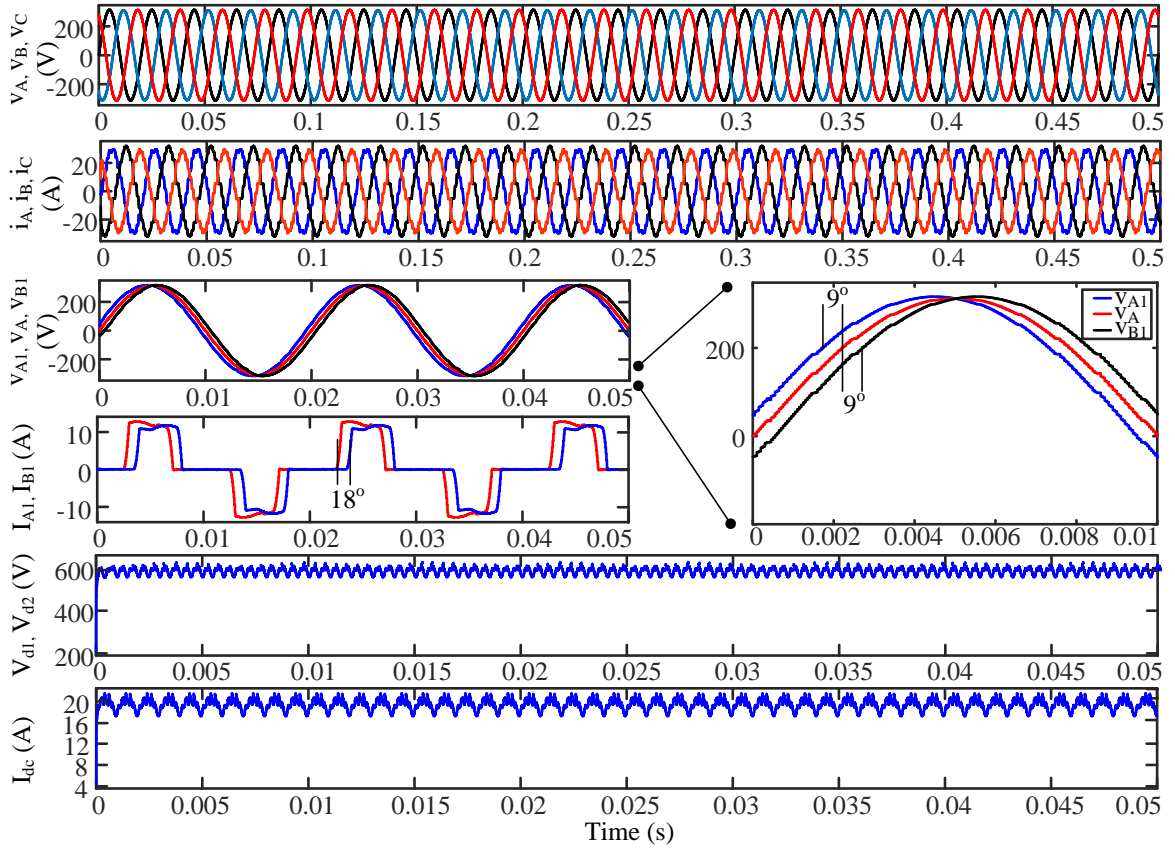
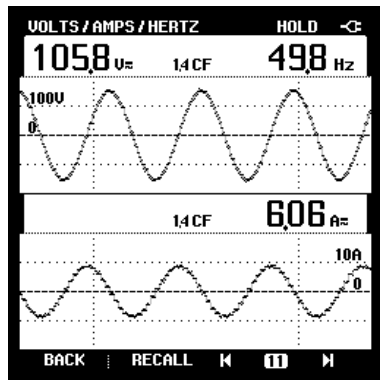


Figure 3.22: Simulated waveforms of three-phase input voltage (v_A, v_B, v_C), input current (i_A, i_B, i_C), phase shifted voltage (v_{A1}, v_A, v_{B1}), PNDBC input currents (I_{A1}, I_{B1}), DC-link voltage (V_{dc}) and DC-link current (I_{dc}) of the non-isolated AMPC.

To verify the simulation results and demonstrate the practicability of the non-isolated AMPC, a laboratory scale prototype of the proposed 20-pulse AMPC is built and the results are shown in Figure 3.23 for LL and FL conditions respectively. A clear agreement between the simulation and experimental results confirms the effectiveness of the non-isolated AMPC configuration for various industrial applications. It is relevant to mention here that the input current THD for non-isolated AMPC is 3.7 % under FL without including additional passive filters at their front-end as shown in Figure 3.23(d). One can further visualize the nonexistence of lower order harmonics and the presence of dominant harmonics around the side band of frequency 1 kHz. The phase shift of $\pm 18^\circ$ is witnessed

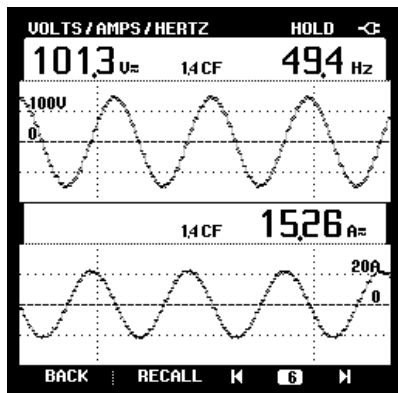
among the input phase of PNDBC A and corresponding input phase of PNDBC B and a minimal DC-link voltage ripple in addition as shown in Figure 3.23(e). Also, a phase difference between the input voltages of PNDBC A and PNDBC B with respect to the supply voltage is observed to be $\pm 90^\circ$ as shown in Figure 3.23(f). The simulated and test results of input phase current ($i_{A,rms}$) formation from the winding voltages/currents of the non-isolated AMPC transformer as shown in Figure 3.24. The test results show the similar trends as that of simulation results, and thus validating the developed design procedure and simulated model of the non-isolated AMPC.



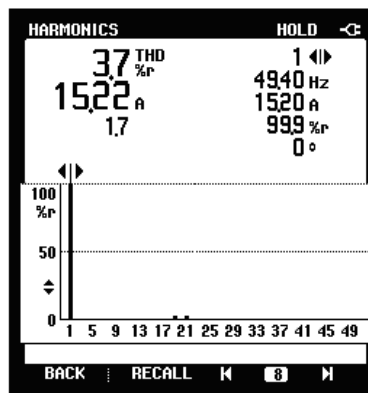
(a)



(b)



(c)



(d)

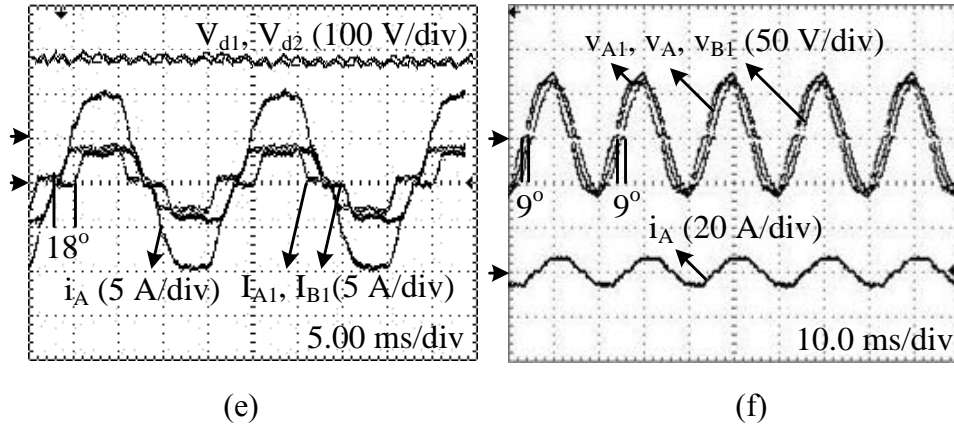
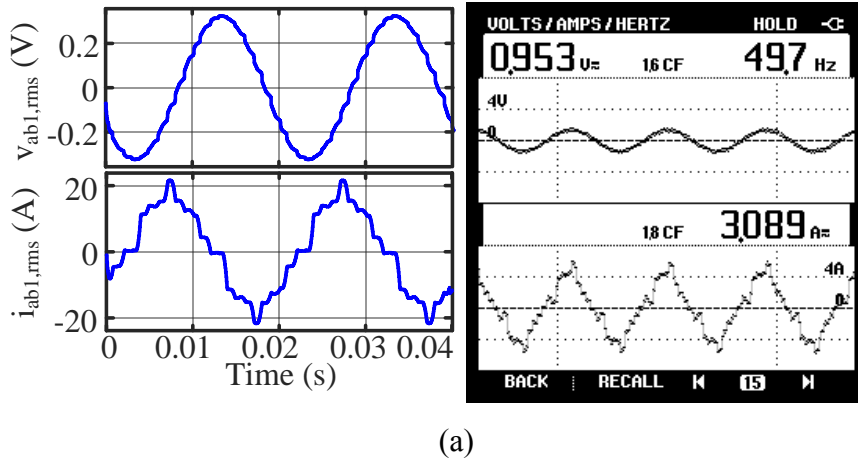
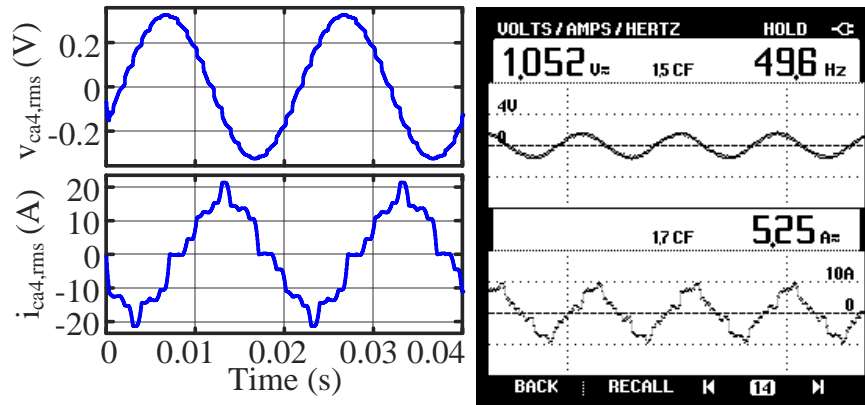
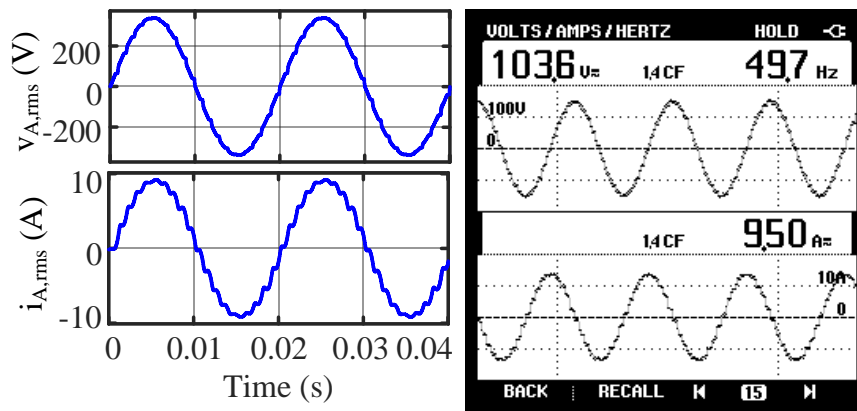


Figure 3.23: Experimental results of (a) Input source voltage (v_A)/current (i_A) under LL condition, (b) Current THD under LL condition, (c) Input source voltage (v_A)/current (i_A) under FL condition, (d) Current THD under FL condition, (e) Input phase current (i_A), PNDBC input currents (I_{A1} , I_{B1}) with output DC-link voltages (V_{d1} , V_{d2}) and (f) Phase shifted voltage (v_{A1} , v_A , v_{B1}) with input phase current (i_A) for the non-isolated AMPC.





(b)



(c)

Figure 3.24: Simulated and experimental results of (a) Winding voltage ($v_{ab1,rms}$)/current ($i_{ab1,rms}$) waveforms (b) Winding voltage ($v_{ca4,rms}$)/current ($i_{ca4,rms}$) waveforms and (c) Input phase voltage ($v_{A,rms}$)/current ($i_{A,rms}$) of the non-isolated AMPC.

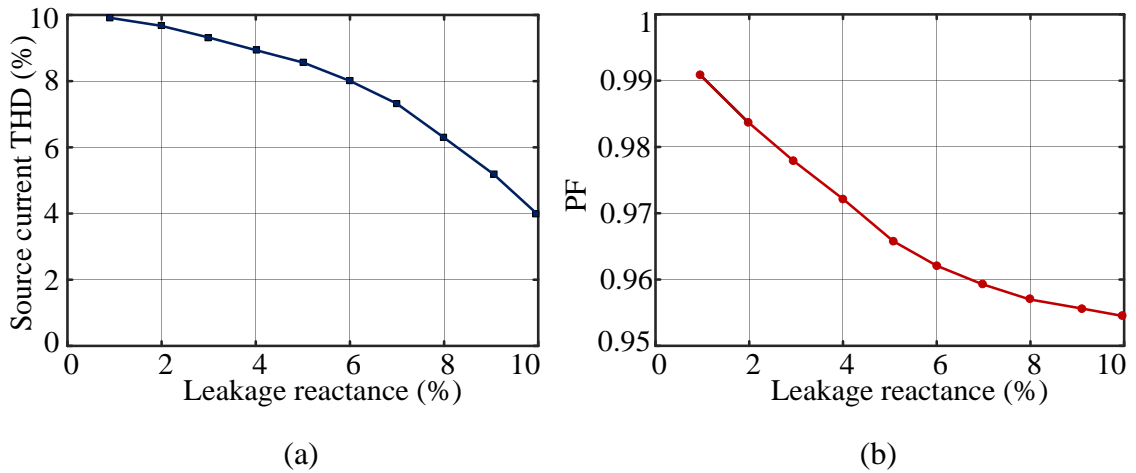


Figure 3.25: Variations of (a) Input source current %THD with varying % leakage reactance and (b) PF with varying % leakage reactance for the non-isolated AMPC.

To elucidate the effect of AMPC transformers leakage reactance on the THD of the input current and operating PF, simulations were performed in MATLAB, and the corresponding result is shown in Figure 3.25(a) and (b). It is concluded that a trade-off has to be considered while selecting the value of leakage reactance since it has a disparate effect on the input current THD and operating PF.

Some of the salient features of the non-isolated AMPC are as follows.

1. The propound design leads to a significant reduction in magnetic rating of the non-isolated AMPC transformer. Thus, qualifying it as a simple, cost-effective and reliable solution for power electronic systems arena.
2. The proposed method of creating prime numbered output phases results in enabling smooth change in current from one conducting pair of diode to the other in every 72° . Also, the leakage inductance of the proposed AMPC transformer is made adequate to reduce the high di/dt effect.
3. Under varying load conditions, the system efficiency is maintained extremely high and also the power quality indices are observed to be well within limits specified by the

IEEE and IEC Std., with the small value of smoothing means at the input and output side.

3.5 COMPARATIVE STUDY

A comparative analysis of the non-isolated MSAT and AMPC with that of the other multi-pulse autoconnected transformer topologies have been carried out for varying load conditions and it is presented in Table 3.3. Table 3.3 presents the comparison of various power quality indices for the MSAT and AMPC transformers with primitive 6-pulse configuration and other multi-pulse autoconnected transformer available in (Abdollahi and Gharehpetian 2016; Kalpana et al. 2010, 2013; Sheelvant et al. 2017; Singh et al. 2010; Singh and Gairola 2008). It is observed from the Table 3.3 that, the input source current THD (i_{THD}) of the non-isolated MSAT and AMPC is 3.04% and 3.16% respectively and it is able to achieve reduced voltage/current THD while maintaining near unity PF for LL and FL conditions.

Table 3.4 gives the performance of the MSAT and AMPC when compared with other multi-pulse techniques in terms of the number of diodes, magnetic rating, current THD, cost, efficiency, and type of current injection circuit (CIC). Among various 20-pulse configurations, the MSAT and AMPC have reduced magnetic rating due to its special winding arrangement which is the notable contribution of this research work. Even though the phase angle between phase staggered voltages and input phase voltages are same in (Abdollahi and Gharehpetian 2016; Kalpana et al. 2013; Singh and Gairola 2008), the winding configuration of the MSAT and AMPC differs from the above-mentioned configurations. Moreover, the phase staggered output voltages can be used for multi-phase motor drives, electric traction, electric furnace, welding systems, telecom systems etc., From Table 3.4 it is inferred that, the superior efficiency with improved power quality performances, reduced cost and magnetic rating are the most commendable advantages of the MSAT and AMPC configurations.

Table 3.3: Comparison of simulation results of MSAT and AMPC autoconfigured transformers with other multi-pulse autoconnected transformers for various power quality indices

Sl. No.	Topologies	AC mains current i_A (A)		% i_{THD}		DF		DPF		PF		DC-link voltage, V_{dc} (V)		% RF
		LL	FL	LL	FL	LL	FL	LL	FL	LL	FL	LL	FL	FL
1	6-Pulse	4.35	24.18	51.0	28.8	0.861	0.979	0.909	0.911	0.783	0.892	610.5	602.2	4.159
2	12-Pulse [1]	4.30	20.80	18.2	12.5	0.986	0.998	0.984	0.990	0.971	0.989	377.4	360.5	1.484
3	12-Pulse [2]	4.50	19.28	20.0	0.90	0.993	0.999	0.999	0.999	0.992	0.999	574.4	559.0	2.683
4	18-Pulse [3]	2.20	23.39	9.80	4.10	0.995	0.999	0.987	0.989	0.984	0.988	510.0	515.0	0.962
5	20-Pulse [4]	3.65	15.22	5.60	3.70	0.998	0.999	0.999	1.000	0.997	0.999	590.2	595.8	0.593
6	20-Pulse [5]	10.4	52.59	7.15	5.50	0.997	0.997	0.998	0.997	0.995	0.995	614.8	610.1	0.581
7	20-Pulse [6]	3.78	18.49	4.60	1.50	1.000	0.996	0.990	1.000	0.994	0.996	341.7	332.1	2.890
8	20-Pulse [MSAT]	9.14	26.39	4.20	3.04	0.991	0.998	0.999	1.000	0.991	0.999	605.5	608.7	0.525
9	20-Pulse [AMPC]	5.47	15.40	4.63	3.16	0.991	0.998	0.999	1.000	0.991	0.999	580.5	590.7	0.517

Table 3.4: Comparison of MSAT and AMPC autoconfigured transformers with other multi-pulse autoconnected transformers

Sl. No.	Topologies	No. of diodes	Magnetic rating (%)	Current THD at the rated load	Approximate cost (% of the load) *	Efficiency at rated load	CIC
1	12-Pulse [1]	12	16.40	3.70 %	7.20 %	98.51 %	Without CIC
2	12-Pulse [2]	12	25.54	0.90 %	8.17 %	93.70 %	With CIC
3	18-Pulse [3]	18	20.90	4.10 %	6.60 %	94.34 %	Without CIC
4	20-Pulse [4]	20	45.47	3.36 %	12.1 %	94.43 %	Without CIC
5	20-Pulse [5]	20	61.29	6.60 %	16.3 %	97.27 %	Without CIC
6	20-Pulse [6]	20	56.13	1.50 %	12.5 %	-	Without CIC
7	20-Pulse [MSAT]	20	40.27	3.04 %	10.7 %	97.65 %	Without CIC
8	20-Pulse [AMPC]	20	30.12	3.16 %	8.03 %	97.73 %	Without CIC

* The total cost estimation of the transformer is done by following the thumb rule. Cost of the transformer is estimated as 4 times the kVA rating of transformer. Moreover, the price may vary based on market growth.

- [1] (Kalpana et al. 2010)
- [2] (Sheelvant et al. 2017)
- [3] (Singh et al. 2010)

- [4] (Kalpana et al. 2013)
- [5] (Abdollahi and Gharehpetian 2016)
- [6] (Singh and Gairola 2008)

3.6 CONCLUSION

This chapter has presented a detailed design, analysis and implementation of non-isolated transformer configurations for power quality improvement. The front-end transformer configurations are perceived by zig-zag and delta connected autotransformer rated for only 40.27% and 30.12% of the nominal load respectively. The efficiency of front-end MSAT and AMPC transformer configurations are 97.69% and 97.73% respectively. The progress in the second configuration is achieved as a result of arranging the phase staggered windings in the delta connected configurations and results in smooth change in current from one conducting pair of diode to the other. Further, a detailed power quality performance analysis and loss calculations have been studied. The MSAT and AMPC based AC-DC converter system exhibits remarkable improvement in power quality with high efficiency. However, increasing the number of prime numbered output phases intending to reduce harmonic distortion with superior input current waveform quality increases the complexity of the proposed configuration. Moreover, the volume and space requirement are also increased when compared with active front-end configurations. Hence, another classification of three-phase front-end AC-DC converter namely active technique-based AC-DC converter for power quality improvement is introduced in the next chapter.

CHAPTER 4

POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING ACTIVE TECHNIQUE

4.1 INTRODUCTION

In the previous chapter, power quality improvement using 20-pulse autoconfigured transformer-based techniques were presented. The suitability of those topologies is found pertinent to medium and high-power application fields. In this chapter, the main objective of power quality improvement is achieved by active techniques for medium and high-power level applications. Unlike autotransformer-based passive techniques, the semiconductor switch-based active techniques are developed for power quality improvement. Further, the voltage sensorless control is proposed for the converter control.

This chapter is organized as follows: Firstly, the topological details of the Vienna type front-end AC-DC converter topology is described, followed by the developed voltage sensorless strategy. Secondly, the boost type Delta connected front-end AC-DC converter is introduced. Similarly, the voltage sensorless control technique is proposed for the front-end Delta connected rectifier. Further, the simulation and experimental results pertaining to both the converters are provided with a detailed comparative evaluation.

4.2 PROBLEM FORMULATION

The advancement of the multi-pulse technique leads to the betterment of input power quality even though, the main issues with this technique are increased magnetic rating, weight, and volume of the system. Hence, active semiconductor switch-based techniques for power quality improvement in front-end AC-DC converter has attained more importance. However, the control complexity of the front-end topology is increased. On

this line, with a motivation to achieve power quality improvement, the voltage sensorless control technique is proposed for the active topologies considered under this research work.

4.3 THREE-PHASE THREE-SWITCH BOOST TYPE VIENNA CONVERTER

The AC-DC converter consists of an active front-end PFC rectifier is shown in Figure 4.1. The front-end system consists of input side DBR followed by a bi-directional three-leg switching circuit. One end of the bi-directional three-leg switching circuit is connected to a DBR and another end is connected to the DC-link midpoint. In the active front-end PFC rectifier, input side voltage formation is dependent on the phase current sign and the input inductance value. This DBR with bi-directional switching topology will produce the three-level voltage at the input stage and hence it is also called three-level converter. The output side of bi-directional switching circuit has been connected to the center-point (M) of two capacitors which produces the upper positive output voltage and lower negative output voltage.

The advantage of three-level converter is that the blocking voltage of the switches is only half of the line-line voltage. As the number of levels increases the fundamental current ripples at the input side is reduced. And, also the size of the input boost inductance has been reduced. This results in lower switching loss and less electromagnetic interference. The DC output voltage V_{dc} , of the proposed system have minimum and maximum voltage of $\sqrt{2} v_{N,rms}$ and $2\sqrt{2} v_{N,rms}$ respectively. For a higher DC output voltage, minimum value of input inductance can be chosen. In the event of supply phase loss, the topology will operate under reduced output power and maintain sinusoidal input current on the remaining phases (Kolar and Friedli 2013).

4.3.1 Design, analysis and control technique of the Vienna type front-end AC-DC converter

In this section, firstly analysis and design of the front-end converter is discussed. Further, the discussion is carried out for the proposed voltage sensorless control technique and loss calculation.

4.3.1.1 Analysis and design of the Vienna type front-end AC-DC converter

The three-phase input voltage are displaced by 120° each other and thus can be written as

$$\bar{v}_a = v_m \sin \omega t; \bar{v}_b = v_m \sin(\omega t + 120^\circ); \bar{v}_c = v_m \sin(\omega t + 240^\circ); \quad (4.1)$$

which leads to

$$\bar{v}_a + \bar{v}_b + \bar{v}_c = 0 \Rightarrow \bar{v}_{aN} + \bar{v}_{bN} + \bar{v}_{cN} = 0 \quad (4.2)$$

By applying KVL at the converter input terminal, the cyclic average voltage is written as,

$$\begin{aligned} v_a &= v_{aM} + v_{MN} \\ v_b &= v_{bM} + v_{MN} \\ v_c &= v_{cM} + v_{MN} \end{aligned} \quad (4.3)$$

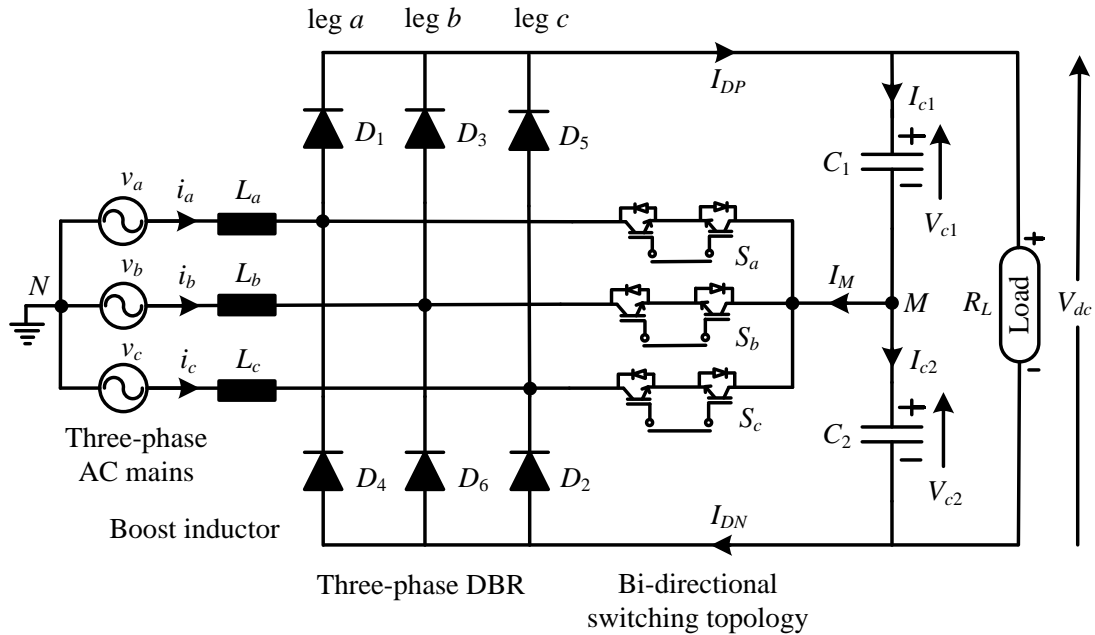


Figure 4.1: Schematic diagram of the Vienna type front-end PFC rectifier.

Using (4.2) & (4.3), the following relation can be obtained.

$$v_{MN} = -\frac{1}{3}(v_{aM} + v_{bM} + v_{cM}) \quad (4.4)$$

After substituting (4.1) & (4.3) in (4.4), the resultant three-phase equations are given as,

$$\begin{aligned} v_a &= v_{aM} - \frac{1}{3}(v_{aM} + v_{bM} + v_{cM}) \\ v_b &= v_{bM} - \frac{1}{3}(v_{aM} + v_{bM} + v_{cM}) \\ v_c &= v_{cM} - \frac{1}{3}(v_{aM} + v_{bM} + v_{cM}) \end{aligned} \quad (4.5)$$

Equation (4.5) is simplified and is expressed in matrix form as,

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} v_{aM} \\ v_{bM} \\ v_{cM} \end{bmatrix} \quad (4.6)$$

For CCM of converter operation, the cyclic switching voltage of all the three-phases are given by (4.7) and it is depending on the DC-link voltage $V_{dc}/2$,

$$\begin{aligned} v_{aM} &= \begin{cases} (1 - D_a) \Rightarrow i_a \geq 0 \\ -(1 - D_a) \Rightarrow i_a < 0 \end{cases} \\ v_{bM} &= \begin{cases} (1 - D_b) \Rightarrow i_b \geq 0 \\ -(1 - D_b) \Rightarrow i_b < 0 \end{cases} \\ v_{cM} &= \begin{cases} (1 - D_c) \Rightarrow i_c \geq 0 \\ -(1 - D_c) \Rightarrow i_c < 0 \end{cases} \end{aligned} \quad (4.7)$$

where D_a , D_b , D_c are the duty ratio of the switch S_a , S_b , S_c respectively. The duty ratio is given by,

$$D_{a,b,c} = \begin{cases} 0 \Rightarrow S_{a,b,c} = OFF \\ 1 \Rightarrow S_{a,b,c} = ON \end{cases} \quad (4.8)$$

The output capacitors can be expressed by (4.9),

$$I_{c1} = C_1 \frac{dV_{c1}}{dt} = I_{DP} - \frac{V_{dc}}{R_L}$$

$$I_{c2} = C_2 \frac{dV_{c2}}{dt} = I_{DN} - \frac{V_{dc}}{R_L}$$
(4.9)

where I_{c1} and I_{c2} are the current through the capacitors C_1 and C_2 respectively and R_L is load connected at the front-end converter. The output DC voltage is the sum of capacitor voltages, C_1 and C_2 and ΔV is the unbalance in the DC-link voltages. These voltages can be expressed by equation (4.10) as follows,

$$V_{dc} = V_{c1} + V_{c2}; \Delta V = V_{c1} - V_{c2}$$
(4.10)

By KCL, the diode current is given in equation (4.11) where I_{DP} is the positive side diode current and I_{DN} is sum of lower diode current. The upper group diodes are named as D_1 , D_3 , D_5 and lower group diodes are named as D_4 , D_6 , D_2 .

$$I_{DP} = I_{a,D1} + I_{b,D3} + I_{c,D5}$$

$$I_{DN} = I_{a,D4} + I_{b,D6} + I_{c,D2}$$
(4.11)

The sum of positive group diode and negative group diode currents are given in terms of duty ratio of the converter as follows,

$$I_{DP;a,b,c} + I_{DN;a,b,c} = (D_{a,b,c})(i_{a,b,c})$$
(4.12)

The average DC-link (upper and lower diodes) currents as in terms of duty ratio with corresponding phase currents are given by

$$I_{DP} + I_{DN} = D_a i_a + D_b i_b + D_c i_c$$
(4.13)

The converter mid-point current is the difference of lower and upper diode currents and can be expressed in terms of

$$I_M = I_{DN} - I_{DP}$$
(4.14)

The cyclic average DC-link current (upper or lower diodes) are obtained by the average of input phase currents which is given by,

$$\frac{|I_a| + |I_b| + |I_c|}{2}$$
(4.15)

The three-phase input phase currents are displaced by 120° each other and hence it can be written as

$$\bar{i}_a = i_m \sin \omega t; \bar{i}_b = i_m \sin(\omega t + 120^\circ); \bar{i}_c = i_m \sin(\omega t + 240^\circ) \quad (4.16)$$

In a three-phase system, the sum of phase current is given by

$$\bar{i}_a + \bar{i}_b + \bar{i}_c = 0 \quad (4.17)$$

The average current through the diode is calculated by (4.18),

$$\frac{6}{T_s} \int_{-\frac{T_s}{12}}^{\frac{T_s}{12}} i_m \cos(\omega t) dt = \frac{3}{\pi} I_m \quad (4.18)$$

The instantaneous DC output power is given by

$$P_{dc} = \frac{V_{dc}}{2} (I_a + I_b + I_c) = \frac{3}{2} V_m I_m \quad (4.19)$$

From the equation (4.1) & (4.17), the instantaneous AC power is given by,

$$\begin{aligned} P_{ac} &= \bar{v}_a \bar{i}_a + \bar{v}_b \bar{i}_b + \bar{v}_c \bar{i}_c \\ P_{ac} &= v_m i_m \sin^2 \omega t + v_m i_m \sin^2(\omega t + 120^\circ) + v_m i_m \sin^2(\omega t + 240^\circ) \\ P_{ac} &= \frac{3}{2} v_m i_m \end{aligned} \quad (4.20)$$

From the (4.19) & (4.20) the input-output power balance has been verified.

A. Design of an input inductor

The input current ripple is reduced by proper value of inductor connected in series with three-phase input voltage. The voltage conversion is happened at a large scale, due to this the inductor value can't be chosen from the data sheets. Therefore, the following equation is the good estimation of inductor value. For phase A, input inductance is calculated by (4.21)

$$L_a = \frac{v_a \times (V_{dc} - v_a)}{i_{a,ripple} \times f_s \times V_{dc}} \quad (4.21)$$

where $i_{a,ripple}$ is the maximum allowable current ripple in phase A which is generally 15% to 20% of the output current.

B. Design of DC-link capacitor

Energy stored in the capacitor for the half cycle of the power ripple is given by (4.22),

$$W_c = \int_0^{\frac{\pi}{2}} p dt = \frac{P_{dc}}{\omega} \quad (4.22)$$

where P_{dc} is the output power and ω is the angular frequency of the input power supply. The DC-link capacitor charges and discharges the power at twice the line frequency. So, DC-link capacitor ripple having twice the line frequency is applied across the DC output. The charge on the capacitor is obtained from (4.23),

$$W_c = \frac{1}{2} CV_{dc\max}^2 - \frac{1}{2} CV_{dc\min}^2 \quad (4.23)$$

where $V_{dc\max}$ and $V_{dc\min}$ are the maximum and minimum allowable DC voltage at the output side. The rating of the device can be calculated from the allowable maximum and minimum voltage at the output side. The required capacitance of the DC-link part is calculated by (4.24),

$$C_{1,2} \geq \frac{2P_{dc}}{\omega(V_{dc\max}^2 - V_{dc\min}^2)} \quad (4.24)$$

From the above equation, the DC-link capacitance is calculated from the output power, angular line frequency and allowable maximum and minimum voltage ripple of the DC-link voltage. The ripple in the DC-link voltage is calculated from (4.25),

$$V_{ripple} = V_{dc\max} - V_{dc\min} \quad (4.25)$$

In practice, the allowable voltage ripple is 1-5% of the output voltage level. The capacitance value is purely depends on the voltage ripple. Higher the voltage ripple lesser the capacitance required and vice versa.

4.3.1.2 Voltage sensorless control, modulation technique and efficiency calculation

The per phase equivalent circuit of the Vienna type front-end AC-DC converter is considered for understanding the basic principle of operation and finding the resultant current is shown in Figure 4.2(a). In Figure 4.2(b) the switch S_a is closed and the positive cycle of phase voltage v_a is applied to the leg a. During this positive cycle, the positive upper diode is in a conduction state and the upper capacitor is charged to the positive peak of the applied voltage. The return path is formed through the anti-serial connected bi-directional switch in which one switch and another switch anti-parallel diode is in conduction and hence closes the current circulation path. During negative cycle of applied phase voltage v_a , the negative lower diode is in a conduction state and the lower capacitor is charged to a negative peak of the applied voltage. The current path is closed by an anti-serial connected bi-directional switch in which one switch anti-parallel diode and other switch is in conduction state as shown in Figure 4.2(c). In both the states the capacitor is charged to $+V_{dc}/2$ and $-V_{dc}/2$. All possible combinations of the switching states and respective voltage/current with respect to mid-point M is given in Table 4.1.

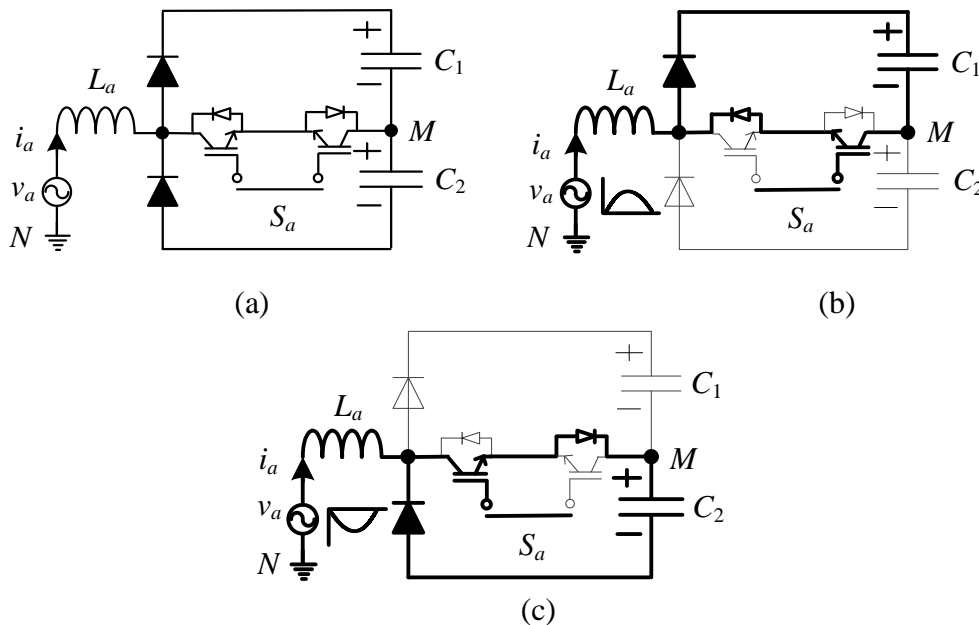


Figure 4.2: (a) Single phase equivalent circuit of the Vienna type front-end converter and its operating modes when (b) positive input cycle, (c) negative input cycle.

Table 4.1: Switching states and respective voltage/current with respect to mid-point (M)

S_a	S_b	S_c	V_{aM}	V_{bM}	V_{cM}	i_M
0	0	0	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	0
0	0	1	$V_{dc}/2$	$-V_{dc}/2$	0	$-I_c$
0	1	0	$V_{dc}/2$	0	$-V_{dc}/2$	$-I_b$
0	1	1	$V_{dc}/2$	0	0	I_a
1	0	0	0	$-V_{dc}/2$	$-V_{dc}/2$	$-I_a$
1	0	1	0	$-V_{dc}/2$	0	I_b
1	1	0	0	0	$-V_{dc}/2$	I_c
1	1	1	0	0	0	0

A. Voltage sensorless control technique

The basic concept of voltage sensorless control is briefly summarized in order to provide an operating behaviour of the front-end rectifier. The equivalent circuit diagram of the input stage of front-end rectifier as shown in Figure 4.3(a). The phase voltage v_a is taken into discussion for further explanation of the voltage sensorless control technique. Under consideration of the stationary equilibrium of the input phase voltage v_{aN} and the corresponding average value v_a' across the bi-directional switch (input diode bridge is not considered) is given by (4.26),

$$v_{aN} = v_a' = V_c \times V_{dc} \quad (4.26)$$

where $V_c = \frac{i_a}{K_i}$ is the control signal obtained from the actual input current. So,

$$v_{aN} = \frac{i_a \times V_{dc}}{K_i} \quad (4.27)$$

and the equivalent resistance can be described by (4.28),

$$R_a = \frac{V_{dc}}{K_i} \quad (4.28)$$

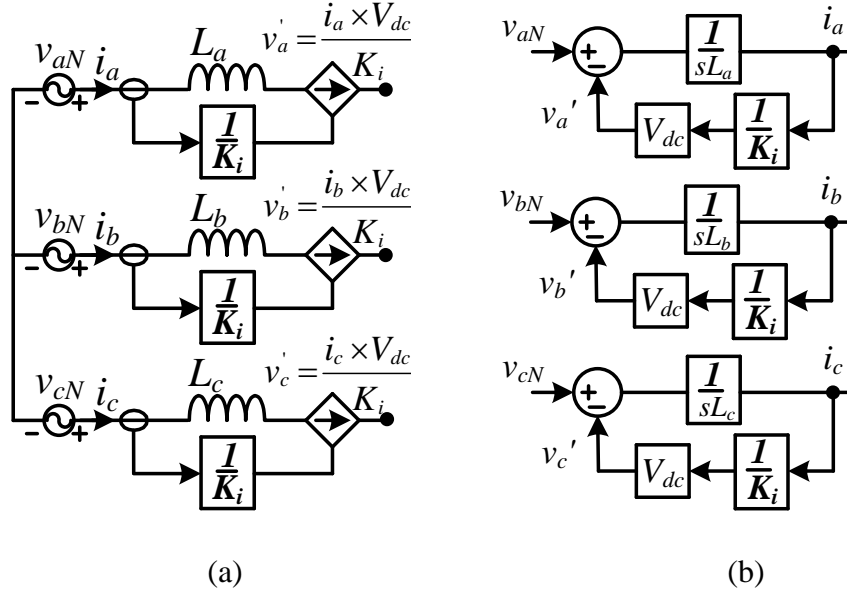


Figure 4.3: (a) Equivalent circuit of the input stage of front-end unity PF rectifier incorporating voltage sensorless control. (b) Block diagram of control technique for input voltage evaluation.

The input current utilization of the system can be easily regulated by the output voltage control by varying the value of K_i . Hence, the proposed sensorless voltage control concept does not require a sensing of the mains phase voltage and relying on the absolute values of the input phase currents.

The dynamic performance of the system under study with first order approximation is given by (4.29),

$$i_a(s) = \frac{v_{aN}(s)}{R_a} \frac{1}{1 + s \frac{L_a}{R_a}} \quad (4.29)$$

In (4.29), the negative feedback of the integration element $1/sL$ is formed by input inductor through modulation stages. The block diagram of the control technique for input voltage evaluation as shown in Figure 4.3(b). Therefore, from the above discussion it is evident that, the input current of the system is directly governing the input voltage information without sensing the input voltage directly.

B. Modulation techniques (MTs)

In order to obtain the resistive fundamental behaviour, i.e., the rectifier system has to emulate a symmetric three-phase star connection of ohmic resistor, there are several possibilities for organizing the switching states within one pulse period. The active switching states can either be arranged symmetrically or asymmetrically with reference to the middle of the pulse period, and the freewheeling state can be placed in the middle, or at the beginning and/or at the end of the pulse period (Baumann and Kolar 2005). By various possible combinations, an optimized way to arrange the switching states can be identified to reduce the switching stress and DC ripples. Generally switching power loss is decided by the switching state sequence within one pulse period and/or by the line-to-line voltage being switched at the transition to a successive switching state. The voltage sensorless control technique is mainly proposed and incorporated in the system. Moreover, the switching power loss only depends on the switching states. So, arranging the switching sequence in accordance with the minimum switching stress is an additional innovation. Furthermore, it is practicable to clamp one power switch in the ON-state for a $\pi/3$ interval resulting in a reduced voltage stress on the switches and legs of three-phase DBR.

Table 4.2: Different MTs for the Vienna type front-end AC-DC converter

Switching State Arrangement	Modulation Technique	Pulse Period ($0-T_s/2$)	Pulse Period ($T_s/2-T_s$)
Asymmetric	MT1	(111) (110) (100)	(111) (110) (100)
	MT2	(111) (110) (010)	(111) (110) (010)
	MT3	(111) (110) (000)	(111) (110) (000)
	MT4	(111) (110) (001)	(111) (110) (001)
Symmetric	MT5	(110) (100) (001)	(001) (100) (110)
	MT6	(101) (110) (001)	(001) (110) (101)
	MT7	(101) (110) (000)	(000) (110) (101)
	MT8	(011) (010) (100)	(100) (010) (011)

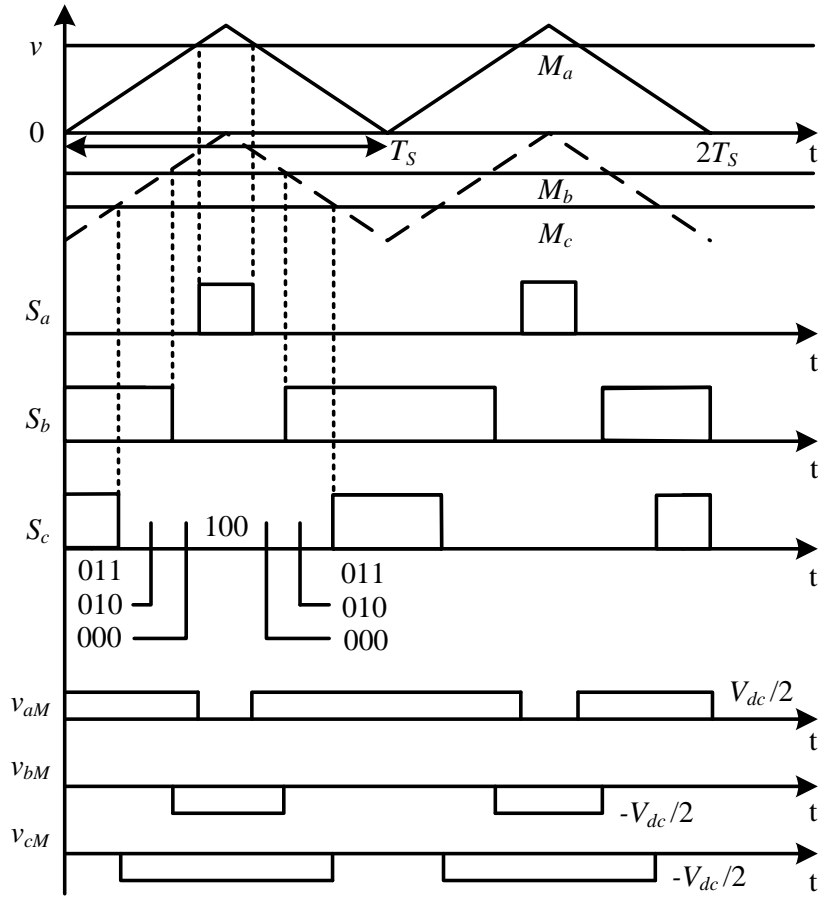


Figure 4.4: Modulation scheme for the Vienna type front-end PFC rectifier.

MTs for the Vienna topology has been studied from (Baumann et al. n.d.) and a remarkable variation has been incorporated so that the minimum switching losses as well as minimum DC ripples are ensured. Based on various conduction sequence, several possibilities of arranging the switching states in such a manner that minimum numbers of switching transitions of the power transistors and/or minimum switching losses occur are given in Table 4.2. The output voltage generation can be specified by modulation index M .

$$M = \frac{i_{N,(a,b,c)}}{I_{dc}} = \frac{\sqrt{2}V_{dc}}{\sqrt{3}v_{N,(a,b,c)}}; M = [0,1] \quad (4.30)$$

Due to the phase symmetry of the converter structure and due to the symmetry of the input AC system, the switching period analysis is restricted to $\pi/3$ interval of the mains period. The magnitude of the current phasors plays an important role to determine the voltage arrangement. The proposed modulation scheme shown in Figure 4.4, for an instant $i_a > 0$ and $i_b, i_c < 0$, the intersection of control signal with triangular carrier results in four switching states (011), (010), (000) and (100), which is given as MT8 in Table 4.2. The switching states of each switches (S_a, S_b, S_c) are indicated as either 0 or 1, where 0 denotes the OFF-state and 1 denotes the ON-state of the switches. Here positive and negative offset value leads to the increase and decrease of ON-time of switching state (100) compared with ON-time of switching state (011) respectively. These switching states determine the charging and discharging of upper and lower capacitors (Dawande et al. 1996; Drogenik and Kolar n.d.; Soeiro and Kolar 2013).

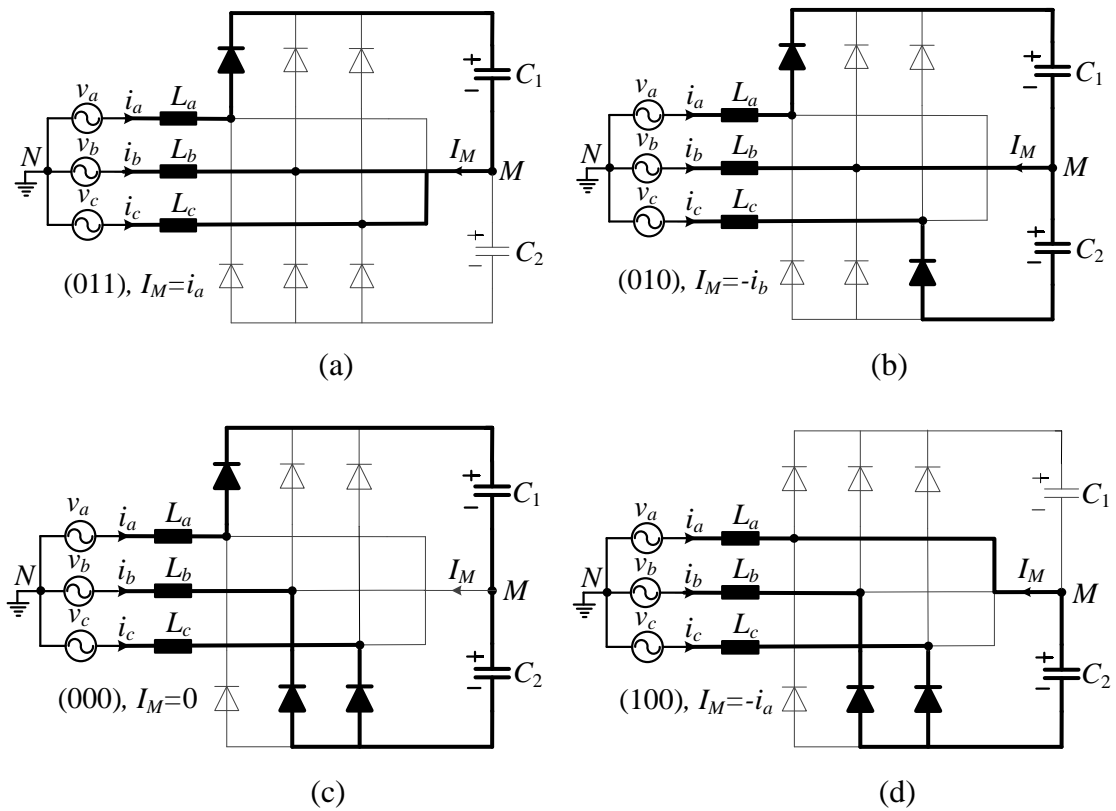


Figure 4.5: Conduction states for the converter when (a) Switching state (011), (b) Switching state (010), (c) Switching state (000), (d) Switching state (100).

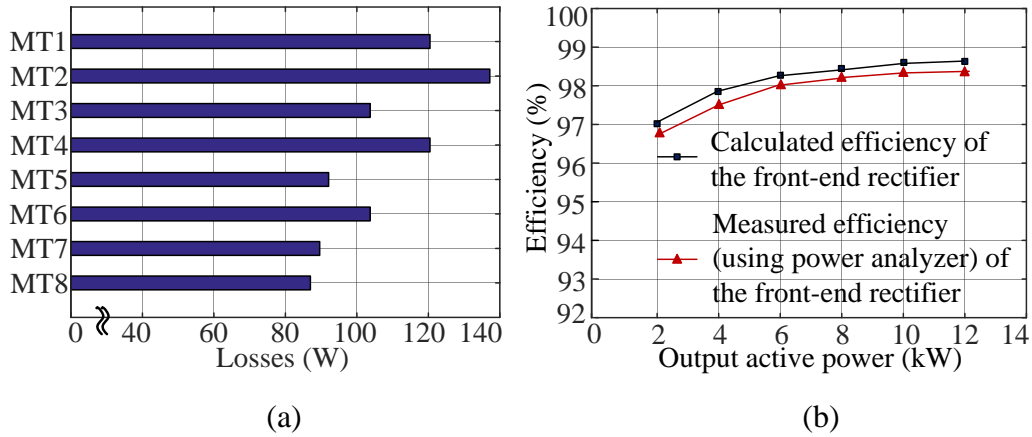


Figure 4.6: (a) Loss distribution of different MT and (b) Calculated efficiency of the Vienna type front-end AC-DC converter.

The resultant converter current is analyzed by the equivalent circuit of the above specified switching states. Figure 4.5 shows the resultant average current at the converter and charging of capacitors for all valid switching states. So, these four switching states have been applied for the switching pulse period $T_s/2$. This will lead to minimum ripple in the sinusoidal input current. The input current ripple is dependent on the carrier frequency. Higher the carrier frequency lesser the input current ripple (Lee and Lee 2016a; b). Also, increasing the carrier frequency not only improves the DC-link voltage balancing but also increases switching losses in the switches. So, the loss distribution in the switches of rectifier for the modulation techniques MT1-MT8 (modulation index of unity) is shown in Figure 4.6(a). It is observed that, proposed MT8 is having lesser loss of only 83.4 W.

The control technique adopted in (Miniböck and Kolar 2005) has been modified for getting above discussed switching states. Figure 4.7 shows the control loop of the front-end rectifier incorporating the voltage sensorless input phase current control in the inner loop and output DC voltage control in the outer loop. Here the voltage error V_{error} between the referral DC voltage, V_{ref} and the sensed DC output voltage V_{dc} is processed by a proportional and integral (PI) controller and the resultant signal is obtained. The sampled input current $i_a/i_b/i_c$ is then analogized with the referral signal and it is processed by PI controller. The signal from current controller is compared with high frequency triangular wave of 20 kHz and modulates (Sandeep and Yaragatti 2017; Vahedi et al. 2016) the

proposed MT in order to generate PWM to the gate of IGBTs. For the input, current $i_a > 0$ and $i_b, i_c < 0$, the resultant switching states given in MT8 have been applied to the bi-directional switches using the control logic proposed in (Saravana Prakash P et al. 2016). Any variation in the measured quantities have been reflected in the duty ratio D_a, D_b, D_c and hence balances the DC-link voltage and maintains the input current shape as sinusoidal.

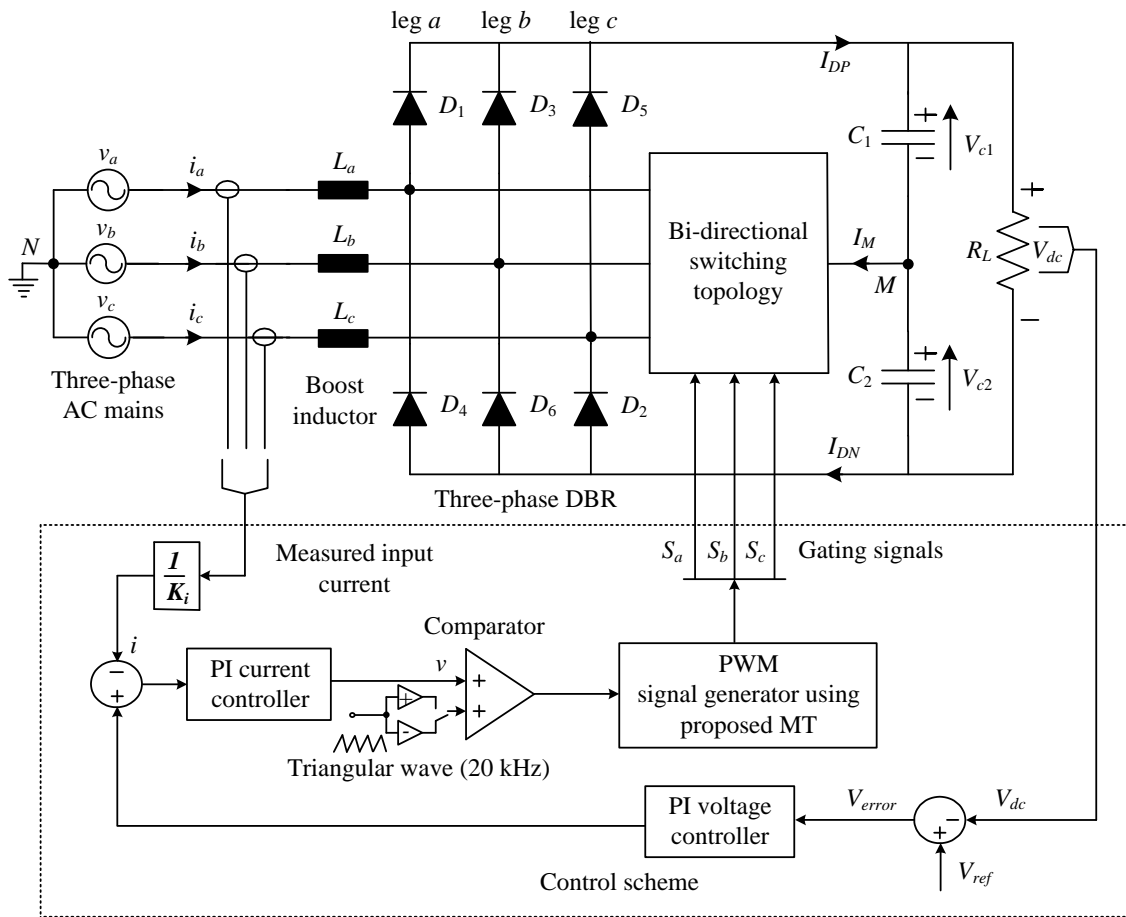


Figure 4.7: Control scheme for the Vienna type front-end PFC rectifier.

C. Efficiency of the overall system

The efficiency of the proposed system incorporated by the optimized MT is determined by considering the individual losses in the system. The various parameters required for the

loss calculation can be taken from data sheet of the device. Total losses associated with the Vienna type front-end AC-DC converter are summarized as,

$$P_T = P_{DBR} + P_{Bi-directional\ switch} \quad (4.31)$$

a) *Losses in three-phase DBR (P_{DBR}):* The power loss components (neglecting the turn-OFF losses) of the DBR is calculated by considering voltage drop of diode $V_f = 0.7$ V, internal resistance of the diode $R_d = 1$ m Ω , and $I_d = 20$ A and is given by (4.32),

$$P_{DBR} = \frac{1}{\pi} \int_0^{\pi} (V_f I_d + I_d^2 R_d) d(\omega t) = V_f I_d + I_d^2 R_d = 14.4 \text{ W} \quad (4.32)$$

So, the total power loss for the three-phase DBR is $6 \times 14.4 = 86.4$ W.

b) *Losses in bi-directional switching converter ($P_{Bi-directional\ switch}$):* The conduction power loss of the IGBT based bi-directional switching converter is calculated by considering voltage drop of IGBT as, $V_f = 1$ V, internal resistance of the diode $R_s = 1$ m Ω , $I_d = 20$ A, and is given by (4.33),

$$P_{Conduction} = f_s \int_0^{T_{on}} (V_f I_d + I_d^2 R_s) dt = (V_f I_d + I_d^2 R_s) \times D = 10.2 \text{ W} \quad (4.33)$$

where D is the duty ratio $D = (T_{ON}/T)$, $T = (1/f_s)$.

The switching power loss of the IGBT based bi-directional switching converter is calculated (Babaei and Farhadi Kangarlu 2013) by considering $V_{SW} = 600$ V, $I_{SW} = 20$ A, $t_{on} = 75$ ns, $t_{off} = 145$ ns. $P_{SW} = \frac{1}{T} [N_{on} E_{on} + N_{off} E_{off}]$, where $N_{on/off}$ is the number of times that the IGBT switches are turned ON/OFF. Here $N_{on/off} = 2$. Energy lost during turn-ON and turn-OFF is given by (4.34),

$$\begin{aligned} E_{on} &= \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6} V_{SW} I_{SW} t_{on} = 1.5 \times 10^{-4} \\ E_{off} &= \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6} V_{SW} I_{SW} t_{off} = 2.9 \times 10^{-4} \end{aligned} \quad (4.34)$$

Thus, $P_{sw} = 17.6 \text{ W}$.

Thus, the total power loss for bi-directional switching converter is $(3 \times 10.2) + (3 \times 17.6) = 83.4 \text{ W}$. Therefore, the total power losses associated for the proposed system is $P_T = 169.8 \text{ W}$, and $\% \text{Efficiency} = \frac{12000}{12169.8} = 98.6\%$. Thus, the efficiency of the overall system at full load is found to be 98.6%. Figure 4.6(b) shows the calculated and measured efficiency of the proposed front-end converter under varying load conditions, which closely matches with each other.

4.3.2 Results and discussion

The Vienna type front-end PFC rectifier has been designed, analysed and its performance is simulated in the MATLAB environment. Under balanced mains, the system has equal amplitudes of the phase voltages with phase displacement of 120° electrical. For the proposed MT, the time response of the system is captured. Figure 4.8 shows the input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the front-end PFC rectifier at rated load conditions.

To test the dynamic performance, the load has been reduced to lower level (20% of FL) at $t = 0.2 \text{ s}$ as shown in Figure 4.8. The input current deviates from the normal sinusoidal waveform with reduced magnitude, the DC-link capacitor voltage is pulsating and the DC-link current is reduced according to the load level. However, just after the time $t = 0.2 \text{ s}$, the input phase current turns into sinusoidal quickly and DC-link voltage maintains constant. At time $t = 0.6 \text{ s}$, full load is applied back and brings back the phase current amplitude as rated value, even maintains a constant DC-link voltage. Besides, the input phase current is in-phase with phase voltage, which meets unity PF operation. It is worth noting that, the DC-link capacitor voltages are also maintaining constant which confirms the proposed method works satisfactorily. Under FL and LL condition, the waveform of supply current, along with its harmonic spectrum is shown in Figure 4.9. The power quality indices obtained from the Vienna type front-end PFC rectifier at varying loads are summarized in Table 4.3.

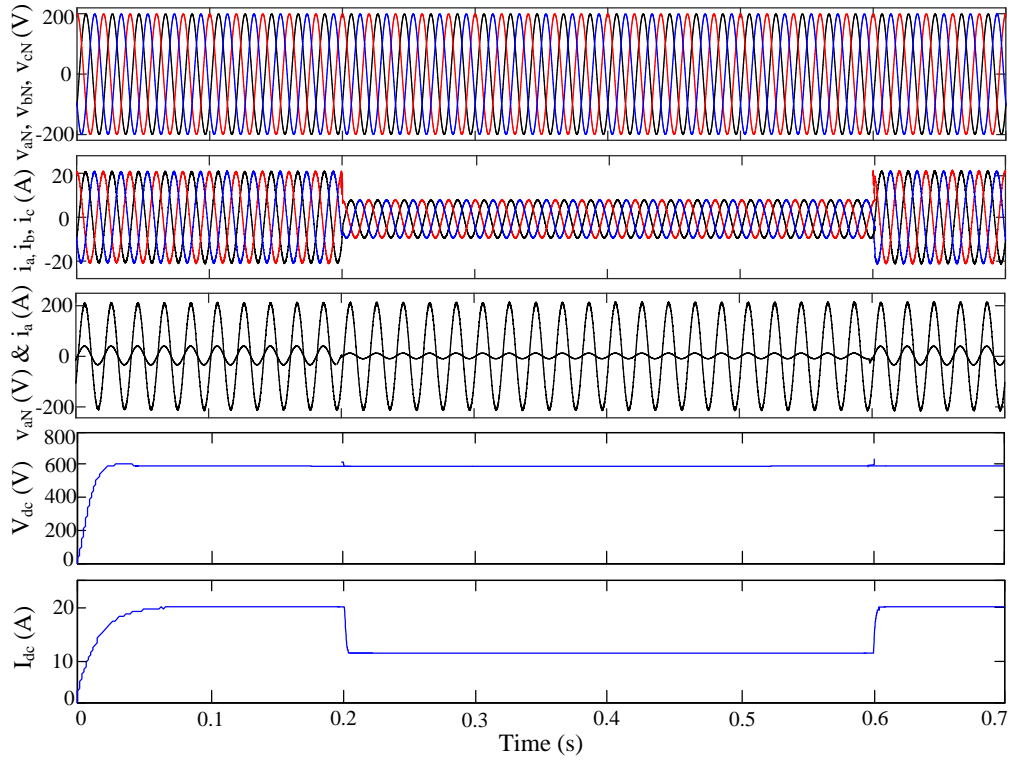


Figure 4.8: Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the Vienna type front-end PFC rectifier under load variations.

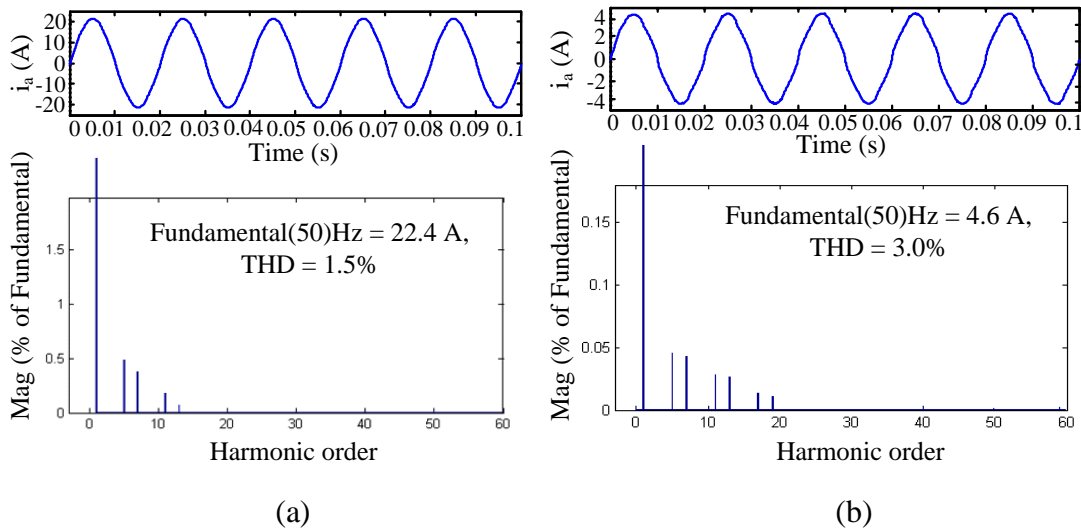


Figure 4.9: Simulation results of the input AC mains current (i_a) along with its frequency spectrum for the Vienna type front-end PFC rectifier at (a) FL and (b) LL conditions.

Table 4.3: Power quality indices for the proposed front-end PFC rectifier under varying load conditions

Load (%)	V_{THD} (%)	i_{THD} (%)	DPF	DF	PF	RF
20	1.2	3.0	0.9867	0.9981	0.9849	0.020
40	1.5	2.5	0.9883	0.9984	0.9868	0.012
60	1.8	2.0	0.9897	0.9987	0.9884	0.009
80	2.1	1.8	0.9919	0.9991	0.9913	0.008
100	2.4	1.5	0.9949	0.9989	0.9938	0.006

Under FL as well as in the LL condition, the power quality parameters are well within the IEEE standard. From the results, it is evident that the elimination of input current harmonics results in improvement of THD and also, maintains the PF close to unity.

Thus, the simulated results have also been analyzed to study the effect of load variation on the THD of input current and PF of proposed PFC converter with that of the conventional 6-pulse rectifier and it is shown in Figure 10(a) and (b). It is evident from the comparison between proposed front-end PFC rectifier with conventional DBR that, the proposed system has source current THD of below 3% and PF has maintained almost unity under varying load conditions which is not in case of 6-pulse rectifier.

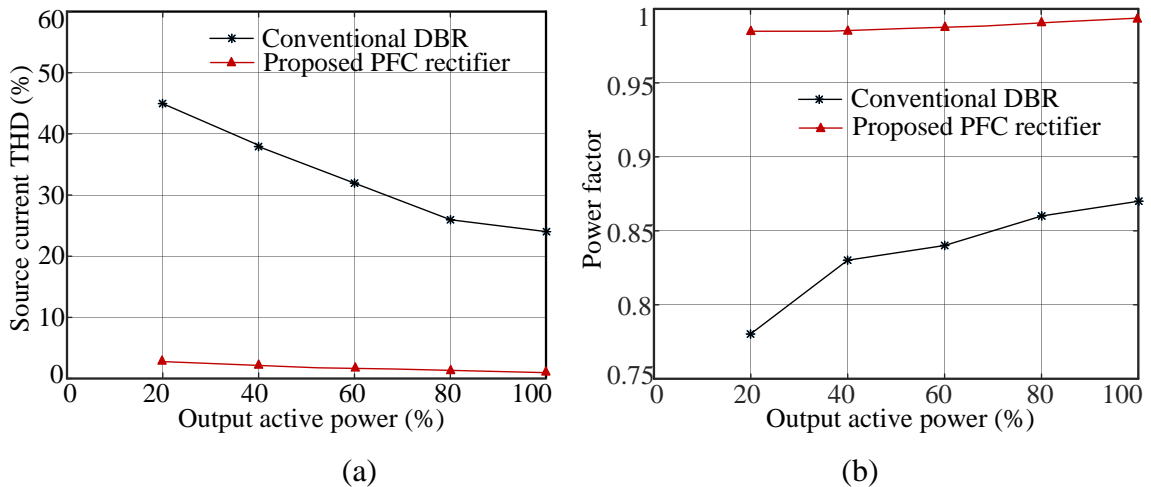


Figure 4.10: Comparison of power quality indices under varying load conditions of an active PFC rectifier with 6-pulse rectifier (a) Variation of THD of input current with load and (b) Variation of PF of input current with load.

A prototype model of the Vienna type front-end AC-DC converter is developed in the laboratory as shown in Figure 4.11. The description of hardware prototype and specification of the front-end AC-DC converter system is given in the Appendix B. Hardware results obtained for the proposed modulation methods under steady state condition are shown in Figure 4.12. The test results taken from the front-end AC-DC converter is at a reduced input voltage of 110 V and are recorded using oscilloscope and a Fluke 434-II power analyzer by connecting a lamp load. An IGBT based DBR has been chosen for hardware realization. The SKM300GM12T4 (Semikron) switch having 300 A current rating has been chosen for the bi-directional switch with a switching frequency of 20 kHz and discrete diode SKKD 26 (Semikron) are employed in the prototype.

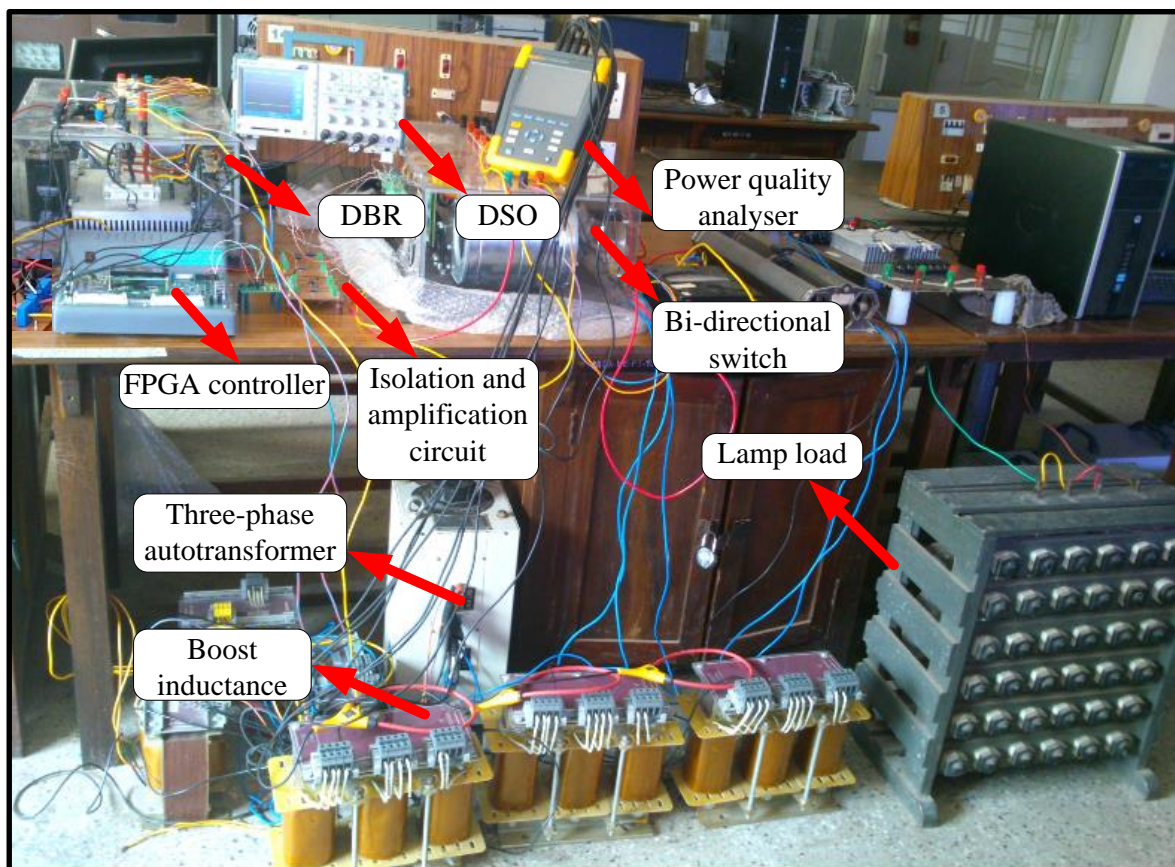
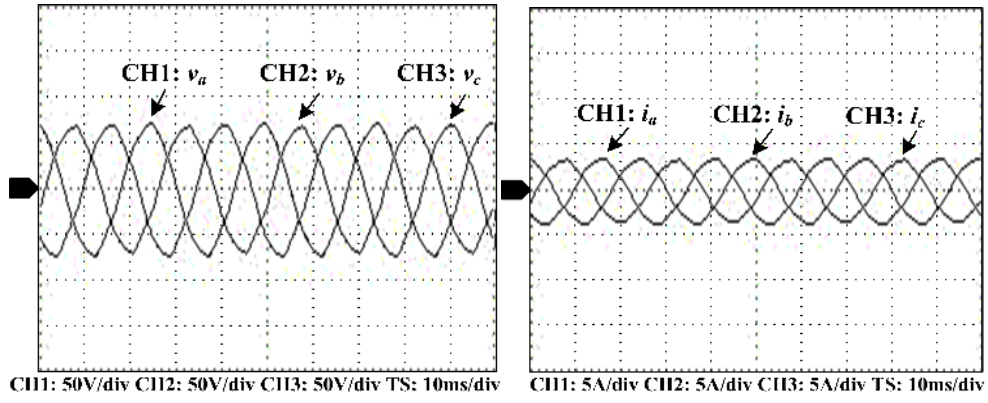
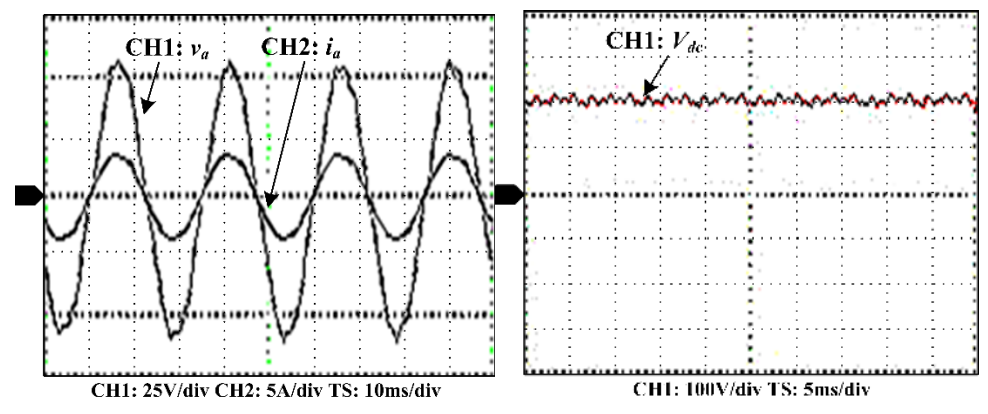


Figure 4.11: Hardware demonstrator of an active three-phase front-end AC-DC converter.



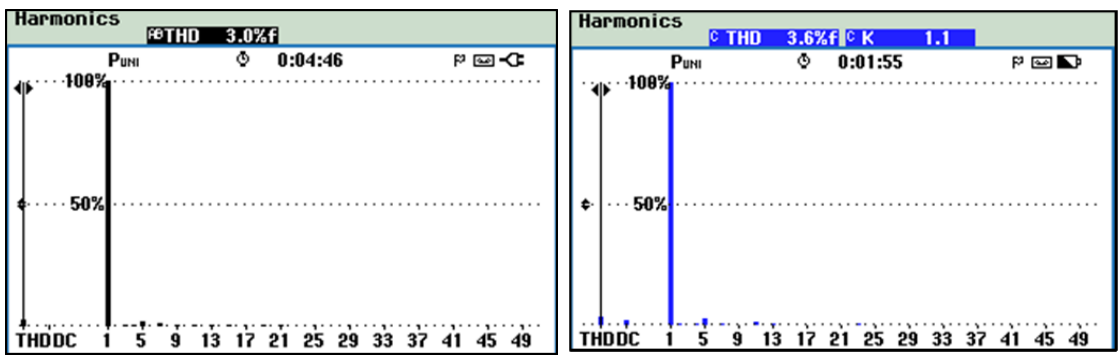
(a)

(b)



(c)

(d)



(e)

(f)

Figure 4.12: Hardware results of (a) Input line-to-line AC voltages (v_{L-L}), (b) Input phase currents, (c) Input voltage and current, (d) DC-link voltage, (e) Input voltage frequency spectrum and (f) Input current frequency spectrum for the Vienna type front-end PFC rectifier under steady state condition.

Figure 4.12(a) & (b) shows the input line-to-line voltages and phase currents respectively. The voltage and current results are shown in the Figure 4.12(c) is in-phase with each other and the Figure 4.12(d) shows the DC-link voltage. The Figure 4.12(e) & (f) shows the frequency spectrum of voltage and current having THD of 3.0% and 3.6% respectively under reduced load rating which is well within the IEEE standard.

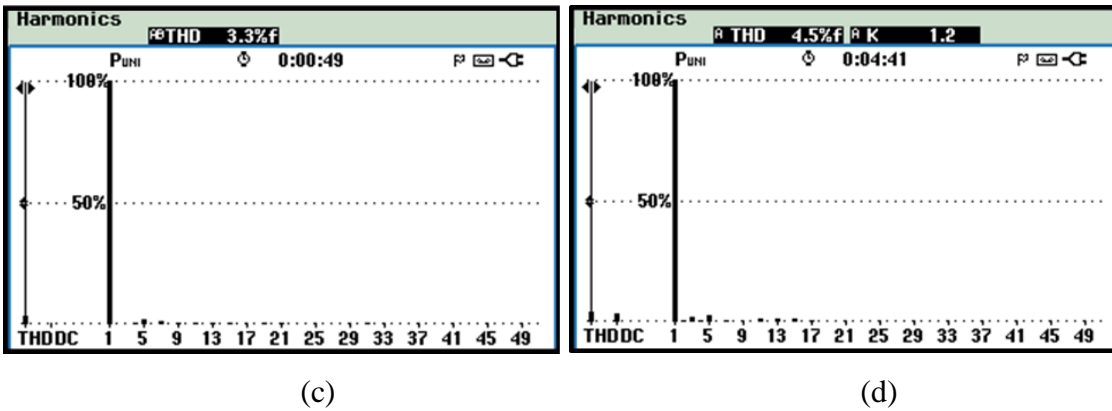
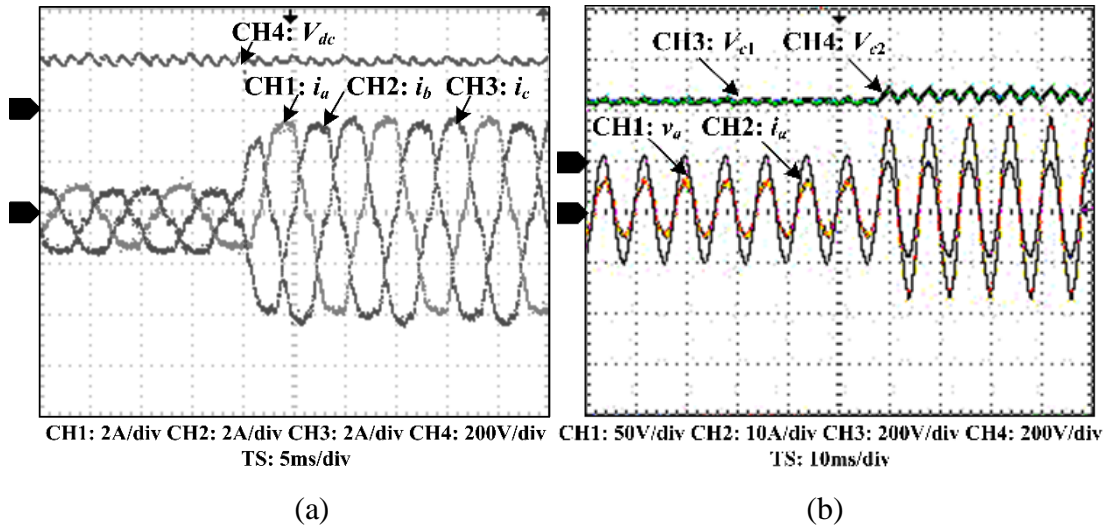


Figure 4.13: Hardware results of (a) Input three-phase currents with DC-link voltage, (b) Input phase voltage (v_a), phase current (i_a) with DC-link voltages (c) Input voltage frequency spectrum and (d) Input current frequency spectrum for the Vienna type front-end PFC rectifier under dynamic load condition.

Under the same aforementioned condition, the system response is captured as in case of dynamic condition (load change). Figure 4.13(a) shows the three-phase input current with DC-link voltage of the front-end AC-DC converter under load change. As seen from the Figure 4.13(b), a small DC-link voltage deviation happens during load change and returns to its reference value quickly without any overshoot. This demonstrates a good dynamic behavior of the proposed system in addition to that the harmonic content of voltage and current THD is 3.3% and 4.5% respectively as shown in Figure 4.13(c) and (d) which is under controllable limits of IEEE standards.

4.4 THREE-PHASE BOOST TYPE DELTA CONNECTED AC-DC CONVERTER

In this section with the same concept of power quality improvement, the boost type Delta connected AC-DC converter with voltage sensorless control technique is presented. The main focus is given to make the system with less control effort and improved power quality performance. The unity PF is achieved at the input side using the converter as shown in Figure 4.14. The configuration is designated by a Delta connection of four-quadrant switch rectifier. Wherein, the Delta connected semiconductor switches are utilized as an active current injection circuit.

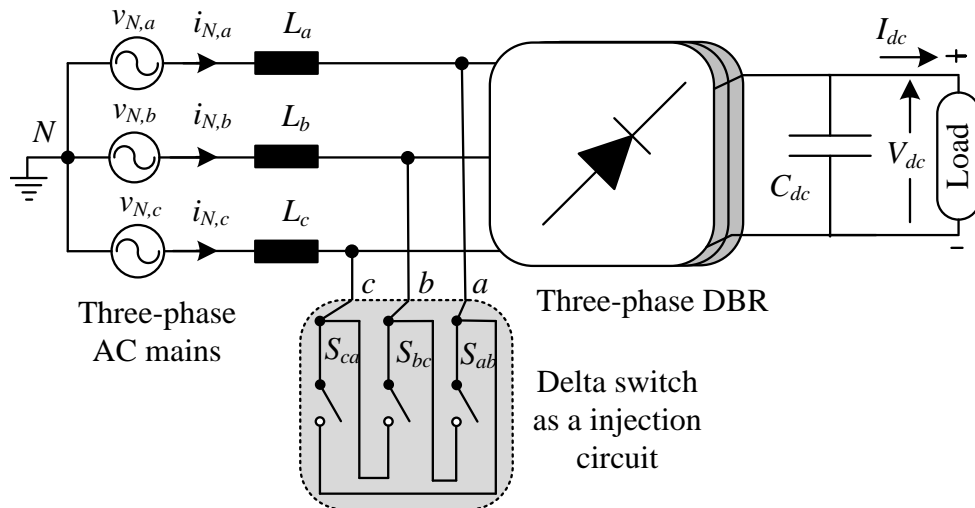


Figure 4.14: Schematic diagram of front-end Delta switch rectifier as PFC rectifier.

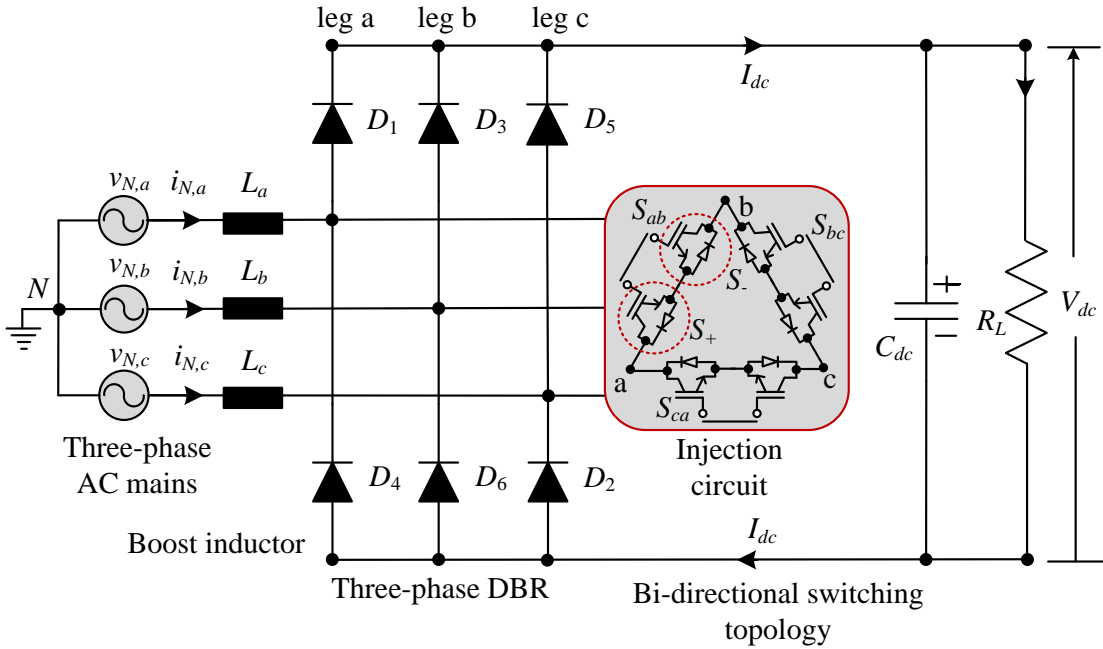


Figure 4.15: Schematic diagram of front-end Delta switch AC-DC converter with detailed circuit configuration.

4.4.1 Design, analysis and control technique of the Delta type front-end AC-DC converter

In this section, firstly the analysis of the front-end converter is discussed. Further, the proposed voltage sensorless control technique and loss calculations are presented in detail.

4.4.1.1 Analysis and design of the Dela type front-end AC-DC converter

In Figure 4.15. the four quadrant switches are allowed to manage the AC side current formation by applying PWM technique, thereby a sinusoidal phase current waveform proportional to the mains voltage can be attained. Because of high current loading an active current injection network is most preferable for high power industrial applications. Furthermore, the proposed method works satisfactorily even in case of single-phase failures, provided the DBR at the inputs are replaced by three-phase thyristor bridge rectifiers. During single phasing, the thyristor switches are operated with the available two phases thereby continues to operate in single-phase mode. Both the front-end DBR and

Delta switch topologies use equal number of switches and free-wheeling diodes (fast recovery diodes). Here the commutation of front-end DBR happens with respect to the switching frequency and hence it is an active PFC rectifier.

The input mains formation of the proposed rectifier bridge-leg depends on the direction of the phase current $i_{N,a}$ and the switching states of semiconductor switches. This does not represent a limitation since current $i_{N,a}$ is in-phase with the mains voltage $v_{N,a}$. Without considering the voltage drop across input inductor, the current equation for phase 'a' is given as

$$i_{N,a} = G * v_{N,a} \quad (4.35)$$

where G is the conductance and $v_{N,a}$ always has the same polarity. The input phases are always connected to the output voltage either to positive or negative terminal except for a synchronous switch ON of all four-quadrant switches ($S_{ab}=S_{bc}=S_{ca}=1$). The output voltage has to be chosen such that it should be greater than input line-to-line rms voltage as given in (4.36),

$$V_{dc} > \sqrt{2} v_{ab,rms} \quad (4.36)$$

The control range of the Delta switch rectifier allows the evolution of current phase displacements at an angular interval of -30° and $+30^\circ$.

$$\phi = (-30^\circ, +30^\circ) \quad (4.37)$$

where ϕ is displacement angle. The conduction states of the Delta type AC-DC converter are allowed up to 60° interval due to symmetry in the input AC mains. The effectively adjustable line-to-line voltage referral values are given in (4.38).

$$\begin{aligned} v_{ab} &= v_{N,a} - v_{N,b} \\ v_{bc} &= v_{N,b} - v_{N,c} \\ v_{ca} &= v_{N,c} - v_{N,a} \end{aligned} \quad (4.38)$$

The control of power semiconductor switches used in the Delta type AC-DC converter can be analysed for 60° sector of the mains period. Hence, the input current quality has been

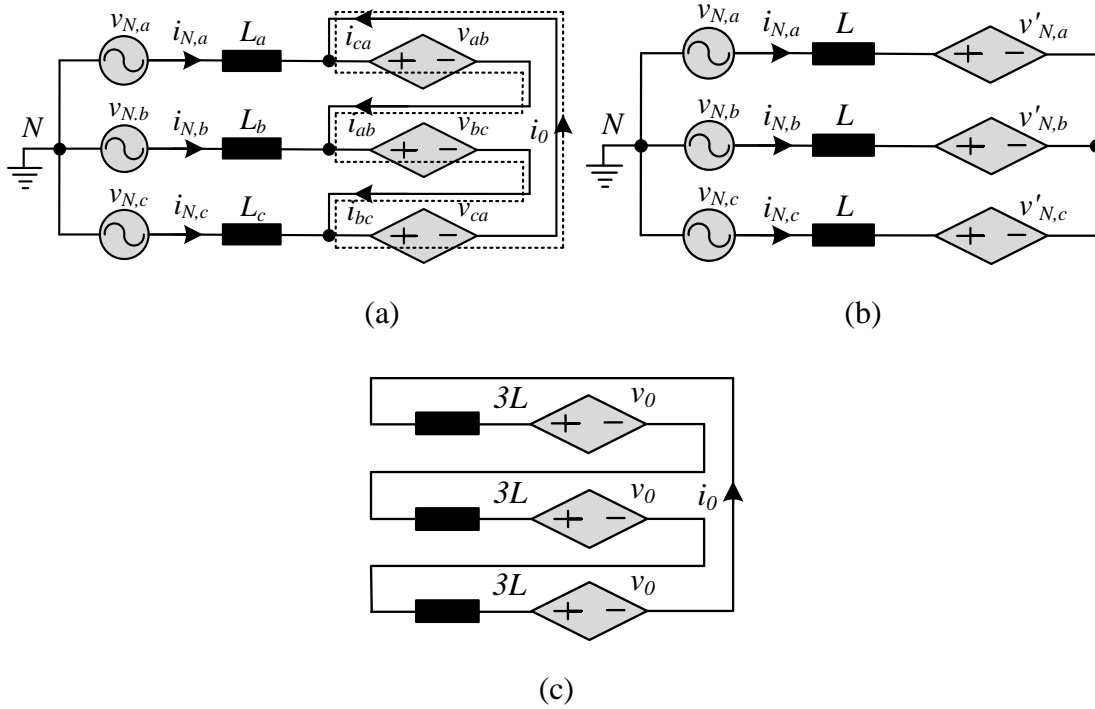


Figure 4.16: Equivalent circuit of (a) AC side part of Delta rectifier. (b) Delta switch rectifier being equivalent to star network. (c) Delta switch rectifier for calculating zero-sequence component i_0 .

improved for the complete control period and causes current malformation at the switching instants.

In order to analyze the Delta rectifier more convenient and easier, it is transformed into equivalent star network as shown in Figure 4.16(a) and (b). The formation of the input voltage is greatly depending on sign of line-to-line current i_{ij} ($ij=ab, bc, ca$) and switching states of power semiconductor S_{ij} .

$$v_{ij} = \text{sign}(i_{ij})(1 - S_{ij})v_{dc} \quad (4.39)$$

The input line-to-line voltage v_{ij} contains zero sequence components, which is termed as circulating component or common mode component of the input voltages and it is given as

$$v_0 = \frac{1}{3}(v_{ab} + v_{bc} + v_{ca}) \quad (4.40)$$

These voltage causes zero sequence current i_0 , add to the line-to-line current and it is given by,

$$i_{ij} = i'_{ij} + i_0 \quad (4.41)$$

These zero-sequence current i_0 (common mode component at the switching frequency) circulates inside the delta switch rectifier as shown in Figure 4.16(c) and it does not contribute for the formation of input phase currents and it is given by,

$$i_0 = \frac{1}{3}(i_{ab} + i_{bc} + i_{ca}) \quad (4.42)$$

The input phase current formation for the phase 'a' is given by,

$$\begin{aligned} i_{N,a} &= i_{ab} - i_{ca} \\ &= (i'_{ab} + i_0) - (i'_{ca} + i_0) \\ &= i'_{ab} - i'_{ca} \end{aligned} \quad (4.43)$$

The input line-to-line voltage of the Delta type AC-DC converter is obtained after subtracting the zero-sequence voltage from the input line-to-line voltage of the system is given by,

$$v'_{ij} = v_{ij} - v_0 \quad (4.44)$$

The corresponding phase voltages are given by,

$$\begin{aligned} v'_{N,a} &= \frac{1}{3}(v'_{ab} - v'_{ca}) \\ v'_{N,b} &= \frac{1}{3}(v'_{bc} - v'_{ab}) \\ v'_{N,c} &= \frac{1}{3}(v'_{ca} - v'_{bc}) \end{aligned} \quad (4.45)$$

The above analysis is carried out for an equivalent star network and in order to make the equal impedances of Delta and equivalent star network, the value of the input boost inductance is reduced by a factor of 3 and it is given by,

$$L_{star} = \frac{1}{3}L_{delta} \quad (4.46)$$

The above relationship indicates that the equivalent star network requires an inductance of $1/3^{\text{rd}}$ of Delta network inductance. In other words, the Delta rectifier requires an input boost inductance of 3 times higher than the star network inductance. However, the

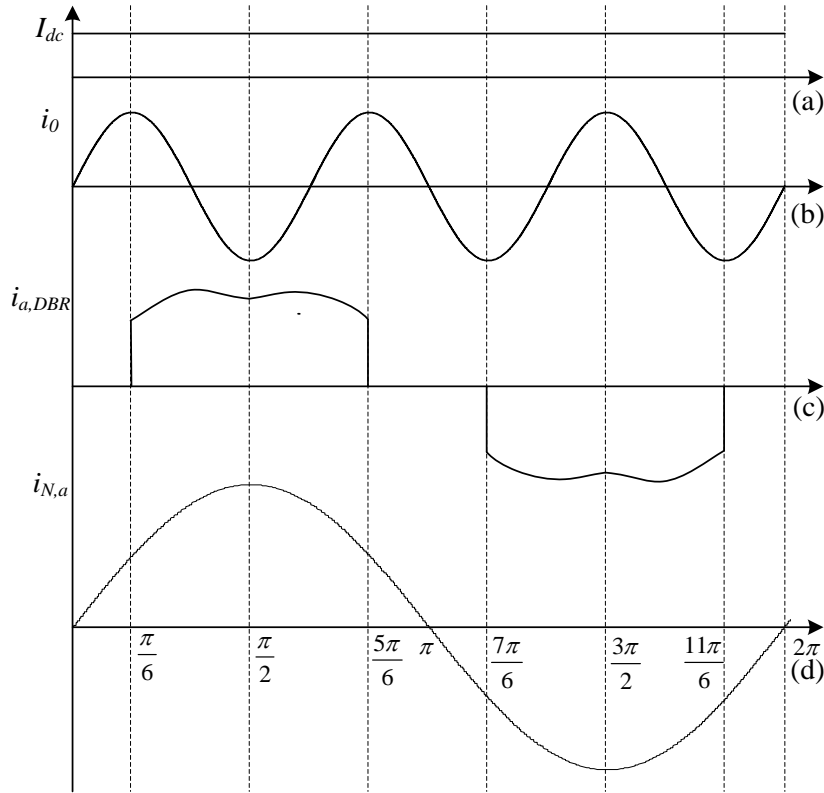


Figure 4.17: Theoretical waveform for the construction of the input current, $i_{N,a}$ (a) Converter output current, I_{dc} . (b) Third harmonic circulating current, i_0 . (c) Input current of DBR phase leg a, $i_{a,DBR}$. (d) Input phase current, $i_{N,a}$.

amplitude of the Delta rectifier line-to-line current is reduced by a factor $(1/\sqrt{3})$ and hence the volume of the inductor is same in both the cases.

The input current ' $i_{N,a}$ ' analysis of the Dela type front-end AC-DC converter and the principles of harmonic current cancellation by active injection circuit is depicted in Figure 4.17 and it shows the construction of the input line current $i_{N,a}$ in each mode of the converter operation. Figure 4.17(a) shows the load current, I_{dc} which is constant. The frequency of the zero-sequence current is three times the source frequency and its magnitude can be one-sixth of the line-to-line current fundamental as shown in Figure 4.17(b). The modified DBR input current is given in Figure 4.17(c). The interaction between the injected current and DBR current shapes the input current as sinusoidal in

shape as shown in Figure 4.17(d). Consequently, the quality of input phase current is improved.

4.4.1.2 Voltage sensorless control and component stresses calculation

A. Voltage sensorless control technique

The current injection technique and its control presented in (Greul et al. 2006; Hartmann et al. 2009, 2012; Miniböck and Kolar 2005) is modified and applied to the Delta type AC-DC converter. The input voltage sensorless control technique is depicted in Figure 4.18. Without measuring the input line-to-line voltage, the driving signal is generated with the help of output voltage signal and input phase current signals. The switching frequency triangular carrier wave is preferred for the pulse generation. The magnitude of the triangular signal is multiplied with the output voltage information for smooth control. The input phase current is directly compared with the triangular signal thereby operates the proposed Delta switch rectifier. This results in the switching harmonics of input currents that are multiples of twice the switching frequency.

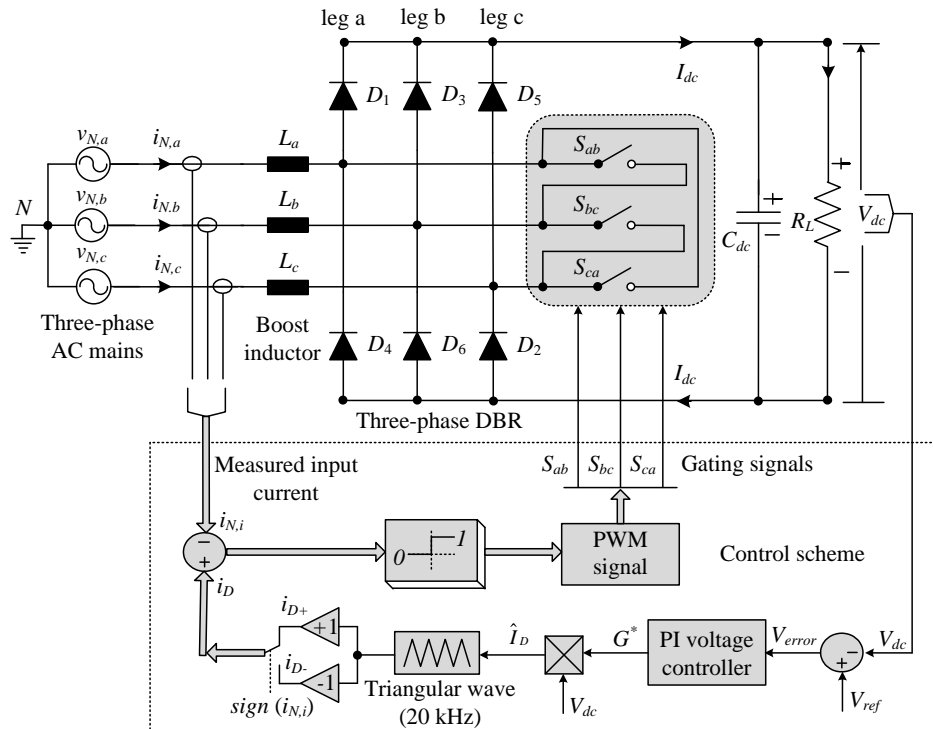
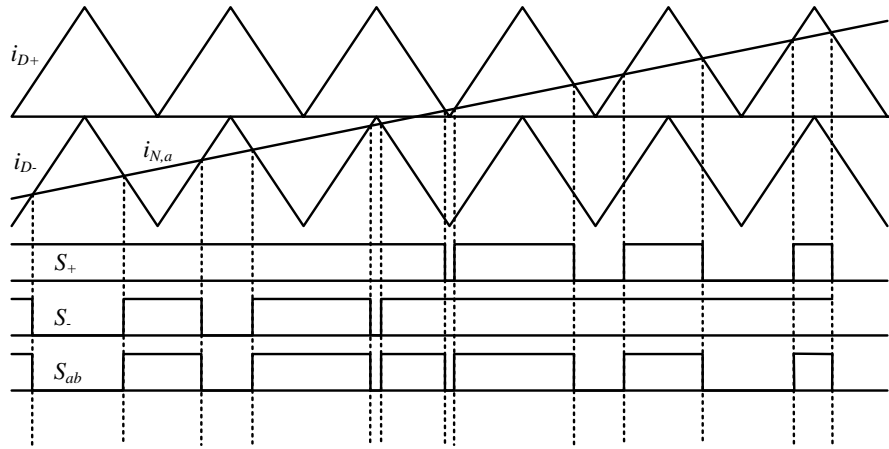
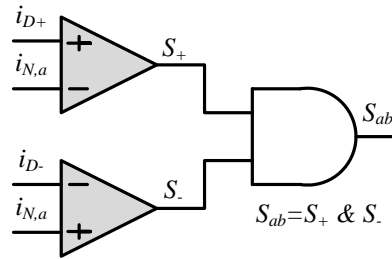


Figure 4.18: Control scheme for the Delta type front-end AC-DC converter.



(a)



(b)

Figure 4.19: (a) Generation of switching functions for the phase ‘a’ of Delta switch rectifier. (b) Combinational logic circuit used to generate the PWM pulse.

Moreover, the sign of the input voltage information is not required for smooth control of input currents results in low realization effort of the proposed input voltage sensorless control technique. The triangular carrier signal \hat{I}_D , is shifted by 180° in case of negative input phase currents ($sign(i_N)$) thereby the input current ripple and size of boost inductor is reduced. The single triangular carrier signal i_D is generated and easily converted into positive and negative carrier signals with adjustable amplitude \hat{I}_D . These positive and negative signals are synchronized and in-phase with each other. These signals i_{D+} and i_{D-} are compared with the measured input phase currents using comparators as shown in Figure 4.19(a). A simple combinational logic circuit generates the PWM pulses for S_{ab} that depends on the sign of the comparison as shown in Figure 4.19(b). This ensures the operation of the Delta type front-end AC-DC converter without detection of sign of the

input voltage results in reliable and robust operation even in unbalanced mains conditions. Similarly, the PWM pulses for S_{bc} and S_{ca} are generated using $i_{N,b}$ and $i_{N,c}$ respectively.

For the CCM, the average value of the voltage across the power semiconductor switches S_+ and S_- shows proportional relationship with the average current. Hence, the voltage across the power semiconductor switches S_+ and S_- increases until it balances the main voltage is given using the relationship with the duty ratio (D) and output voltage (V_{dc}) as follows,

$$|v_N| = V_{S,avg} = D \cdot V_{dc} = \frac{\hat{i}_N}{\hat{I}_D} V_{dc} \quad (4.47)$$

where, $V_{S,avg}$ is the average value of voltage across the power semiconductor switches S_+ and S_- .

From (4.47), the ohmic behavior of the Delta type AC-DC converter is confirmed which is validated by the following relationship.

$$|i_N| = \frac{\hat{I}_D}{V_{dc}} |v_N| \quad (4.48)$$

$$G^* = \frac{\hat{I}_D}{V_{dc}} \quad (4.49)$$

where G^* is the reference value of conductance which can be defined by the ratio of amplitude of carrier signals to the amplitude of output voltage signal. The non-ideality in the power circuit, PWM signals and gate driver circuits greatly influences the quality of input current. The input voltage sensorless control technique compares the actual and reference current thereby reduces the non-ideality and improves the input current quality. Moreover, the digital implementation is easy with this control technique.

B. Component stresses calculation

The ON-state losses of the components used in the Delta type AC-DC converter topology are determined by the average and rms values of voltage and current. The following

analytical approximations are derived which can be used for dimensioning the components. The following assumptions are made to derive the analytical expressions:

1. Ohmic fundamental mains behavior.
2. A pure sinusoidal phase current shape.
3. Linear inductance of the boost inductors (the value of boost inductance is not dependent on the input current level).
4. No low frequency voltage drop across the boost inductor;
5. A constant switching frequency.

a) *Bi-directional switches*: The bi-directional switches used in the proposed AC-DC converter topology consists of two IGBT based switches with anti-parallel diodes. The average value of the current through the semiconductors are not zero, although the entire average value of the current through the bi-directional switch is zero (for a full line frequency fundamental period). The modulation index is defined as,

$$M = \frac{\sqrt{3}\hat{v}_N}{V_{dc}} \quad (4.50)$$

The average and rms currents through the bidirectional switches are given by,

$$I_{S,avg} = \hat{I}_N \left(\frac{1}{2\pi} - \frac{M}{4\sqrt{3}} \right) \quad (4.51)$$

$$I_{S,rms} = \hat{I}_N \sqrt{\left(\frac{1}{6} - \frac{\sqrt{3}}{8\pi} \right) - \frac{M}{2\sqrt{3}\pi}} \quad (4.52)$$

b) *Free-wheeling diodes*: The average and rms currents stresses on the free-wheeling diodes are,

$$I_{FWD,avg} = \hat{I}_N \left(\frac{M}{2\sqrt{3}} \right) \quad (4.53)$$

$$I_{FWD,rms} = \hat{I}_N \left(\frac{2}{\sqrt[4]{27}} \right) \sqrt{\frac{M}{\sqrt{3}\pi}} \quad (4.54)$$

c) *Main diodes*: The average and rms currents stresses on the main diodes, D_m are,

$$I_{D_m,avg} = \hat{I}_N \left(\frac{M}{2\sqrt{3}} \right) \quad (4.55)$$

$$I_{D_m,rms} = \hat{I}_N \sqrt{\frac{M(5+2\sqrt{3})}{12\pi}} \quad (4.56)$$

d) *Output capacitor*: The rms current stress on the output capacitor for a ripple free load current I_{dc} is calculated using,

$$I_{C_{dc},rms} = \sqrt{I_{S,rms}^2 - I_{S,avg}^2} \quad (4.57)$$

$$I_{C_{dc},rms} = \hat{I}_N \sqrt{\frac{5M}{2\pi} - \frac{3M^2}{4}}$$

e) *Boost inductor*: The value of boost inductance greatly depends on the amplitude of ripple current. The maximum amplitude of the ripple current occurs at the point where semiconductor switches have equal duty ratio. Thus, the ripple current is given by,

$$\Delta i_{L,ripple} = \frac{V_{dc}}{\frac{3}{2} L f_s} \frac{\sqrt{3}}{2} M \left(1 - \frac{\sqrt{3}}{2} \right) \quad (4.58)$$

The ripple current is limited to $\Delta i_{L,ripple} = k \hat{I}_N$. Thus, the boost inductance is given by,

$$L = \frac{V_{dc}}{k \hat{I}_N f_s} \frac{M}{\sqrt{3}} \left(1 - \frac{\sqrt{3}}{2} M \right) \quad (4.59)$$

The value of k and M determines the inductance value.

f) *Third harmonic content*: Third harmonic line-to-line currents (zero sequence component) reduces the peak value of the power component currents, which can be considered as a circulating current in the Delta connected bi-directional switches. In this case, the third harmonic current magnitude is one-sixth of the fundamental component of the line-to-line current. The average and rms values of the main diode currents with third harmonic current injection is given by,

$$I_{D,avg} = \frac{19}{18} \frac{\hat{I}_N}{\sqrt{3}\pi} \quad (4.60)$$

$$I_{D,rms} = \frac{\sqrt{37}}{12} \frac{\hat{I}_N}{\sqrt{3}} \quad (4.61)$$

This average and rms values of the main diodes shows only minor differences with respect to the values calculated for pure sinusoidal current. The additional objective of the third harmonic current injection is that, the range of modulation is extended when compared to the conventional rectifier.

4.4.2 Results and discussion

Simulation is carried out to determine the performance of the Delta type front-end AC-DC converter using MATLAB/Simulink and the results are shown in Figure 4.20. The parameters used for the simulation are given in Appendix B. The simulated results shown in Figure 4.20 are input phase voltages, input phase currents, voltage and current per phase, DC-link voltage and DC-link current under varying load conditions. The per phase voltage and current are in-phase with each other which ensures unity PF operation of the proposed converter.

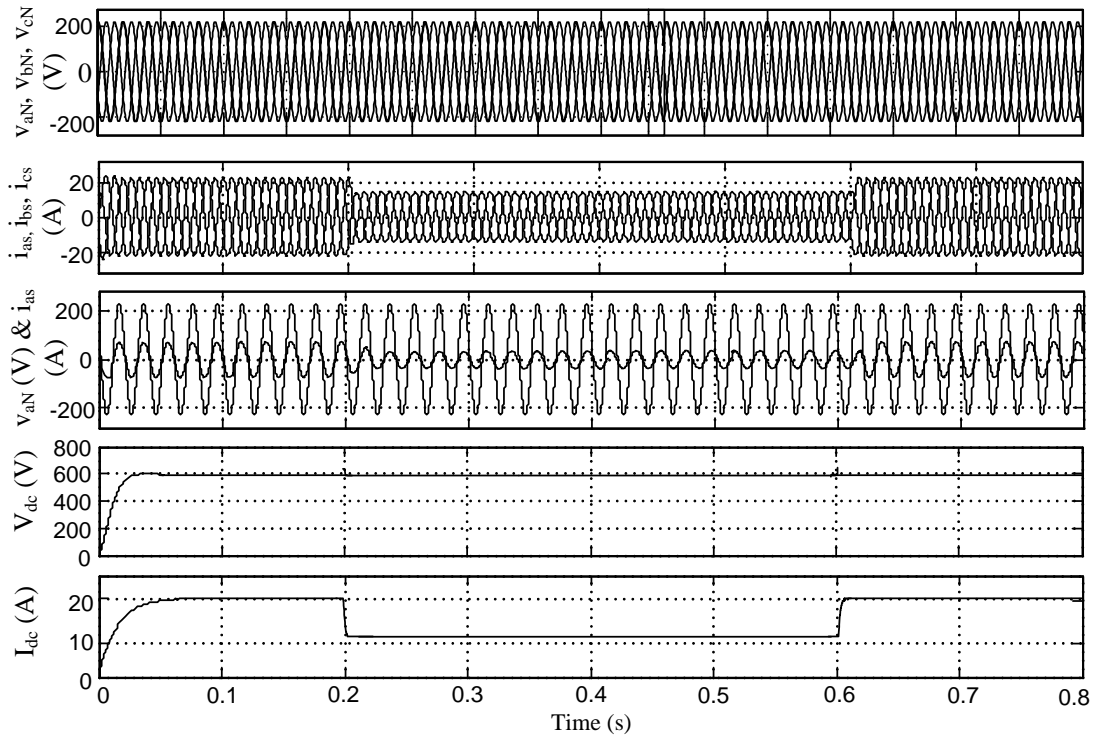
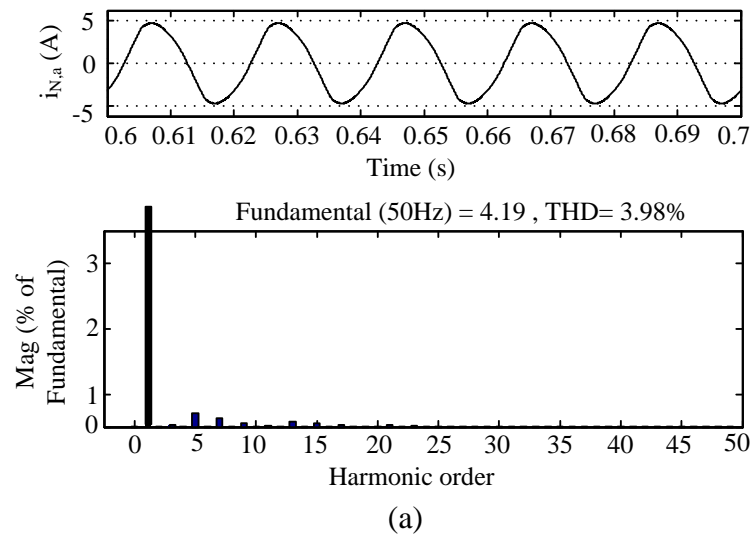
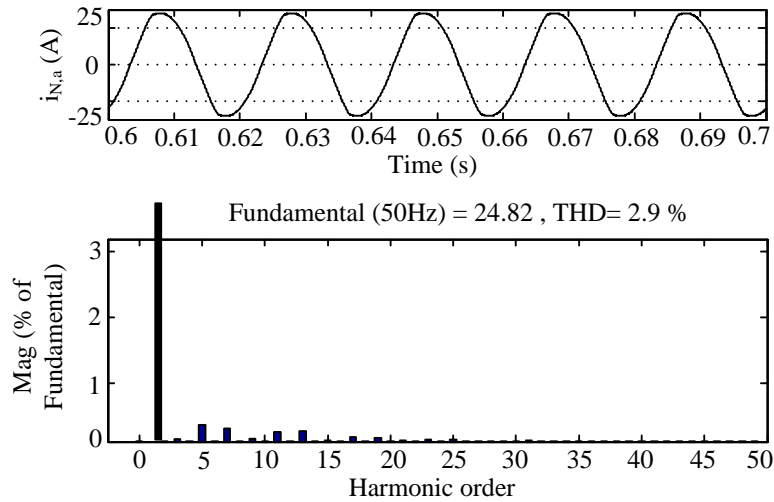


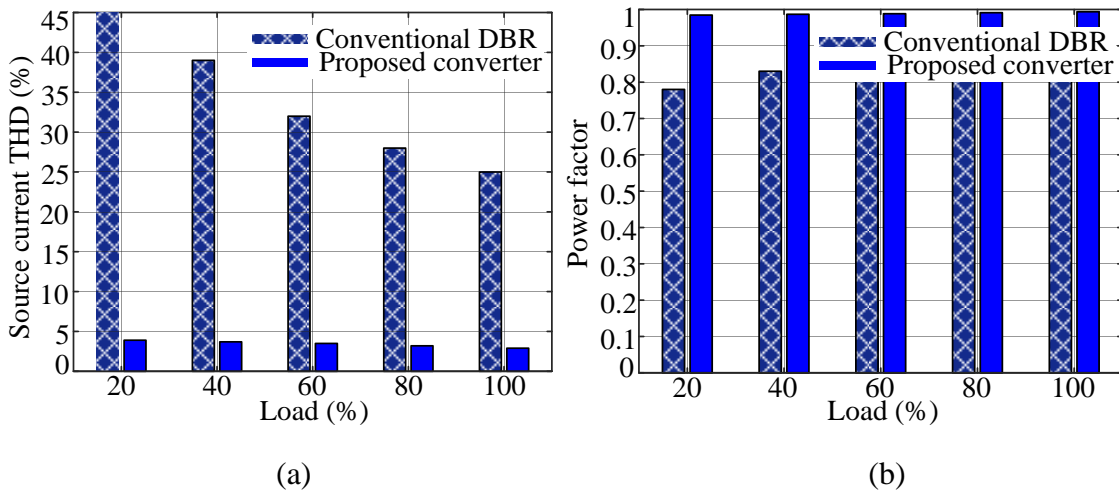
Figure 4.20: Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the Delta type front-end converter under load variations.





(b)

Figure 4.21: Frequency spectrum of input line current $i_{N,a}$ at (a) LL condition (20%).
(b) FL condition (100%).



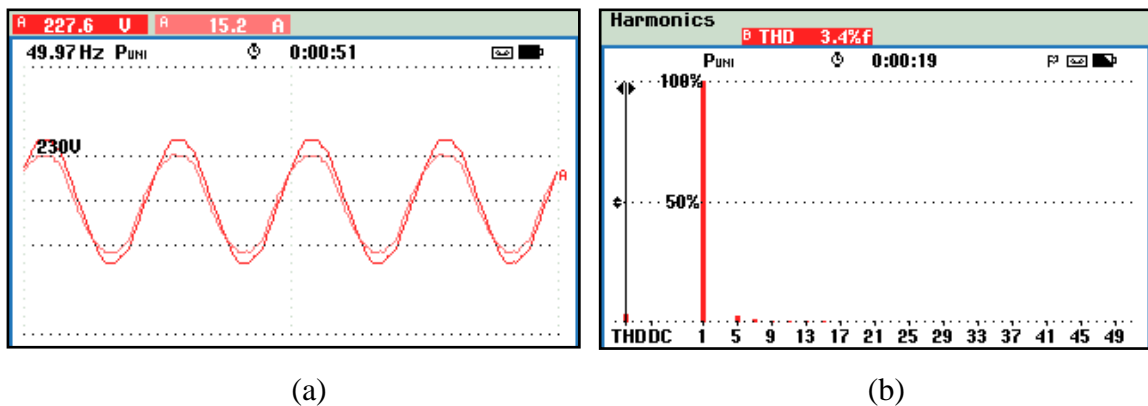
(a)

(b)

Figure 4.22: Comparison of power quality indices with varying load of front-end AC-DC converter with conventional 6-pulse DBR. (a) Variation of THD of input current with load and (b) Variation of PF of input current with load.

Figure 4.21 shows the frequency spectrum of the Delta type front-end converter. From the frequency spectrum, a current THD of 3.98% and 2.9% is observed under LL and FL conditions respectively which is well within the IEEE standards. Figure 4.22(a) & (b) shows the comparison of input line current THD and PF of the Delta type front-end converter with that of conventional 6-pulse DBR for varying load conditions. It is inferred from the Figure 4.22(a) and (b) that the proposed converter yields less THD and almost unity PF respectively.

A laboratory prototype is developed to demonstrate the operation of the Delta type front-end converter and the hardware results are taken at a reduced input voltage of 100 V as shown in Figure 4.23. The details of the laboratory prototype are given in Appendix B. Figure 4.23(a) shows the input voltage and current which are in-phase with each other and the corresponding input current THD shown in Figure 4.23(b). From Figure 4.23(b), it is observed that the Delta type front-end converter maintains the current THD of 3.4%. The output DC-link voltages and the injected voltage of Delta switch rectifier are shown in Figure 4.23(c) and (d) respectively. Figure 4.23(e) shows the injected voltage and current that are in-phase with each other.



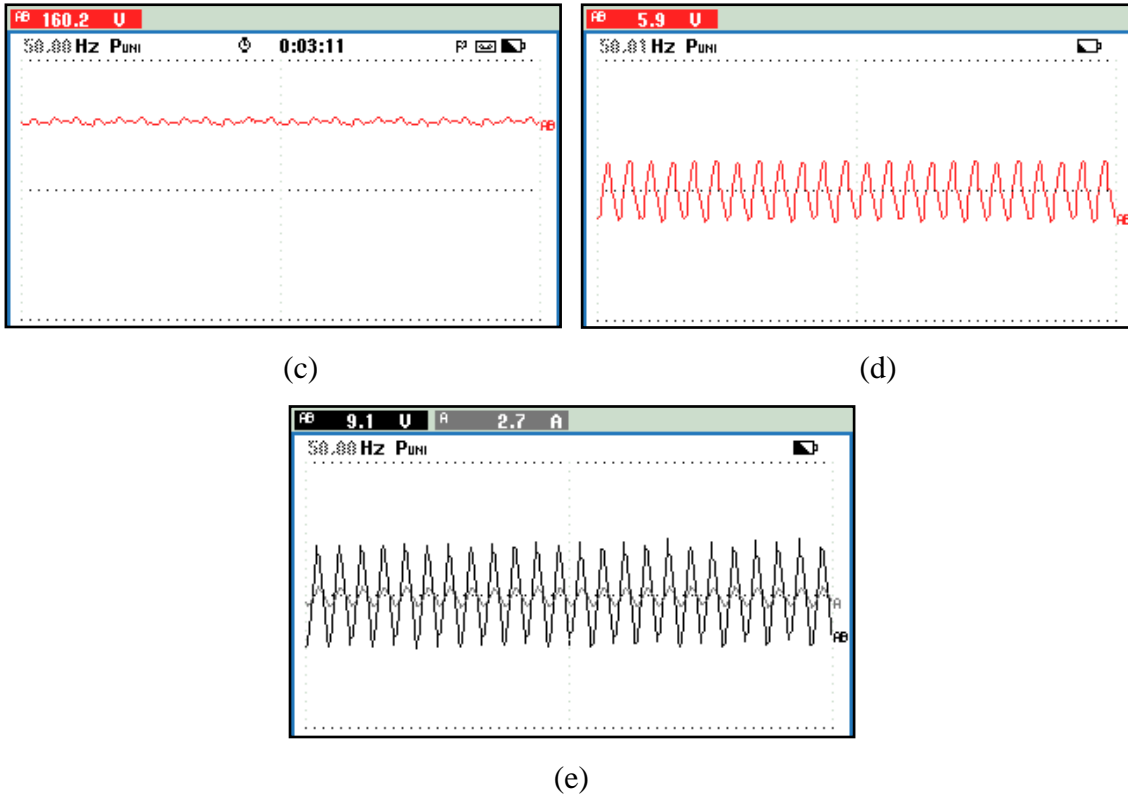
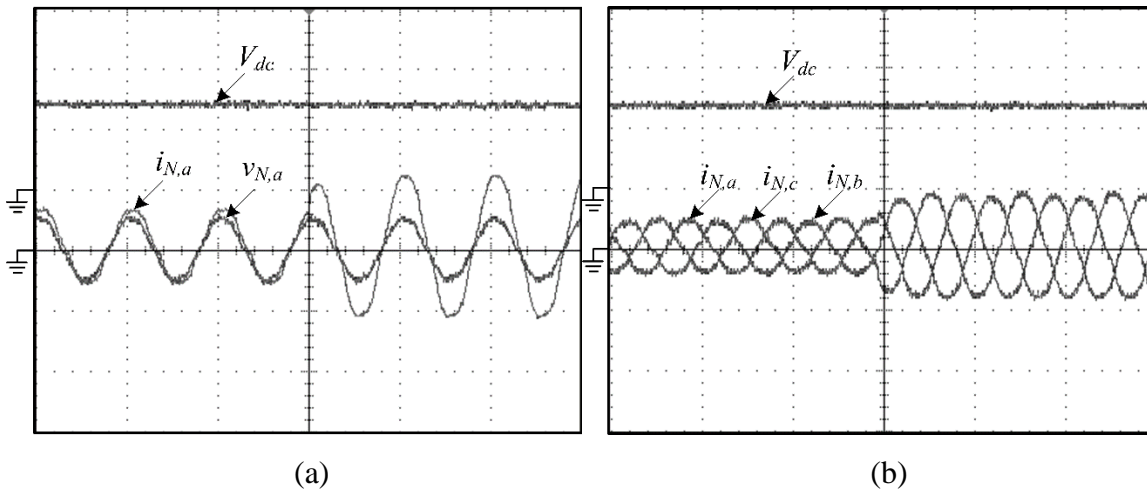


Figure 4.23: Hardware results of the Delta type AC-DC converter (a) Input voltage, $v_{N,a}$ and current, $i_{N,a}$ (b) Harmonic spectrum of input current, $i_{N,a}$ (c) Output DC-link voltages, V_{dc} (d) Injected voltage. (e) Injected voltage and current.



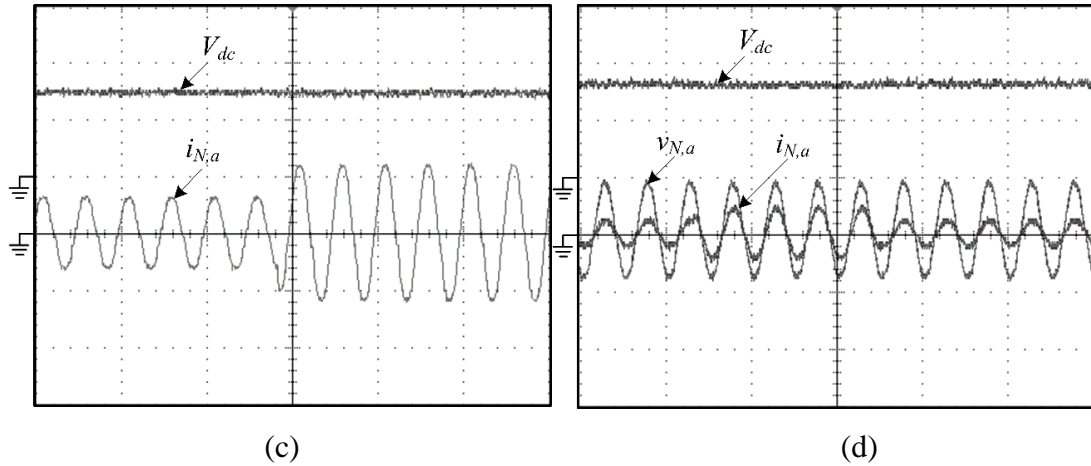


Figure 4.24: Hardware results of the Delta type AC-DC converter under varying load conditions (a) Input current $i_{N,a}$ (10 A/div) and voltage $v_{N,a}$ (100 V/div) with DC-link voltage V_{dc} (100 V/div); Time scale (20 ms/div). (b) Input three-phase currents (10 A/div) with output DC-link voltage V_{dc} (100 V/div); Time scale (20 ms/div). (c) Input current $i_{N,a}$ (10 A/div) and output DC-link voltage V_{dc} (100 V/div); Time scale (10 ms/div). (d) Input current $i_{N,a}$ (10 A/div) and voltage $v_{N,a}$ (100 V/div) with DC-link voltage V_{dc} (100 V/div); Time scale (10 ms/div).

The performance of the Delta type front-end AC-DC converter is also verified under load variations. Figure 4.24(a) shows the input phase voltage and current with DC-link voltages. Figure 4.24(b) shows the input three-phase currents and output DC-link voltage. Figure 4.24(c) shows the input phase current and DC-link voltage. The high-speed dynamic load variation under LL to FL and FL to LL is applied and the system performance is captured as shown in Figure 4.24(d). It is inferred from Figure 4.24(a)-(d) that, the voltage sensorless control logic is able to maintain DC-link voltage constant even under the varying load conditions and also maintains power quality parameters well within the IEEE and IEC standards without measuring input voltage information. The power quality indices such as DPF, DF and PF are obtained from the Delta type front-end AC-DC converter for varying load conditions and it is summarized in Table 4.4. It is inferred from the Table 4.4 that, the proposed system maintains THD of less than 4% and near unity PF during wide variation in load.

Table 4.4: Power quality indices for the Delta type front-end AC-DC converter under varying load conditions

Load (%)	v_{THD} (%)	i_{THD} (%)	DPF	DF	PF
20	1.2	3.9	0.9867	0.9981	0.9849
40	1.5	3.7	0.9883	0.9984	0.9868
60	2.3	3.5	0.9897	0.9987	0.9884
80	2.8	3.2	0.9919	0.9991	0.9913
100	3.1	2.9	0.9949	0.9989	0.9938

The Delta switch AC-DC converter results in the following advantages:

1. Third harmonic line-to-line currents (zero sequence components) reduces the peak value of the power component currents.
2. Due to the third harmonic current injection, the range of modulation is extended when compared to the conventional rectifier.
3. The input voltage sensorless control technique requires less computational involvement and improves the input current quality thereby reduces the current THD.
4. The operation of the Delta type front-end AC-DC converter without detection of sign of the input voltage results in reliable and robust operation in unbalanced mains conditions.
5. The volume of the input boost inductance is same as equivalent star network, since the line-to-line current is reduced by a factor of $1/\sqrt{3}$.
6. Low conduction loss, high efficiency and reliability.

4.5 COMPARATIVE STUDY

The superiority of the three-phase front-end AC-DC converters are validated by comparing the proposed method with available literature methods. There are many topologies available in the literature, but only some of them were considered for comparison as given in Table 4.5. In (Pejović and Janda 1999), the modulation and injection circuits are passive which has the input current THD of 7%-12% with efficiency of 91.4%. In (Kanaan et al. 2004; Vázquez et al. 2009), the modulation and injections circuits are active and yields input current THD of 11% and 5% with the efficiency of 97% and 90%. Further, (Greul et al. 2006) has only active modulation circuit and (Hartmann et al. 2012) has only active injection circuit with efficiency of 97.2% and 94.6% respectively. In the Vienna converter, without any injection circuit and only with active modulation circuit results in input current THD of 1.5% and efficiency of 98.6%. In the Delta converter, without any modulation circuit and only with active injection circuit results in input current THD of 2.9% and efficiency of 98%. Here, the experimental efficiency is measured with the help of power quality analyzer. It is evident that, the three-phase front-end AC-DC converters with voltage sensorless control technique offers acceptable current THD and better efficiency when compared to other topologies reported in the Table 4.5. The improvement in efficiency is due to the lesser voltage/current stress on the semiconductor switches and diodes. Moreover, the proposed control technique results in lesser number of sensors and hence the proposed system is a logical solution for high power applications.

Table 4.5: Comparison of the three-phase front-end AC-DC converters with some of the available systems in the literature

Topologies	Modulation circuit	Injection circuit	No. of passive components	No. of active components	Switching frequency	No. of Sensors	Current THD	Efficiency
[1]	Passive	Passive (star-delta transformer)	7	Nil	-	-	7%-12%	91.4%
[2]	Active	Active	6	5	100 kHz	Current-2	11.0%	97.0%
[3]	Active	Active	7	5	50 kHz	Voltage-3 Current-2	5.00%	90.0%
[4]	Active	-	18	6	50 kHz	Current-3	2.00%	97.2%
[5]	-	Active	6	6	72 kHz	Voltage-4 Current-3	2.30%	94.6%
Vienna converter	Active	-	6	3	20 kHz	Voltage-1 Current-3	1.50%	98.6%
Delta switch converter	-	Active	6	3	20 kHz	Voltage-1 Current-3	2.90%	98.0%

[1] (Pejović and Janda 1999)

[2] (Vázquez et al. 2009)

[3] (Kanaan et al. 2004)

[4] (Greul et al. 2006)

[5] (Hartmann et al. 2012)

4.6 CONCLUSION

This chapter has presented a detailed analysis and implementation of the active front-end AC-DC converters with voltage sensorless control technique for power quality improvement. The voltage sensorless control technique does not rely on any input voltage information, which results in reliable and robust operation and hence it requires less computational involvement. The system results in less THD at the input current and voltage and maintains PF close to unity. Also, the other power quality parameters such as DPF and DF are well within the IEEE standards. In order to increase the robustness of the front-end AC-DC converter, a hybrid improved power quality front-end AC-DC system is introduced the next chapter.

CHAPTER 5

POWER QUALITY IMPROVEMENT IN THREE-PHASE FRONT-END AC-DC CONVERTERS USING HYBRID TECHNIQUE

5.1 INTRODUCTION

In the previous chapter, power quality improvement using active techniques were presented. In this chapter, the power quality improvement is achieved using hybrid technique which is well applicable for medium and high-power applications. Unlike previous techniques, the hybrid technique comprises of active modulation and passive injection circuits and thereby increases the robustness of the front-end AC-DC converter system. Further, the hybrid technique based front-end AC-DC converter system can be used for the retrofit applications wherein DBR is used as a front-end converter.

This chapter is organized as follows: The topological details with operating modes of the front-end AC-DC converter is described in detail, followed by the analysis of the modulation and injection circuits. Further, the simulation and experimental results pertaining to the front-end AC-DC converter is provided with a detailed comparative evaluation.

5.2 PROBLEM FORMULATION

The improvement in active front-end AC-DC converter system results in enhanced power quality parameters at the input AC mains. However, the semiconductor switches required for the topological implementation are high and also requires complex control techniques with accurate sensing effort. Further, high power applications require high power semiconductor switches and thereby increase the cost of the system. To overcome the above-said disadvantages, a combination of active modulation and passive injection

circuits is used for the power quality improvement. Hence the power handling capability of the circuit increases in addition to the system robustness.

5.3 THREE-PHASE HYBRID FRONT-END AC-DC CONVERTER

The three-phase front-end hybrid AC-DC converter is connected to the load for improving the input current quality is shown in Figure 5.1. The current injection technique and its control schemes presented in (Itoh and Ashida 2008; Kanaan et al. 2012; Mohan et al. 1993; Naik et al. 1995; Pitel et al. 1994; Saravana Prakash et al. 2017; Saravana Prakash P and Kalpana 2016) are modified and applied to the proposed converter. Here the zig-zag transformer is utilized as the passive current injection circuit. The active modulation circuit composes of 6-pulse DBR and three-level step-up boost DC-DC converter. The zig-zag transformer modifies the current in the DC-link to be $(i_{dc} + i_3)$ and $(i_{dc} - i_3)$ as indicated in Figure 5.1, wherein i_{dc} is the DC part of the current and i_3 is the third-harmonic modulation current flowing in the DC-link inductors. The neutral of zig-zag transformer carries the current i_{zN} , and the phase winding of the zig-zag transformer is connected to three-phase AC mains. Here a sinusoidal phase current waveform proportional to the mains voltage can be attained. Because of higher current loading, an active current modulation network is preferred for high power industrial application.

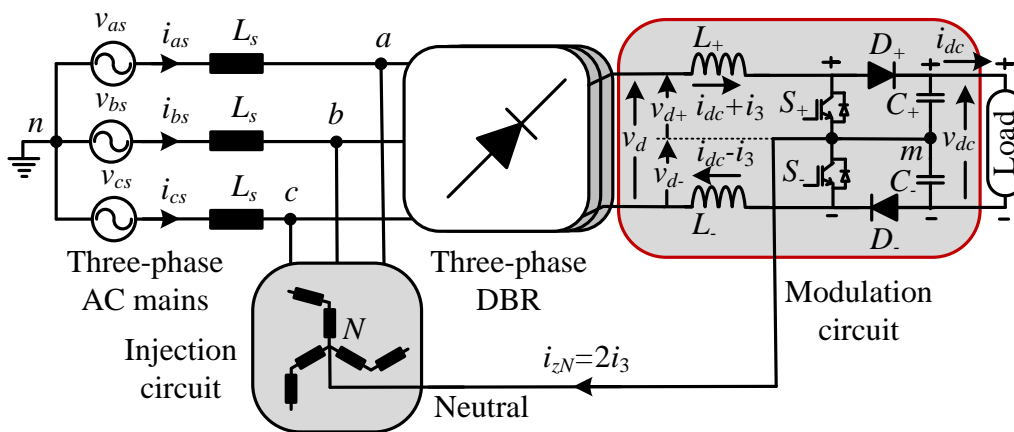


Figure 5.1: Schematic diagram of three-phase front-end hybrid AC-DC converter.

The operational range of the converter is selected in such a way that the output voltage (v_{dc}) must be greater than that of input line-to-line rms voltage, $v_{dc} = \sqrt{6} v_{ab,rms}$. The main advantage of this hybrid AC-DC converter is that the system can sustain to work on single-phase failure. During single-phasing, the system power level is reduced but still maintains the sinusoidal current shape in the other phases. This can be achieved by blocking the injection switches and maintains synchronous gating for S_+ and S_- . So that the system works as a single-phase PFC rectifier with the available AC mains.

5.3.1 Analysis and design of three-phase front-end AC-DC converter using hybrid technique

In this section, the analysis and design of both active modulation and passive injection circuit are presented in detail.

5.3.1.1 Analysis of front-end DBR with passive injection circuit

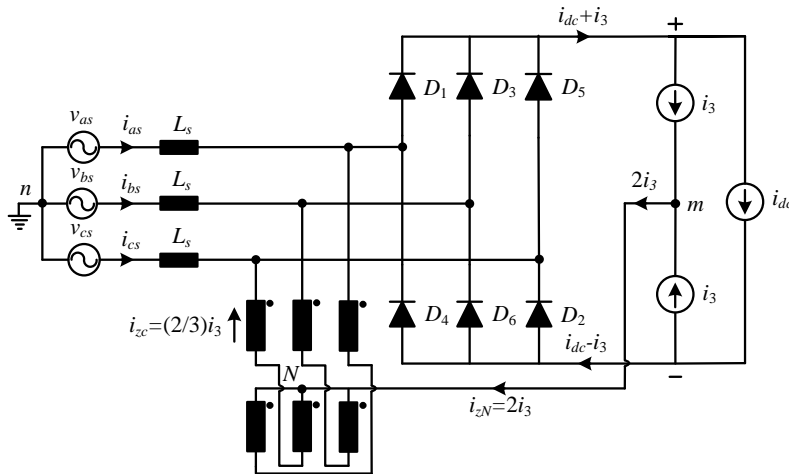
The input current analysis of the hybrid front-end AC-DC converter and the principles of harmonic current cancellation by third harmonic current injection are explained using Figure 5.2(a). The front-end DBR consists of upper positive group diodes (D_1, D_3, D_5) and lower negative group diodes (D_4, D_6, D_2). The input phase voltages namely v_{as}, v_{bs} and v_{cs} , determines conducting states of the DBR such that one of the upper positive diodes conducts when it is connected to the line with the highest of the phase voltages. Similarly, one of the lower negative diodes conducts when it is connected to the line with the lowest of the phase voltages. Depending on the diode conducting states, a line period is divided into six segments of 60° in phase angle, wherein a pair of diodes are in a conduction state. For convenience, the line period is considered from -30° to 330° .

The six modes of the hybrid front-end AC-DC converter with circulating third harmonic current is shown in Figure 5.2(b)-(g). When the output DC current is constant, and the source impedance of the power supply are equal in each phase, the third harmonic injection current ($i_{dc \pm i_3}$) is same. Under this condition, the input voltage v_d to the three-level boost converter having small magnitude variation and it is considered as constant for

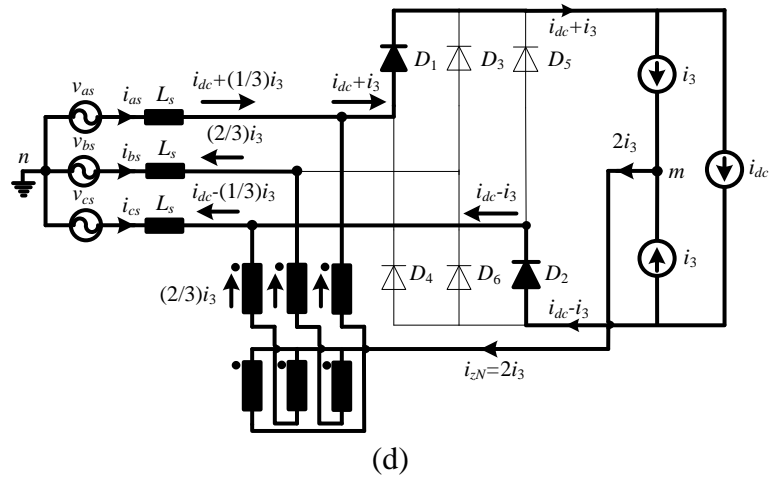
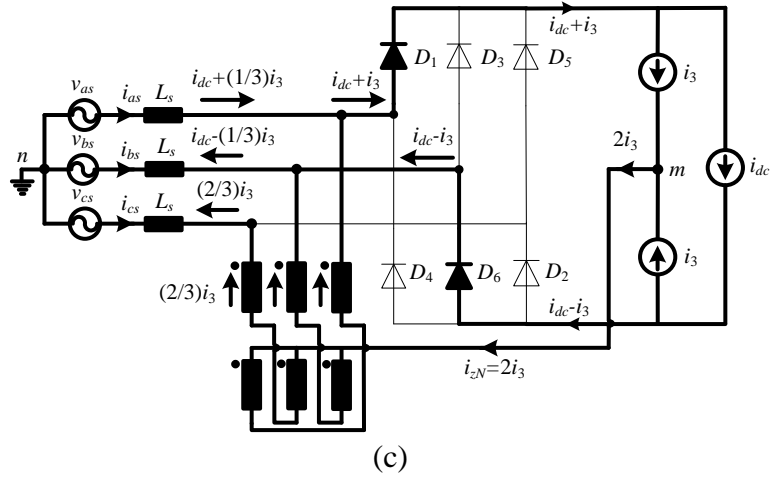
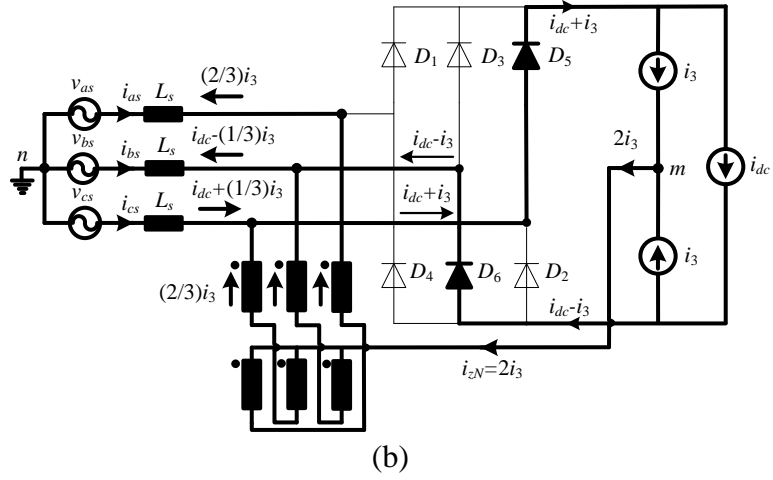
further analysis. The hybrid front-end AC-DC converter uses third harmonic current injection technique and hence the DC side of the rectifier can be represented as third harmonic current sources. Moreover, the analysis of the input currents and their harmonic properties can be performed easily by designing the converter model as current sources. Hence, ideal current sources are used instead of switching leg and the DC inductances. The input ports of the boost converters are modeled as current sources of value i_3 . The current sources assume the ripple of the third harmonic in the DC current. Moreover, currents of the sources are equal to the time average of the corresponding inductor current during the switching period. Further, the hybrid front-end AC-DC converter requires a finite value of source inductance for minimum distortion in the line current, and hence the source inductance is installed as part of the system. Due to this source inductance, the output DC current has a ripple free waveform. To facilitate the analysis, the following assumptions are made: The voltage drop of diodes are negligible, load current i_{dc} is continuous and constant in magnitude, switching losses are neglected and switching frequency is infinite thereby the DC inductance is zero. If i_{dc} is equal to i_{zN} , the resulting input current is given in (5.1)

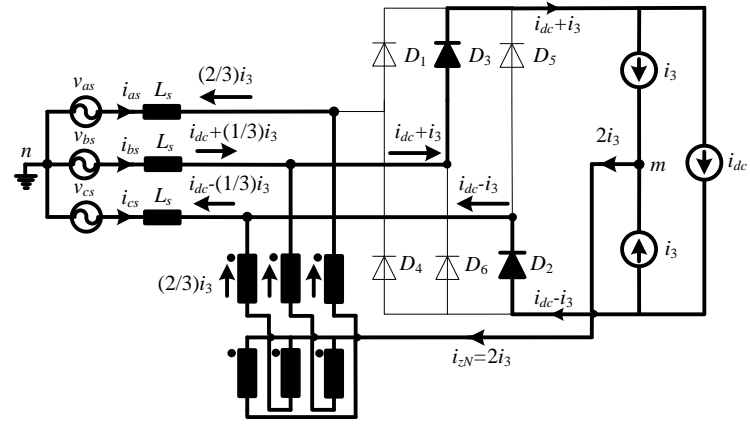
$$i_{as}(\omega t) = 1.1661i_{dc} \sin(\omega t) + 0.009i_{dc} \sin(5\omega t) + 0.01i_{dc} \sin(7\omega t) + 0.018i_{dc} \sin(11\omega t) - 0.0151i_{dc} \sin(13\omega t) + \dots \quad (5.1)$$

From (5.1), the magnitude of 5th, 7th, 11th and 13th order harmonics is less in the input line current i_{as} .

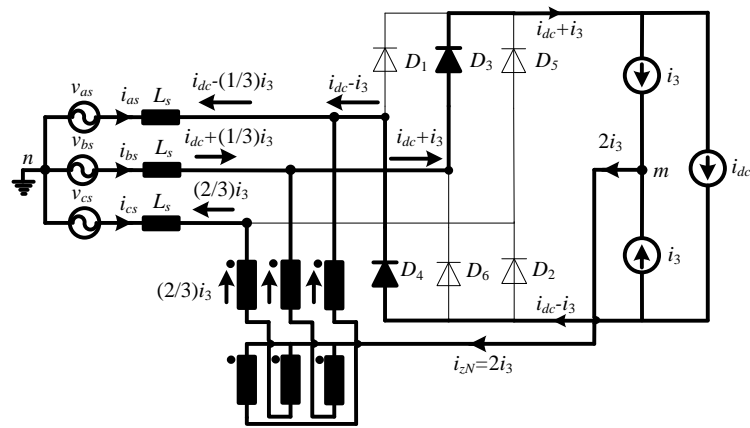


(a)

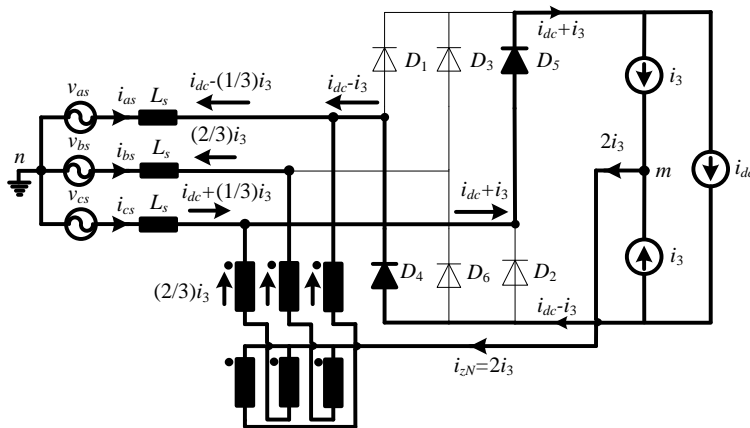




(e)



(f)



(g)

Figure 5.2: Equivalent circuit indicating the circulating third harmonic current for (a) The analysis of input line current (b) Conduction of D_5 and D_6 (c) Conduction of D_6 and D_1 (d) Conduction of D_1 and D_2 (e) Conduction of D_2 and D_3 (f) Conduction of D_3 and D_4 (g) Conduction of D_4 and D_5 .

Table 5.1: Diode conducting sequence and currents of the hybrid front-end converter

Conduction angle	-30° to 30°	30° to 90°	90° to 150°	150° to 210°	210° to 270°	270° to 330°
Upper diode	D_5	D_1	D_1	D_3	D_3	D_5
Lower diode	D_6	D_6	D_2	D_2	D_4	D_4
i_{D1}	0	$i_{dc}+i_3$	$i_{dc}+i_3$	0	0	0
i_{D2}	0	0	$i_{dc}-i_3$	$i_{dc}-i_3$	0	0
i_{D3}	0	0	0	$i_{dc}+i_3$	$i_{dc}+i_3$	0
i_{D4}	0	0	0	0	$i_{dc}-i_3$	$i_{dc}-i_3$
i_{D5}	$i_{dc}+i_3$	0	0	0	0	$i_{dc}+i_3$
i_{D6}	$i_{dc}-i_3$	$i_{dc}-i_3$	0	0	0	0
i_{zc}	$(2/3) i_3$	$(2/3) i_3$	$(2/3) i_3$	$(2/3) i_3$	$(2/3) i_3$	$(2/3) i_3$
i_{as}	$(2/3) i_3$	$i_{dc}+(1/3) i_3$	$i_{dc}+(1/3) i_3$	$(2/3) i_3$	$i_{dc}-(1/3) i_3$	$i_{dc}-(1/3) i_3$
i_{bs}	$i_{dc}-(1/3) i_3$	$i_{dc}-(1/3) i_3$	$(2/3) i_3$	$i_{dc}+(1/3) i_3$	$i_{dc}+(1/3) i_3$	$(2/3) i_3$
i_{cs}	$i_{dc}+(1/3) i_3$	$(2/3) i_3$	$i_{dc}-(1/3) i_3$	$i_{dc}-(1/3) i_3$	$(2/3) i_3$	$i_{dc}+(1/3) i_3$

The conducting diodes and currents of the converter are given in Table 5.1. The computation of input phase currents is performed based on the direction of the currents shown in Figure 5.2(b)-(g). From the diode conduction state analysis, it is evident that at any point of time only two diodes are in conduction and thereby equal amount of current flows in the branches of the zig-zag transformer.

Figure 5.3 shows the construction of the input line current i_{as} in each mode of converter operation. Figure 5.3(a) shows the load current which is constant, and the injected voltage, positive and negative bus voltages are given Figure 5.3(b). The frequency of the injected voltage is three times the source frequency, and its magnitude can be calculated from (5.5). The corresponding injected current through the zig-zag transformer is shown in Figure 5.3(c). The modified DBR input current is given in the Figure 5.3(d). The interaction between the injected current and DBR current shapes the input current as sinusoidal is shown in Figure 5.3(e).

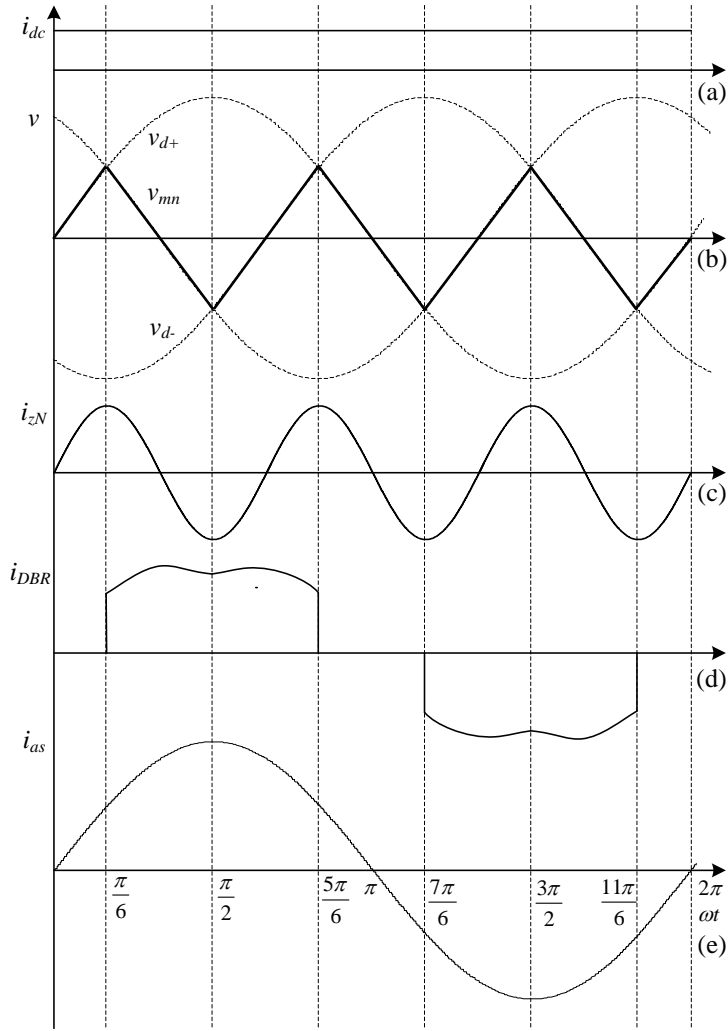


Figure 5.3: Theoretical waveforms for the construction of the input current, i_{as} (a) Converter output current, i_{dc} . (b) Converter output voltage (v_{d+} , v_{d-}) with injected voltage, v_{mn} . (c) Injected current, i_{zN} . (d) DBR input current i_{DBR} . (e) Input current, i_{as} .

The voltage across the capacitors are given by,

$$v_{+m} = \frac{v_{+-}}{2}; v_{mn} = v_{+n} - v_{+m}; v_{+-} = v_{+n} - v_{-n} \quad (5.2)$$

So, $v_{mn} = \frac{v_{+n} + v_{-n}}{2}$ and the Fourier expansion of the voltages v_{+n} and v_{-n} are expressed as

follows:

$$v_{+n} = \frac{3\sqrt{2}}{2\pi} v_{ab} \left[1 + \frac{1}{4} \sin(3\omega t) - \frac{2}{35} \sin(6\omega t) + \frac{1}{40} \sin(9\omega t) + \dots \right] \quad (5.3)$$

$$v_{-n} = \frac{-3\sqrt{2}}{2\pi} v_{ab} \left[1 + \frac{1}{4} \sin 3(\omega t + 60^\circ) - \frac{2}{35} \sin 6(\omega t + 60^\circ) + \frac{1}{40} \sin 9(\omega t + 60^\circ) + \dots \right] \quad (5.4)$$

The resultant voltage v_{mn} is given by,

$$v_{mn} = \frac{3\sqrt{2}}{8\pi} v_{ab} \sin(3\omega t) + \frac{3\sqrt{2}}{80\pi} v_{ab} \sin(9\omega t) + \dots \quad (5.5)$$

This voltage is also equal to v_{mN} . Since the zig-zag transformer is connected to the input terminals, the neutral point N is essentially of the same potential as the supply neutral n . From (5.5), the magnitude of the 9th harmonic is less which is only 10% of the 3rd harmonic component, wherein the magnitude of the 3rd harmonic current depends on the impedance of the zig-zag transformer. Since, the DC current is modulated at a third harmonic frequency, each current injection branch consists of series connected windings of the zig-zag transformer having inductance L_z tuned close to the third harmonic frequency. The impedance of the zig-zag transformer to the third harmonic current is zero. Hence, the injected current $2i_3$ is divided equally into the three windings of the zig-zag transformer and magnitude of $(2/3)i_3$ flows through each winding. The voltage across each winding of the zig-zag transformer is given by,

$$\begin{aligned} v_{aN} &= v_a - v_N = R_{az} i_{aN} + L_{az} \frac{di_{aN}}{dt} \\ v_{bN} &= v_b - v_N = R_{bz} i_{bN} + L_{bz} \frac{di_{bN}}{dt} \\ v_{cN} &= v_c - v_N = R_{cz} i_{cN} + L_{cz} \frac{di_{cN}}{dt} \end{aligned} \quad (5.6)$$

where, $v_a = v_{as} - (R_{az} i_{aN} + L_{az} \frac{di_{aN}}{dt})$ and $i_{aN} = i_{a1} - \frac{2}{3} i_3$;

$v_b = v_{bs} - (R_{bz} i_{bN} + L_{bz} \frac{di_{bN}}{dt})$ and $i_{bN} = i_{b1} - \frac{2}{3} i_3$;

$v_c = v_{cs} - (R_{cz} i_{cN} + L_{cz} \frac{di_{cN}}{dt})$ and $i_{cN} = i_{c1} - \frac{2}{3} i_3$

The currents i_{a1} , i_{b1} , and i_{c1} are the fundamental components flowing through respective branches of the zig-zag transformer. R_{az} , R_{bz} , R_{cz} and L_{az} , L_{bz} , L_{cz} are the resistance and inductance of the zig-zag transformer windings respectively.

The sum of the voltages is written as,

$$v_{aN} + v_{bN} + v_{cN} = -3v_N = -[R_z(2i_3) + L_z \frac{d(2i_3)}{dt}] \quad (5.7)$$

$$v_N = \frac{R_z}{3}(2i_3) + \frac{L_z}{3} \frac{d(2i_3)}{dt} \quad (5.8)$$

This shows that v_N is third harmonic voltage and it is expressed in polar form as,

$$\bar{v}_N = \frac{2}{3} \bar{z}_3 \bar{i}_3 \quad (5.9)$$

where \bar{z}_3 is the impedance of each phase windings of the zig-zag transformer at the third harmonic frequency.

As discussed, the zig-zag winding impedance offers zero impedance to the third harmonic component and infinite impedance to all other harmonics. Thus, the neutral voltage v_N is equal to zero. The output voltage of DBR with respect to the midpoint m is given by,

$$v_{d+} = v_m \cos(\omega t - \frac{2p\pi}{3}) \quad (5.10)$$

where $p=0$ for $\pi/6 < \omega t < 5\pi/6$; $p=1$ for $5\pi/6 < \omega t < 3\pi/2$ and $p=2$ for $3\pi/2 < \omega t < \pi/6$

$$v_{d-} = v_m \cos(\omega t - \frac{2q\pi}{3}) \quad (5.11)$$

where $q=0$ for $\pi/2 < \omega t < 7\pi/6$; $q=1$ for $7\pi/6 < \omega t < 11\pi/6$ and $q=2$ for $11\pi/6 < \omega t < \pi/2$

The diode current in the three-level boost converter is given as,

$$i_{D+} = \frac{v_m}{v_{c+}} \left\{ i_{dc} \cos\left(\omega t - \frac{2p\pi}{3}\right) + \frac{i_{dc}}{3} \left[\cos\left(4\omega t - \frac{2p\pi}{3}\right) + \cos\left(2\omega t + \frac{2p\pi}{3}\right) \right] \right\} \quad (5.12)$$

$$i_{D-} = \frac{v_m}{v_{c-}} \left\{ i_{dc} \cos\left(\omega t - \frac{q\pi}{3}\right) - \frac{i_{dc}}{3} \left[\cos\left(4\omega t - \frac{q\pi}{3}\right) + \cos\left(2\omega t + \frac{q\pi}{3}\right) \right] \right\} \quad (5.13)$$

The Fourier analysis of the above currents shows the existence of multiples of third harmonic components. This harmonic current produces ripples in the output voltage. The harmonic currents of the order $3h$, $h=1,3,5\dots$ flows through C_+ . Similar harmonic currents flowing through C_- are in-phase opposite to that of C_+ . Due to this harmonic cancellation, the ripples in the output voltage is zero. However, harmonic currents of order $6h$, $h=1,2,3\dots$ flowing through the capacitors will produce ripples in the output voltage (Mohan et al. 1993). The DC output current I_{dco} is given as,

$$I_{dco} = \frac{3\sqrt{3}}{2\pi} \frac{v_s}{v_{dc}} \left(i_{dc} + \frac{i_3}{8} \right) \quad (5.14)$$

where v_s is the peak value of the AC supply phase voltage.

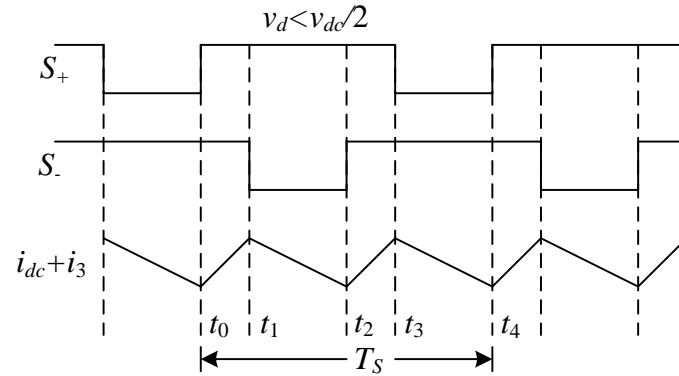
5.3.1.2 Analysis of three-level boost type modulation circuit

The three-level boost converter consists of three-phase DBR at the input side, and the output side consists of capacitive voltage divider arrangement with equal capacitor value of C_+ and C_- possess voltage of $v_{dc}/2$ with respect to the center-point, m . The input sinusoidal voltage is applied to the front-end DBR. The rectified voltage v_d , at the output of DBR is applied to the three-level boost converter. For analysis, the inductive and capacitive resistance is assumed to be zero, and three-level boost converter switches are operating at switching frequency of f_s , which is larger than the input frequency f . The three-level boost converter having two switches operates in four possible switching states of 00, 01, 10 and 11.

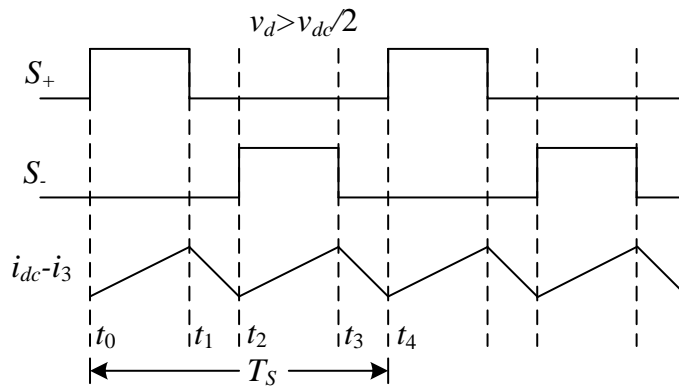
The above mentioned four switching states of three-level boost converter operates based on the magnitude of rectifier output voltage and capacitive mid-point voltage. So,

depending upon the magnitude of rectifier output voltage and capacitive mid-point voltage, the converter operates in two different operating areas.

If the input voltage is less than the capacitive mid-point voltage ($v_d < v_{dc}/2$), the inductor current rises positively to v_d and the duty ratio of the switches is less than 0.5. The discharging voltage across the inductor is $v_d - (v_{dc}/2)$. For this operating range, the switching pulse along with inductor current as shown in Figure 5.4(a). If the input voltage is higher than the capacitive mid-point voltage ($v_d > v_{dc}/2$), the inductor voltage charges to $v_d - (v_{dc}/2)$ and discharges to the voltage level of $v_{dc} - v_d$. For this operating range, the switching pulse along with inductor current is shown in Figure 5.4(b).



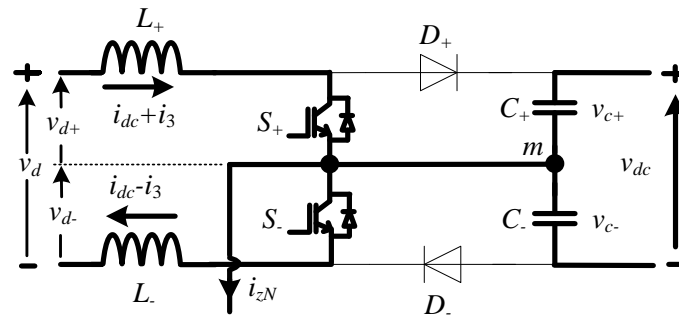
(a)



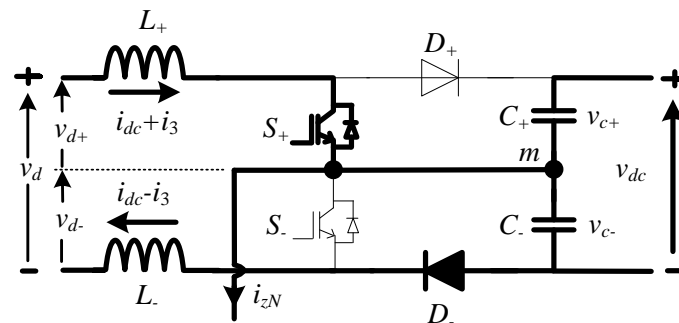
(b)

Figure 5.4: Waveforms of three-level boost converter switching cycle and inductor current when (a) $v_d < v_{dc}/2$ and (b) $v_d > v_{dc}/2$.

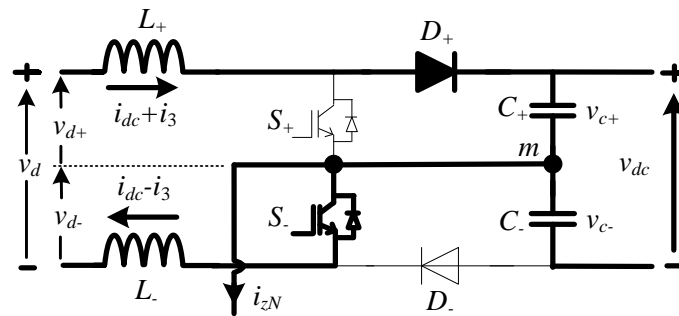
A. Modes of operation:



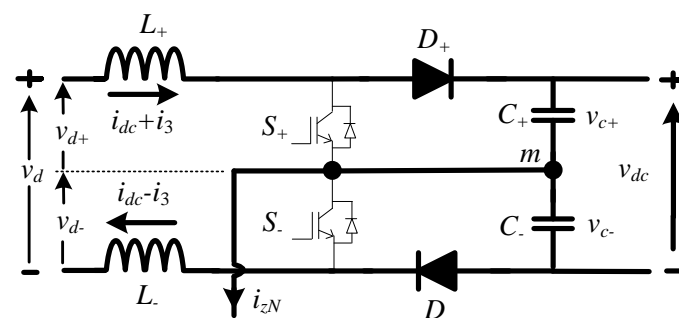
(a)



(b)



(c)



(d)

Figure 5.5: Operating modes of three-level boost converter (a) Mode 1, (b) Mode 2, (c) Mode 3 and (d) Mode 4.

Mode 1: In this mode both the switches S_+ and S_- are switched ON as shown in Figure 5.5(a). So, the inductor voltage v_{L+}/L_- is equal to the rectifier output voltage v_d ie, $v_{L+}=v_{d+}$ and $v_{L-}=v_{d-}$. In this mode, the inductors are in charging state and the previously charged capacitors are supplying the load current. The equations pertaining to this mode is as follows:

$$v_{L+}/L_- = v_d; i_{c+} = i_{c-} = -i_{dc}; v_{dc} = v_{c+} + v_{c-} \quad (5.15)$$

Mode 2: In this mode, the upper switch S_+ is turned ON and the lower switch S_- is turned OFF as shown in Figure 5.5(b). The inductor voltage v_{L+}/L_- is the difference between rectifier output voltage and the lower capacitor voltage C_- . The upper capacitor is supplying energy to the load and the lower capacitor stores energy from the supply. So, this lower capacitor C_- is in charging state. The inductors are in either charging or discharging state. The equation pertaining to this mode is as follows:

$$v_{L+}/L_- = v_d + v_{c-}; i_{c+} = -i_{dc}; i_{c-} = i_{L+} - i_{dc}; v_{dc} = v_{c+} + v_{c-} \quad (5.16)$$

Mode 3: In this mode, the upper switch S_+ is turned OFF and lower switch S_- is turned ON as shown in Figure 5.5(c). The upper capacitor C_+ is charging and lower capacitor C_- is discharging. The lower capacitor supplies the load current. The inductors are in either charging or discharging state. The equation pertaining to this mode is as follows:

$$v_{L+}/L_- = v_d + v_{c+}; i_{c+} = i_{L+} - i_{dc}; i_{c-} = -i_{dc}; v_{dc} = v_{c+} + v_{c-} \quad (5.17)$$

Mode 4: In this mode, the upper switch S_+ and lower switch S_- are turned OFF as shown in Figure 5.5(d). The resulting inductor voltage is the difference of rectifier output voltage and capacitors output voltage. The inductors are in discharging mode, and the capacitors are in charging mode. The rectifier output voltage supplies the load current. The equation pertaining to this mode is as follows:

$$v_{L+}/L_- = v_d - v_{c+} - v_{c-}; i_{c+} = i_{c-} = i_{L+} - i_{dc}; v_{dc} = v_{c+} + v_{c-} \quad (5.18)$$

B. Inductor ripple currents:

The ripple current of the two inductors is shown in Figure 5.6. When $v_d < v_{dc}/2$ and $v_d = 0.25v_{dc}$, where the duty ratio is $D=0.5$, the maximum ripple current in the inductors as given by,

$$\Delta i_{\max} = \frac{v_d}{L_{+/-}} D \frac{T_s}{2} = \frac{v_{dc} T_s}{16L_{+/-}} \quad (5.19)$$

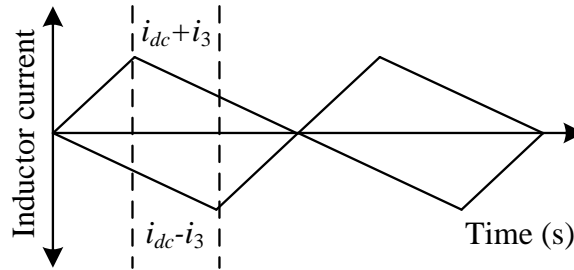


Figure 5.6: Inductors ripple current waveform of three-level boost converter.

When $v_d > v_{dc}/2$ and $v_d = 0.75v_{dc}$, where the duty ratio is $D=0.5$, the resultant maximum ripple current in the inductors is given by,

$$\Delta i_{\max} = \frac{v_d - 0.5v_{dc}}{L_{+/-}} D \frac{T_s}{2} = \frac{v_{dc} T_s}{16L_{+/-}} \quad (5.20)$$

The conventional boost converter having maximum ripple current at $v_s = 0.5v_{dc}$ is given by,

$$\Delta i_{\max} = \frac{v_d}{L} D T_s = \frac{v_{dc} T_s}{4L} \quad (5.21)$$

which is higher than the three-level boost converter. So, from the ripple current expression, the three-level boost converter requires four times less inductance compared to the conventional boost converter. From (5.19) or (5.20), the inductance is given by,

$$L_{+/-} = \frac{v_{dc}}{16 f_s \Delta i_{\max}} \quad (5.22)$$

From the ripple current analysis, it can be concluded that the inductor ripple current in three-level boost converter is one-fourth of that of the conventional boost converter. In other words, for the same ripple current, the three-level boost converter requires four times less inductance than the conventional boost converter. The inductor loss due to the resistance is a significant design parameter. The selection of L/R ratio and switching device losses are the major contributors for efficient operation of the converter. The proposed circuit has four times less inductance which means that four times less stored energy for the same input current. According to the magnetics, the energy storage density of the core is $\frac{1}{2} (B^2/\mu)$, which is only determined by the flux density B and effective magnetic permeability μ , that are same for both the cases. Therefore, the inductor in the three-level boost converter has about one-fourth the size of that in the conventional boost converter.

Moreover, the input ripple current is reduced by proper value of inductor connected in series with three-phase input supply. As the voltage conversion happens on a huge scale, the inductor value can't be chosen from the data sheet. Therefore, the following equation gives a good estimate of inductor value used at the input side of power supply system. For phase A, the input inductance is calculated by,

$$L_s = \frac{v_{as} \times (v_{dc} - v_{as})}{i_{a,ripple} \times f_s \times v_{dc}} \quad (5.23)$$

where v_{as} is supply phase voltage, v_{dc} is output DC voltage, $i_{a,ripple}$ is the maximum allowable ripple current, f_s is the switching frequency. The maximum allowable ripple current in input phase currents are normally 15-20% of the output current (Prakash P et al. 2018). Similarly, for the other phases input inductance can be calculated. From the literature, it has been observed that the magnitude of modulation current does not vary with the limited value of source inductance (Mohan et al. 1993).

The value of the capacitor has been chosen in such a way that, the output ripple is less. The rating of the capacitor can be calculated from the allowable maximum and minimum voltage at the output side. The required capacitance of the DC-link part is calculated by,

$$C_{+/-} \geq \frac{2P_{dc}}{\omega(v_{dc,max}^2 - v_{dc,min}^2)} \quad (5.24)$$

From the above equation, the DC-link capacitance is calculated from the output power, P_{dc} , angular line frequency, ω and allowable maximum and minimum voltage ripple of the DC-link voltage. In practice, the permissible voltage ripple is 1-5% of the output voltage level. The capacitance value purely depends on the voltage ripple (Prakash P et al. 2018).

5.4 CONTROL TECHNIQUE FOR THE HYBRID FRONT-END AC-DC CONVERTER

The reference signal is generated by voltage and current controllers as shown in Figure 5.7. The third harmonic current reference is generated from the input voltages. The magnitude and phase angle are calculated, and it is processed by the controller. The balancing of the two voltages of the capacitor has been counted in the reference generation, and hence the capacitive center-point output voltage is regulated. The signal from the current controller is compared with a high-frequency triangular wave of 20 kHz to generate PWM to the gate of IGBTs switches of the three-level boost converter.

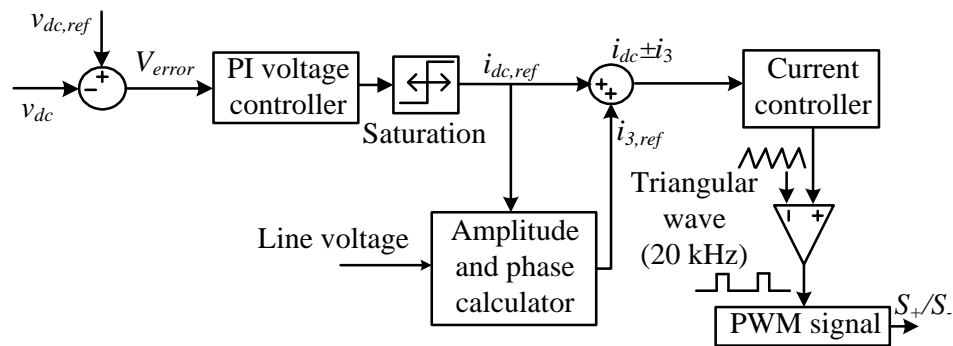


Figure 5.7: Control scheme for the hybrid front-end AC-DC converter.

5.5 RESULTS AND DISCUSSION

The MATLAB based simulation is carried out to study the performance of the hybrid front-end AC-DC converter and the results are shown in Figure 5.8. The parameters used for the simulation are given in Appendix C. The simulated results shown in Figure 5.8 are input phase voltages, input phase currents, voltage and current per phase, DC-link voltage and DC current under varying load conditions. The per phase voltage and current are in-phase with each other which ensures almost unity PF operation of the hybrid front-end AC-DC converter.

Figure 5.9 shows the frequency spectrum of the hybrid front-end converter. From the frequency spectrum, a current THD of 4.83% and 3.90% is observed under LL and FL conditions respectively which is well within the IEEE standards.

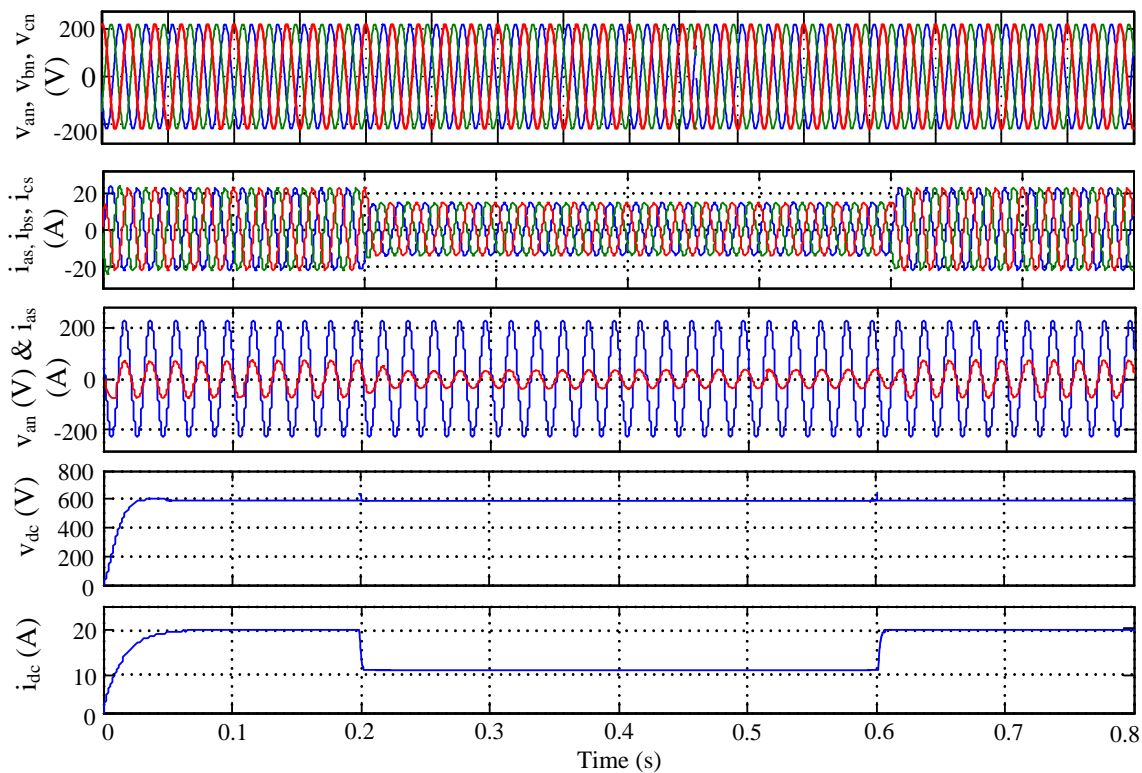


Figure 5.8: Simulation results of input phase voltage, input phase current, input voltage and current, DC-link voltage, and DC current for the hybrid front-end converter under load variations.

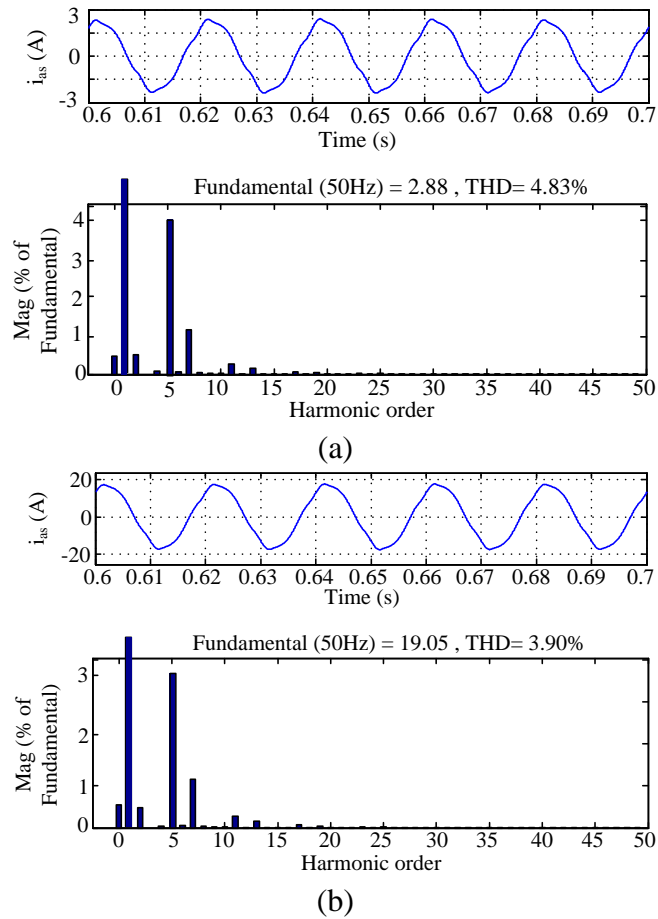


Figure 5.9: Frequency spectrum of input line current i_{as} at (a) LL condition (20%) (b) FL condition (100%).

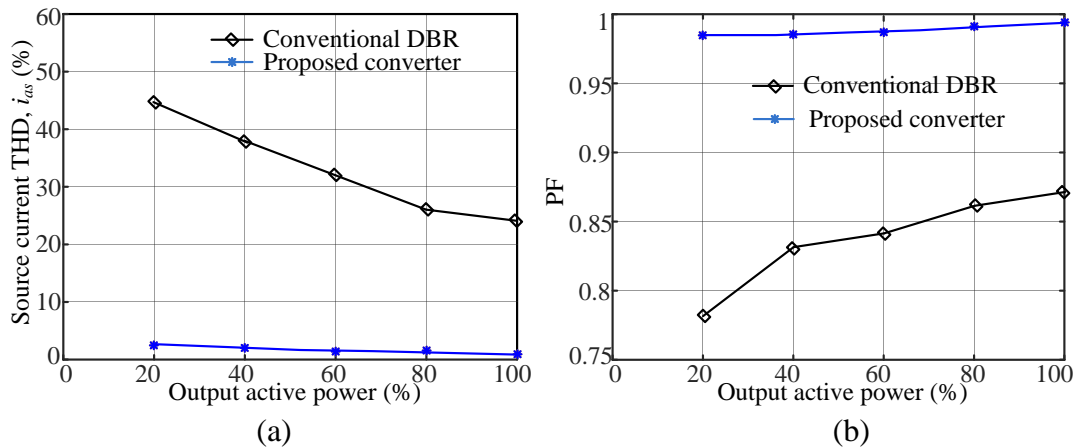
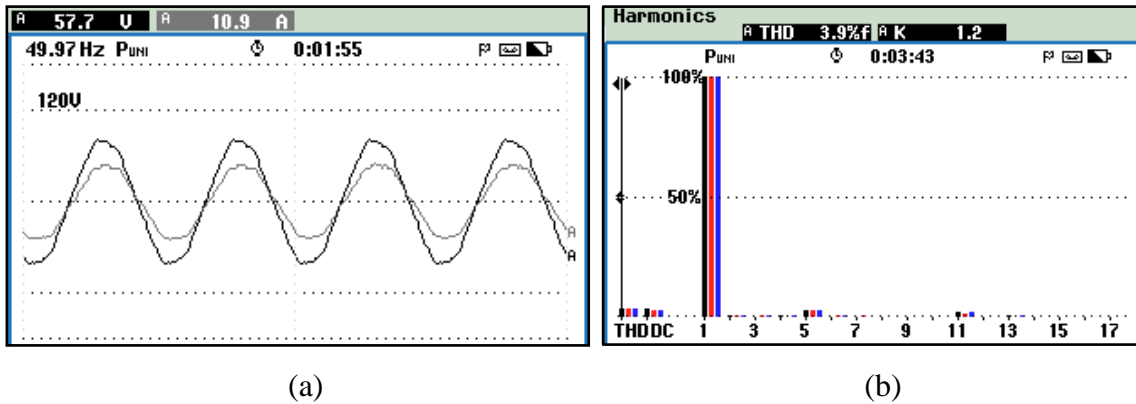


Figure 5.10: Comparison of power quality indices with varying load of front-end AC-DC converter with conventional DBR (a) Variation of THD of input current with load and (b) Variation of PF of input current with load.

Figure 5.10(a) and (b) shows the comparison of input line current THD and PF of the hybrid three-phase front-end AC-DC converter with that of 6-pulse DBR for varying load conditions. It is inferred from the Figure 5.10 that the hybrid three-phase front-end AC-DC converter yields less THD and PF almost unity.

A laboratory prototype is developed to demonstrate the operation of the hybrid front-end AC-DC converter and extensive tests have been conducted at a reduced input voltage of 100 V (line-to-line rms). The tests results are shown in Figure 5.11. Figure 5.11(a) shows the hybrid front-end AC-DC converter input phase voltage and phase current which are in-phase with each other and the corresponding input current THD is shown in Figure 5.11(b). From Figure 5.11(b), it is observed that the hybrid front-end AC-DC converter maintains the current THD of 3.9%. The output DC-link voltages and the injected neutral current of the zig-zag transformer are shown in Figure 5.11(c) & (d) respectively. Figure 5.11(e) shows the injected voltage and current of zig-zag transformer which are in-phase with each other and frequency is three times the source frequency.



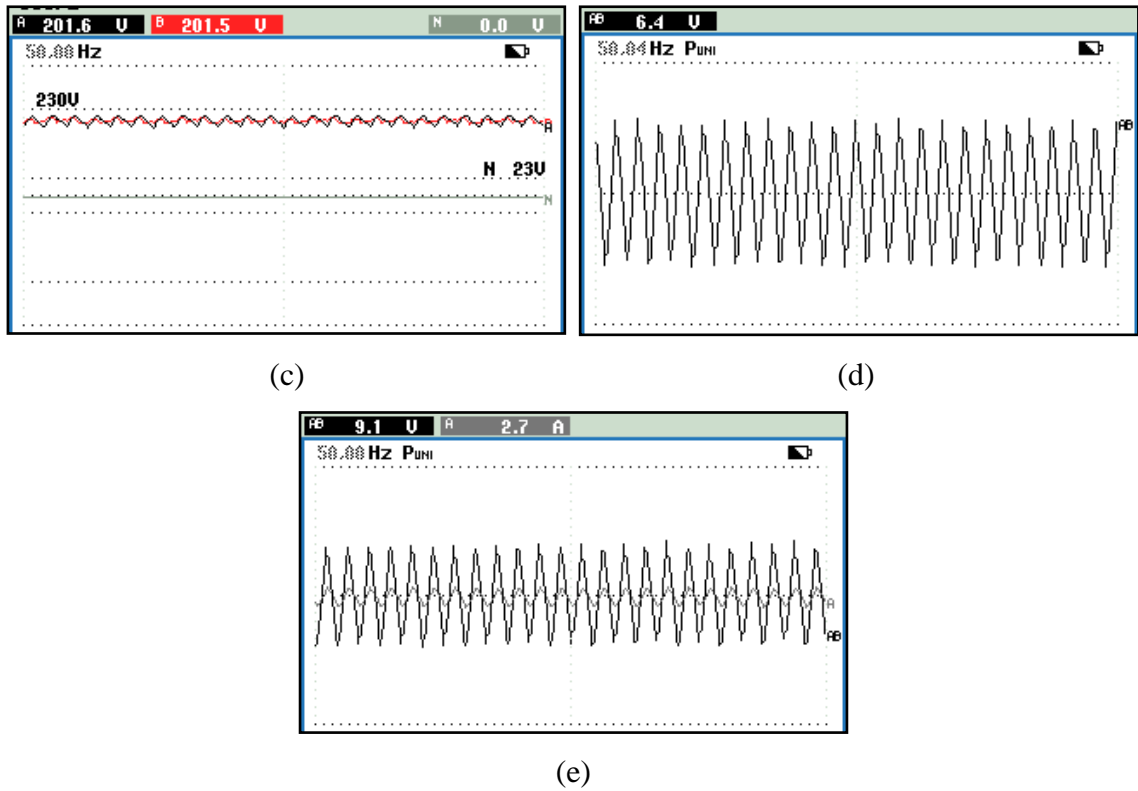
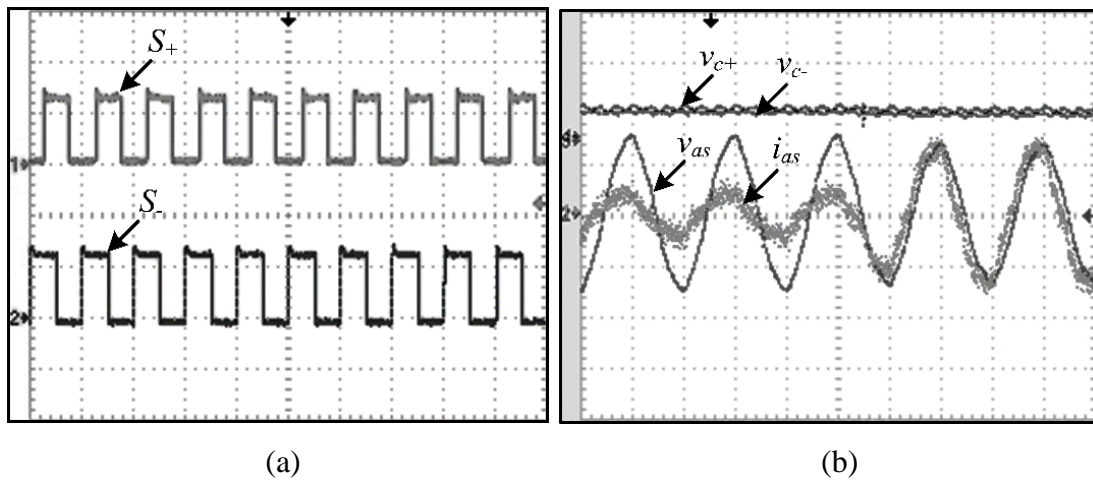


Figure 5.11: Hardware results of the hybrid front-end AC-DC converter (a) Input phase voltage, v_{as} and phase current, i_{as} (b) Harmonic spectrum of input current, i_{as} (c) Output DC-link voltages, v_{C+} , v_{C-} (d) Injected neutral voltage of zig-zag transformer, v_{mN} . (e) Injected neutral voltage, v_{mN} and current, i_{zN} of zig-zag transformer.



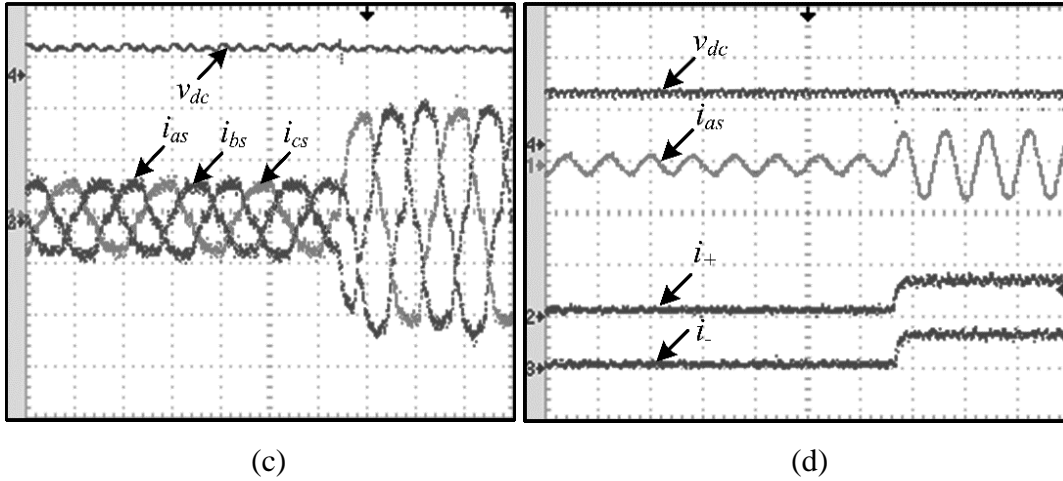


Figure 5.12: Hardware results of the hybrid front-end AC-DC converter (a) Switching pulses for S_+ (5V/div) and S_- (5V/div); Time scale (50ms/div) (b) Input phase current i_{as} (5A/div) and phase voltage v_{as} (20V/div) with DC-link voltages v_{c+} (200V/div), v_{c-} (200V/div); Time scale (10ms/div) under varying load conditions. (c) Input three-phase currents (2A/div) with output DC-link voltage v_{dc} (500V/div); Time scale (10ms/div) under varying load conditions. (d) Input phase current i_{as} (5A/div), output DC-link voltage v_{dc} (400V/div) with load currents i_+ (5A/div), i_- (5A/div); Time scale (20ms/div) under varying load conditions.

The performance of the hybrid front-end AC-DC converter is also verified under load variation. Figure 5.12(a) shows the three-level boost converter switching pulses generated from the control logic. Figure 5.12(b) shows the input phase voltage and current with DC-link voltages. Figure 5.12(c) shows the three-phase input currents and output DC-link voltage. Figure 5.12(d) shows the input phase current, DC-link voltage with load current variation. From the test results, the output voltage ripple is calculated as 22.22 V which is less than the maximum allowable voltage ripple. It is inferred from Figure 5.12 (b)-(d) that, the proposed control logic can maintain DC-link voltage constant even under the varying load conditions and also maintains power quality parameters well within the IEEE and IEC standards.

The power quality indices obtained from the hybrid front-end AC-DC converter for varying load conditions are summarized in Table 5.2. It is inferred from the Table 5.2 that, the front-end system maintains THD of less than 5% and unity PF during wide variation in load. The limits of current harmonics along with simulated and test results are tabulated in Table 5.3. Using power quality analyzer, the magnitude of harmonic order in case of hardware results are captured. The amplitude of third and multiples of third order harmonics are zero. Further, even-numbered harmonics and harmonics above 15th order are nearly zero, so it has not been included in Table 5.3. For the calculation of total demand distortion (TDD), the ratio I_{sc}/I_L is found to be in the range of 20-50 by considering full load current as 20 A and impedance as 3%. The formula used for finding the value of short circuit current is $I_{sc}=\text{full load current}/\text{impedance}$. The input current distortion limit is calculated using the formula of TDD, and it is given by the ratio of the root-sum-square value of the harmonic current to the maximum demand load current, I_L ,

$$I_{TDD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + \dots}}{I_L} \quad (5.25)$$

The load demand current of the system under study is considered as 20 A (by assuming that the proposed system is connected to PCC and no other system is presented). The TDD is calculated from the tabulated values of simulation and hardware results. The % I_{TDD} is found to be 2.23% under simulation case and 2.33% under hardware case. In both the cases, the TDD value is less than the limits given by the IEEE 519-2014.

Table 5.2: Power quality indices for the hybrid front-end AC-DC converter under varying load conditions

Load (%)	v_{THD} (%)	i_{THD} (%)	DPF	DF	PF
20	1.2	4.8	0.9867	0.9981	0.9848
40	1.5	4.6	0.9883	0.9984	0.9867
60	1.8	4.5	0.9897	0.9987	0.9884
80	2.1	4.1	0.9919	0.9991	0.9910
100	2.4	3.9	0.9949	0.9989	0.9938

Table 5.3: Comparison of simulation and hardware results of harmonic contents in the input line current

Current distortion limits as per IEEE Std 519-2014 when $(I_{sc}/I_L)=(20<50)$	Simulation		Hardware	
	Harmonic order (h)	Amplitude (%)	Harmonic order (h)	Amplitude (%)
$(3 \leq h < 11) = 7.0$	1	100	1	100
	3	0	3	0
	5	2.15	5	2.3
	7	1.1	7	1.6
	9	0	9	0
$(11 \leq h < 17) = 3.5$	11	0.19	11	1.3
	13	0.65	13	0.7
	15	0	15	0

5.6 COMPARATIVE STUDY

The detailed comparison of the hybrid front-end AC-DC converter with some of the systems available in the literature in terms of the type of modulation circuit, injection circuit, number passive and active components used, switching frequency, current THD, and efficiency are presented in Table 5.4. There are many topologies available in the literature, but only some of them were considered for comparison. The hybrid front-end AC-DC converter is superior than the systems available in the literature in terms of current THD and efficiency. Even though the efficiency is quite high in (Nishida et al. 2014), the number of passive and active components required are higher, and the current THD is almost equal. Poor dynamic response and less efficiency are the associated drawbacks of the passive modulation circuit. The active modulation/injection circuit requires accurate control parameters derived either from input or output variables which is more complicated and challenging task. The proposed system uses a zig-zag transformer as the injection circuit wherein the kVA rating is only 20% of the load rating. Moreover, the injection circuits used in (Itoh and Ashida 2008; Pejovic and Janda 1998; Pejović and Janda 1999) are isolated star-delta transformer which requires more kVA rating than the

proposed zig-zag transformer based current injection circuit. Further, the injection circuit used in (Kanaan et al. 2004; Nishida et al. 2014; Vázquez et al. 2009) are active switches which require less space than the transformer-based system. However, active injection circuit requires more control effort and continuous maintenance thereby increasing engineering effort. Hence, zig-zag transformer-based current injection circuit is more reliable and maintenance free circuit. Here, the experimental efficiency is measured with the help of power quality analyser. The increased efficiency of the hybrid front-end AC-DC converter is due to the less kVA rated zig-zag transformer and reduced rating and size of three-level boost inductors. The switching scheme also reduces the conduction losses of the modulation circuit. From the above comparison, it is evident that the hybrid front-end AC-DC converter has better performance compared to some of the systems available in the literature. Moreover, the hybrid front-end AC-DC converter is well applicable for retrofit applications.

Table 5.4: Comparison of the hybrid AC-DC converter with some of the available systems in the literature

Topologies	Modulation circuit	Injection circuit	Number passive components	Number active components	Switching frequency	Current THD	Efficiency
[1]	Passive	Passive (star-delta transformer)	7	Nil	-	7% - 12%	91.4%
[2]	Passive	Passive (zig-zag transformer)	8	Nil	-	4.01%	96.0%
	Passive	Active	8	3	70 kHz	4.01%	98.0%
[3]	Active	Active	6	3	50 kHz	5.00%	90.0%
[4]	Active	Active	6	5	100 kHz	11.0%	97.0%
[5]	Active	Passive (star-delta transformer)	5	2	10 kHz	7.20%	96.2%
[6]	Active	Passive (star-delta transformer)	6	2	20 kHz	4.77%	-
Hybrid AC-DC converter	Active	Passive (zig-zag transformer)	6	2	20 kHz	3.90%	97.0%

[1] (Pejović and Janda 1999)

[2] (Nishida et al. 2014)

[3] (Kanaan et al. 2004)

[4] (Vázquez et al. 2009)

[5] (Itoh and Ashida 2008)

[6] (Pejovic and Janda 1998)

The hybrid front-end AC-DC converter has the following advantages:

1. High efficiency is obtained because the main current passes through only two diodes of the three-phase DBR.
2. The injection circuit uses the zig-zag transformer which requires less copper and thereby reduced kVA rating.
3. The usage of zig-zag transformer avoids the possibility of resonance. Since zig-zag transformer offers very high impedance for the positive and negative sequence voltages.
4. The hybrid front-end AC-DC converter can be incorporated as a cost-effective retrofit solution to the existing wide range of DBR type utility interfaced applications.

5.6 CONCLUSION

This chapter presents a detailed analysis and implementation of a hybrid front-end AC-DC converters for power quality improvement. The developed hybrid front-end AC-DC converter uses zig-zag transformer as third harmonic current injection circuit and three-level boost converter as modulation circuit. The three-level boost converter has realized with less boost inductance, an only half rating of the conventional boost converter inductance thereby resulting in less ripple current and also the device rating has reduced by half of the output voltage. The third order current harmonic reduction is achieved by the zig-zag transformer. The hybrid front-end AC-DC convertre resulted in less input current and voltage THD and maintained PF close to unity.

CHAPTER 6

MAIN CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 GENERAL

The main objective of this investigation has been to design and develop various power quality improvement techniques used in three-phase front-end AC-DC converters. At the same time, it is aimed to explore new configurations and techniques in three-phase front-end AC-DC converters based on thorough literature review. Accordingly, these converters are classified on the basis of the power quality improvement techniques. There are three types of power quality improvement techniques used in the thesis namely passive, active and hybrid technique. The investigations reported in this thesis cover all these categories and have fulfilled these objectives successfully. The investigations are carried out for the following techniques: two categories of 20-pulse AC-DC converter employing MSAT and AMPC configurations, Vienna and Delta rectifiers employing voltage sensorless control technique and a hybrid AC-DC converter. A brief conclusion pertaining to different aspects of the work is already presented at the end of each chapter. A summary of the main conclusions is presented in this chapter, which is followed by suggestions for further work in this research area.

6.2 MAIN CONCLUSIONS

The design and development of three-phase front-end AC-DC converters are carried out in various categories. The performance of various types of front-end AC-DC converters have been studied under varying load conditions. These performance indices of front-end converters are evaluated on the developed systems with resistive load. The general conclusion of each chapter has been summarized as follows:

In Chapter 1, introduction about the front-end AC-DC converters in terms of its importance, applications, and problems have been discussed. Further, the power quality standards and thesis outline have been presented.

In Chapter 2, a comprehensive review of front-end AC-DC converters have been presented to explore a wide spectrum on different configurations. A broad classification of AC-DC converters is made to give a good guideline for easy selection of an appropriate converter for a specific application. The classification and the literature review have also highlighted the thrust areas of front-end AC-DC converter which are not reported and must be investigated in detail. From the literature, three types of potential front-end AC-DC converter topologies, MSAT and AMPC, Vienna and Delta, and hybrid AC-DC converters have been chosen for power quality improvement at input AC mains.

In Chapter 3, firstly the asymmetric MSAT converter is perceived by realizing a zig-zag configuration within a delta connected autotransformer together rated for only 40.27% of the nominal load. This progress is achieved as a result of combining zig-zag and delta connected configurations while sharing a part of windings being in common. Further, the detailed power quality performance analysis and loss calculations have been studied. The developed topology is simulated and experimentally verified. The results show the improvement in the power quality parameters. Further, a reduced magnetic rating AMPC is derived from the previously developed configurations for power quality improvement. The detailed design approach to develop a 20-pulse non-isolated AMPC has been discussed. Further, the non-isolated AMPC configuration has resulted in reduced magnetic rating of 26% of the load rating, leading to an energy-efficient utility interfaced converter for the cost-effective system. This progress is achieved as a result of arranging the phase staggered windings in the delta connected configurations and results in a smooth change in current from one conducting pair of diodes to the other. Further, a detailed power quality performance analysis and loss calculations have been studied. A numerical simulation has been carried out for evaluating the performance of the 20-pulse AMPC configuration considering the various power quality indices under load variation. The experimental results obtained from the laboratory prototype has been presented to validate the viability

and potential prospects of the non-isolated AMPC configuration. Finally, the detailed comparison of the MSAT and AMPC configurations with that of other multi-pulse AC-DC converter systems shows the supremacy of the proposed configuration. Also, the passive type front-end AC-DC converter exhibits remarkable improvement in power quality at the input AC source current with high efficiency and hence the passive type front-end AC-DC configurations is more suitable for applications necessitating to comply with the IEEE and IEC requirements.

In Chapter 4, two topologies of an active front-end AC-DC converter with voltage sensorless control technique have been proposed for power quality improvement. This voltage sensorless control technique does not rely on any input voltage information, which results in reliable and robust operation. Firstly, the feasible switching states of the Vienna type front-end AC-DC converter have been identified and incorporated into the system for maintaining the reduced switching stress/loss and ripples. The triangular carrier-based control logic has been applied and the system results in less input current/voltage THD and also maintains unity PF. Also, the detailed loss calculation, efficiency and hardware design details have been developed. The Vienna type active front-end AC-DC converter has been designed, simulated and experimentally verified under steady state and dynamic state. Further, a Delta type front-end AC-DC converter having active current injection circuit has been implemented. Due to the reduced line-to-line current in the Delta configuration results in lesser current ripples and thereby the device rating has been reduced by half of the output voltage. The third order current harmonic reduction has been realized by Delta connected semiconductor switches and its associated PWM generation which results in low frequency zero-sequence current circulating inside the Delta switch rectifier. The input voltage sensorless control was proposed for the Delta switch rectifier which requires less computational involvement and improves the input current quality. Also, the Delta type front-end AC-DC converter has been modeled, designed and its performance was analyzed by MATLAB simulation under varying load conditions. An experimental setup has been implemented and the performance of the system has been verified from the hardware results. Both the active front-end AC-DC converters result in less THD on the input current

and voltage and maintains close to unity PF. Also, the other power quality parameters such as DPF and DF are well within the IEEE standards. The comparative study distinguished the developed techniques among other popular ones highlighting their ability in overcoming some of the shortcomings in the available solutions.

In Chapter 5, a front-end AC-DC converter employed with third harmonic current injection circuit using a zig-zag transformer and three-level boost converter has implemented for medium and high-power applications. The three-level boost converter has been realized with less boost inductance, an only half rating of the conventional boost converter inductance thereby resulting in less ripple current and also the device rating has reduced by half of the output voltage. The third order current harmonic reduction is achieved by the zig-zag transformer. With less magnetic rating, only 20% of the load rating is sufficient to realize the zig-zag transformer. The hybrid front-end AC-DC converter has modeled, designed and its performance was analysed by MATLAB simulation under varying load conditions. An experimental setup has been developed, and the performance of the system is verified from the hardware results. The hybrid front-end AC-DC converter resulted in less input current and voltage THD and maintained PF close to unity. Also, the other power quality parameters such as DPF and DF are well within the IEEE standards. Finally, the comparison of results has demonstrated some of the promising features of the hybrid front-end AC-DC converter against others.

6.3 SUGGESTIONS FOR FUTURE WORK

The main objectives set for this research work have been successfully achieved, however, it is felt during the course of this investigation that the various issues noticed about power quality improvement techniques in three-phase front-end AC-DC converter may be further investigated in detail. Some of them are enlisted here for further investigations.

1. The generalization and improvement in performance of multi-pulse AC-DC converter for different pulse number, converter configuration and technique employed may be carried out.

2. The study carried out in this research work has been based on use of uncontrolled AC-DC converters for rectification. This study can be further extended for applications using controlled AC-DC converters.
3. The study may also be extended to explore the use of different improved power quality converters for power quality improvement in high rating applications. For bi-directional power flow such as conveyors, cranes, voltage source converters may be used for improving the power quality indices.
4. An investigation can be carried out for multi-level converters for power quality improvement. The operation of these converters can be further extended to PWM along with the multi-pulse techniques.
5. A robust and efficient active current injection circuit topology at back-end of the multi-pulse AC-DC converter can be implemented with precise control strategy for the power quality improvement.
6. The emphasis may be given on reduction of sensors and control techniques. This will lead to saving in capital cost as well as enhancing the reliability of the converter system.
7. The improvement in modulation and injection circuit also require a detailed investigation for improving performance in terms of power quality parameters.
8. The detailed investigation of three-phase front-end AC-DC converter configurations can be carried out to analyze the system under input voltage distortion and single-phase fault condition.

APPENDIX A

SPECIFICATION OF THE THREE-PHASE FRONT-END AC-DC CONVERTERS USING PASSIVE TECHNIQUE

A.1 MSAT

Converter specification of MSAT based 20-pulse AC-DC converter:

- Input voltage: 415 V, 50 Hz
- Source impedance: $z_s = 3\%$
- PNDBC diode modules: SEMIKRON SKKD 15/12
- Load power: 12 kW
- DC-link voltage: 600 V.

Physical design and construction of MSAT:

- Leakage reactance: 5%
- Flux density: 0.8 T
- Current density: 2.3 A/mm².

The number of winding turns and standard wire gauge (SWG) selected for the MSAT:

Transformer windings		w ₁	w ₂	w ₃	w ₄	w ₅	w ₆	w ₇	w ₈	w ₉	w ₁₀	w ₁₁	w ₁₂	w ₁₃
T _A	No. of turns	46	2	150	80	42	46	110	50					
	SWG	13	32	20	17	13	13	39	32					
T _B	No. of turns	46	10	36	238	94	36	8	122	130	38	38	130	122
	SWG	13	17	17	17	13	17	12	16	16	39	39	16	16
T _C	No. of turns	46	184	80	10	138	2	50	110					
	SWG	13	15	12	17	15	32	32	39					

A.2 AMPC

Converter specification of AMPC based 20-pulse AC-DC converter:

- Input voltage: 415 V, 50 Hz
- Source impedance: $z_s = 3\%$
- PNDBC diode modules: SEMIKRON SKKD 26
- Load power: 12 kW
- DC-link voltage: 600 V.

Physical design and construction of AMPC:

- Leakage reactance: 5%
- Flux density: 0.8 T
- Current density: 2.3 A/mm².

The number of winding turns and SWG selected for the AMPC:

Transformer windings		w ₁	w ₂	w ₃	w ₄	w ₅	w ₆	w ₇	w ₈	w ₉	w ₁₀	w ₁₁
T _A	No. of turns	4	148	83	182	109	58					
	SWG	15	17	21	18	18	18					
T _B	No. of turns	19	71	326	71	19	120	138	36	36	138	120
	SWG	15	16	18	16	14	18	18	21	18	18	18
T _C	No. of turns	182	83	148	4	58	109					
	SWG	19	21	17	15	18	18					

APPENDIX B

DESCRIPTION OF EXPERIMENTAL PLATFORM FOR THE THREE-PHASE FRONT-END AC-DC CONVERTERS USING ACTIVE TECHNIQUE

This chapter describes the various parts of experimental setup and software used to implement the developed control strategies and a detailed description of the laboratory prototype.

B.1 OVERVIEW OF THE EXPERIMENTAL PLATFORM FOR VIENNA TYPE AC-DC CONVERTER

The generalized schematic diagram representation of the developed experimental prototype is shown in Figure B.1. The FPGA controller board is employed which performs DC voltage, AC current sensing, and all the control computations programmed through MATLAB/Simulink. The experimental setup comprises of the following main units:

- A computer for rapid-prototyping and real-time control
- A FPGA altera family board with inbuilt compiler to run the program developed, signal feedback, control signal generation and communicating with the PC
- Interface cards (Isolations and dead band circuit, etc.)
- Power circuit board (IGBTs and gate drivers)
- The current sensors and voltage sensors
- The load box

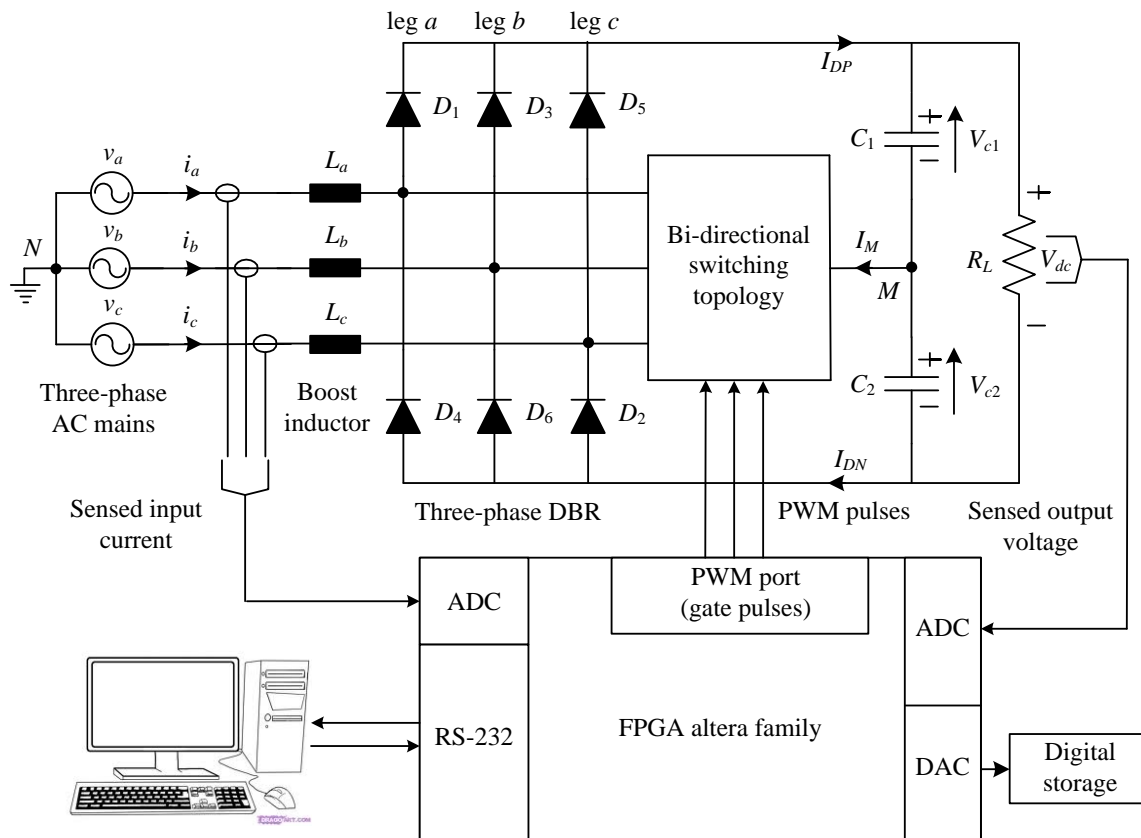


Figure B.1: Schematic diagram of hardware implementation of three-phase active front-end AC-DC converter using FPGA controller.

B.2 FPGA CONTROL BOARD

The FPGA controller is designed to enable a rapid prototyping and real-time simulation of various engineering applications. It provides a real-time interface for connecting the external devices to the processor inbuilt. It is based on the fast-digital processor (Altera Cyclone-IV) and the controller board consists of a EP4CE30F484 processor with associated on-chip peripherals. The picture of the FPGA controller and its additional I/O pins is shown in Figure B.2. The user has the flexibility to develop the desired model using Simulink which is further compiled and dumped into the controller. In addition to I/O pins,

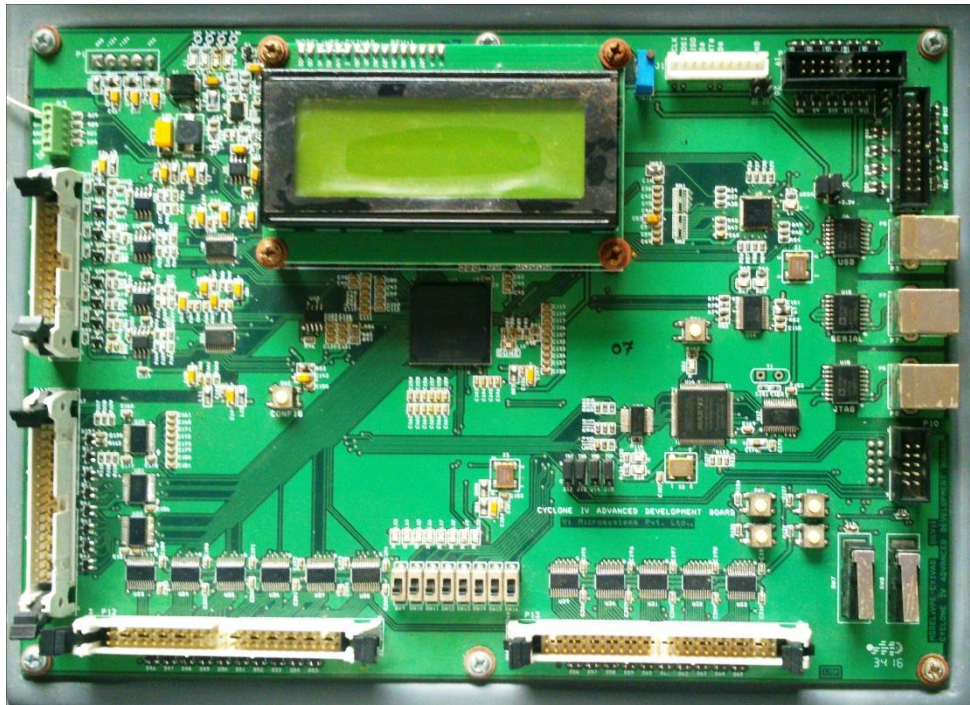


Figure B.2: Digital card of FPGA controller board.

it consists of analog-to-digital (ADC) and digital-to-analog (DAC) converters for sensing the external feedback signals measured from the system under control. The following are the key specifications of the FPGA control board:

- Cyclone-IV EP4CE30F484 FPGA
- 28848 Logic Elements
- 594 K bits Embedded Memory
- 66 Nos of 18 x 18 Embedded Multipliers
- 4 Nos of General purpose PLL
- 20 Nos of Global clock Networks
- 8 no of user I/O bank
- Flash Memory EPCS16 used to configure the FPGA at power OFF & Reset condition.
- On-Board Isolated USB-Blaster used to configure the flash memory & FPGA device.

- 16-channel ADC
 - Resolution: 12-bit
 - Interface: SPI
 - Input Range: ± 10 V or ± 5 V software configurable
 - Speed: 500 kSPS each

- ADC channels inputs are terminated at 26 pin FRC connector.
- One number of 4 channel 12-bit SPI Bipolar DAC used to convert the digital data into analog signal.
 - Resolution: 12-bit
 - Interface: SPI
 - Output Range: ± 10 V or ± 5 V software configurable
 - Speed: 10us settling time

- One 20 x 4 LCD display to display the alpha numeric character outputs.
- PWM output are terminated at 34 pin FRC connector.
 - 16 PWM output signals are generated through level translator IC.
 - 8 capture input signals/quadrature encoder interface.
- FPGA receives external 8 capture input signals through level translator IC.
- Other 84 PWMs are terminated in separate 2 Nos of 50pin header.
- One 8-bit DIP switch to give binary input to FPGA.
- 8 LEDs to display the 8-bit binary output.
- 4 Micro switches are used to give binary input to FPGA.
- 2 Limit switches are used to give binary input to FPGA.
- 2 Nos of 20-pin connectors are available & each having 18 I/O lines.
- On-Board Isolated RS232 communication used to communicate with PC.
- On board Isolated USB interface with TMC protocol for Data acquisition.

B.3 GATING SIGNAL ISOLATION AND AMPLIFICATION CIRCUIT

Practically, the power switch exhibits a finite delay time during switching ON and OFF. Thus, it is essential to introduce a small dead time termed as dead band among the switching of power switches constituting a leg or the switches whose simultaneous switching ON leads to the shoot-through condition. In this work, SKYPER 42R is used for driving the PWM signals, which has inbuilt dead band circuit. Further, gate driver is an essential part of the power circuit that is responsible for providing the required source and sinking current of the gate to source capacitance of the power switch. It interfaces and isolates the control circuit from the power circuit and also controls the dynamic behaviour and short circuit protection of the IGBTs. The input signal level is 0-15 V and interlocking time between the input signals is 2 μ s. It monitors the errors namely power supply under-voltage (below 13.5 V), short-circuit between collector and emitter. The error reset time is typically 9 μ s. On detection of error, the gate driver switches OFF the IGBT. The integrated short pulse suppression avoids very short switching pulses at the power semiconductor caused by high frequency interference pulses at the driver input signals. Switching pulses shorter than 500 ns are suppressed and not transmitted to the IGBT.

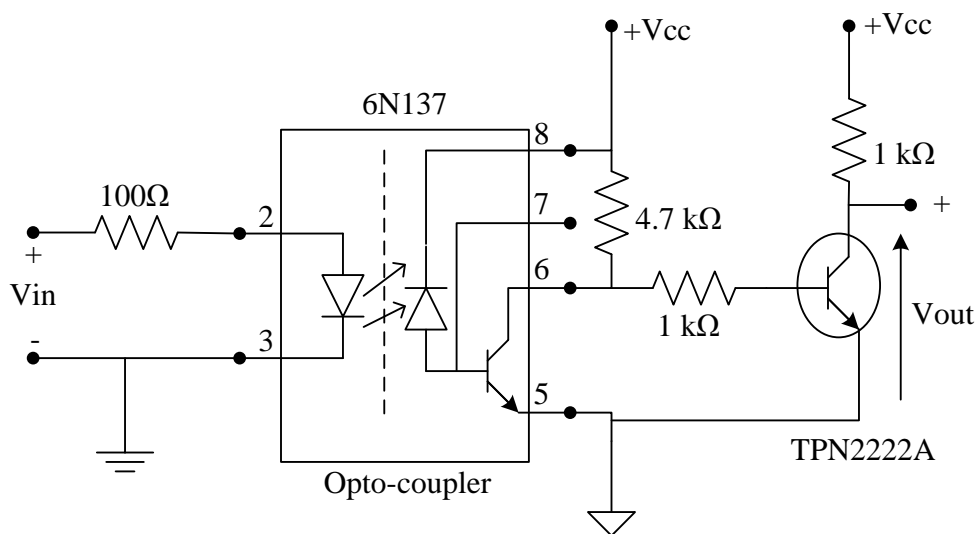


Figure B.3: Isolation and amplification circuit diagram for PWM pulses.

The output PWM signal from DAC output of FPGA can be of maximum 10 V, whereas, the driver circuit of the converter requires an input voltage of 15 V. Thus, the output of the DAC needs to be boosted before it is fed to the converter's driver. Although the driver SKYPER 42R is designed with isolation up to 4 kV, from safety as well as reliability point of view, separate isolation circuit for high frequency is provided through optocoupler 6N137. The optocoupler 6N137 consists of a light emitting diode and an integrated photon detector and is suitable for high speed applications. It needs supply voltage of 0-15 V and base current is 5 mA. After the desired isolation, the signals are amplified through NPN switching transistors 2N2222. The maximum collector-emitter voltage (V_{CE0}) is 30 V and maximum collector base voltage (V_{CBO}) is 60 V. The turn-OFF time is 250 ns. The input ground and the output ground of the optocoupler are isolated thus ensuring protection for the processor in case of a faulty condition. Figure B.3 shows the isolation and amplification circuit for PWM signal generation.

B.4 VOLTAGE AND CURRENT SENSOR CIRCUIT

A Hall effect voltage sensor LV 25-P is used for sensing of voltages such as DC, AC, pulsed with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit). It can measure voltage up to 500 V for 10 mA current. It has a closed loop (compensated) Hall effect voltage sensor. Figure B.4 shows the connection diagram of a LV 25-P voltage sensor. For sensing the voltage, a current proportional to the sensed voltage must be passed through an external resistor R_{in} which is selected by the user and installed in series with the primary circuit of the sensor as shown in Figure B.4. The input resistor R_{in} : the transducer's optimum accuracy is obtained at the nominal input current. The resistor R_{in} should be calculated so that the nominal voltage to be sensed corresponds to a primary current of 10 mA. The resistor R_m is a measuring resistance which is chosen between the maximum and minimum value of 100 Ω and 190 Ω respectively for ± 15 V supply.

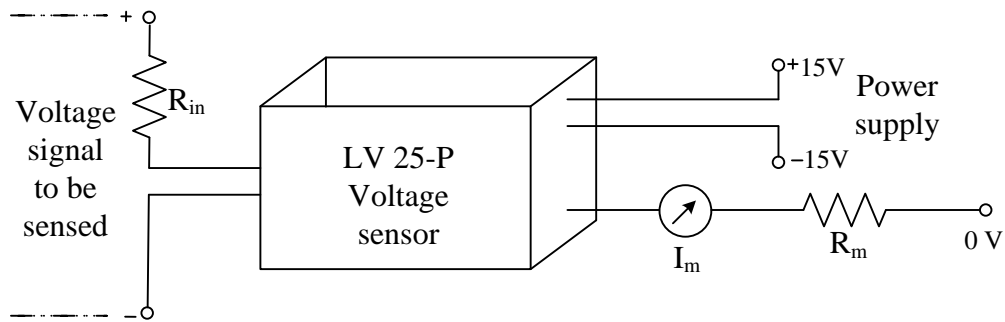


Figure B.4: Connection diagram for voltage sensor.

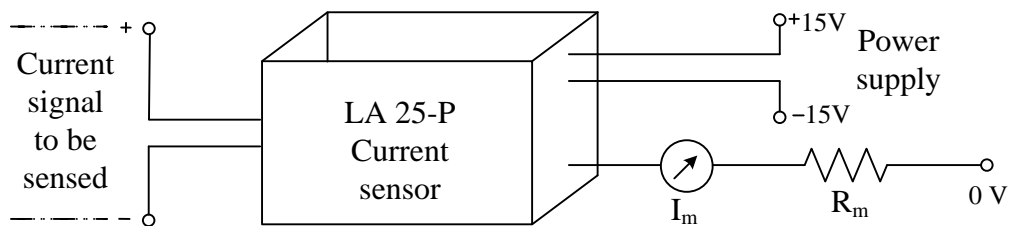


Figure B.5: Connection diagram for current sensor.

The currents of the system are measured using current sensor LA 25-P. The current sensors gives an output voltage signal, which is proportional to the input sensed current. The turns ratio of these sensor is properly chosen. Two loops are wound around the current sensor to obtain the output signals within the range of ± 10 V as per the specification of ADC channels. The current sensing and scaling circuit is shown in Figure B.5. The procedure for design of the sensors is adopted from (Mishra et al. 2010).

B.5 IGBT BASED CONVERTER

In this investigation, a Semikron make IGBT module is chosen, which consists of a bi-directional switch-based module (SKM300GM12T4) mounted on heat sink. This module is suitable for up to 20 kHz switching frequency and is having inbuilt thermal

protection. To protect the devices, from high dv/dt transients, snubber capacitors of $0.47 \mu\text{F} / 1500 \text{ V}$ have also been connected. The IGBT module is constructed in such a way that, it can be used either as three-phase DBR or bi-directional converter and also each leg is utilized as per the requirement. Further, the DC-link capacitors are either connected or disconnected from the circuit to enable the circuit as per the requisites. The rationale behind a generalized module is to facilitate the realization of any topology smoothly with a minimum effort of only requiring to make suitable external connections.

B.6 CONVERTER SPECIFICATION OF VIENNA TYPE AC-DC CONVERTER

The specification of the Vienna type AC-DC converter as follows:

- Three-phase source voltage, v_{ab} : 400 V (line-line rms)
- Source frequency, f : 50 Hz
- Switching frequency, f_s : 20 kHz
- DC-link capacitor, C : 900 μF
- DC-link voltage, V_{dc} : 600 V
- Load power, P_{dc} : 12 kW
- Bi-directional Switch, S_a, S_b, S_c : Semikron SKM300GM12T4
- Diode, D : Semikron SKKD 26.

B.7 CONVERTER SPECIFICATION OF DELTA TYPE AC-DC CONVERTER

The specification of the Delta type AC-DC converter as follows:

- Three-phase source voltage, v_{ab} : 400 V (line-line rms)
- Source frequency, f : 50 Hz
- Boost inductance, L : 3 mH
- Switching frequency, f_s : 20 kHz

- DC-link capacitor, C_{dc} : 900 μF
- DC-link voltage, V_{dc} : 600 V
- Load power, P_{dc} : 12 kW
- Bi-directional Switch, S_a, S_b, S_c : Semikron SKM300GM12T4
- Diode, D : Semikron SKKD 26.

APPENDIX C

SPECIFICATION OF THE THREE-PHASE FRONT-END AC-DC CONVERTER USING HYBRID TECHNIQUE

The specification of the current injection based hybrid AC-DC converter as follows:

- Three-phase source voltage, v_{ab} : 400 V (line-line rms)
- Source frequency, f : 50 Hz
- Boost inductance, L_s : 3 mH
- Switching frequency, f_s : 20 kHz
- DC inductor, $L_{+/-}$: 2 mH
- DC-link capacitor, $C_{+/-}$: 900 μ F
- DC-link voltage, v_{dc} : 600 V
- Load power, P_{dc} : 12 kW
- Switch, $S_{+/-}$: Semikron SKM200GB125D
- Diode, $D_{+/-}$: MUR3020PT
- VA rating of zig-zag transformer: 20 % of the rated load.

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