LOW POWER INTEGRATED CONTINUOUS-TIME TRANSCONDUCTANCE-CAPACITOR FILTERS TARGETED TO OPERATE ON 0.5 V SUPPLY VOLTAGE

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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October, 2014

This work is dedicated to

My

Beloved Parents

DECLARATION

by the Ph.D. Research Scholar

I hereby ***declare*** that the Research Thesis entitled **LOW POWER INTEGRATED CONTINUOUS-TIME TRANSCONDUCTANCE-CAPACITOR FILTERS TARGETED TO OPERATE ON 0.5 V SUPPLY VOLTAGE** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Doctor of Philosophy*** in the department of ***Electronics and Communication***, is a ***bonafide report of the research work carried out by me***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to *certify* that the Research Thesis entitled **LOW POWER INTEGRATED CONTINUOUS-TIME TRANSCONDUCTANCE-CAPACITOR FILTERS TARGETED TO OPERATE ON 0.5 V SUPPLY VOLTAGE**, submitted by **Vasantha M. H.** (Register Number: EC09F02) as the record of the research work carried out by him, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of ***Doctor of Philosophy***.

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ACKNOWLEDGEMENTS

Foremost, I would like to express my sincere gratitude and high esteem to my research adviser **Dr. Laxminidhi Tonse** for his constant guidance, care and valuable suggestions provided throughout my research work. He helped me with his expert advise, provoking and insightful discussions which has made me to understand and think intuitively about the circuits. I am fortunate to have him as my advisor and this work drew upon his motivation, enthusiasm and immense knowledge. My heartfelt thanks to him for spending his valuable time for shaping this thesis in present form.

I am grateful to the heads of the Electronics and Communication Engineering department. I thank Prof. Sumam David, the head of the department (HoD) during my enrollment to the Ph.D. program, Prof. Muralidhar Kulkarni, HoD during my Ph.D work and present HoD Prof. M. S. Bhat for their moral and administrative support.

My sincere thanks goes to the RPAC committee members, Dr. Mohan Kumar from Mechanical department, Dr. Shubhanga A from E & E Department, and Dr. Prakash Raghavendra from IT department for spending their time and giving valuable suggestions to improve the content and quality of my research work.

I wish to express my gratitude to Prof. Harishchandra Hebbar, Director MCIS Manipal, for helping me to get relieved from my job. I would like to thank him and Prof. Ramashesha for their valuable guidance and support during my research work.

I am greatful to my Director, Dr. G. R. C. Reddy, National Institute of Technology Goa (NITGoa) for his kind support and help. Also my thanks goes to Dr. Lalit K. Jiwani, HoD, ECE Department, NIT Goa for his kind coperation.

I am grateful to Prof. M. S. Bhat for his kind help and support and Prof. Ramesh Kini for supporting with all necessary CAD tools in VLSI lab in spite of his busy schedule. Thanks to Ms. Rekha Bhat for the technical discussions and support during filter design, layout, PCB design, testing process of fabricated chip and writing thesis. I am indebted to all the teaching and non teaching staff of the Electronics and Communication Engineering Department of NITK, Surathkal and MCIS, Manipal.

I thank Mr. Sanjeev Poojari for the timely arrangement made for purchasing components required for the test board and for unconditional support during chip test. Thanks to Mr. Tilak for maintaining the servers in VLSI lab, Ms. Prabha for helping out with issues of PC maintenance. I also thank the office staff Mr. Shaik Mohammad and Ms. Pushpalatha, for their help and support in department office. I thank Mr. Rathesh for his support while populating the PCB. Thanks to Mr.Vasudev and Mr.Ashok, for their laboratory support. I also thank the staff in the Academic Section, Administration Section and Resident Engineer Section of NITK Surathkal for their support during my stay at NITK campus

Heartfelt thanks to my friend Shajahan E.S. for the technical, personnel discussions and for being part of wonderful moments we had together. I thank all my fellow lab mates- Prashantha Kumar H., Suryakrishna K., Rajesh Shetty K., Bini A.A., Jagadeesha D.N, Luwa Faisal, Chandrika for their help and for the stimulating technical and non-technical discussions. Thanks to Assistant lecturers Kiran Kumar Lad, Jayaram Reddy, Genesh for their support in the lab and Kiran Kumar Lad for his the expert knowledge in softwares which is to solve my problems within no time. Also I thank Rajeev Komar and Prajaktha Panse S., M.Tech research students, who helped me in resolving technical issues on circuits and in cadence tool.

My heartfelt thanks to my elder brother Mohan M.H., younger brother Mahesh M.H. and my sister Padmaja for their moral support and inspiration during my research work. I thanks my mother-in-law Manorama T.B for the support and blessings she rendered. I do remember and owe the blessings of my father-in-law late T.B. Chandrashekar. Thanks to all relatives and friends, who supported me to finish my work.

My wife Sowmya Vageeshwari has been a true and great supporter and has unconditionally loved me during my good and bad times. I wish to express my whole hearted thanks for showing immense love, care and understanding that kept me going many a times. Thanks to Anshika M.Rao, my lovely daughter, whom god has blessed us during my research work, for bringing motivation and extra zeal in my work.

My sincere and heartfelt gratitude goes to my parents, K. Harishchandra Rao and Girija H. Rao for their supports, encouragement and blessings. I am word less to express my thanks for their patience, hard work and unselfish sacrifice they made to bring me to what I am today. I owe the success of my career to them and sincerely dedicate this work to them.

Finally, I would like to thank God for blessing me with good health, strength and peace during my research work.

ABSTRACT

KEYWORDS: Low power; Low voltage; Continuous-time G_m-C filter; Cochlea architecture; Fixed-transconductance bias; Design centering; Transmission line parameters; ABCD parameters.

This research work presents continuous-time G_m-C low-pass filters in 0.18 μm standard CMOS process for operation on 0.5 V supply. The filters use bulk-driven transconductors as their building blocks. Two filters are designed to validate the proposed ideas. One is a fourth order low-pass filter offering Butterworth response with a bandwidth of 1 MHz. This filter uses standard cascade of biquad architecture. The second filter uses Cochlea architecture and offers a second order Butterworth response with 500 kHz bandwidth.

Of the two filters, the fourth order filter is realized on silicon and fabricated using 0.18 μm standard CMOS technology from United Microelectronics Corporation (UMC). Measurement results reveal that, the filter is power efficient consuming a power of 56.4 μW from 0.5 V supply while offering a dynamic range of 45 dB. The figure of merit (FOM), computed in terms of energy, is found to be 0.355 fJ. When compared with similar low voltage filters realized on silicon, the proposed filter has the lowest FOM.

The Cochlea low-pass filter is a proof of concept realization. This filter also uses 0.18 μm n-well standard CMOS process from UMC. Simulation results show that the filter consumes a power of 20 μW operating on 0.5 V supply offering a dynamic range of 51 dB. Simulated FOM is found to be 0.225 fJ.

A bias circuit to fix the bulk-transconductance / gate-transconductance of the transistor in the transconductor is proposed based on constant current generating circuit.

This circuit helps to fix the gate/bulk transconductance of a transconductor operating on 0.5 V power supply. A mathematical analysis has been presented in support of the simulation results. The absolute maximum bulk-transconductance deviation from nominal value for the proposed scheme is found to be less than 0.4 % for $\pm$10 % change in supply voltage from nominal 0.5 V, at room temperature and for all process corners. The absolute maximum deviation in transconductance is less than 10 % for the proposed circuit across the process, supply voltage and temperature variations. The two conventional circuits, on the other hand, are found to offer absolute maximum deviation of about 25.8 % and 35.96 %.

In the last part of this research, a two-port transmission-line (ABCD) parameter based modeling technique has been presented. This technique accurately models a class of filters in presence of non-idealities of the transconductor such as finite output resistance and parasitic capacitance. In the proposed approach, the filter model is derived/obtained only through CAD simulations as compared with that of conventional state-space method which is based on small-signal equivalent circuit of the filter. The technique has been demonstrated using the second order Cochlea filter.

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ABBREVIATIONS

G_m-C	Transconductor-Capacitor
OTA	Operational transconductance amplifier
THD	Total harmonic distortion
HD_3	Third-harmonic distortion
SoC	System-on-chip
THD	Total harmonic distortion
FOM	Figure of merit
UMC	United Microelectronics Corporation
DR	Dynamic range
VNA	Vector network analyzer
SA	Spectrum analyzer
MOS	Metal oxide semiconductor
CMFB	Common mode feedback
PCB	Printed circuit board
DIP	Dual in-line package
NMOS	N-channel metal oxide semiconductor
PMOS	P-channel metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
PVT	Process, supply voltage and temperature

NOTATION

f	Frequency in Hertz
ω	Angular frequency in radians per second
g_m	Gate-transconductance in Siemens
g_{mb}	Bulk-transconductance in Siemens
C_{bd}	Bulk-drain capacitance in Farads
C_{gd}	Gate-drain capacitance in Farads
γ	Body effect parameter
η	Ratio of Bulk-transconductance to Gate-transconductance

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Emerging market for implantable medical electronics, wireless micro-sensors and new generation portable multimedia devices demands lowest power consumption for various reasons like long battery life, cooling requirements, miniaturization etc. (López-Morillo et al., 2012). Powering such devices by battery is quite not attractive, when the devices are deployed to operate in remote locations, due to associated charge replenishing and battery replacement issues. Also, the advances in battery technology is not at par with the demand and growth of computation and communication technology. Alternative energy sources are becoming need of the hour to power such devices. Some examples are scavenging energy from non-conventional sources like solar cells, fuel cells, vibration-to-electric, RF inductive coupling, wireless power transmission etc. To integrate these alternative power sources, the DC supply voltage may have to kept at a low value (Raghunathan et al., 2005; Min-Allah et al., 2007; Chalasani and Conrad, 2008; Chang et al., 2010). In the near future, it is not uncommon to expect DC voltage bus being at 0.5 V.

Growing semiconductor technology has allowed for continuous reduction in the feature size of the semiconductor devices. Voltage scaling associated with the reduced device size have gained popularity with improved power efficiency, speed and device density, specially in digital circuits (Pouwelse et al., 2003). As an example, performance improvement achieved with scaling of the devices is shown in Fig. 1.1 (Bohr, 2009). The figure highlights the increase in the transistor count made possible by the technology growth over the years..

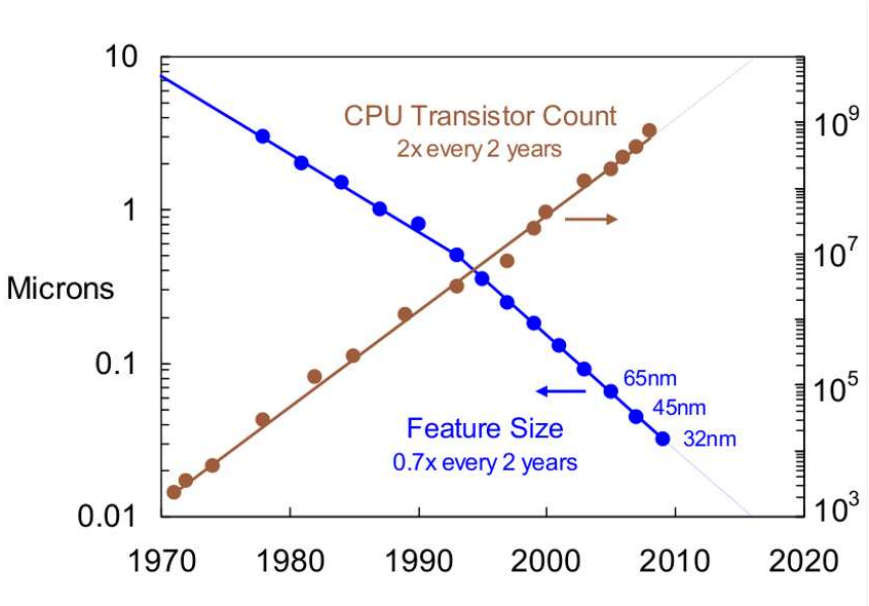


Figure 1.1: Scaling of transistors and improvement in the transistor count over the years (Bohr, 2009).

Continuous technology scaling has improved the performance in terms of reduced power and reduced cost per transistor (Chang et al., 2010). The low power requirements of digital systems without trading speed, have motivated the industry to move towards low voltage operation and similarly for major hand held and medical applications (Rajput and S.S.Jamuar, 2002; Yan and Sanchez-Sinencio, 2000). Further, the increasing use of mobile electronic products has motivated the industry towards reducing the power for analog and mixed signal circuits too (Allen et al., 1995).

In a typical system on-chip (SoC), analog and RF front end exist along with the digital circuit and integrated to consume power efficiently (Brock and Rajamani, 2003). Unlike digital design, where the trade-off is mainly on two parameters such as speed and power, the analog design has multidimensional design trade-offs (Razavi, 1999). Tuning to these trade-offs is challenging at low voltage (Enz and Vittoz, 1996). This poses a huge demand for low-voltage analog circuit design in standard digital CMOS technology.

Scaling dimensions in CMOS technology also demand proportional scaling in sup-

ply voltage as well (Mead, 1994). An expected trend in scaling of transistor dimension (gate length) and the supply voltage as predicted by the International Technology Roadmap for Semiconductors (ITRS) in 2012 is shown in Fig. 1.2 (ITRS, 2012). It can be seen that a continuous scaling in supply volatge is expected and may reach to 0.5 V by the year 2020. In analog circuits, the low voltage operation is bound to degrade the circuit performance, in particular the dynamic range and bandwidth. The main bottleneck for analog circuit design in standard CMOS technologies is that the threshold voltage of transistors do not scale with supply voltage (Thompson, 1998; Bohr, 2009). This can also be observed from the ITRS data as plotted in Fig. 1.2.

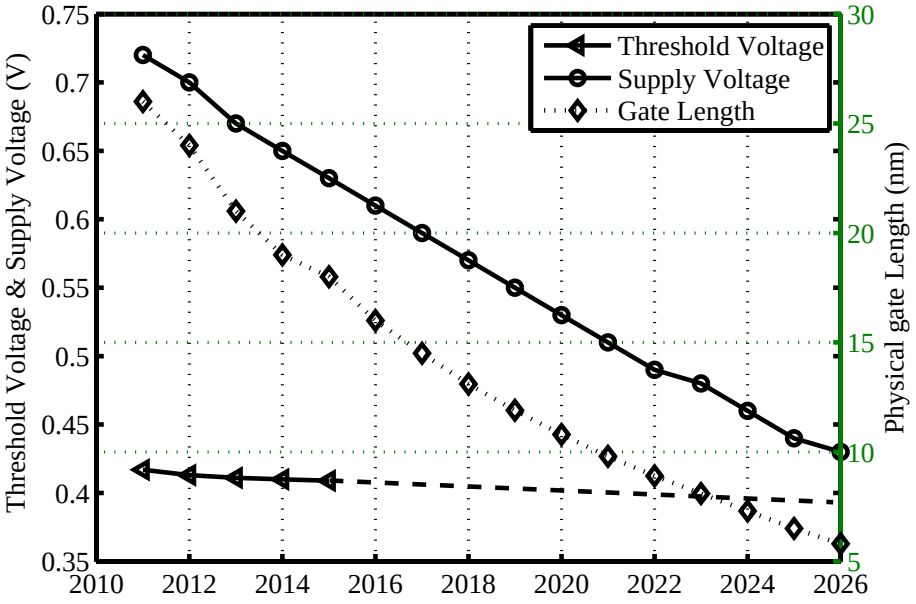


Figure 1.2: Supply voltage, threshold voltage and transistor scaling then, now and expected in future (ITRS, 2012).

There are a few solutions that exist to overcome the limitations posed by threshold voltage. One solution to combat this issue is to switch over to nano-technology with low threshold voltage devices (Tang et al., 2006). However, this requires the designers to move to new technology. But, some of the issues in these technologies like channel length modulation effect, drain induced barrier effect, tunneling can be of concern.

These may increase the market turn-over time and cost. Another solution would be to operate all the device in subthreshold region (Tai et al., 2006) for low power. This calls for availability of accurate models for the devices operating in sub-threshold; therefore, a careful design is necessary. Floating gate MOSFETs can also be used, where one can tune the threshold voltage for low voltage analog application, but at the expense of increased cost.

Bulk-driven technique is found to be useful for low voltage and low power analog circuit design (Guzinski et al., 1987). Here, the signal is applied to the bulk terminal of MOSFET and biasing is done through the gate terminal of the device. Voltage at the bulk terminal modulates the current flow through the transistor. Advantage of bulk driven device over gate driven device is that it is possible to have both positive and negative bias voltages (V_{BS}) for the device. With a small forward bias applied to the source-body junction, the threshold voltage of the MOSFET can be lowered. However, it is to be noted that the gain achieved is very low, since it is the bulk-transconductance (g_{mb}) of the device responsible for the gain and not the gate transconductance (g_m). This can pose some limitations on the achievable gain-bandwidth product.

This research explores the bulk-driven technique for realizing transconductors for low voltage applications operating on 0.5 V supply. The research uses Transconductor-Capacitor (G_m-C) filters as test-vehicle to validate the proposed ideas. It is interesting to note that, very few filters are found to be reported in the literature for 0.5 V operation and all of them have active-RC architecture, the first being reported in 2005 (Chatterjee et al., 2005). Active-RC filters offer higher dynamic range when compared to G_m-C filters for a given power. However, the filter bandwidth is limited by the realizable gain-bandwidth of the operational transconductance amplifier (OTA) for the given power. If, the dynamic range requirement is relaxed, G_m-C filters can be designed to offer higher bandwidth for the same power. Accordingly, a fourth order G_m-C Butterworth low-pass filter has been designed in this research to offer a bandwidth of 1 MHz operating on

0.5 V supply. The filter is designed in 0.18 μm standard CMOS process and has the highest bandwidth among similar filters operating on 0.5 V reported in the literature. The filter has been realized on silicon. The post-silicon test results show that filter has a dynamic range of 45 dB and is energy efficient with lowest figure-of-merit (FOM). The test results stand as testimony to the design techniques proposed in this research.

Another issue addressed in this work is the design of bias circuit required to fix the transconductance at 0.5 V supply operation against process, voltage and temperature (PVT) variations. It is important to fix the transconductance of the transconductor since the characteristic (bandwidth) of the filter depends on the transconductance. Transconductance of bulk driven devices are about 4 to 5 times smaller than that of gate driven device. A small change in the bulk transconductance can give rise to large percentage change in the over all transconductance of the transconductor. Designing circuits to fix the transconductance with in the tolerable limits is challenging at lower voltages down to 0.5 V. Few major issues in designing fixed-transconductance bias circuit at low-voltages are listed as follows:

- Lower voltage headroom prevents the use of cascode structure for bias circuits.
- Short channel devices when operated at low voltage, do not follow square law.
- Small variations in supply voltage can result in large variation in the transconductance.

In this research, a bias circuit has been proposed that fixes the gate-transconductance/ bulk-transconductance of a transistor (in the transconductor) against PVT variations. Comparison has also been made with the conventional circuits to highlight the efficiency of the proposed circuit in fixing the transconductance. Mathematical analysis has been given in support of the proposed circuit.

In addition, a second-order Cochlea filter which uses G_m-C architecture is designed as it is found to have low power consumption. Such filters are commonly found their use in Silicon Cochlea. Low power requirement, moderate bandwidth, requirement of gain

enhancement at band-edge (*Q*-tuning) of silicon Cochlea make this filter architecture well suited (Lyon and Mead, 1988). Design of such filters are found to be interesting, useful for humankind and same is explored at 0.5 V. The design is validated through simulation results for the maximum bandwidth which is achievable. The filter can be easily tuned for the desired *Q*, one of the important requirements of silicon Cochlea.

In the last part of this work, a method to model the filter based on two-port ABCD parameters has been proposed. The proposed method helps the designer to model a class of transistor level filters accurately. The model can be arrived through simulations without much of designers attention. The accurate model helps in design centering the filter in presence of parasitics. The process of re-tuning the response of a filter for the desired bandwidth in presence of parasitics is called as *design centering* and this is normally done with the aid of approximate model of transistor level filter. In this work an attempt is made to highlight the limitations of the conventionally used state-space based approach for modeling the filter. The cochlea filter has been used as the test vehicle to validate the proposed technique.

1.2 PRIOR WORK

The technique of body biasing is found to be useful for low-voltage digital circuits (Von Arnim et al., 2005; Narendra et al., 2004; Tschanz et al., 2002; Chen et al., 1996). For analog circuits, though the bulk driven MOS transistor concept was proposed in 1987 (Guzinski et al., 1987), it was not so popular among the designers. Of late, lack of sufficient head room in low voltage circuits has motivated the analog designers to move towards bulk-driven circuits. Bulk driven techniques have been used for designing analog circuits like transconductors, OTAs, filters, phase locked loops (PLLs) etc. at supply voltages below 1 V (Chatterjee et al., 2005; Vlassis, 2012).

The first integrated continuous-time active filter presented is of G_m-C type (Mould-

ing and Wilson, 1978). In the last three decades, different techniques have been explored to design and implement efficient integrated continuous-time filters. A summary of different architectures for OTA and filters with single-ended and differential input/output can be found in (Geiger and Sanchez-Sinencio, 1985; Sanchez-Sinencio and Silva-Martinez, 2000). For filters operating on voltages in the range 2-5 V, dynamic range and bandwidth were of prime concern (Tsividis, 1994; Zele and Allstot, 1996; Laxminidhi et al., 2009). Later, due to increase in demand for battery operated SoC designs and with low voltage designs gaining their importance, power consumption has begun to become one of the prime concerns; for example, the OTAs and filters presented in (Rosenfeld et al., 2004; Blalock et al., 1998; Haga et al., 2005; Raikos and Vlassis, 2010).

Improved performance associated with technology node-scaling has boosted the interest and importance in low-voltage analog designs, particularly body driven techniques at 0.5 V (Chatterjee et al., 2005; Vlassis, 2012; Raikos et al., 2012). With the trade-off between power dissipation and frequency of operation (Razavi, 1998), the aim of minimizing the power consumption has put restrictions on the maximum speed which is achievable. With lower power consumption, pushing the bandwidth of the filter to limits is a major challenge. In this research work, an attempt is made in this direction.

Quite a significant research has been carried out on integrated continuous time filters operating on supply voltages above 1 V; to say 1.8 V and 3.3 V. However, there are only a few filters found in literature that are operated on sub-1 V. The first significant work on integrated continuous time filter operating on 0.5 V was presented in (Chatterjee et al., 2005). It is a fifth-order elliptic low-pass active-RC filter in 0.18 μm CMOS process with triple-well NMOS devices. The filter has a cut-off frequency of 135 kHz with power dissipation of 1.1 mW. The OTAs used in this filter are gate driven. The use of triple-well process enabled the control over transistor threshold voltage for both NMOS and PMOS transistors through body bias tuning. Such tuning along with additional

circuits used to achieve necessary performance are found to increase the complexity of OTA.

In a similar work presented in (Trakimas and Sonkusale, 2009), a Butterworth low-pass filter was designed for 10 kHz bandwidth in 0.18 μm technology node operating on 0.5 V. However, the paper emphasizes only the OTA design, and details of the filter are not revealed; they are not found in literature either.

A G_m-C filter with bulk driven inputs presented in (Grech et al., 2005) operates on 0.9 V power supply which uses Cochlea architecture in n-well CMOS process. Another G_m-C biquad filter presented in (Carrillo et al., 2008) is designed in 0.35 μm technology to operate on 1 V power supply. It offers bandwidth of 17.5 KHz at a power of 45 μW with a dynamic range of 63.7 dB. A 1.5 V, 10 kHz bandwidth, OTA-C lowpass filter is presented in (Carrillo et al., 2010). The filter designed in 0.35 μm n-well CMOS process uses folded cascode OTA. A 3 MHz OTA-C low-pass filter is also presented in (Carrillo et al., 2011) that uses bulk-driven technique. Designed in 0.35 μm n-well CMOS process, this filter operates on 1.2 V.

In (Zhang and El-Masry, 2007), a filter operating on 1.8 V is designed in 0.18 μm process. This filter has been considered here since it uses bulk input transistors. The filter is a third order elliptic filter having a 3 dB bandwidth of 1 MHz, dynamic range of 45 dB and consuming 4.07 mW of power.

In all the bulk-driven 1 V / sub-1 V filters, the use of large gate-length of 1 μm or above is found to be common. The reasons for this are the following.

- Pseudo differential architecture, used to mitigate head-room issue for transconductors/ OTAs, make the transconductor vulnerable to mismatches. Large sized transistors are used to minimize the mismatch.
- Large gate-length increases the output resistance of the transistor and hence, the dc gain of the transconductor/OTAs.
- Large gate area (width $\times$ length) also helps in reducing $1/f$ noise offered by the

transistors (Razavi, 2004) which otherwise, can be a significant contributor to the output noise of the filter when the bandwidth is comparable to $1/f$ noise corner-frequency.

However, increase in transistor size results in increase in parasitics. This puts limitation on the maximum realizable bandwidth. Note that, this is in addition to the limitation posed by the use of bulk-transconductance which is smaller than the gate-transconductance. Therefore, sub-1 V designs in the literature, are found to have bandwidth of only few tens of kilo hertz.

This research focuses on the design of continuous-time filters having bandwidth of few hundreds of kilo hertz to 1 MHz, but still operating on 0.5 V. For high frequency filters, G_m-C architecture is considered to be best suited because of its open-loop nature and the same has been used in this research.

Transconductors play a major role in deciding the characteristics of a G_m-C filter, since the filter bandwidth is directly proportional to the transconductance of the transconductor. Therefore, it is important for the designer to ensure that transconductance of the transconductor remains within the limits across process, voltage and temperature (PVT) variations. In literature, there are a couple of circuits available that fix the transconductance of gate driven transistors (Steininger, 1990; Zele and Allstot, 1996). But the performance of these circuits fail to offer the desired performance against variations in supply voltage. Also, channel length modulation effect is found to aggravate the situation specially with short channel devices. An improved circuit was proposed in (Pavan, 2004) which mitigated all the problems of its predecessor circuits. These circuits, though designed to fix the gate-transconductance (g_m), can be used for bulk-driven transconductors since the bulk-transconductance (g_{mb}) is directly proportional to gate- transconductance. However, it is important to check the adaptability of the available circuits in the regime of 0.5 V operation. The circuit in (Pavan, 2004), is complex and is found not suitable for low voltage operation since it demands stack-

ing of several transistors between supply rails. The circuits presented in (Steininger, 1990; Zele and Allstot, 1996) are explored in this research and are also found to have limitations. As an outcome of this research, a new bias scheme has been proposed for 0.5 V transconductors and is found to offer superior performance compared to its counterparts.

1.3 ORGANIZATION OF THE THESIS

The rest of the thesis is organized as follows,

- Chapter 2 - Design of a fourth-order continuous-time G_m-C low-pass Butterworth filter operating on 0.5 V supply has been discussed in this chapter. The chapter, also details about layout considerations along with the design centering process followed.
- Chapter 3 - This chapter discusses and brings out the limitations of conventional bias circuits used to fix the transconductance when operating on 0.5 V supply. A fixed bias circuit is proposed in this chapter along with analytical justifications.
- Chapter 4 - The filter circuit design presented in Chapter 2 is fabricated on silicon. The results of the fabricated chip has been detailed in this chapter. The chapter also discusses the test-buffer circuit and the printed circuit board (PCB) designed for characterizing the chip. A comparison of the filter is also made with similar low-voltage filters found in literature.
- Chapter 5 - A second order Cochlea low-pass filter having Butterworth response is designed as a proof of concept of realizing filters in standard CMOS process operating on 0.5 V. Simulated performance of the filter is presented and compared with similar designs found in the literature.
- Chapter 6 - This chapter proposes a two-port ABCD parameter based approach for accurately modeling and design centering a class of filters. A second-order Cochlea filter with bulk driven transconductors is used as test vehicle for validating the proposed method.
- Chapter 7- Conclusions and future directions are presented.

CHAPTER 2

DESIGN OF LOW VOLTAGE TRANSCONDUCTOR-CAPACITOR FILTER

The main focus of the research, as outlined in Chapter 1, is the design of G_m-C filters for low voltage applications. A fourth order G_m-C filter is chosen as the test vehicle to validate a few of the ideas proposed in this research. The filter is designed in 0.18 μm n-well CMOS process from UMC technologies and chosen to have Butterworth response with a 3-dB bandwidth of 1 MHz. This chapter presents the complete design of the filter. The specifications of the filter are summarized below.

- Filter response type : Butterworth
- Filter order (n) : 4
- 3-dB bandwidth (f_o) : 1 MHz
- Realization : Cascade of biquads
- Architecture : G_m-C
- Supply voltage (V_{DD}) : 0.5 V
- Technology : 0.18 μm standard CMOS process from UMC

2.1 FILTER ARCHITECTURE

There are two approaches, namely **cascade approach** and **direct approach**, that are being used extensively by analog engineers for implementing higher-order continuous-time filters (Tsividis, 1994). Higher order filters are required when the stop band characteristics of the lower order filters are not sufficiently sharp enough to reject the undesired frequency band for a given application. In first approach, higher order filters are

realized by cascading second order filter sections and a first order section (for realizing odd-order filter). Each second order filter section implements a complex conjugate pole pair of the transfer function and the first order section realizes the real pole of the transfer function (in case the filter is of odd order). This approach is relatively easy in terms of filter realization and tuning. Each section can be tuned independently for the pole frequency and the quality factor of the complex conjugate poles to be realized. The second approach, also known as **LC ladder approach**, the filter is realized as a passive RLC filter. The RLC circuit is then converted to active circuit that is free of inductors. This is more complicated when compared to the former approach. But this approach results in lower sensitivities of the pass band frequency response to individual element values.

In this work, cascade approach has been used due to its simplicity. A second order filter is characterized by the transfer function shown in (2.1)

$$\frac{V_{out}}{V_{in}} = \frac{1}{\left(\frac{s}{\omega_o}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_o}\right) + 1} \tag{2.1}$$

where ω_o is the pole frequency and Q is the quality factor. The transfer function is then realized using G_m-C integrators. A systematic approach for realizing the second order transfer function using G_m-C integrators is explained as follows.

The transfer function given in (2.1) can be re-written in the form,

$$\frac{V_{out}}{V_{in}} = \frac{\left(\frac{\omega_o}{s}\right)^2}{1 + \frac{1}{Q}\left(\frac{\omega_o}{s}\right) + \left(\frac{\omega_o}{s}\right)^2} \tag{2.2}$$

Note that, the term $\frac{\omega_o}{s}$ denote the integration. Cross-multiplying and re-arranging (2.2),

$$V_{out} = \left(\frac{\omega_o}{s}\right)^2 V_{in} - \left(\frac{\omega_o}{s}\right)^2 V_{out} - \frac{1}{Q}\left(\frac{\omega_o}{s}\right) V_{out} \tag{2.3}$$

It can be seen that two integrators of the form $\frac{\omega_o}{s}$ are necessary to realize the transfer function. One can set both the integrators to have the same transfer function of the form $\frac{\omega_o}{s}$. For a more general case, the integrators may be assumed to have different transfer functions, say $\frac{\omega_{o1}}{s}$ and $\frac{\omega_{o2}}{s}$. If we define $\omega_o = \sqrt{\omega_{o1}\omega_{o2}}$, then (2.3) can be re-written in the form,

$$V_{out} = \left(\frac{\omega_{o1}\omega_{o2}}{s^2}\right)V_{in} - \left(\frac{\omega_{o1}\omega_{o2}}{s^2}\right)V_{out} - \frac{1}{Q}\left(\frac{\sqrt{\omega_{o1}\omega_{o2}}}{s}\right)V_{out} \quad (2.4)$$

$$= \left[\left(\frac{\omega_{o1}}{s}\right)V_{in} - \left(\frac{\omega_{o1}}{s}\right)V_{out} - \frac{1}{Q}\sqrt{\frac{\omega_{o1}}{\omega_{o2}}}V_{out}\right]\frac{\omega_{o2}}{s} \quad (2.5)$$

From (2.5), it can be inferred that, V_{out} is integral of the term inside the square bracket.

Defining $\left[\left(\frac{\omega_{o1}}{s}\right)V_{in} - \left(\frac{\omega_{o1}}{s}\right)V_{out} - \frac{1}{Q}\sqrt{\frac{\omega_{o1}}{\omega_{o2}}}V_{out}\right] = V_b$, (2.5) takes the form

$$V_{out} = V_b\left(\frac{\omega_{o2}}{s}\right) \quad (2.6)$$

Equation (2.6) can be easily realized using G_m-C integrator and the schematic is shown in Fig. 2.1 where $\omega_{o2} = \frac{G_m}{C_2}$.

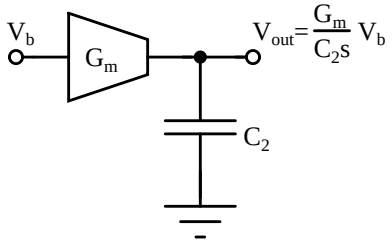


Figure 2.1: G_m-C integrator to realize the transfer function V_{out}/V_b.

Considering the equation of V_b, it can be re-written in the form,

$$V_b = \left[V_{in} - V_{out} - \frac{1}{Q}\sqrt{\frac{\omega_{o2}}{\omega_{o1}}}V_b\right]\frac{\omega_{o1}}{s} \quad (2.7)$$

From (2.7), V_b is integral of the term inside the square bracket with a proportional constant ω_{o1}. This equation can be realized as shown in Fig. 2.2 where $\omega_{o1} = \frac{G_m}{C_1}$ and

$G_{m2} = \frac{\sqrt{\omega_{o2}/\omega_{o1}}}{Q} G_m$.

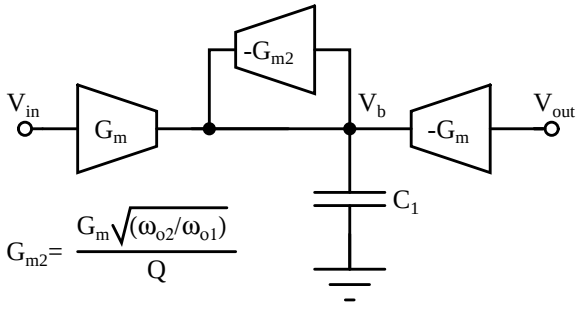


Figure 2.2: G_m-C circuit to realize (2.7).

Combining the integrators in Fig. 2.1 and Fig. 2.2 will lead to the second order low-pass filter commonly known as 'biquad' and is shown in Fig. 2.3.

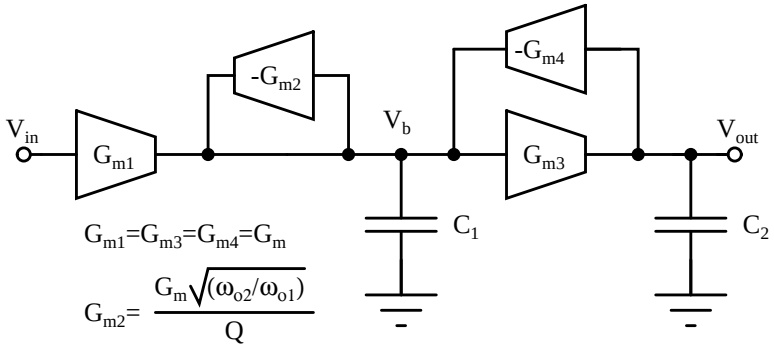


Figure 2.3: Second order G_m-C low-pass filter resulting after combining Fig. 2.1 and Fig. 2.2.

Further, if $\sqrt{\omega_{o2}/\omega_{o1}}$ is set equal to Q or in other words if G_{m2} is set equal to G_m, ω_o and Q can be defined in-terms of G_m and C

$$\omega_o = \frac{G_m}{\sqrt{C_1 C_2}} \tag{2.8}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{2.9}$$

If the transconductors are allowed to take independent values G_{m1}-G_{m4} as shown in

Fig. 2.3, the transfer function of the filter takes the form as in 2.10,

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{m1}}{G_{m4}}}{\left[\frac{C_1C_2}{G_{m3}G_{m4}}\right]s^2 + \left[\frac{G_{m2}C_2}{G_{m3}G_{m4}}\right]s + 1} \tag{2.10}$$

The corresponding ω_o and Q values are

$$\omega_o = \frac{G_{m3}G_{m4}}{\sqrt{C_1C_2}} \tag{2.11}$$

$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}\frac{C_1}{C_2}} \tag{2.12}$$

It is clear from (2.11) and (2.12) that the filter can be tuned for the desired pole frequency (ω_o) and quality factor (Q) by a proper choice of transconductances and capacitances.

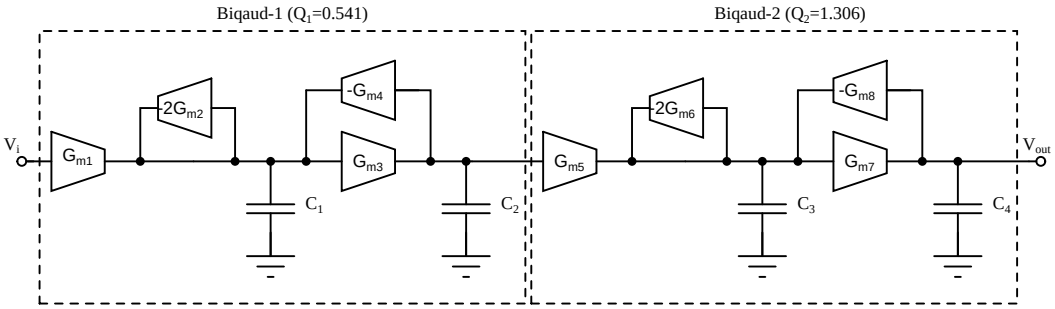
2.1.1 Cascade of Second Order Sections

Fourth order low-pass Butterworth filter is realized by connecting two biquads in cascade. Pole frequency f_o and Q of individual sections required to obtain the Butterworth response having a desired 3-dB bandwidth ($f_{-3\,\mathrm{dB}}$) for a fourth order filter is obtained from the filter table (Franco, 2009). f_o and Q of individual sections for $f_{-3\,\mathrm{dB}}$=1 MHz can be listed as follows

- First 2^{nd} order section : f_{o1} = 1 MHz ; Q_1=0.541.
- Second 2^{nd} order section : f_{o2} = 1 MHz ; Q_2=1.306.

Though the 2^{nd} order sections can be arranged in any order, it is common to arrange them in the ascending order of Q i.e. low-Q section first in the signal path. This is done in order to avoid the possible loss of dynamic range due to signal clipping if the high-Q sections are placed first in the signal chain.

The fourth order Butterworth low pass G_m-C filter is shown in Fig. 2.4. All transconductors are assumed to be equal having a transconductance of 10 μS. Accordingly, the capacitor values are computed. Fig. 2.5 shows the response of this ideal filter along with the response of individual 2^{nd} order sections.



G_m= 10 µS ; C_1 = 1.696 pF ; C_2= 1.45 pF ; C_3= 4.093 pF; C_4= 0.601 pF

Figure 2.4: Fourth order G_m-C low-pass filter architecture.

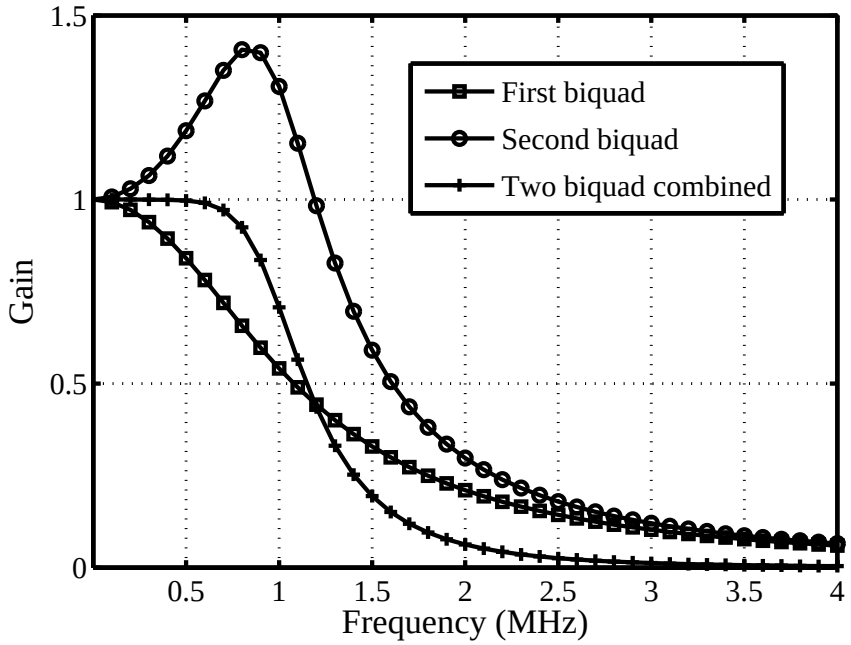


Figure 2.5: Response of fourth order G_m-C low-pass filter architecture.

After arriving at the ideal G_m-C architecture, the next task is to design the transconductor.

2.2 TRANSCONDUCTOR DESIGN

It is common among the designers to use fully differential operation due to its inherent merits over the single ended counterparts. And so is the case with the filter realized in this research. In addition, for designing transconductors operating on 0.5 V supply in standard CMOS process, it is imperative to use pseudo-differential operation due to lack of sufficient voltage head room and swing limitations. Transconductor, in this design, is realized to have bulk-driven inputs due to its advantages as outlined in Chapter 1. Fig. 2.6 shows the schematic of the differential-input differential-output bulk driven transconductor and its symbol.

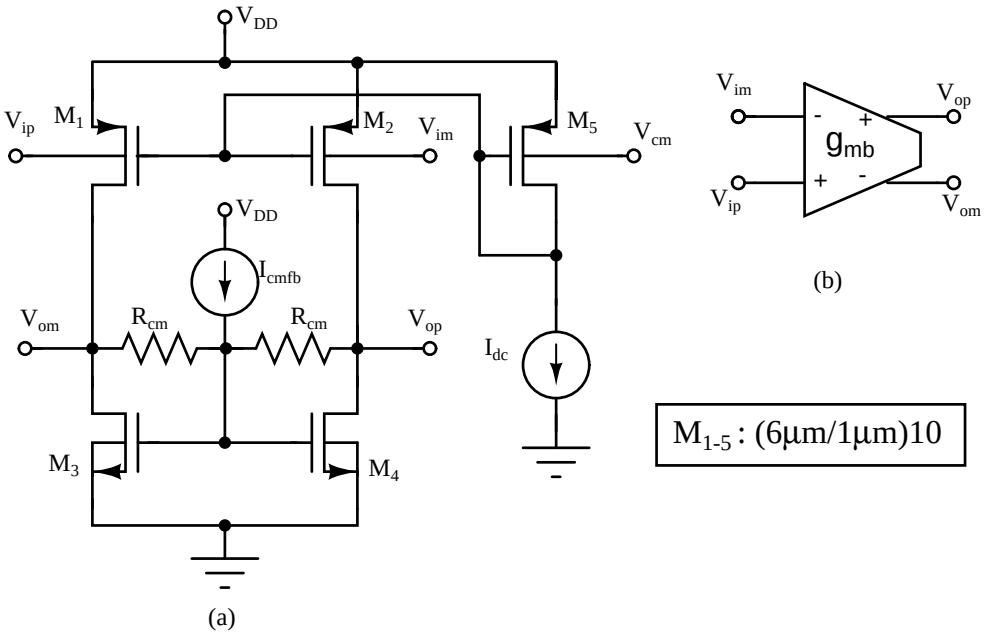


Figure 2.6: Bulk-driven pseudo-differential transconductor (a) Schematic. (b) Symbol.

v_{ip} and v_{im} are the differential inputs and v_{op} and v_{om} are the differential outputs. M_1 and M_2 are the PMOS input transistors and are sized to offer a bulk-transconductance of 10 μS when carrying a current of 2 μA. The gate of these transistors are biased to carry the required quiescent current i.e. 2 μA through a current mirror transistor M_5. The input common-mode of the transconductor is chosen to be 0.25 V i.e. $V_{DD}/2$. Transistors M_3 and M_4 form the NMOS current source load, which operates in sub-threshold region.

The gate of these transistors is biased by a common mode feedback circuit (CMFB) which sets the output common-mode of the transconductor to 0.25 V. The drain current of NMOS transistor operating in sub-threshold region is given in (2.13) (Taur et al., 1998),

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) V_T^2 \, e^{(V_{GS}-V_{TH})/(mV_T)} (1 - e^{-V_{DS}/V_T}) \tag{2.13}$$

where V_T is the thermal voltage and is about 26 mV at room temperature. In (2.13), the drain current can be assumed independent of V_{DS} i.e. $(1 - e^{-V_{DS}/V_T}) \approx 1$, if V_{DS} is more than about 4-5 times that of V_T . The drain-source voltage (V_{DS}) of M_3 and M_4 (in Fig. 2.6) is at output common mode voltage ($V_{DS,3,4}$=250 mV). Hence the above assumption is valid and the drain current can be assumed to be independent of V_{DS}. I_{DS} remains constant for a given V_{GS} and therefore, NMOS transistors M_3 and M_4 act as current source loads. The resistance R_{cm} and current source I_{cmfb} are part of the CMFB circuit and act as level shifter (Chatterjee et al., 2005) to set the gate bias required for NMOS current source load. Details of the CMFB circuit has been discussed in a separate section.

A careful look at the circuit reveals that there exists a parasitic capacitance between the input and output terminals of the transconductor. This is due to the body-drain junction capacitance of the PMOS input transistors i.e. C_{bd} of M_1 appearing between v_{ip} and v_{om} and similarly, C_{bd} of M_2 appearing between v_{im} and v_{op}. These capacitances introduce a right half s-plane zero to the voltage transfer function of the transconductor. A single-ended small-signal equivalent circuit of the transconductor is shown in Fig. 2.7. In the figure, g_{mb} is the transconductance of the input bulk driven transistor M_1. C_{in} and C_{out} are the effective parasitic capacitances at the input and output respectively. r_{in} and r_{out} are the effective input and output resistances. C_{bd} is the effective body-drain junction capacitance.

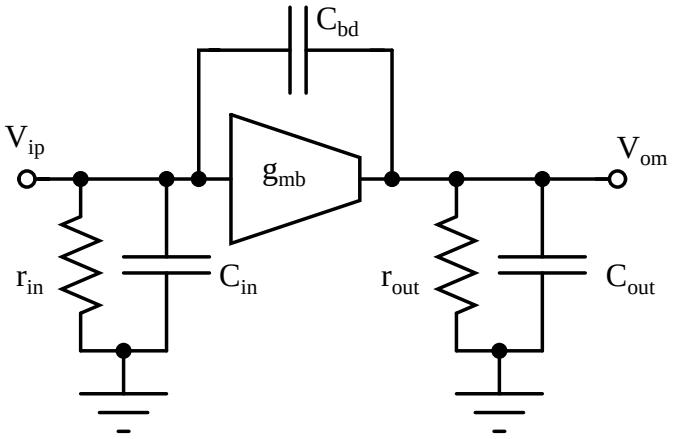


Figure 2.7: Single ended small-signal equivalent circuit of the transconductor.

Voltage transfer function of the differential transconductor can be written as

$$\frac{V_{op}-V_{om}}{V_{ip}-V_{im}} = \frac{g_{mb}r_{out}\left[1-\frac{C_{bd}}{g_{mb}}s\right]}{1+r_{out}(C_{out}+C_{bd})s} \tag{2.14}$$

It is seen from (2.14) that there exists a right half s-plane zero at $s = \frac{g_{mb}}{C_{bd}}$ and this zero causes the frequency response to deviate from the ideal for frequencies beyond $\frac{g_{mb}}{C_{bd}}$ rad/sec. Infact, the effect of this right half s-plane zero starts to creep-into the response at frequencies about a tength of $\frac{g_{mb}}{C_{bd}}$ rad/sec. If a filter is built using such a transconductor, it may be difficult to get a desired response for frequencies beyond one tength of $\frac{g_{mb}}{C_{bd}}$ rad/sec. For the transconductor designed in this work, C_{bd} is found to be 42 fF leading to a right half s-plane zero at 238 Mrad/sec (38 MHz). Therfore it may be very difficult to design and tune a fourth-order filter having a bandwidth of 1 MHz and offering stop-band performance at least upto 10 MHz. For this reason, it is required to minimize C_{bd} itself or its effect. Minimizing C_{bd} would call for the use of small size transistors. But this is not recommended as it would increase the mismatch between transistors. This work proposes a scheme to effectivelly compensate for the effect of C_{bd} by adopting a technique of mutual cancellation.

2.2.1 Compensation for Right Half *s*-Plane Zero

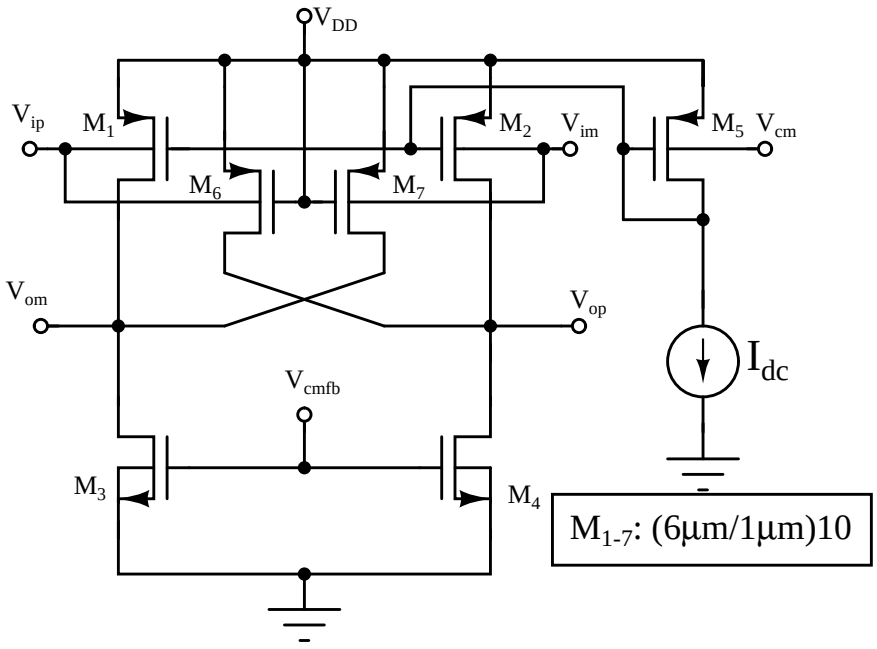


Figure 2.8: Schematic of bulk-driven transconductor with compensation for right half s-plane zero.

A simple scheme to compensate for the effect of right half *s*-plane zero is shown in Fig. 2.8. For a fully differential transconductor, v_{ip} and v_{im} are equal in magnitude and out of phase; similarly v_{op} and v_{om}. This feature has been exploited in the compensating scheme by using two cross-connected PMOS dummy transistors M_6 and M_7. C_{bd} of M_6 tend to cancel any coupling between the v_{ip} and v_{om} that occurs due to C_{bd} of M_1. Similarly, M_7 compensates for C_{bd} of M_2. These dummy transistors do not take any active part in transconductor action. It is to be noted that this scheme will only compensate for the capacitance but will not cancel the effect of capacitor altogether.

To justify the effect proposed scheme, frequency response of the transconductor is plotted in Fig. 2.9 without and with compensation. It is evident from the figure that the transconductor with compensation offers a first order response with a roll-off of -20 dB per decade. Without the compensation, the phase lag exceeds 90°(excess phase) and the magnitude response is pulled upwards beyond frequency of 3 MHz, thus clearly in-

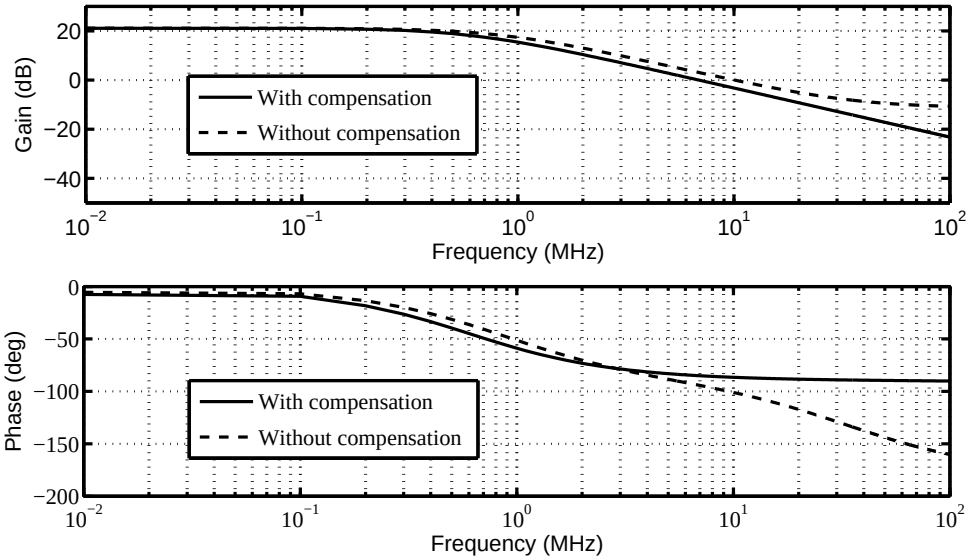


Figure 2.9: Frequency response of transconductor without and with compensation for right-half *s*-plane zero.

dicating the effect of right half *s*-plane zero. The phase response of the compensated transconductor tends to -90^o at higher frequencies. It is also observed that the compensation scheme reduces the effective bandwidth of the transconductor. This is expected since the PMOS transistors M_6 and M_7 increase the effective capacitance at the output nodes v_{op} and v_{om} respectively.

The resistors R_{cm} shown in Fig. 2.6 are realized by using the NMOS transistors. The complete schematic of the transconductor is shown in Fig. 2.10. The NMOS transistors M_8 and M_9 are used to realize R_{cm} and they operate in sub-threshold region. They are sized to offer high resistance of the order of few hundreds of mega ohms so that they do not load the transconductor differentially.

2.3 COMMON-MODE FEEDBACK CIRCUIT

In G_m-C filters, output of one transconductor drives the input of another transconductor. Therefore, it is common to set the output common-mode DC voltage of the transconductor equal to the input common-mode DC voltage. Further, to maximize the swing,

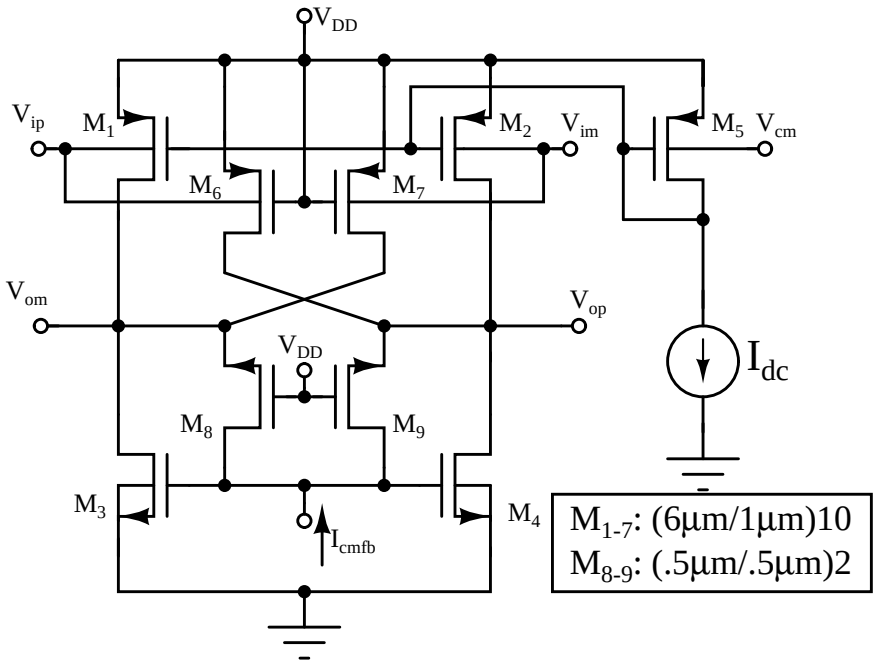


Figure 2.10: Complete schematic of the bulk-driven transconductor.

input and output common mode voltages are set to $V_{DD}/2$.

A master-slave circuit arrangement has been used in this work, to set the output common-mode voltage of transconductor. The master circuit sets the common-mode of a master transconductor using a negative feedback loop. The so generated tuning current is distributed to all the transconductors of the filter through current distribution circuit. The schematic of the master CMFB circuit is shown in Fig. 2.11.

Transistors M_1, M_2 and M_6 form the master transconductor which is identical to the common-mode equivalent half circuit of the transconductor shown in Fig. 2.10. The output common mode DC voltage of the master transconductor is sensed and compared with the reference common mode voltage ($V_{cm,ref}$) by the error amplifier. The negative feedback loop sets the current I_{cmfb} such that the output common-mode voltage ($V_{o,cm}$) is made equal to the reference voltage ($V_{cm,ref}$). The resulting I_{cmfb} is distributed to all the transconductors using current distribution circuit. The capacitor C_{cm} is used in parallel with M_6 to improve the stability of the common-mode loop. The master

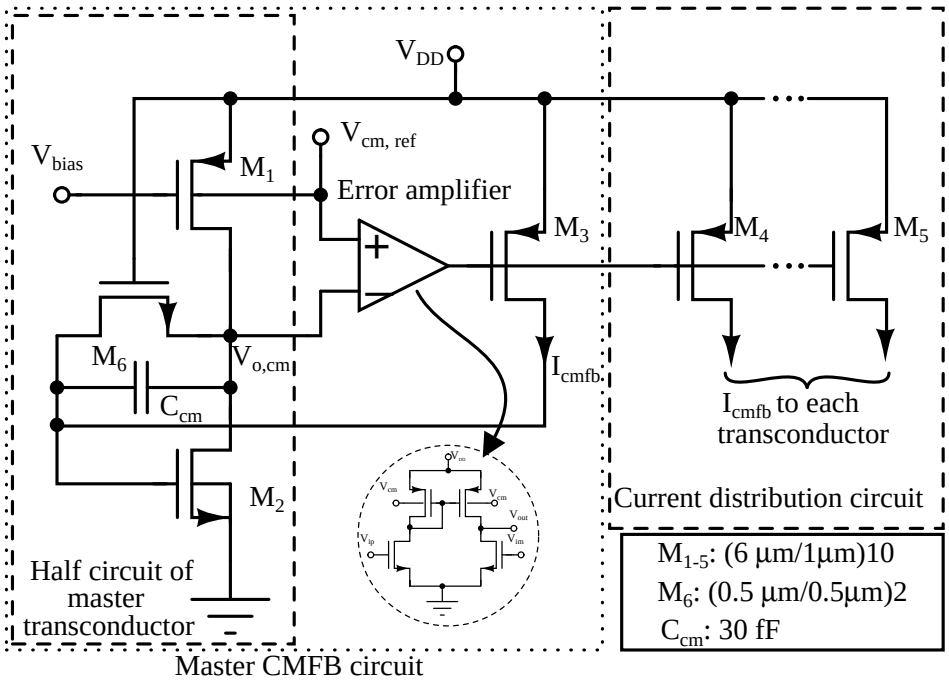


Figure 2.11: Schematic of common-mode feedback circuit.

CMFB circuit consumes about 3.05 μW at 0.5 V power supply. The Fig. 2.12 shows the response of common mode loop for a common mode disturbance (common mode current impulse of 2 μA for a duration of 1 ns). The loop is found to be stable.

2.4 FILTER LAYOUT

The schematic and layout plan for the unit transconductor is shown in Fig. 2.13(a) and Fig. 2.13(b) respectively. The PMOS transistor M_5 which generates the gate bias voltage (V_{bias}) for PMOS transistors M_1 and M_2 is realized as a parallel combination of two identical transistors (say $M_{5,A}$ and $M_{5,B}$ as shown in Fig. 2.13(a)) each having a size equal to half of that of M_5. This is done to achieve symmetry in the transconductor layout which is essential to maintain a good match between the two half circuits of the transconductor.

The complete scheme of filter layout is shown in Fig. 2.14(a) and the corresponding schematic of the fully differential filter is shown in Fig. 2.14(b). Transconductor cells

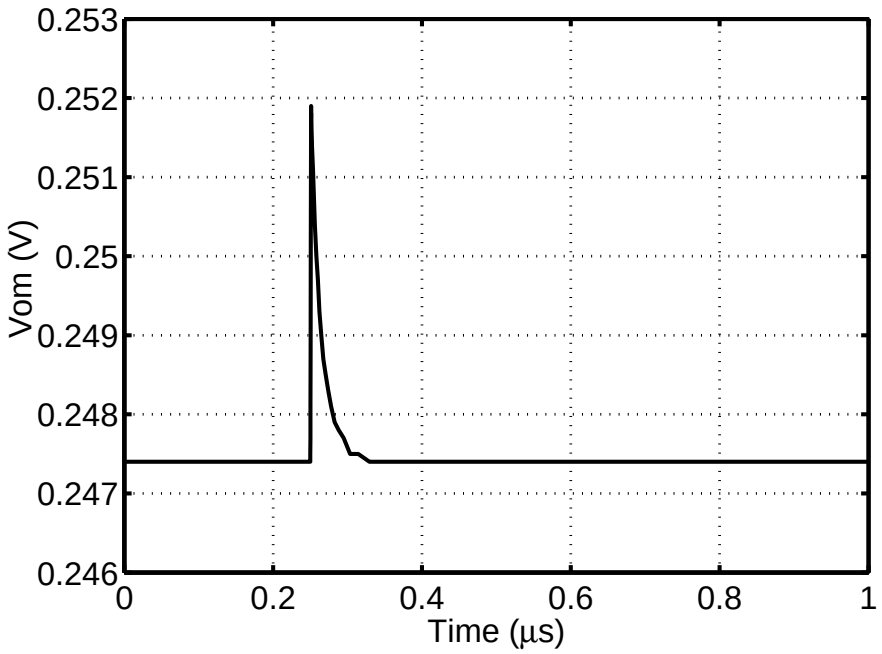


Figure 2.12: Response of CMFB circuit to common-mode current impulse.

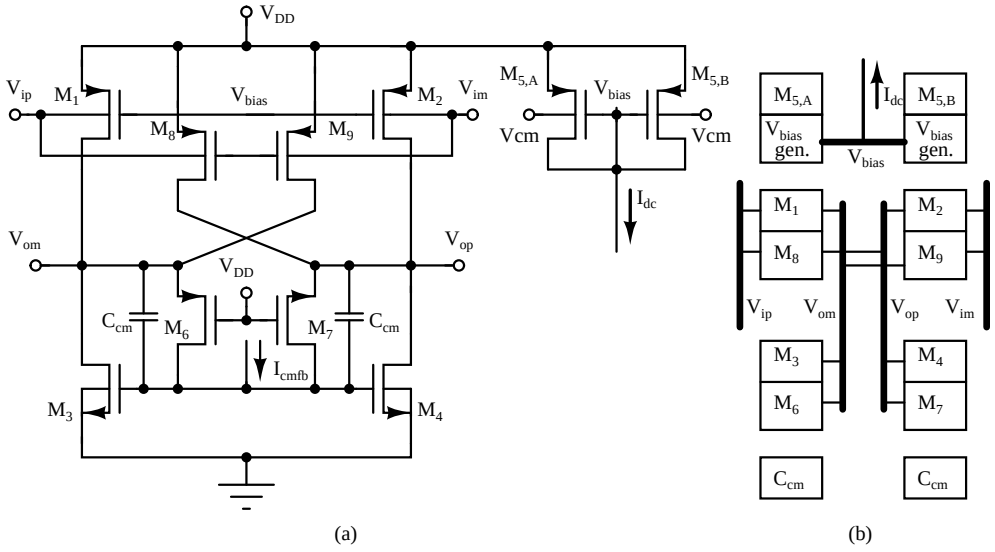


Figure 2.13: (a) Schematic of unit transconductor. (b) Layout scheme of unit transconductor.

are represented by simple blocks and the integrating capacitors are shown as gray colored boxes. The differential interconnects between these blocks are clearly shown to emphasize the fact that care has been taken to ensure that the inter connect parasitic capacitances seen by the differential lines are equal (Pavan, 1999). All the vertical routing

are made using *metal-1* and *metal-3*, while *metal-2* and *metal-4* are used for horizontal

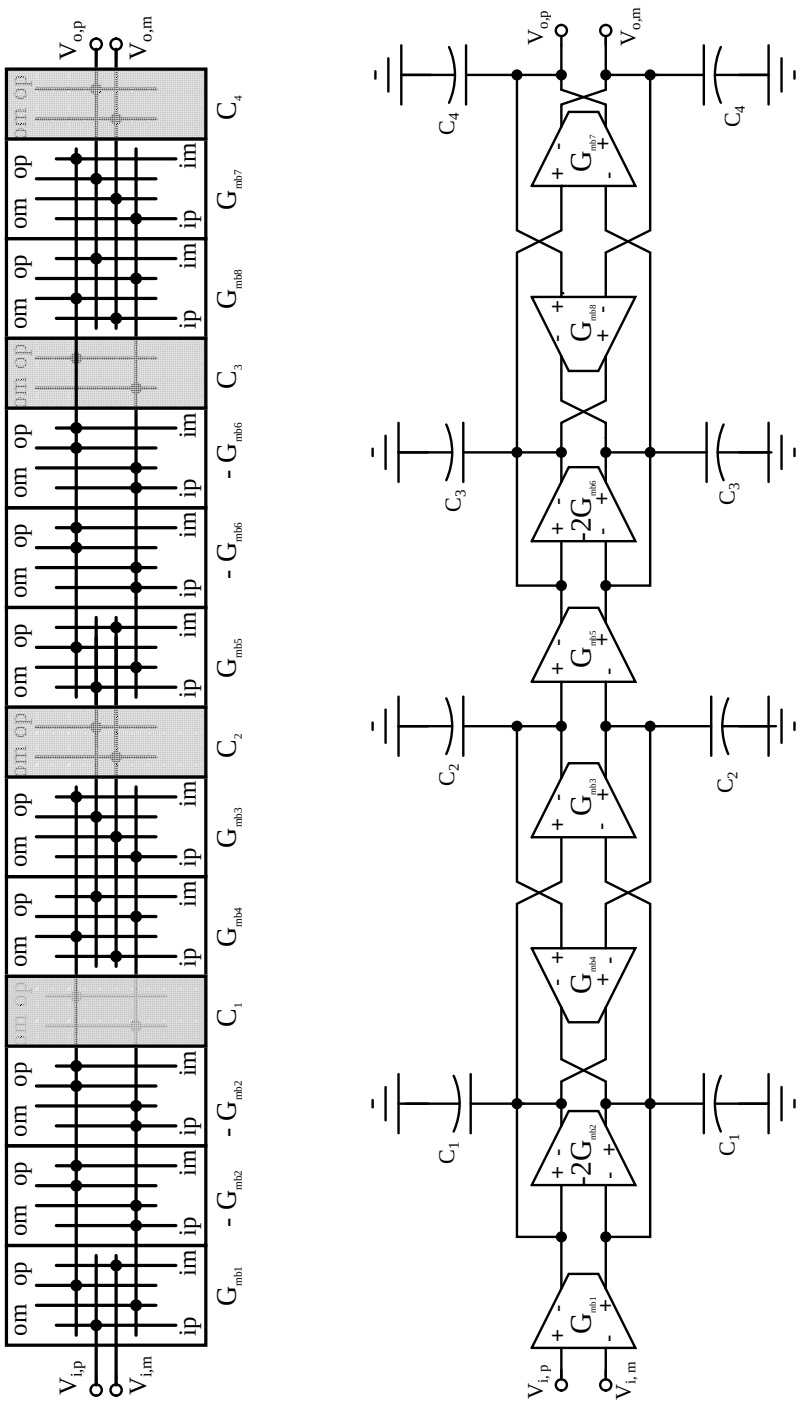


Figure 2.14: (a) Transconductor and capacitor placement scheme of filter layout. (b) Schematic of fully differential fourth order G_m-C filter.

routing. *metal-5* and *metal-6* are used only for routing associated with metal-insulator-metal (MIM) capacitors which are used as integrating capacitors.

A screen-shot of the filter layout is shown in Fig. 2.15 along with the test-buffers. The test buffers are used to drive the large capacitive load offered by the filter chip and input impedance of the measuring instruments. The total area occupied by the filter alone is $(500\times\ 250)\,\mu m^2$ (excluding test buffers). Empty space available in the chip are filled with bypass capacitors. NMOS and PMOS capacitors are used for bypassing. Simulations are done on the layout extracted netlist. Magnitude and phase response of the laid out filter are shown in Fig. 2.16 and Fig. 2.17 respectively. It is observed

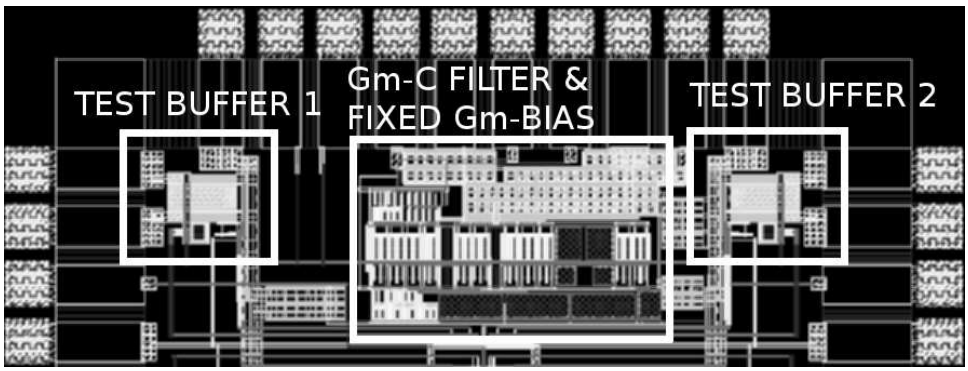


Figure 2.15: Screen-shot of layout of the complete filter along with test buffers.

that the response of the laid out filter deviates from ideal. Under ideal conditions the values of integrator capacitance C_1,C_2, C_3 and C_4 along with the bulk-transconductance decides the 3 dB bandwidth of the filter. But non-idealities, like parasitic capacitance and finite input/output impedance of the transconductors cause the frequency response to deviate from the Butterworth response. Typically, the filter response is brought back to ideal by tuning intended integrating capacitors using design centering method. Space mapping technique is found to be effective for design centering such filters (Laxminidhi and Pavan, 2007). This technique requires approximate model of the entire transistor level filter (Laxminidhi, 2007). The state-space technique is found very useful method. The design centering of the filter for the post layout extracted parasitics is done to get the response close to ideal 4^{th}order Butterworth response. Here, the integrator capacitors

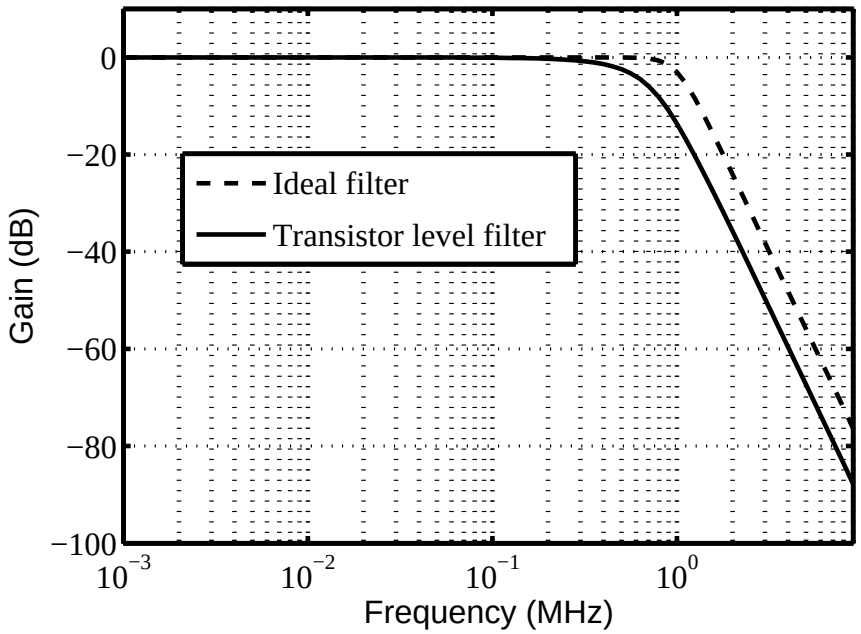


Figure 2.16: Magnitude response of the transistor level filter after extracting the layout parasitics.

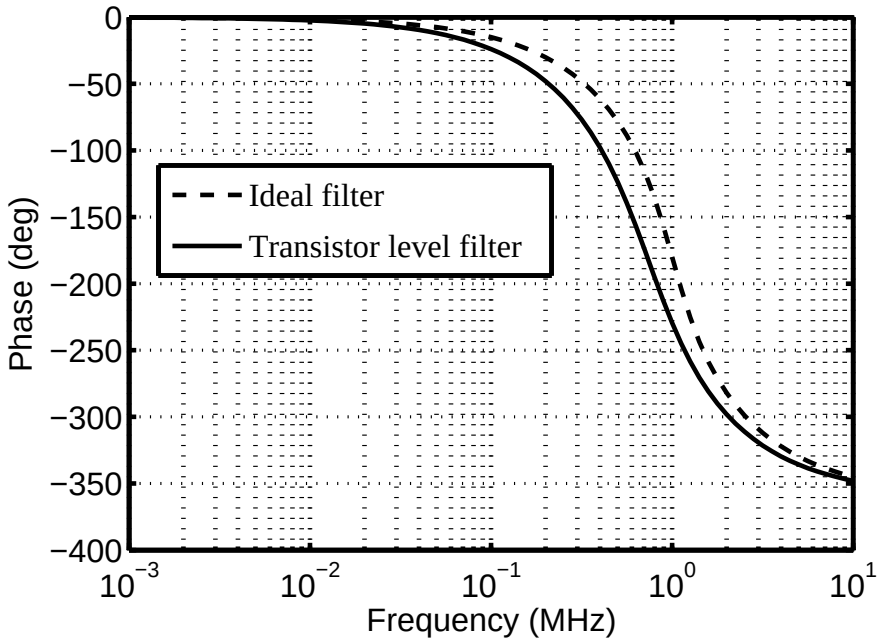


Figure 2.17: Phase response of the transistor level filter after extracting the layout parasitics.

C_1, C_2, C_3 and C_4 as used as variables to tune the filter response.

2.5.1 State Space Method

State-space model of a physical system is a mathematical model which defines the system with a set of input, output and state variables related by first-order differential equations. The most general state space representation of a linear time invariant (LTI) system with p inputs, q outputs and n state variables is written in the following form:

$$\dot{x}(t) = \mathbf{A}x(t) + \mathbf{B}u(t) \tag{2.15}$$

$$y(t) = \mathbf{C}x(t) + \mathbf{D}u(t) \tag{2.16}$$

$x(t)$ is called the 'state vector' of size $n\times 1$, $y(t)$ is the 'output vector' of size $q\times 1$, $u(t)$ is the 'input (or control) vector' of size $p\times 1$. **A** is a $n \times n$ matrix called 'state matrix', **B** is the $n \times p$ matrix named 'input matrix', **C** is the 'output matrix' of size $q \times n$ and **D** is the 'feedthrough (or feedforward) matrix' of size $q \times p$.

2.5.2 State Space Model for the Biquad

As a first step in deriving the model, state-space model for the first biquad is deduced. The voltage at the two integrating nodes of the biquad are taken as state variables. Fig. 2.18 shows the single ended small-signal equivalent circuit of the biquad (Fig. 2.3). V_{o1} and V_{o2} are the two state variables. The resistance r_1 is the effective resistance at node V_{o1}. It is to be noted that the transconductance g_{mb2} is absorbed into r_1. Therefore, r_1 is obtained by the parallel combination of $\left(\frac{1}{g_{mb2}}\right)$ and finite input/output resistances of the transconductors connected to that node. The capacitor c_1 includes all the parasitic capacitance (input and output) of the transconductors appearing at that node and intended integrating capacitance C_1. Similarly, the resistance r_2 and c_2 are computed.

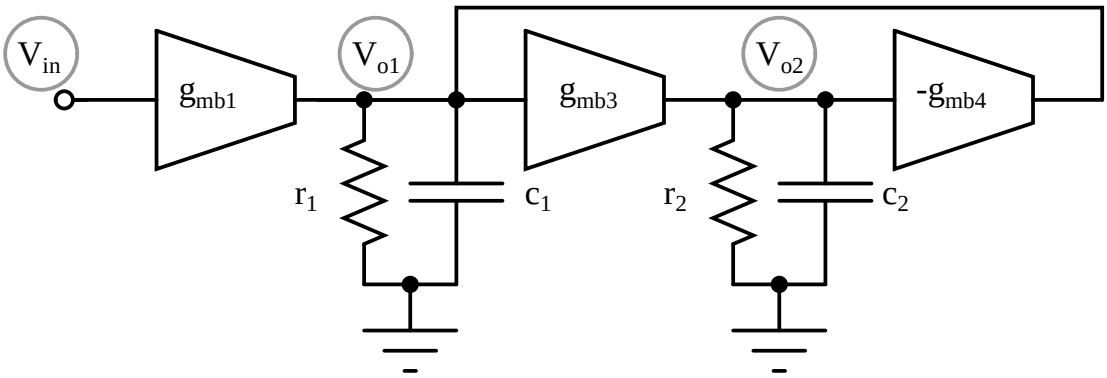


Figure 2.18: Small-signal equivalent circuit of second order G_m-C filter with state variable nodes.

But, for r_2 and c_2 it is also important to absorb the input impedance of the following biquad. The biquad has one input (V_{in}), one output (V_{o2}) and two state variables (V_{o1} and V_{o2}). Therefore, in (2.15) and (2.16), **A** is a 2×2 matrix, **B** is a 2×1 vector and **C** is a 1×2 vector. **D** is a null matrix since there is no feed feedforward path from input to output. Various elements of (2.15) and (2.16) can be written as follows

$$x(t) = [V_{o1}\ V_{o2}]^T \tag{2.17}$$

$$u(t) = [V_{in}] \tag{2.18}$$

$$y(t) = [V_{o2}] \tag{2.19}$$

$$\mathbf{A} = \left[\begin{array}{c|cc} & V_{o1} & V_{o2} \\ \hline V_{o1} & -\dfrac{1}{r_1 c_1} & -\dfrac{g_{mb4}}{c_1} \\ V_{o2} & \dfrac{g_{mb3}}{c_2} & -\dfrac{1}{r_2 c_2} \end{array}\right] \tag{2.20}$$

$$\mathbf{B} = \left[\begin{array}{c|c} & V_{in} \\ \hline V_{o1} & \dfrac{g_{mb1}}{c_1} \\ V_{o2} & 0 \end{array}\right] \tag{2.21}$$

$$\mathbf{C} = [0\ 1] \tag{2.22}$$

The transconductance, resistance and capacitance values are taken from DC operating point of the designed transistor level filter and are listed below.

$$g_{mb1,3,4} = 10\,\mu\text{S}, \quad g_{mb2} = 20\,\mu\text{S},$$
$$r_1 = 43\,k\Omega, \quad r_2 = 2.1\,M\Omega,$$
$$c_1 = 1.88\text{ pF}, \quad c_2 = 0.61\text{ pF}.$$

The frequency response of derived state-space model of the biquad is compared with that of the transistor level circuit in Fig. 6.3. The response is obtained for one arbitrary set of intended integrating capacitances C_1 and C_2. The model is found to be fairly accurate replica of the actual biquad. A similar exercise has been executed for the

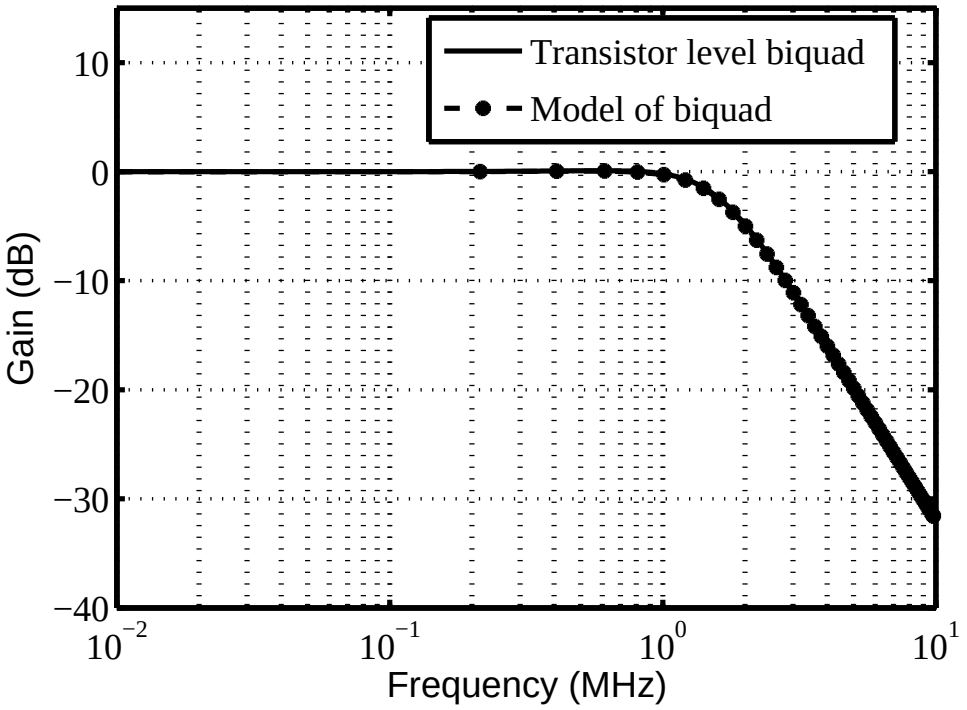


Figure 2.19: Magnitude response of the first biquad: transistor level and state-space model

second biquad (having Q=1.306) and the model is derived. The model of the fourth order filter is then derived by cascading the two biquad models, which is easily achieved in *MATLAB*. The frequency response of the so modeled filter is compared with the transistor level filter in Fig. 2.20.

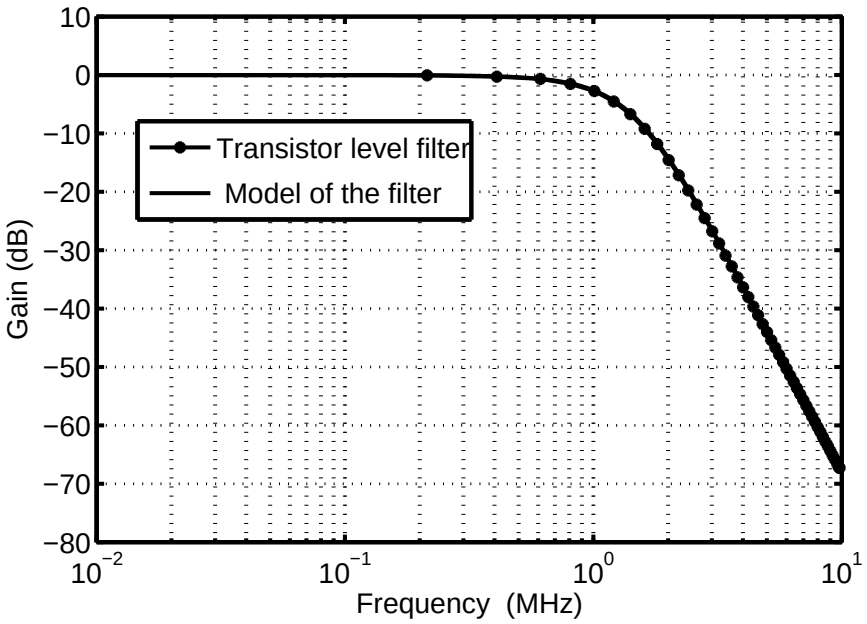


Figure 2.20: Magnitude response of the fourth order filter: transistor level and state-space model.

2.5.3 Design Centering Process

The procedure used to design center the filter in presence of layout parasitics is similar to that outlined in (Laxminidhi and Pavan, 2007). For the sake of completeness, the procedure is briefly outlined below.

1. The state-space model of the filter, derived in section 2.5.2, is optimized to offer a response (say, $M(f)$) close to ideal (say $I(f)$). The optimization is done by tuning the intended integrating capacitors $\mathbf{C} = [C_1\ C_2\ C_3\ C_4]$ by using *fminsearch* routine in *MATLAB*. Let us denote this set of capacitors as $\mathbf{C_M}$.

2. The so obtained $\mathbf{C_M}$ is put in the schematic of the transistor level filter. Since the model is accurate, the response of the transistor level filter for the set of capacitors $\mathbf{C_M}$ will also closely match with that of ideal. Therefore, it is now ensured that the schematic is design centered in presence of transconductor parasitics.

3. These capacitors are then used in the layout and the response of the layout extracted netlist (say $L(f)$) is obtained. $L(f)$ will be in deviation from ideal, but this is only due to the layout parasitics.

4. The response $L(f)$ is taken to *MATLAB* and the model response $M(f)$ is tuned to $L(f)$. The final optimized capacitor set is denoted by $\mathbf{C_L}$. It can be noted that

each capacitor in $\mathbf{C_L}$ has two components i.e. for i^{th} capacitor $\mathbf{C_{iL}} = \mathbf{C_{iM}} + \mathbf{C_{i,par}}$ where, $\mathbf{C_{i,par}}$ is the parasitic capacitance introduced due to the layout.

5. The layout parasitic capacitor, present at each integrating node, is then estimated using the equation $\mathbf{C_{par}} = \mathbf{C_M} - \mathbf{C_L}$.

6. The intended integrating capacitors which need to be put in the layout is now calculated as $\mathbf{C_{L,\,to\,be\,put}} = \mathbf{C_M} - \mathbf{C_{par}}$.

7. The response of the layout extracted netlist, with $\mathbf{C_{L,\,to\,be\,put}}$ placed in the layout, is obtained to ensure that it is in close match with the ideal.

Figure. 2.21 and Fig. 2.22 shows the magnitude and phase response of the post layout filter after design centering. It is seen that the post layout response matches closely with the ideal response. The final set of intended integrating capacitors is [0.454 0.367 3.294 0] pF. Note that, the capacitance required at the fourth integrating node (i.e. output) is entirely contributed by parasitics. Simulations are carried out to observe the

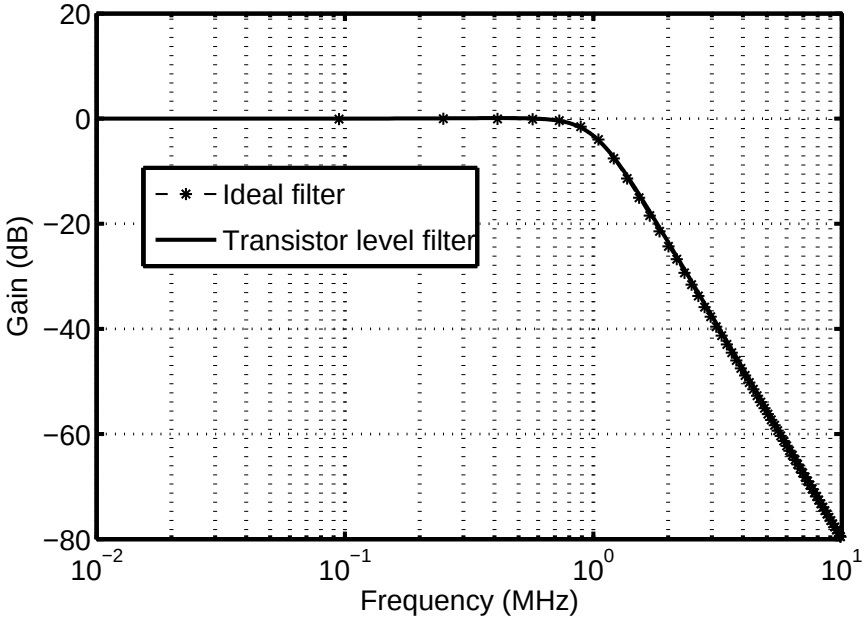


Figure 2.21: Magnitude response of transistor level filter after design centering.

frequency response at various process corners, supply voltage and temperature variations. The Fig. 2.23 shows the normalized magnitude response at various process corners namely, *tt* (typical), *ss* (slow NMOS slow PMOS), *ff* (fast NMOS fast PMOS),

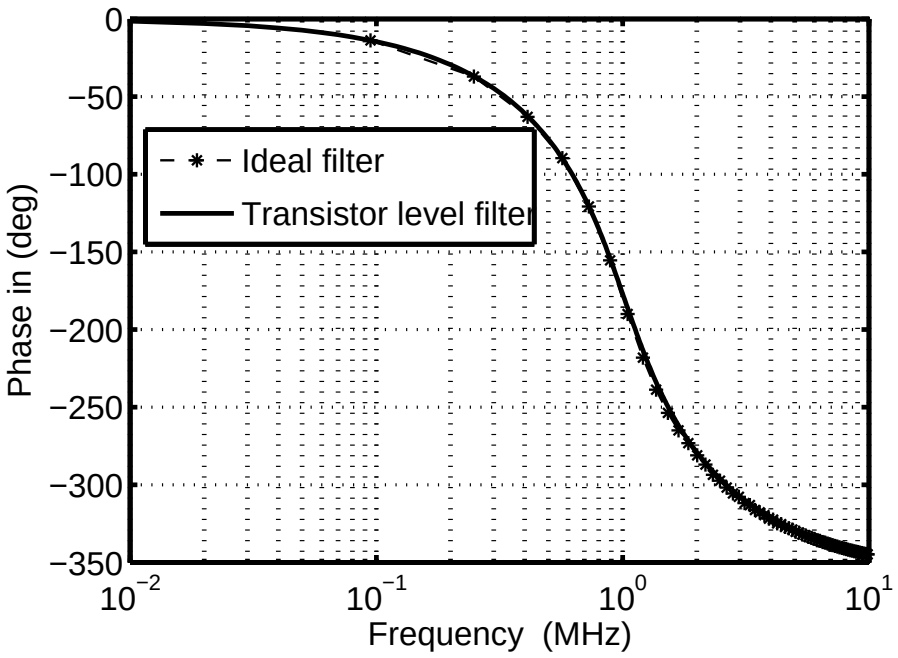


Figure 2.22: Phase response of transistor level filter after design centering.

snfp (slow NMOS fast PMOS) and *fnsp* (fast NMOS slow PMOS). It is observed that the change in bandwidth across the corners is less than $\pm 1.67\,\%$ at room temperature and nominal supply voltage of 0.5 V. The normalized magnitude response for 0-

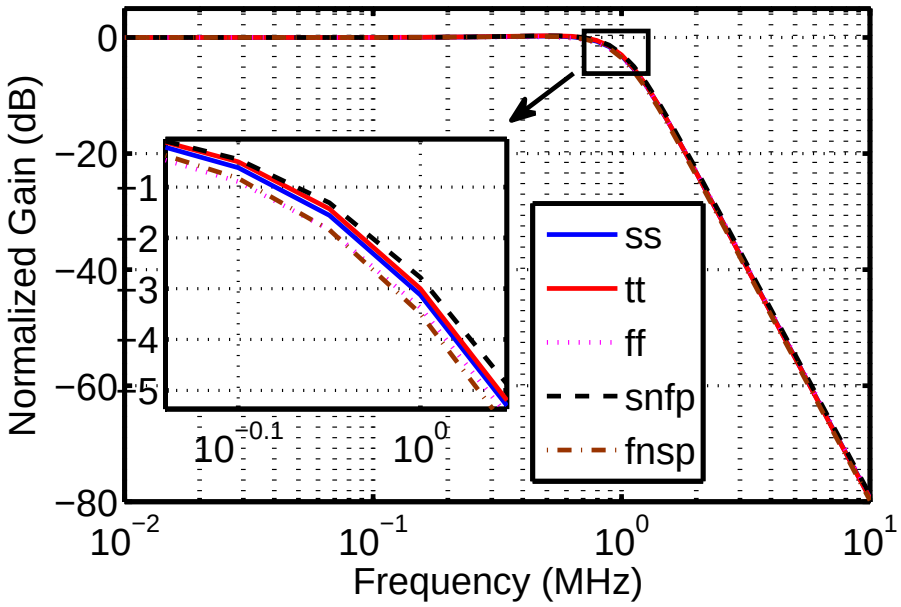


Figure 2.23: Magnitude response across different process corners at room temperature.

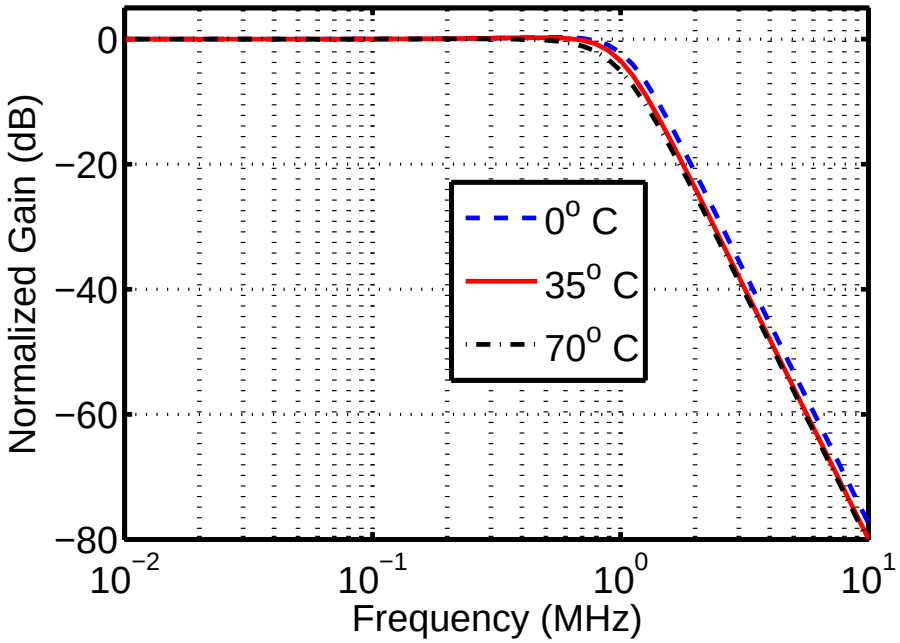


Figure 2.24: Magnitude response for change in temperature range of 0-70 °C at typical corner and nominal supply voltage of 0.5 V.

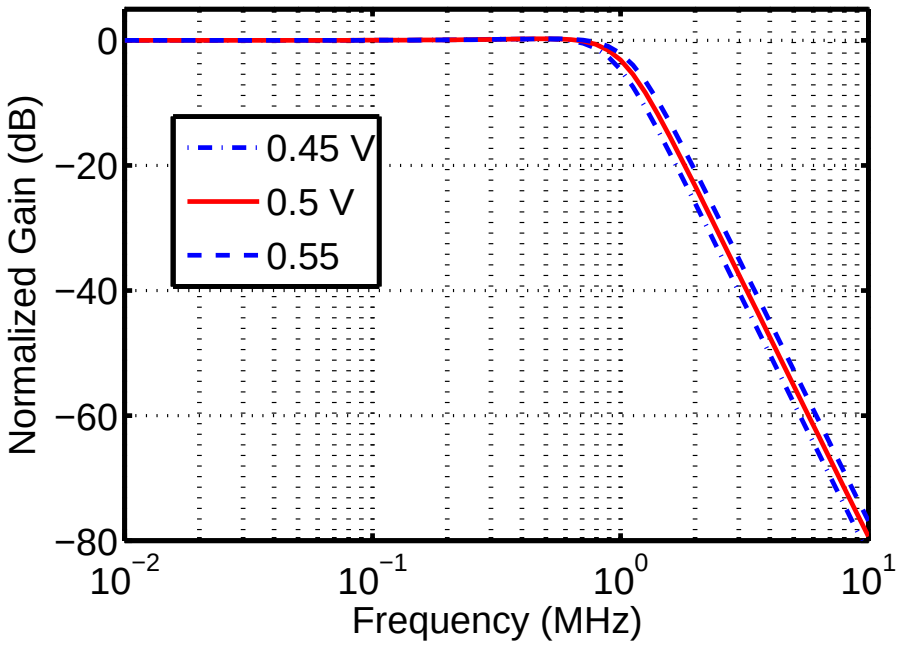


Figure 2.25: Magnitude response for 10 % change in supply voltage from its nominal value of 0.5 V at room temperature, at typical process corner.

70 °C change in temperature at nominal supply voltage and typical corner is shown in Fig. 2.24. It indicates that the change in bandwidth is less than ±9.1 %. The normal-

ized frequency response variation for $\pm 10\,\%$ change in supply voltage from its nominal value of 0.5 V at room temperature and at typical process corner is shown in Fig. 2.25. From the figure it is observed that the change in bandwidth is less than $\pm 7.07\dot{\%}$.

2.5.4 Monte Carlo Analysis

The mismatch between the devices in the transconductor can effect the bandwidth of the filter, specially when the transistors are operated in subthreshold region. To observe the effect of mismatch on the bandwidth a Monte Carlo simulation has been carried out on the complete layout extracted filter. Figure 2.26 shows the distribution of the 3-dB bandwidth for 200 samples. It is observed that the distribution has a mean of about 950 kHz with standard deviation of about 30 kHz. A plot of normalized magnitude response for all 200 samples is shown in the Fig. 2.27. The results show that there is no serious degradation in the filter bandwidth and response.

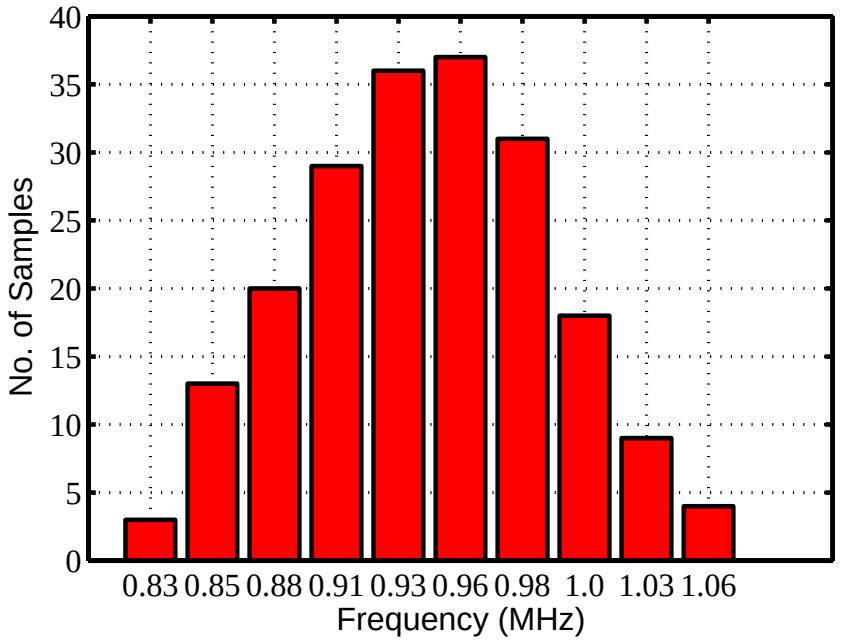


Figure 2.26: Distribution of 3-dB bandwidth obtained from the Monte Carlo simulation.

The designed low-pass fourth-order Butterworth G_m-C filter is fabricated using

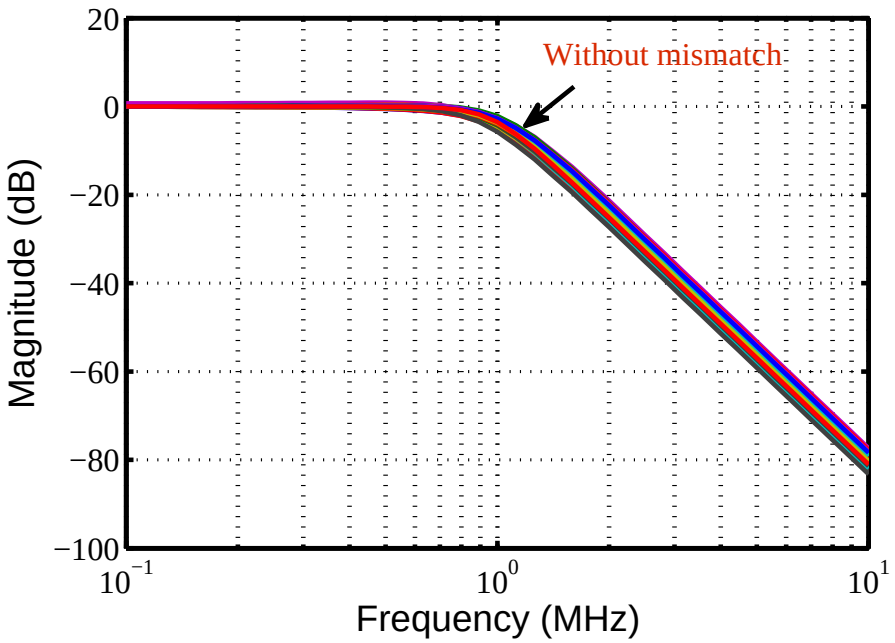


Figure 2.27: Normalized magnitude response of the filter obtained from Monte Carlo simulation.

UMC 0.18 μm CMOS process. The filter is fabricated on silicon at *IMEC*, Belgium through *EUROPRACTICE* and the test results are presented in Chapter 4. The next chapter explains a fixed bias circuit proposed to fix the bulk/gate transconductance of a transconductor for sub-1 V supply operations which is necessary to fix the filter response across PVT.

CHAPTER 3

FIXED TRANSCONDUCTANCE BIAS GENERATING CIRCUIT

Integrated circuits are always designed for robustness against the changes in the variation in its environment such as supply voltage and temperature. In addition, the designer is also required to ensure that his design is robust against process variations. If not taken care, the performance of the post fabrication design can go beyond the tolerance limits in which case, the design may become useless.

For continuous-time G_m-C filters, the frequency response is the primary parameter of interest. The response of such filters depends on transconductance and capacitance. The change in capacitance over process, voltage and temperature variations is found to be minimum while the transconductance can change by more than 30%. Therefore, it is imperative to maintain a constant transconductance across PVT. For gate driven transconductors, it is necessary to fix the gate transconductance while if the transconductor is bulk-driven, it is required to fix the bulk-transconductance. In literature there are a few circuits that are designed to fix the transconductance of gate driven transconductor (Steininger, 1990; Zele and Allstot, 1996; Pavan, 2004). However, there is no work found in the literature which is dedicated to fix the bulk-transconductance. An alternative approach, which is found in the literature, is to use a dedicated automatic tuning loop which fixes the time constant of the circuit and is commonly applicable to both gate driven and bulk driven transconductors (Schaumann and Tan, 1989; Stevenson and Sanchez-Sinencio, 1998; Chatterjee et al., 2005). Though this is found to be quite effective, but at the expense of increased complexity, area and power.

The conventional fixed transconductance bias circuits lack the necessary headroom while operating on low supply voltages down to 0.5 V. The circuits in (Steininger, 1990; Zele and Allstot, 1996; Pavan, 2004) have serious limitations as their performance predominantly depends on the accuracy of current mirroring. The mirroring accuracy could be very poor in low supply voltage operation. The circuit in (Pavan, 2004), in addition, is complex. In the light of these observations, a need is felt for a simple circuit that can fix the transconductance (gate/body) of a transconductor to the best possible extent when operating at supply voltages down to 0.5 V. This chapter proposes a simple circuit to fix the gate/body transconductance of a transistor in a transconductor cell for 0.5 V supply operation. The pseudo-differential transconductor used for designing the filter in the chapter 2 has been used as the test vehicle to validate the proposed circuit. The chapter also brings out the limitations of the circuits proposed in (Steininger, 1990; Zele and Allstot, 1996) through necessary simulations.

Though these circuits basically attempt to fix the gate transconductance, it is assumed (at-least to the first order) that fixing the gate transconductance would also fix the bulk-transconductance due to the following reason. The bulk-transconductance of the transistor operating in saturation region is given by

$$g_{mb} = \eta \times g_m \tag{3.1}$$

where, g_m is the transconductance and η is given by

$$\eta = \frac{\gamma}{2\sqrt{2\phi_b + V_{SB}}} \tag{3.2}$$

γ is body effect parameter is given by $\gamma = \sqrt{2q\varepsilon_s N_A}/C_{ox}$. For a given technology node, γ is independent of supply voltage and temperature. ϕ_b is the surface potential and its variation against the variations in supply voltage and temperature is assumed to be negligible. If the source-to-bulk voltage (V_{SB}) is maintained constant, then from (3.2),

the dependency of η on temperature and supply voltage variation will be negligible. Therefore, g_{mb} will have the same variation as that of g_m against temperature and supply voltage.

The transconductor whose bulk-transconductance need to be fixed is shown in Fig. 3.1. Transistors M_1-M_4 form the pseudo-differential transconductor. The current I_{BIAS} in the two legs of the transconductor sets the gate/body transconductance of the PMOS input transistors.

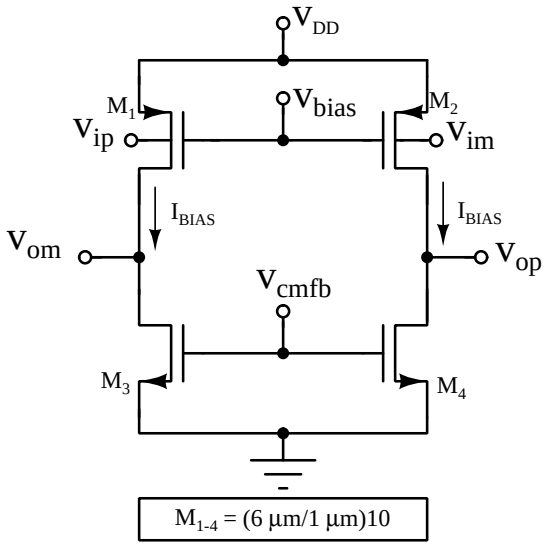
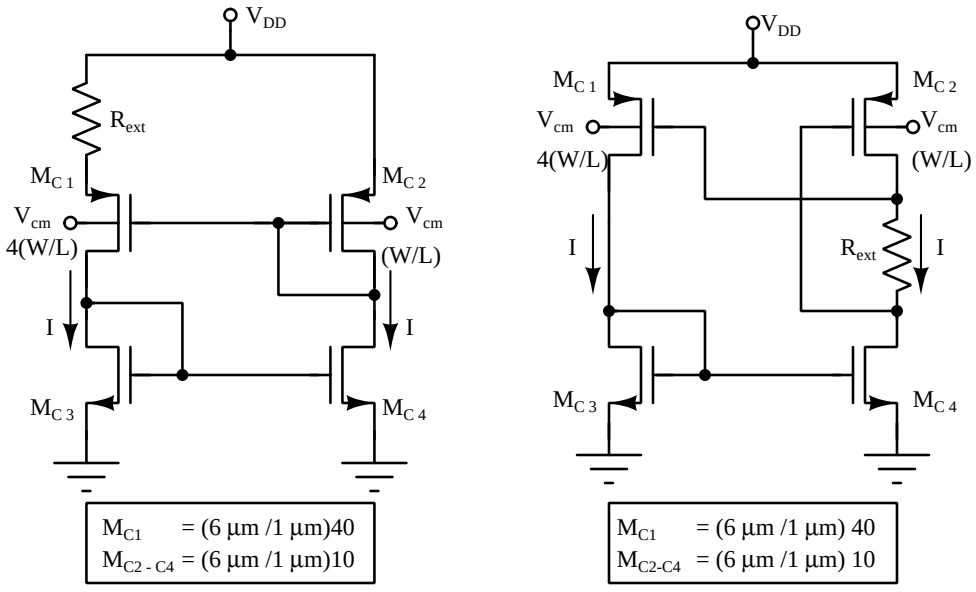


Figure 3.1: Schematic of bulk-driven pseudo-differential transconductor.

The following section highlights the limitations of conventional fixed bias circuits when used for a low-voltage transconductor.

3.1 CONVENTIONAL BIAS CIRCUITS

Figure 3.2 shows PMOS version of the two conventional circuits. In both the circuits, a negative feedback loop servos the gate-transconductance of transistor M_{C2} to a resistor R_{ext} which is assumed to be thermally stable ($g_{m,M_{C2}} = 1/R_{ext}$). The current I set up in M_{C2} should be mirrored as I_{BIAS} to the input transistors M_1 and M_2 of the transconductor



(a) (b)

Figure 3.2: Conventional fixed bias circuits: (a) Simple scheme presented in (Steininger, 1990). (b) Modified circuit to eliminate back-gate effect presented in (Zele and Allstot, 1996).

(in Fig. 3.1). If M_{C2} and $M_{1,2}$ are equally sized then it is required that $I_{BIAS} = I$ so as to have $g_{m,M_{1,2}} = g_{m,M_{C2}} = 1/R_{ext}$.

Figure 3.3 shows a simple biasing scheme to distribute the current from the fixed transconductance bias circuit to the transconductor. Here, the current I set up in M_{C2} is mirrored to $M_{1,2}$ using a current distribution circuit formed by M_{C5} and M_5. The transistor M_5 is local to the transconductor while M_{C5} is local to the fixed bias circuit. Similar arrangement can be made for all transconductors of interest. It is to be noted that, current distribution is preferred over voltage distribution for analog integrated circuits specially when the transconductors are located far away from the bias generating circuit.

However, the following points can be observed for the above conventional fixed bias circuit and bias distribution scheme.

- The analysis assumes square law for the devices and that the currents are mirrored

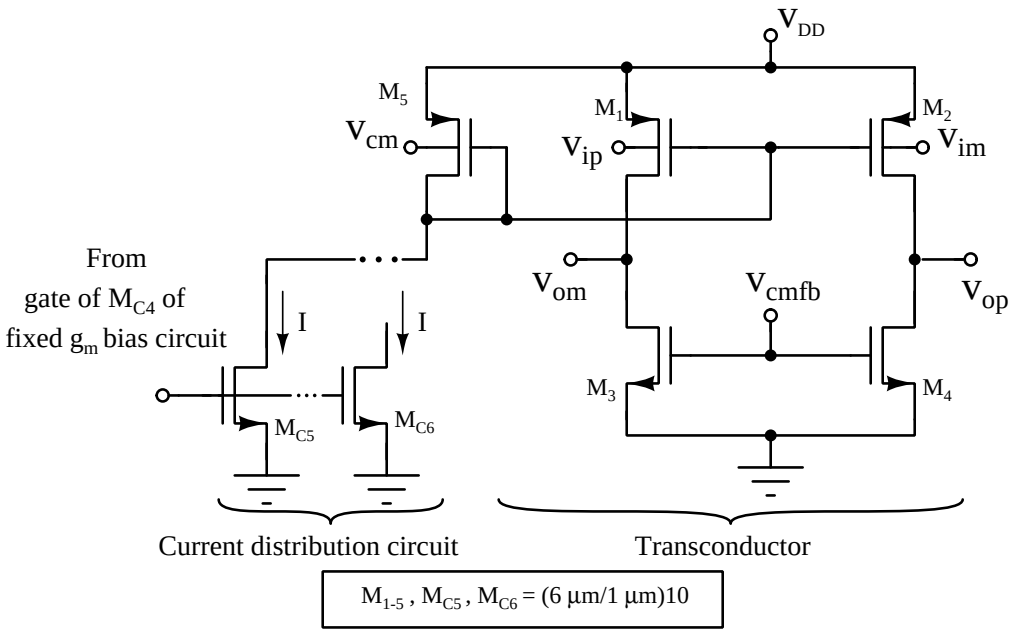


Figure 3.3: The transconductor and the biasing scheme used to distribute the current generated in fixed transconductance bias circuit to the transconductor.

accurately by M_{C3} and M_{C4} i.e. ($I_{D,M_{C1}} = I_{D,M_{C2}} = I$). However, this assumption becomes weak since high output conductance of M_{C3} and M_{C4} affect the mirroring accuracy and can be significant in the case of short channel devices.

- With the lower supply voltage (V_{DD}) in standard CMOS process, NMOS current mirror can be in-accurate due to two reasons. First, the transistor M_{C4} may be forced to operate in triode region by diode connected M_{C4} and the second is that even with M_{C4} in saturation, M_{C3} and M_{C4} may have different drain-source voltages.
- M_{C5} also carries the current I since they are sized equal and $V_{DS,C5} = V_{DS,C4}$.
- It is M_5 which carries I and not $M_{1,2}$ since, the mirroring between M_5 and $M_{1,2}$ is inaccurate.

From the observations put forward above, it is clear that the circuit will neither be in a position to track $g_{m,M_{C2}}$ to R_{ext} nor in a position to track $g_{m,M_{1,2}}$ to R_{ext}. Thus resulting in a significant dependency of $g_{m,M_{1,2}}$ on PVT.

To validate the above mentioned short-falls of the conventional circuits, the circuit in Fig. 3.2(b) is designed to bias the pseudo-differential transconductor shown in Fig. 3.1 using the bias distribution scheme shown in Fig. 3.3. Simulations are done

to assess the performance of the circuit for supply voltage in the range 0.5 V$\pm$10%, temperature in the range 0-70^{o}C and five process corners of UMC 0.18 μm technology. The observed variations in transconductance and bulk-transconductance across PVT are shown in Fig. 3.4. V_{SB} of the PMOS transistors are kept constant at 0.25 V during the simulation.

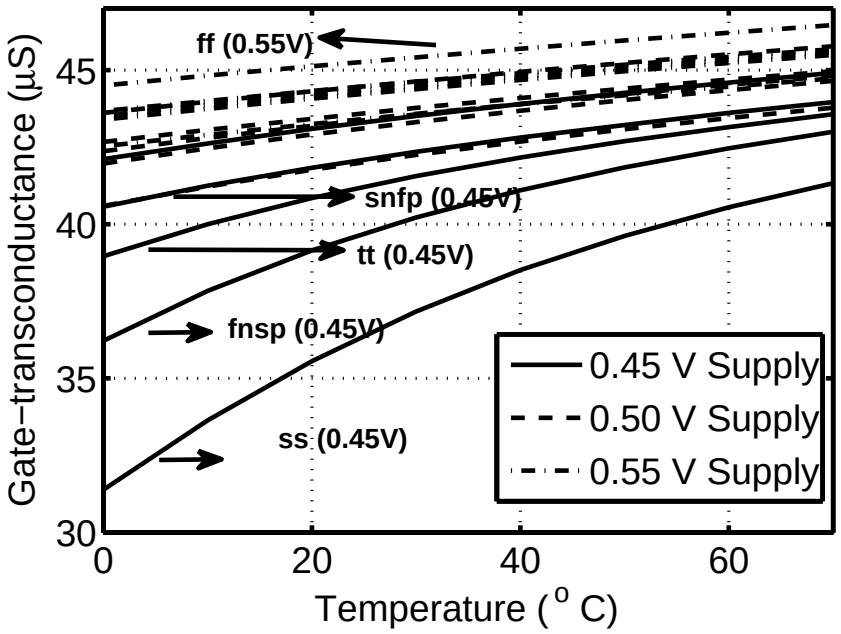
It is to be noted that the R_{ext} is tuned to set the bulk-transconductance of $M_{1,2}$ to the desired 10 μS at nominal PVT. For supply voltage below 0.5 V, it can be seen that the circuit fails to offer effective performance. At 0.45 V, for *ss* (slow NMOS slow PMOS) corner, the performance is very poor with the bulk-transconductance deviating by 15 % below the nominal value of 10 μS at room temperature. The variation is even verse (about -25 %) when the temperature is zero degrees Celsius. For supply voltages above 0.5 V the deviations is found to be below 10 % for all corners and temperature. For *ff* (fast NMOS fast PMOS) corner, the deviation in bulk-transconductance is found to be about 5 % (maximum positive deviation) at 70°Cand 0.55 V.

Variation in the gate-transconductance and bulk-transconductance are similar since V_{SB} of the input transistors are kept constant. The variation in transconductance across supply voltage for different corners is highlighted in Fig. 3.5. The figures (a) and (b) show the gate-transconductance and bulk-transconductance variation respectively for $\pm$10 % change in supply voltage from nominal value, at room temperature and five process corners.

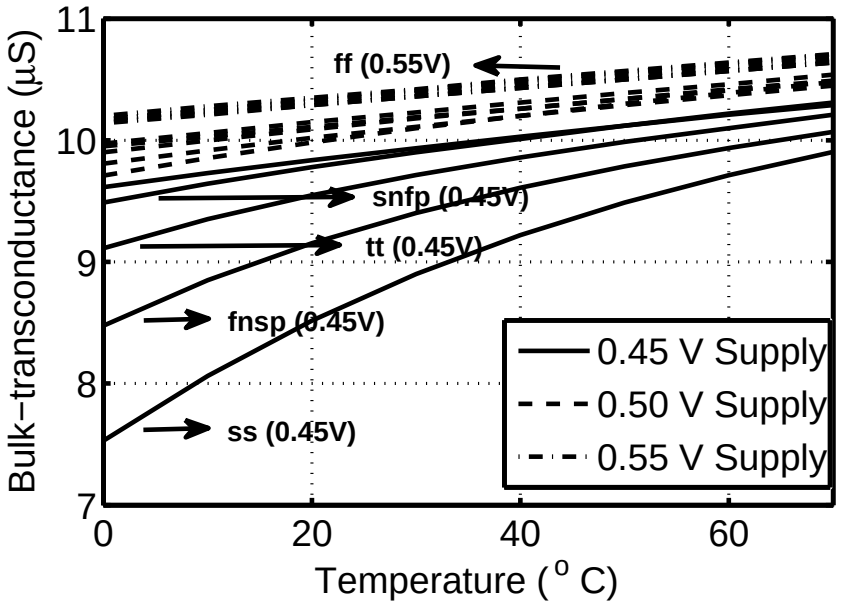
3.2 PROPOSED FIXED-BIAS CIRCUIT

3.2.1 Proposal

The conventional technique to fix the transconductance failed to offer the desired performance at voltages below 0.5 V for one of the corners (*ss* corner). This means that,

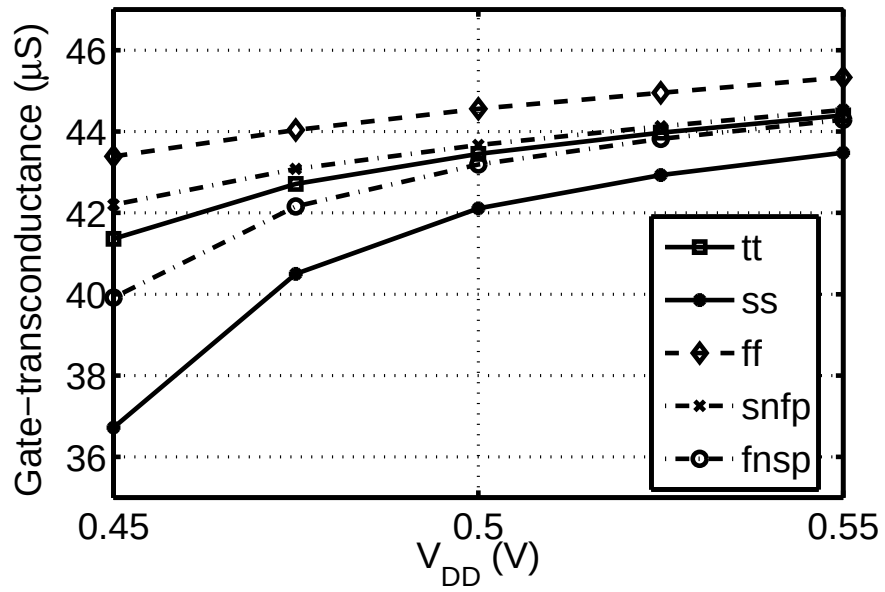


(a)

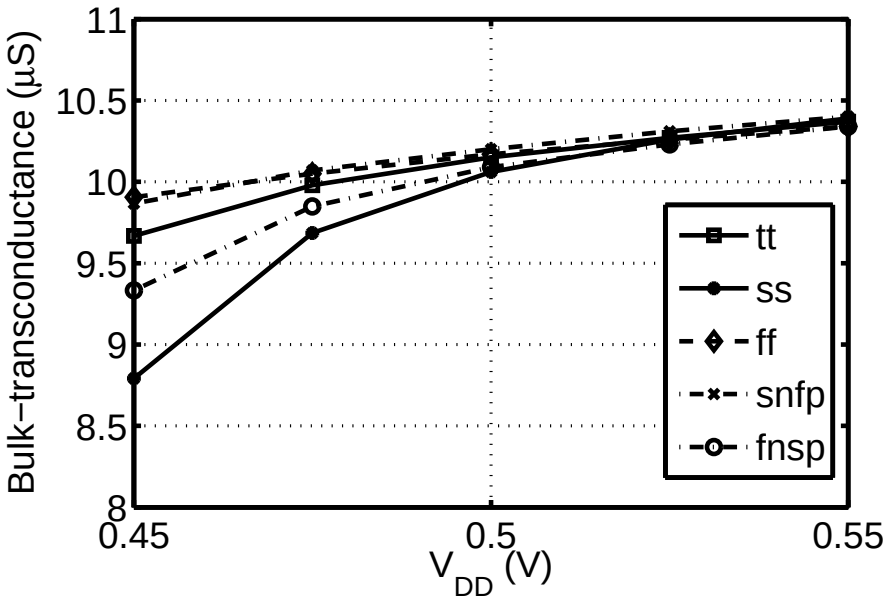


(b)

Figure 3.4: Performance of conventional fixed bias circuit across PVT variations: (a) Gate-transconductance (b) Bulk-transconductance (in both the cases, V_{SB} of the PMOS transistors is maintained at constant).



(a)



(b)

Figure 3.5: Performance of conventional fixed bias circuit for supply voltage and five process corners at room temperature: (a) Gate-transconductance. (b) Bulk-transconductance (in both the cases, V_{SB} of the PMOS transistors is maintained at constant).

50 mV deviation in supply voltage from the nominal 0.5 V can degrade the performance of the filter if the chip falls on *ss* corner. Under practical operating conditions, it is very difficult to maintain the supply voltage under tight limits. In semiconductor industry, it is common to expect that the design offers satisfactory performance for all process corners, as this would increase the yield.

A fixed transconductance bias circuit attempts to tune the current in the transistor in such a way to compensate for the transistor parameter variations across PVT. If this tuned current is not mirrored accurately to the desired transconductor cell, the transconductance of the transconductor will obviously be in deviation and the same has been observed in the case of conventional fixed bias circuit. Though an attempt is made to improve the mirroring accuracy through the bias distribution circuit (Fig. 3.3), inaccurate mirroring in the fixed-transconductance bias circuit and in the transconductor cell had notable effect.

As an alternative method, we propose to fix the current in the transistor constant across PVT variations. It is interesting to see that if the current is fixed in the transistor, its transconductance will be independent of supply voltage. However, the transconductance will still be dependent on temperature and process.

Assuming that the PMOS input transistor of the transconductor is in saturation, its transconductance can be written as

$$g_m = \sqrt{\mu_p C_{ox} \left(\frac{W}{L}\right) I_D} \tag{3.3}$$

If the drain current I_D is maintained constant, the change in g_m normalized to its nominal value $g_{m,nom}$ can be written in the form

$$\frac{\Delta g_m}{g_{m,nom}} = \frac{1}{2}\left(\frac{\Delta \mu_p}{\mu_{p,nom}} - \frac{\Delta t_{ox}}{t_{ox,nom}}\right) \tag{3.4}$$

where, t_{ox} is the oxide thickness and $t_{ox,nom}$ is nominal value. Since, t_{ox} is independent of temperature, the change in g_m due to temperature is only due to associated change in the mobility μ_p. The dependency of μ_p on temperature as per BSIM3v2 model is given by (3.5),

$$\mu_p(T) = \mu_p(T_o)\left(\frac{T}{T_o}\right)^{-0.5} \tag{3.5}$$

$\mu_p(T)$ is the mobility of the PMOS transistor at any temperature T (in °K), $\mu(T_o)$ is the mobility at nominal temperature T_o (in °K), i.e. $\mu(T_o) = \mu_{p,nom}$. From (3.5), it can be seen that at 70°C, the mobility decreases by 6.5 % from its nominal value computed at room temperature (27°C). This implies from (3.4), that the transconductance will change only by -3.25 % (at 70°C) from its nominal value.

Let us now consider the effect of process variation. For 0.18 μm standard CMOS process used in this work, worst case was found for *ss* and *ff* corners. For *ss* corner, $\frac{\Delta\mu_p}{\mu_{p,nom}}$ =-3 % and $\frac{\Delta t_{ox}}{t_{ox,nom}}$ =2.5 % which results in net deviation of -2.75 % for g_m from its nominal value evaluated at *tt* corner. Similarly, for *ff* corner, $\frac{\Delta\mu_p}{\mu_{p,nom}}$ =+3 % and $\frac{\Delta t_{ox}}{t_{ox,nom}}$ =-2.5 % resulting in 2.75 % change in g_m from its nominal value.

From the above analysis, it is observed that, if the current in the transconductor is set constant, the maximum percentage variation in the transconductance is about $\pm$6 % across PVT variations. Therefore, it is worthwhile to use a 'fixed-current bias circuit' in place of 'fixed-transconductance bias circuit' for low voltage. The following subsection outlines the implementation of such a circuit.

3.2.2 Fixed-Current Bias Circuit

A simple scheme to fix the drain current of a transistor is shown in Fig. 3.6. A negative feedback loop sets the drain current of the transistor M_{f1} to a constant value $I_{BIAS} = V_{ref}/R_{ext}$ where, V_{ref} is a constant voltage and R_{ext} is a thermally stable off-chip resistor. The gate voltage of M_{f1} is used to drive the input transistors ($M_{1,2}$ in the figure) of the

transconductor. If M_{f1} is sized equal to that of $M_{1,2}$, the current in $M_{1,2}$ will also be equal to I_{BIAS}. This current will be independent of PVT since V_{ref} and R_{ext} are assumed to be independent of PVT.

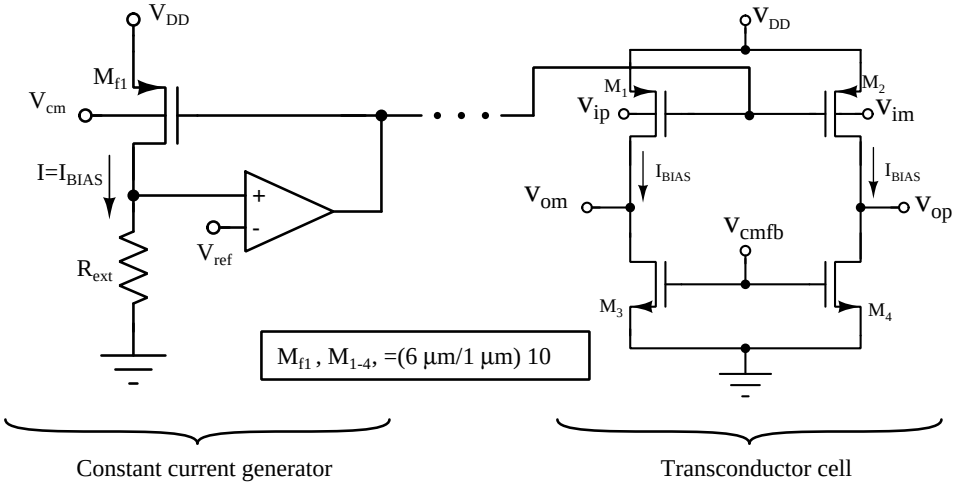


Figure 3.6: A simple constant current bias generator.

The simple scheme, however, is not suitable for biasing transconductors that are placed far away from the bias generating circuit. This is because it uses voltage distribution scheme for biasing the transconductors and any voltage drop in the path can lead to systematic mismatch between the transconductors. In such situations, current distribution is commonly preferred as the voltage required to bias the transistors can be generated locally at the transconductor.

The simple current generating circuit shown in Fig. 3.6 is modified to achieve current distribution without the loss of accuracy and is shown in Fig. 3.7. The transistor M_{f1} is sized equal to that of input transistors $M_{1,2}$ of the transconductor. M_{f2} and M_5 are also sized equal. Similar to the simple current generating scheme (shown in Fig. 3.6), the negative feedback loop sets the current (I_{BIAS}) in M_{f1} equal to V_{ref}/R_{ext}. The error amplifier is realized using a simple pseudo-differential amplifier with a current-mirror load as shown in the inset of Fig. 3.7.

It is to be noted that the errors arising due to mismatch in mirroring are effectively

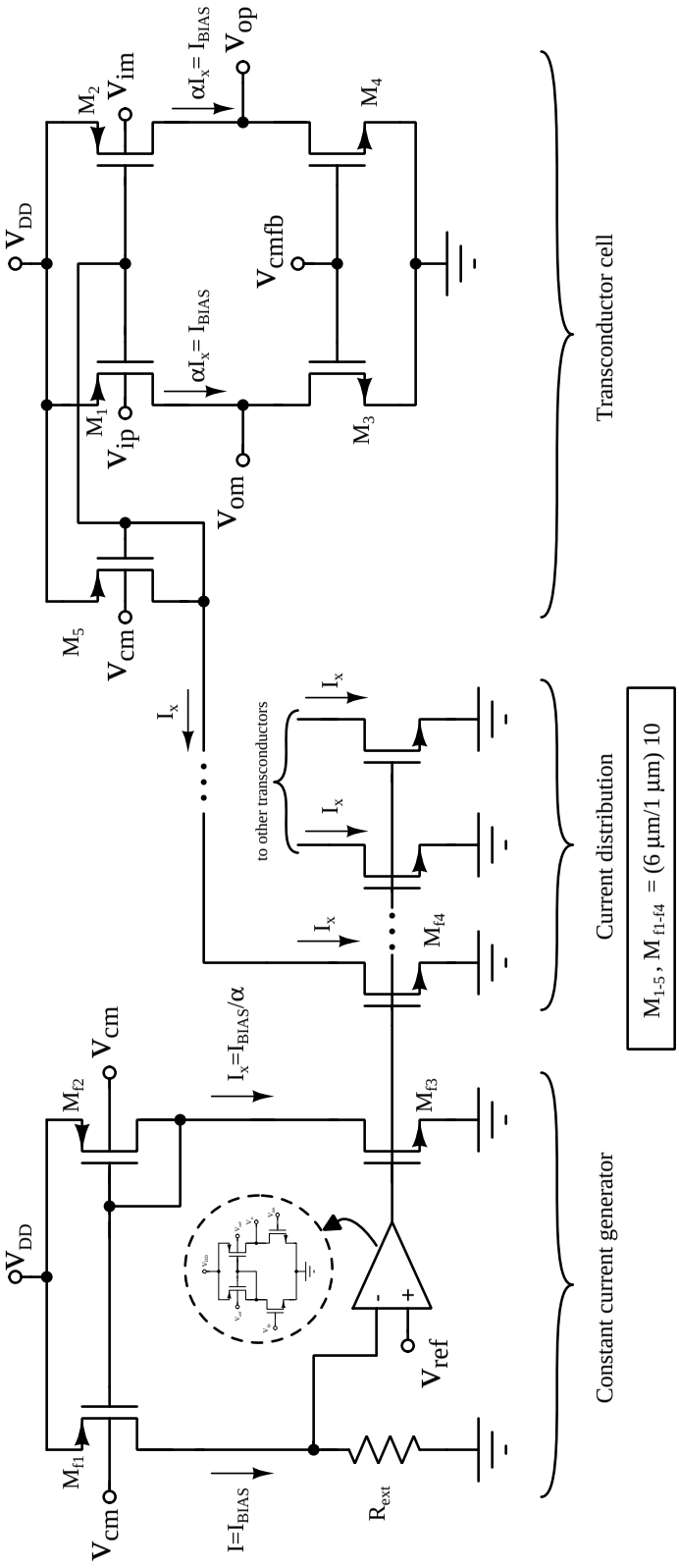


Figure 3.7: Modified constant current bias generator along with current distribution scheme.

canceled. Thanks to the effective bias distribution scheme. The feedback loop has a current mirror formed by M_{f1} and M_{f2}. Due to the V_{DS} mis-match, $I_{D,f2} \neq I_{D,f1}$. Let us say, $I_{D,f2} = I_x = I_{BIAS}/\alpha$. This current is then distributed through M_{f4}, M_{f5},... to all the transconductors. Here, there will not be any error in mirroring of currents, since V_{DS} of M_{f3}, M_{f4}, M_{f5} ... are all made equal by the circuit arrangement. For example, $V_{DS,f3} = V_{DS,f4}$ since M_{f2} and M_5 have equal size (or in other words equal current density) and therefore, transistor M_5 will carry a current I_x ($= I_{BIAS}/\alpha$). In the transconductor, the current in M_5 is mirrored to $M_{1,2}$, but with an error. This error is equal and opposite to that between M_{f1} and M_{f2}. As a result, the current in $M_{1,2}$ will be exactly equal to that of M_{f1}, or in other words, $I_{D,1} = I_{D,2} = I_{BIAS}$.

From the above analysis, it is evident that, as long as the current generated in the current generator circuit is constant, the current set up in the transconductor will also be constant. In this work, the transconductors are required to carry $2\,\mu$A for a bulk-transconductance of approximately $10\,\mu$S. Therefore, R_{ext} is set at $125\,\text{K}\Omega$ assuming V_{ref} =0.25 V.

3.2.3 Results and Discussion

The proposed circuit is simulated and tested for robustness. Two schemes are used for testing the circuit.

Scheme-1: Input common-mode voltage V_{CM} of the transconductor, which sets the body voltage of all PMOS transistors, is allowed to vary with the supply voltage V_{DD} such a way that the body-source voltage (V_{SB}) is maintained constant at 0.25 V for all PMOS transistors. i.e. V_{CM} is set equal to $V_{DD} - 0.25$ V.

Scheme-2: V_{CM}, the body voltage of all PMOS transistors, is set to $V_{DD}/2$.

Variations in gate-transconductance and bulk-transconductance are plotted in Fig. 3.8 for scheme-1 across PVT. As expected in (3.4), both the transconductances have negative temperature coefficient. The absolute maximum deviation from the nominal $10.15\,\mu$S

(as per the simulated value) across PVT is observed to be about 9.8 % for both the transconductances. This deviation higher than 6 % as per the analysis made in subsection 3.2.1. This is attributed to secondary effects that are not considered while estimating the percentage change in transconductance and the dependency of finite gain of the error-amplifier on PVT.

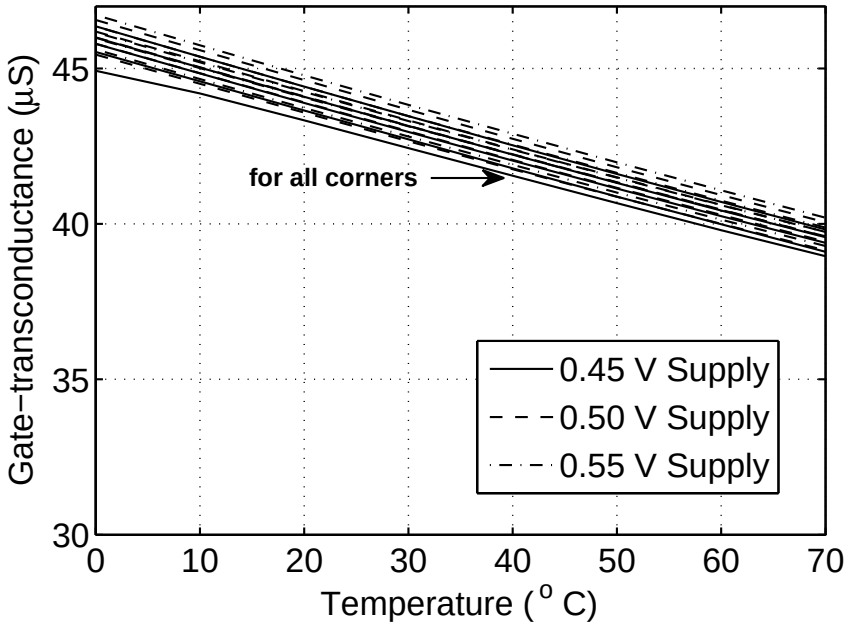
To emphasize the performance of the proposed circuit for power supply and corner variation, the transconductances are plotted as a function of supply voltage for all five corners in Fig. 3.9. It is clear that, the constant current generating circuit along with the efficient bias distribution scheme is effective in maintaining both the transconductances (gate and bulk) intact across the ± 10 % variation around the nominal supply voltage of 0.5 V and across the corners. The absolute maximum deviation, in both the cases, is found to be about 1.6 %. Note that with the conventional fixed-transconductance bias circuit, the variation was 25 %.

In Fig. 3.10, the transconductances are plotted for the scheme-2 as a function of supply voltage at all process corners. The following points may be noted.

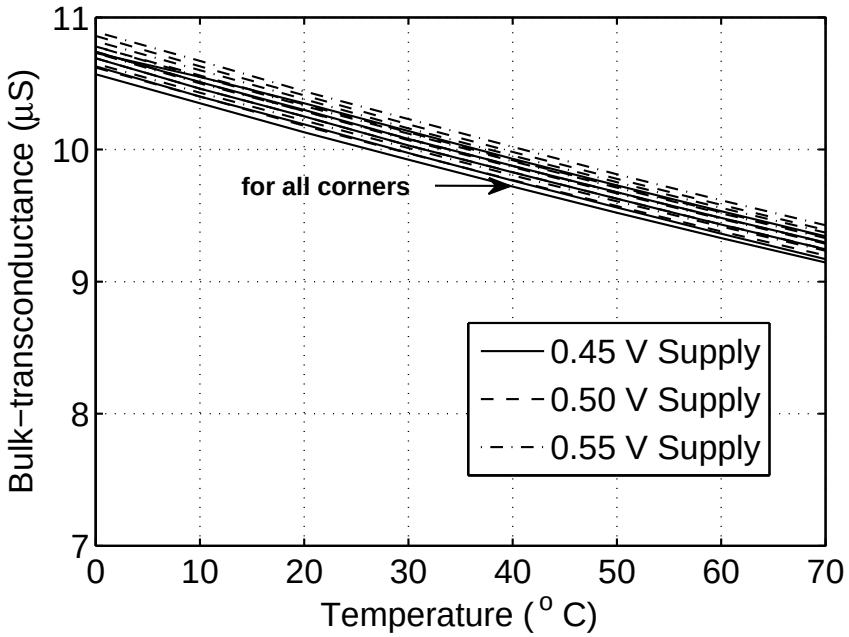
- The gate-transconductance remains constant similar to that of scheme-1. The absolute maximum deviation from the nominal value is 1.6 %
- The bulk-transconductances is found to have a higher variation when compared to scheme-1. The absolute maximum deviation is observed to be 5.7 %.

In scheme-1, source-bulk voltage V_{SB} is maintained constant, while in scheme-2, the bulk voltage is maintained constant at the input common-mode voltage $V_{DD}/2$. Therefore, in scheme-2 V_{SB} becomes a function of supply voltage. As per (3.1), g_{mb} is a function of g_m and η. In scheme-2, with η being a function of V_{SB} as given in (3.2), the variation in g_{mb} is expected to be different from that of g_m. A mathematical analysis has been carried out to justify the results shown in Fig. 3.10 and is as follows.

For scheme-2, since the bulk node is maintained at $V_{DD}/2$, V_{SB} will also be at $V_{DD}/2$. The nominal value of η therefore, is computed for $V_{SB} = V_{DD,nom}/2$ and can be written

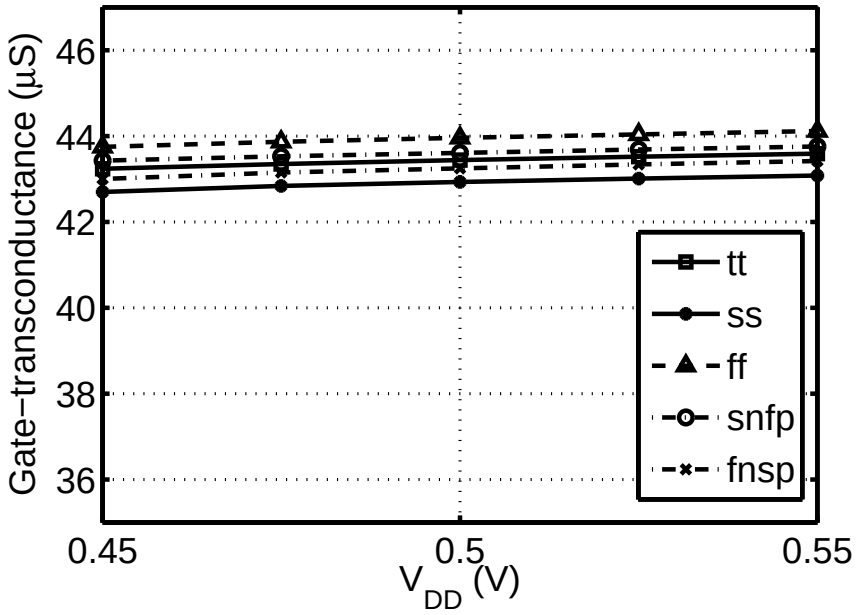


(a)

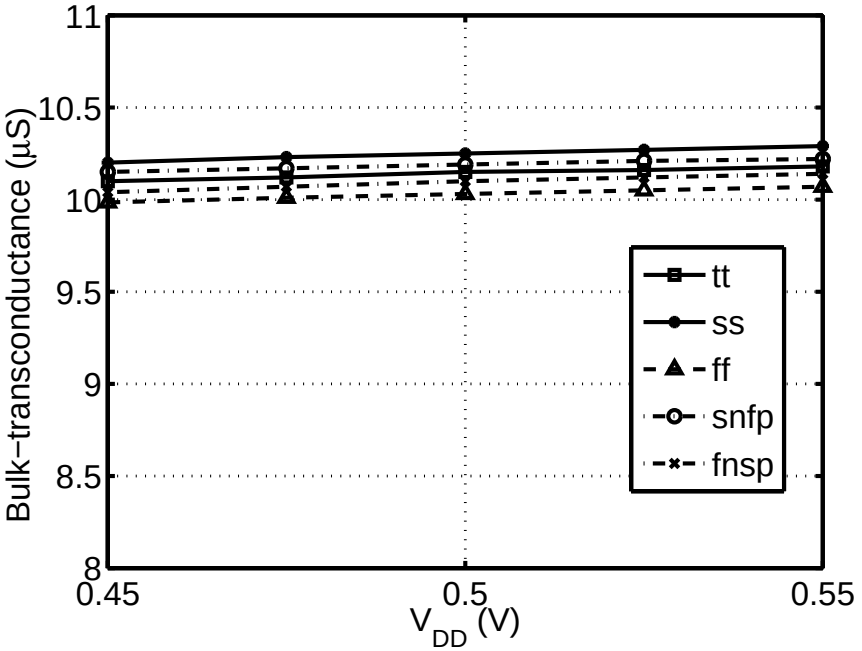


(b)

Figure 3.8: Performance of the proposed circuit for scheme-1 across PVT variations: (a) Gate-transconductance. (b) Bulk-transconductance.



(a)



(b)

Figure 3.9: Performance of the proposed circuit for scheme-1 across power supply and corner variations: (a) Gate-transconductance. (b) Bulk- transconductance.

as

$$\eta_{nom} = \frac{\gamma}{2\sqrt{2\phi_b + \frac{V_{DD,nom}}{2}}} \tag{3.6}$$

Let us say V_{DD} change from its nominal value $V_{DD,nom}$ to $V_{DD,nom}(1+\alpha)$ where, $-0.1 \leq \alpha \leq 0.1$ (α=1 indicate 10% change). η can then be written in the form,

$$\eta = \frac{\gamma}{2\sqrt{2\phi_b + \frac{V_{DD,nom}(1+\alpha)}{2}}} \tag{3.7}$$

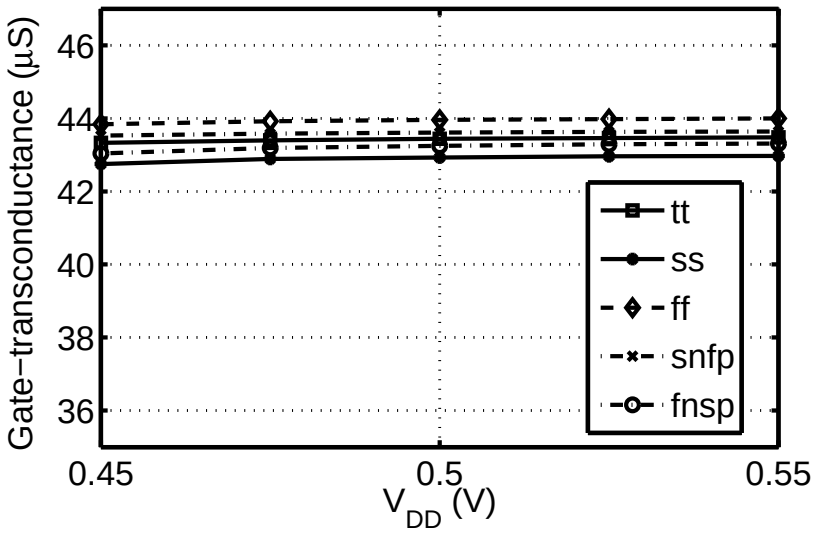
$$= \frac{\eta_{nom}}{\sqrt{1 + \frac{\alpha V_{DD,nom}/2}{2\phi_b + (V_{DD,nom}/2)}}} \tag{3.8}$$

Using Taylor series expansion, (3.8) can be further simplified to a form given in (3.9)

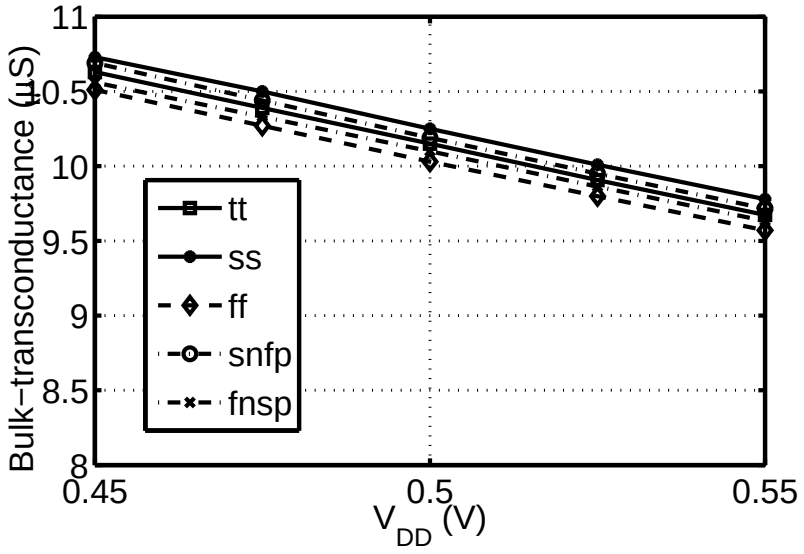
$$\eta \approx \eta_{nom}\left[1 - \frac{\alpha V_{DD,nom}/2}{2\phi_b + (V_{DD,nom}/2)}\right] \tag{3.9}$$

From (3.9) it can be seen that η is a linear function of α. η_{nom} and ϕ_b can be computed using the parameters obtained from the process documents. With $V_{DD,nom}$ =0.5 V and α=0.1, the maximum percentage deviation in η can be computed and is found to be 4.3 %. The same can be observed in Fig. 3.10(b) for a given corner. Another point to note is that η is independent of process corners and the same can be seen in Fig. 3.10(b) (slope of g_{mb} is almost constant across corners).

In order to compare the performance of the proposed schemes (scheme -1 and scheme-2) with that of the conventional scheme (V_{SB} same as scheme-1 in Fig. 3.2(b)), the gate-transconductance is plotted as a function of supply voltage for two corners viz. *tt* and *ss* in Fig. 3.11. Similarly the bulk-transconductance is plotted for the same two corners in Fig. 3.12. Performance of the proposed schemes and conventional schemes are tabulated in Table 3.1. Note that for a fair comparison, 1.8 V transistors are used in all the circuits. From the table numbers, it can be seen that the proposed schemes are



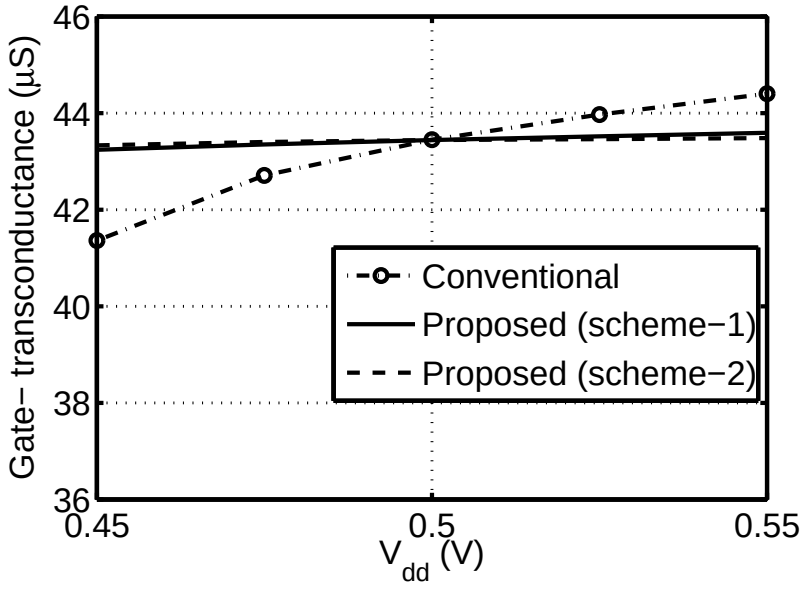
(a)



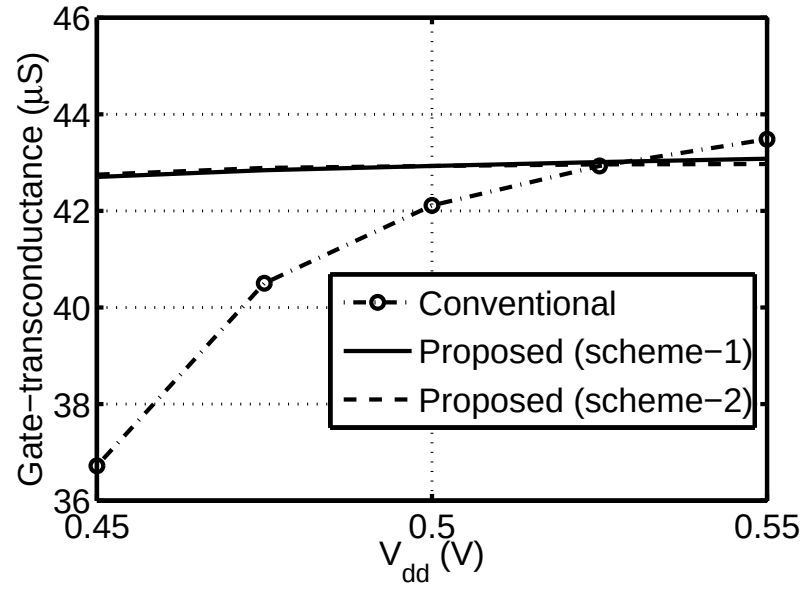
(b)

Figure 3.10: Performance of the proposed circuit for scheme-2 across power supply and corner variations: (a) Gate-transconductance. (b) Bulk- transconductance.

very effective when compared to the conventional schemes.

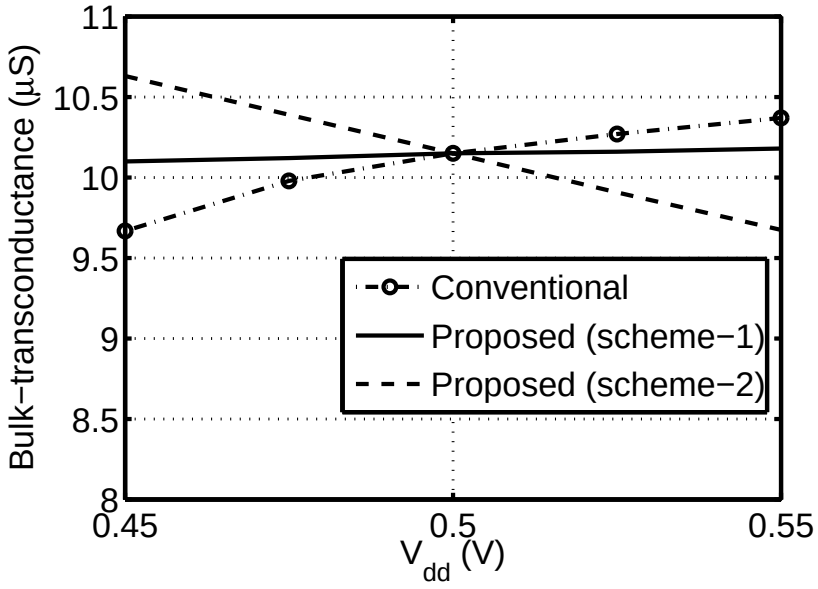


(a)

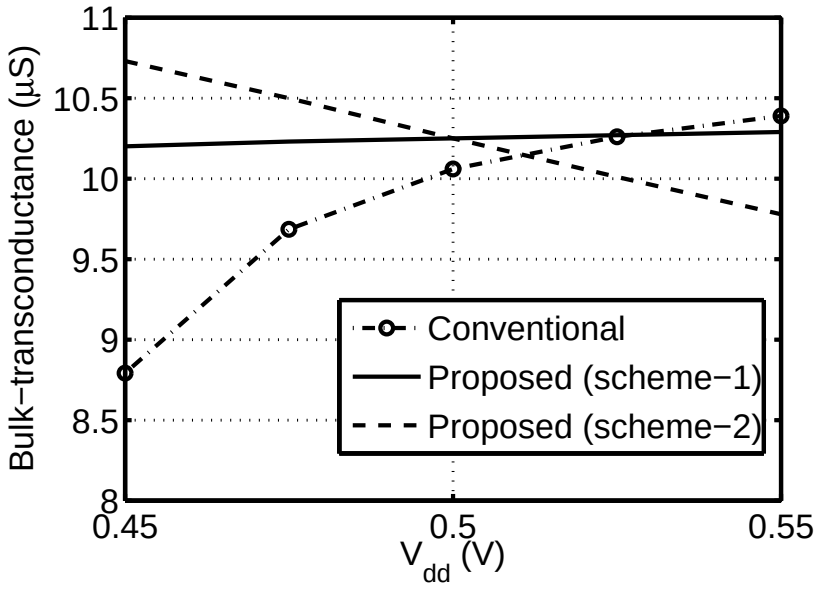


(b)

Figure 3.11: Comparing the gate-transconductance obtained from the proposed fixed bias circuit (scheme -1 and scheme -2) with that of the conventional fixed transconductance bias circuit: (a) *tt* process corner. (b) *ss* process corner.



(a)



(b)

Figure 3.12: Comparing the bulk-transconductance obtained from the proposed fixed bias circuit (scheme -1 and scheme -2) with that of the conventional fixed transconductance bias circuit (a) *tt* process corner. (b) *ss* process corner.

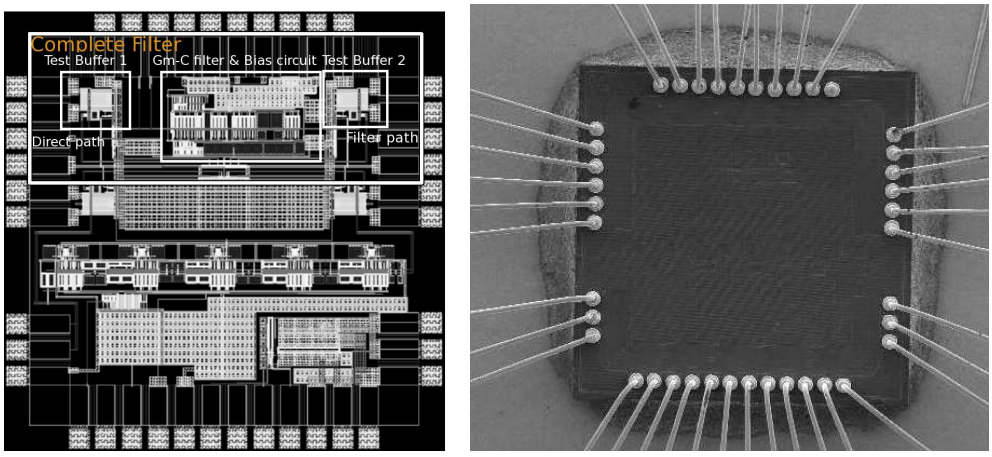
Table 3.1: **Comparison of proposed work with conventional circuits: Table showing absolute maximum percentage deviation in g_{mb} from its nominal value.**

Test cases	V_{DD}=**0.5 V** Temperature= **room (27°C)** Corner = **All**	V_{DD}=**0.45 V** Temperature= **room (27°C)** Corner =**All**	V_{DD}=**0.5 V** Temperature= **0 – 70°C** Corner = ***tt***	V_{DD}=±10%***0.5 V** Temperature= **0 – 70°C** Corner = ***tt***	V_{DD}=±10%***0.5 V** Temperature= **0 – 70°C** Corner = **All**
Conventional circuit (Fig. 3.2(a))	4.4	28.0	6.68	11.3	35.96
Conventional circuit (Fig. 3.2(b))	0.8	12.3	3.5	4.56	25.8
Proposed circuit (Scheme-1)	0.79	2.23	7.7	0.49	9.8
Proposed circuit (Scheme-2)	0.98	5.5	8.87	4.73	13.8

CHAPTER 4

TEST SETUP AND RESULTS

The experimental results of the fabricated chips along with the details of test setup is presented in this chapter. The test-chip is fabricated in a 0.18 μm standard CMOS process from UMC through the Europractice mini@sic program at IMEC Belgium. Fig. 4.1 shows the layout and die photograph of the chip along with bond wires. Apart from the filter, the chip has two more designs. The total active die area of the chip is 2.25 mm^2, and the G_m-C filter along with accessories occupies an area of 0.25 mm^2. All three designs in the chip have independent power and ground lines so that the design not in use is turned off to avoid any interference. Figure 4.2 shows the bonding diagram of the chip to the package. The chip is packaged in a 44-pin JLCC package. The pin details of chip is given in Appendix A.



(a) (b)

Figure 4.1: (a) Layout of complete filter with input/output pads. (b) IC photograph with bond wires.

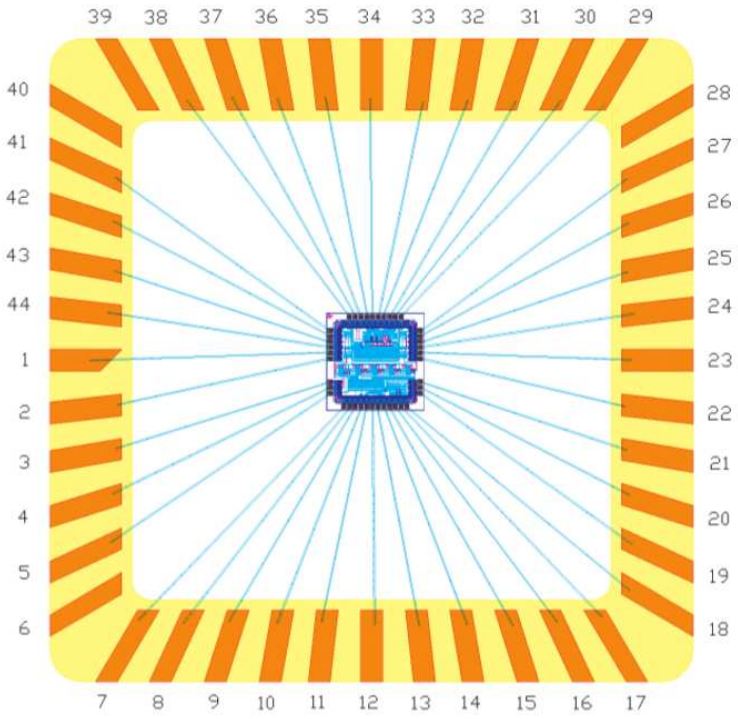


Figure 4.2: Bond diagram of filter chip.

4.1 THE TEST SETUP

The filter is not designed to drive parasitics of package and test board. Therefore, it is necessary to buffer the filter output before it is taken out of the chip for measurements. These buffers are commonly called as 'test buffers' in literature. When characterizing packaged filter chips, the effects of test buffer along with the parasitics of package and test board must be de-embedded from the response of the filter. A block schematic of the test setup used to characterize the filter chip is shown in Fig. 4.3.

There are two techniques available in the literature to characterize the packaged continuous-time filters. The first technique proposed by Nauta (Nauta, 1992) uses the test setup shown in Fig. 4.3. It is a simple method and is useful when in the frequency range of interest, the signal feed-through from input to output due to package and board has negligible effect on the measurements. The second method proposed by (Pavan and Laxminidhi, 2007) is a method specially designed for characterizing high frequency fil-

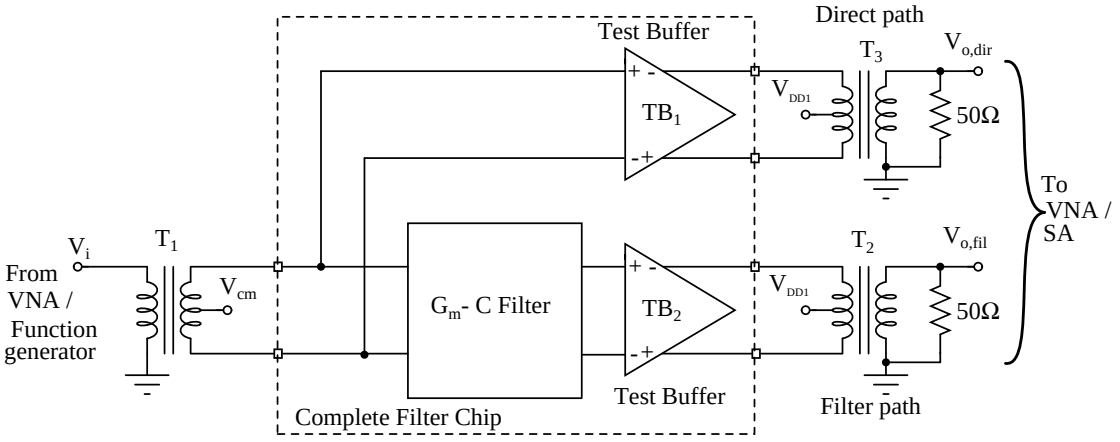


Figure 4.3: On-chip filter characterization set up circuit.

ters where there can be a significant effect of signal feed-through on the measurements. The former technique has been adopted for characterizing the filter in this work since the frequency range of interest is only upto 10 MHz and the signal feed-through can be assumed negligible.

In the test setup shown in Fig. 4.3, transformer T_1 converts the single-ended stimulus (from a Vector Network Analyzer (VNA) or Function Generator) into a fully differential signal that excites the filter. TB_1 and TB_2 are two nominally identical on-chip test buffers designed to drive external loads. These test-buffers are biased with sufficiently large currents to drive the external loads and are only activated during characterization. TB_1 senses the input of the filter and forms the direct measurement path, while TB_2 senses the filter output and forms filter path. Transformers T_2 and T_3 convert the test-buffer outputs into single-ended signals that are measured by the test instruments (VNA or Spectrum Analyzer (SA)).

The signal flow graph of the test setup can be drawn as shown in Fig. 4.4. The transfer function H_{in} is formed by path from the point of stimulus feed and the filter input. This includes the transformer T_1 and the input path parasitics. H_f is the transfer function of the filter. H_b is the transfer function from the test buffer input to the balun (T_2, T_3) output. From the signal flow graph, it can be deduced that

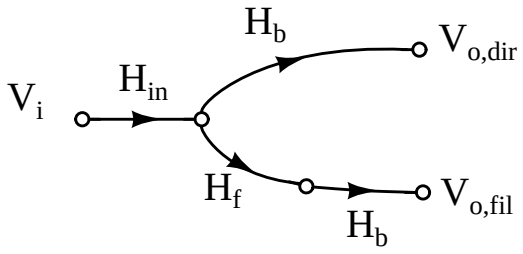


Figure 4.4: Signal flow graph of filter characterization setup circuit.

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} \tag{4.1}$$

A VNA has been used to measure the *S*-parameters of the filter path and direct path. Assuming a fairly good impedance match, the filter transfer function can be computed from the *S*-parameters of the filter path and direct path as given in (4.2).

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} = \frac{S_{21,fil}(f)}{S_{21,dir}(f)} \tag{4.2}$$

4.2 TEST-BUFFER DESIGN

Figure 4.5 shows the schematic of the test-buffer circuit. The test buffer is designed to operate on a 3.3 V supply (V_{DD1}). A higher supply voltage is used to ensure that the linearity of the buffer is at a level sufficiently above that of the filter.

The test buffer has two stages. The first stage is a PMOS source follower. This stage offers a high input impedance which is capacitive. The size of PMOS input transistors M_1 and M_2 is made small to minimize the input capacitance, because this input capacitance has to be absorbed into the integrating capacitor present at the filter output node. The second stage of the test buffer is a differential transconductor. The transistors M_3 and M_4, form a input differential pair of a differential amplifier. These transistors are sized to have a large gate overdrive voltage in order to get a very good linearity. The

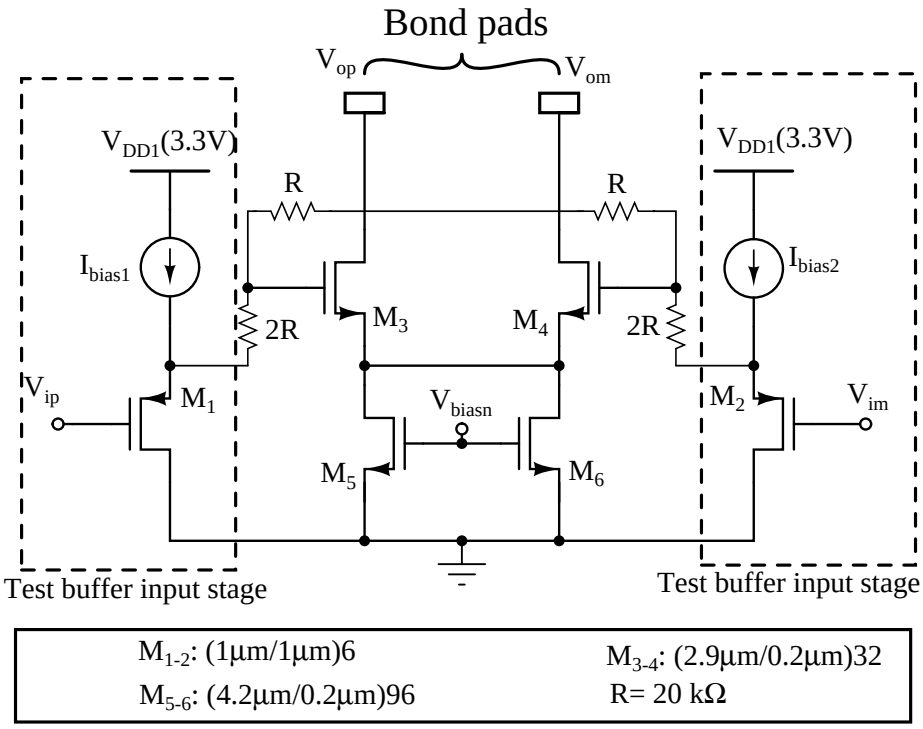


Figure 4.5: Schematic of test buffer circuit.

signal at the output of first stage is attenuated by factor 3 before it is fed to the input differential pair. This is to ensure that the signal amplitude is within the linear range of M_3 and M_4 transistors, and the distortion introduced by the test-buffer is very small when compared to that introduced by the designed filter. The transistors M_5 and M_6 together form a tail current sink to generate the necessary bias for differential operation. Each leg of test-buffer differential pair is designed to carry current of nearly 15 mA at a power supply of 3.3 V.

The necessary bias for the test buffer is generated by the bias circuit shown in Fig. 4.6. An off-chip current of 100 μA, generated using the IC LM 334, is used to generate the bias for the test buffer circuit. Transistors M_1 and M_2 form the current mirror to generate the necessary bias current for the input stage of test-buffer circuit (I_{bias1} and I_{bias2} in Fig. 4.6). The bias voltage (V_{biasn}) is generated by transistors M_4-M_{10}.

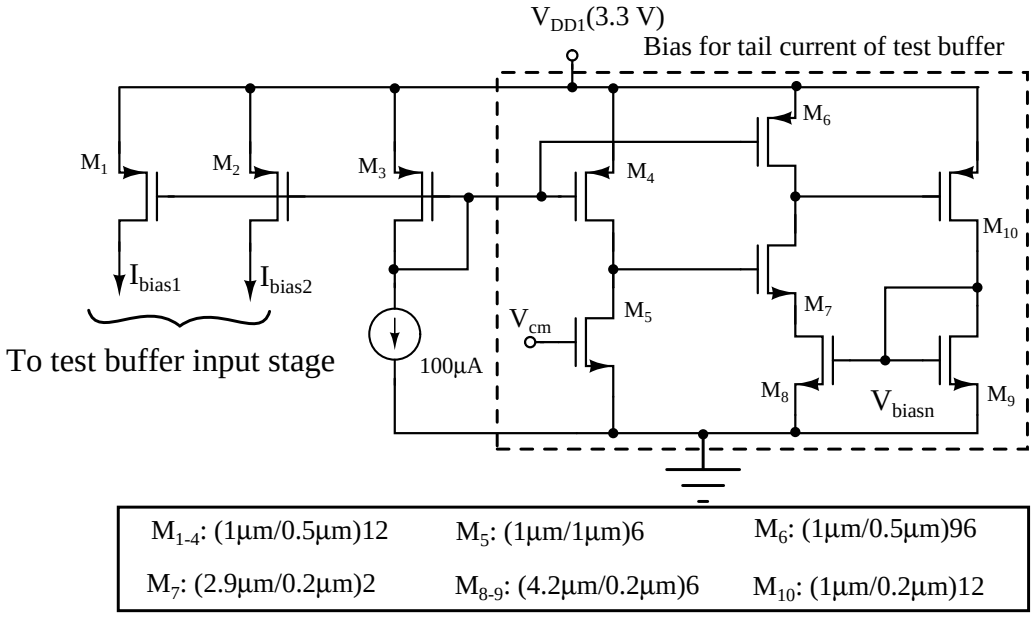


Figure 4.6: Bias generation for test buffer circuit.

4.3 DESIGN OF TEST BOARD

A two layered printed circuit board (PCB) is designed and fabricated to characterize the filter chip. The board measured $4.4'' \times 4.125''$ in size. A photograph of the populated PCB is shown in Fig. 4.7. The baluns T1-T3, referring to Fig. 4.3, are realized from a wide-band transformers ADT1-6WT from Mini-Circuits. They have a frequency range of 0.03-150 MHz with an insertion loss of 3 dB. Decoupling capacitors are used at each power pin in order to decouple the supply voltage from any interference and/or noise which can couple through parasitics. A 10 μF electrolytic capacitor (for suppressing low frequency noise) and a 10 nF polyester film capacitor (for decoupling high frequency noise) are placed very close to each power pin. The same has been followed for common-mode reference voltage too.

The board has one LM334 based current sink circuit to sink a current of 100 μA from the chip. This current is used to generate the bias for the test-buffer circuit inside the chip.

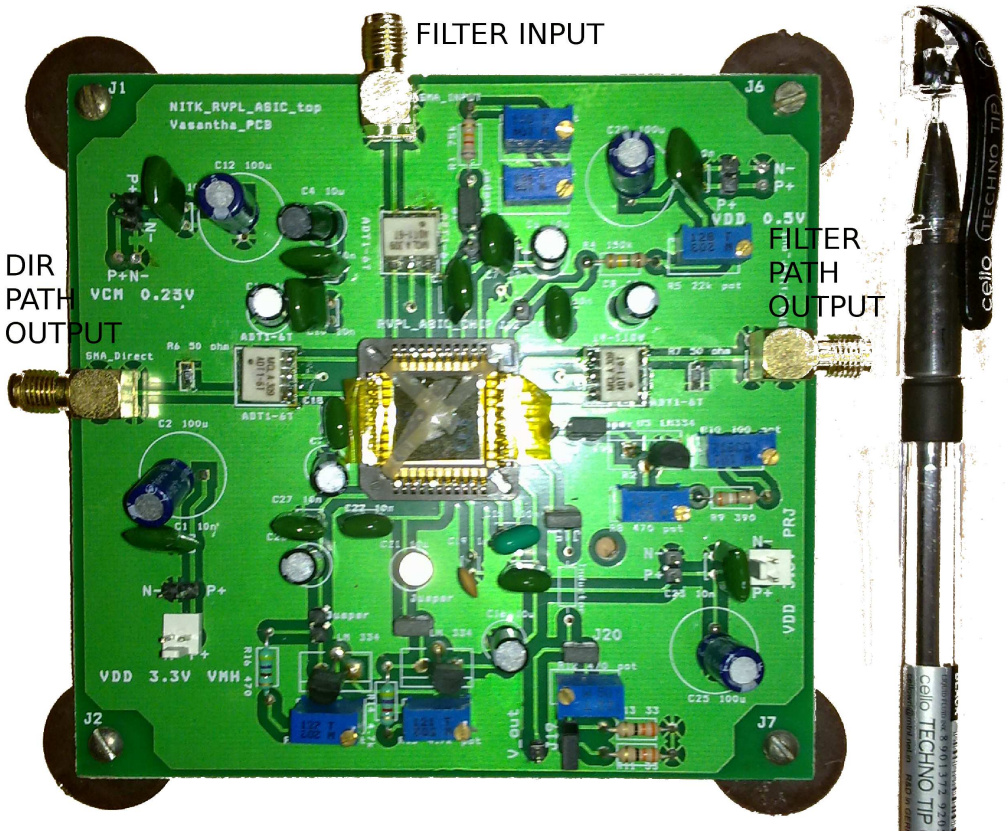


Figure 4.7: Photograph of 2 layered PCB mounted with all the components.

4.3.1 Power Supply Design

The chip requires three regulated voltages viz 0.5 V to power the filter (V_{DD}), 0.25 V as common-mode reference voltage for the filter (V_{cm}) and 3.3 V for the test buffer (V_{DD1}). An adjustable laboratory power supply is sufficient for 3.3 V. But, for 0.5 V and 0.25 V it is not advisable to use such a power supply, for the reason that a small change in any adjustment (intentional or accidental) can change the voltage by a large percentage. Therefore, a dedicated regulated power supply has been designed for 0.5 V and 0.25 V. The details of which are given in Appendix C.

4.4.1 Measured Frequency Response

Figure 4.8 shows the normalized magnitude response of the filter chip. When compared with the ideal response, the actual filter response is found to be in deviation near the band-edge. However, the stop band performance of the filter is in close match to the ideal with 80 dB/decade roll-off as expected. Note that the ideal response is shown in figure is the fourth order Butterworth response that matches with the stop band performance of the filter chip.

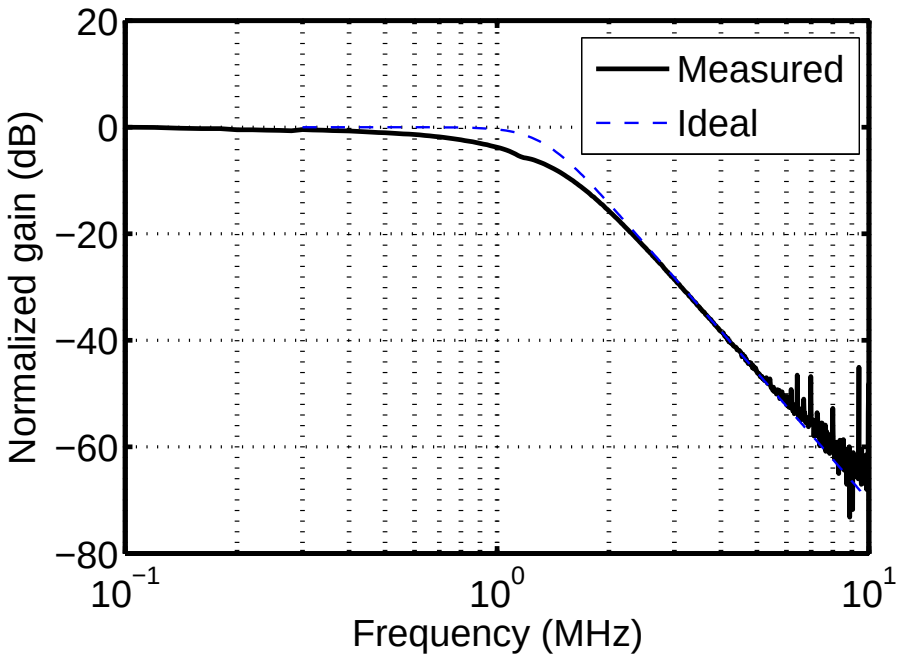


Figure 4.8: Measured magnitude response of the filter chip.

Figure 4.9 shows the magnitude response of the filter for 18 samples of the fabricated chip. Consistency in the responses of the filter samples justify the good repeatability.

The response is also observed for the 10 % change in supply voltage from its nom-

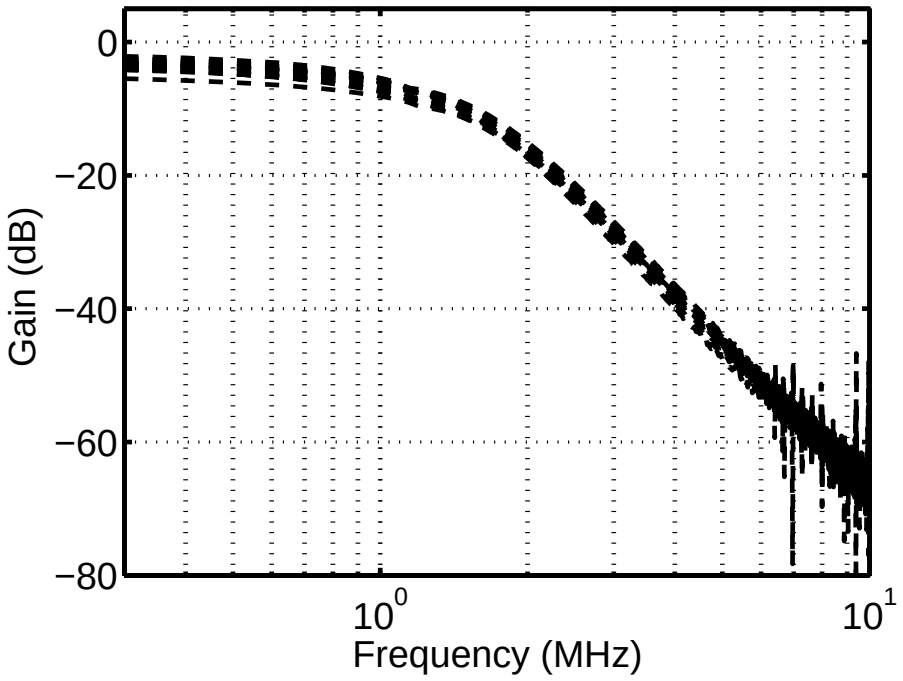


Figure 4.9: Magnitude response of the filter for 18 samples of fabricated chips.

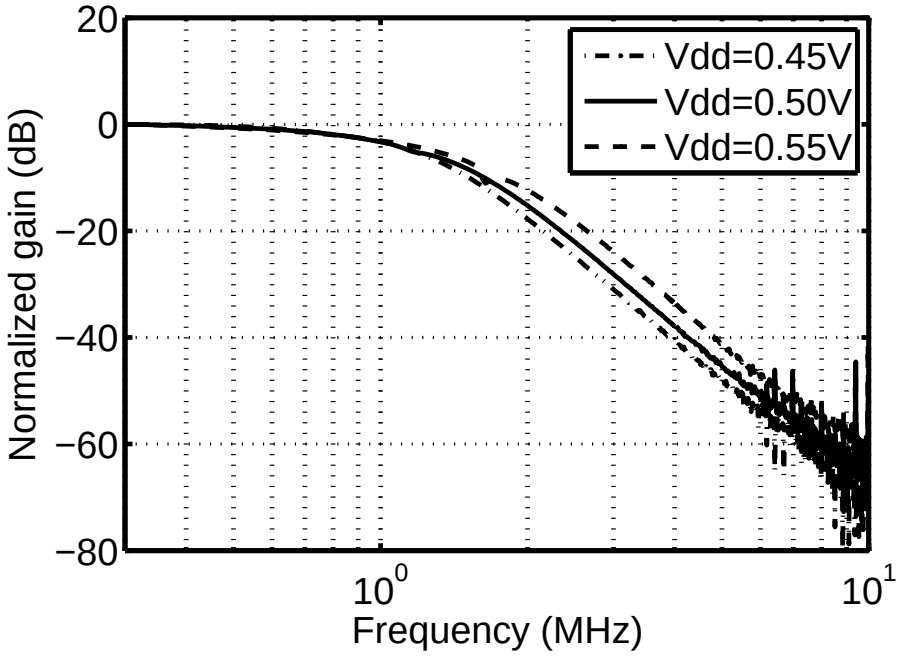


Figure 4.10: Frequency response variations for $\pm 10\,\%$ change in supply voltage at room temperature.

inal value of 0.5 V and is shown in Fig. 4.10. It is observed that the change in bandwidth is less than $\pm 1.0\,\%$ at room temperature. It is to be noted that the fixed-G_m

bias circuit, presented in chapter 3, offers a maximum deviation of 0.45 % in bulk-transconductance for the same variation in the supply voltage (source-bulk voltage (V_{SB}) kept constant). The measured filter response show a good correlation with the results of fixed-transconductance bias circuit.

4.4.2 Noise Spectral Density

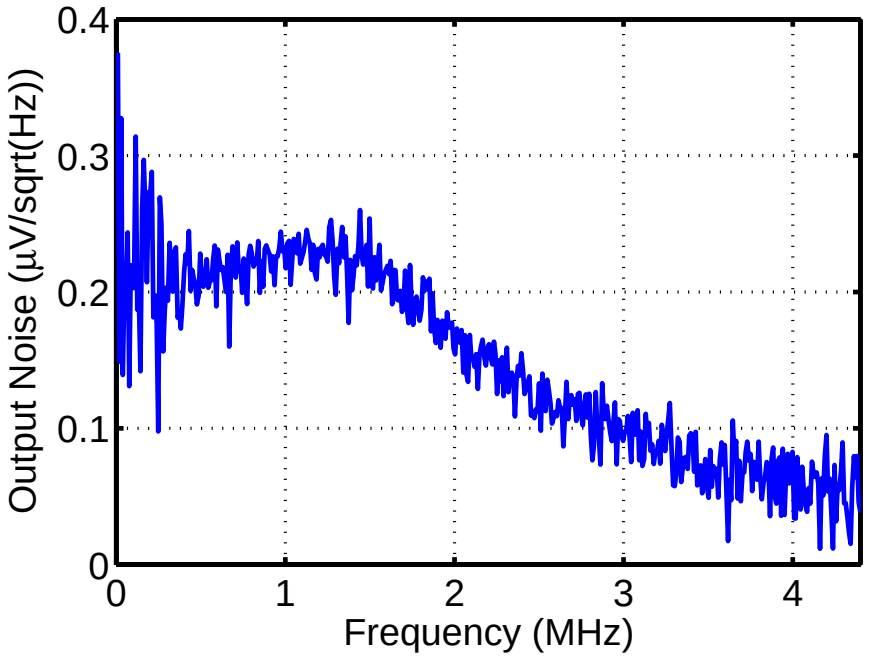


Figure 4.11: Measured output noise spectral density of the filter.

Figure 4.11 shows the output voltage noise spectral density of the filter. The measured integrated output noise of the filter over the frequency range of 40 kHz to 1.1 MHz is 217.2 μV (rms).

4.4.3 Distortion

Tests are conducted to measure the distortion performance of the filter. Figure 4.12 shows the third harmonic distortion (HD_3) of the filter as a function of input tone frequency. During this test, peak-to-peak value of the differential tone is kept constant at

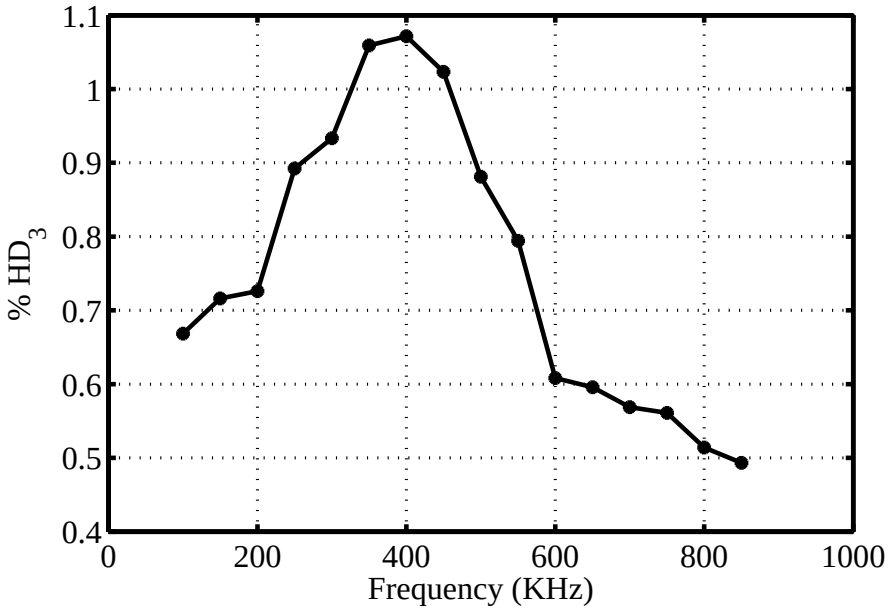


Figure 4.12: HD_3 vs f_{in} for a fixed input peak-to-peak voltage of 140 mV.

140 mV. It is observed that the distortion is maximum near one-third of the bandwidth ($f_o/3$) and decreases as one move away from this frequency on either side. At low frequencies, the distortion currents from the transconductors tend to cancel each other, thus lowering the distortion. At higher frequencies ($f > f_o/3$), the distortion decreases since the harmonic components (dominant third harmonic) fall out of the band and thus gets attenuated naturally by the filter.

The HD_3 as a function of input peak-to-peak (differential) voltage is plotted in Fig. 4.13 for a fixed frequency of 330 kHz ($f_o/3$). The filter offers 1 % HD_3 for an input differential peak-to-peak voltage of 135 mV.

The performance of the filter is summarized in the Table 4.1.

The designed filter performance is compared with some of the filters available in the literature and is given in the Table 4.2. A figure of merit (FOM) (Laxminidhi et al., 2009) is used for comparing the various filters which is computed using the formula given in (4.3).

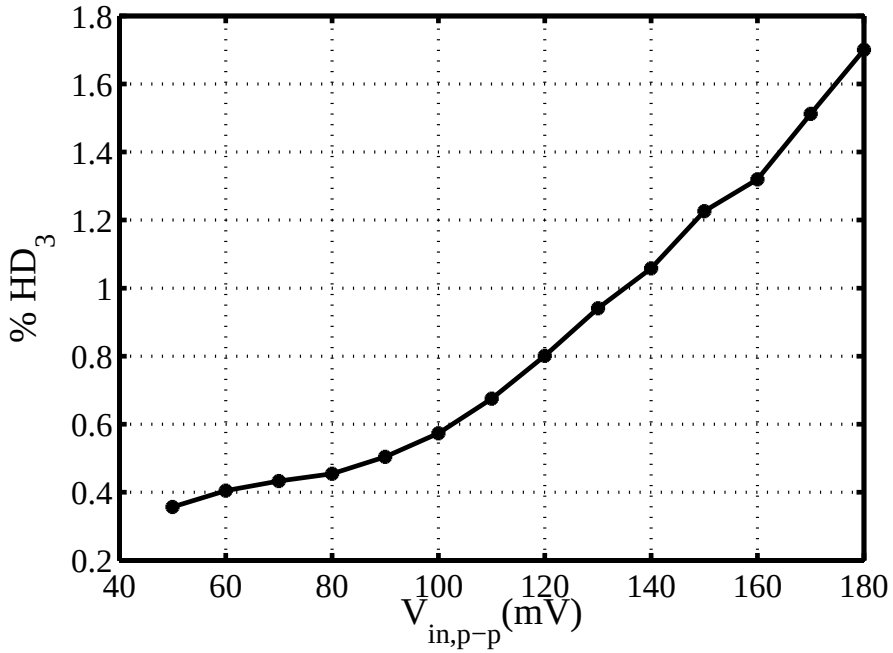


Figure 4.13: HD_3 vs input differential peak-to-peak voltage for a fixed frequency 330 kHz.

Table 4.1: **Performance parameters of fourth order Butterworth low-pass filter.**

Parameters of the filter	**Measured values**
Supply [V_{DD}]	0.5
Technology [μm]	0.18
3-dB Bandwidth [MHz]	1
Power dissipation [μW]	56.4
Integrated output noise [μV_{rms}]	217.22
Input [mV_{pp}]@ 750 kHz for 1 % THD	192
Dynamic range [dB]	45
Area [mm^2]	0.125
Bandwidth variation for $\pm 10\% V_{DD}$	± 1.00

$$FOM = \frac{P_{diss}}{pQ_{max} f_o DR^2} \tag{4.3}$$

where, P_{diss} is the power dissipation (Watts), p is the number of filter poles, Q_{max} is the maximum quality factor of the filter poles, f_o is the filter cut-off frequency (Hertz) and DR is the dynamic range of the filter. The unit of FOM is Joules (J).

Note that for a fair comparison with (Chatterjee et al., 2005) and (Zhang and El-

Masry, 2007), while measuring the linearity, the test is conducted by applying a tone frequency 750 kHz (near the band-edge). Also, the dynamic range is calculated as the ratio of the rms differential input voltage at 1 % total harmonic distortion (THD) to integrated input noise over the frequency range of 40 KHz to 1.1 MHz.

It can be observed from Table 4.2 that the filter presented in this research offers the lowest FOM (in comparison with sub-1 V filters realized on silicon). A lower FOM indicates more power efficient design.

Table 4.2: **Comparison of present work with filters available in the literature.**

Reference	**Bandwidth [MHz]**	**Order [n]**	**Supply Voltage [V]**	**Power [μW]**	Q_{max}	**Dynamic range@1% THD [dB]**	**Topology**	**Tech-nology [μm]**	**FOM [fJ]**
(Chatterjee et al., 2005)	0.135	5	0.5	1100	6.2	56.6[1]	Active-RC	0.18	0.58
(Zhang and El-Masry, 2007)	1.05	3	1.8	4070	1.99	45[2]	G_m-C	0.18	20.53
(Carrillo et al., 2008)	0.0175	2	1	45	0.89	63.7[3]	G_m-C	0.35	0.62
(Carrillo et al., 2010)	0.010	2	1.5	648	0.707	62.6[3]	G_m-C	0.35	25.18
(Carrillo et al., 2011)	3	2	1.2	382	0.707	69.6[3]	G_m-C	0.35	.009
(Arya et al., 2013)	0.9705	3	0.5	332	0.707	63.13	G_m-C	0.13	.078
Present work	1.0	4	0.5	56.4	1.3	45[4]	G_m-C	0.18	0.355

[1]Ratio of input @100 kHz for 1 % THD to integrated input noise,[2]Ratio of input @1 MHz for 1 % THD to integrated input noise,[3]Ratio of input @1 kHz for 1 % THD to integrated input noise, [4]Ratio of input @750 kHz for 1 % THD to integrated input noise

CHAPTER 5

LOW VOLTAGE COCHLEA FILTER

5.1 INTRODUCTION

G_m-C bi-quadratic filters can be realized in many ways. The popular architecture has been presented in chapter 2. One of its variants has been extensively used in silicon Cochlea designed to mimic the human Cochlea (Lyon and Mead, 1988; Slaney, 1988; Sarpeshkar et al., 1998; Grech et al., 2003). In this chapter, design of such a biquad has been addressed for low power low-voltage applications.

5.2 FILTER ARCHITECTURE

The schematic of a second order low-pass filter, used in the silicon Cochlea, proposed by (Lyon and Mead, 1988), is shown in Fig. 5.1. Several number of such filters are connected in cascade as a filter bank to realize a silicon Cochlea.

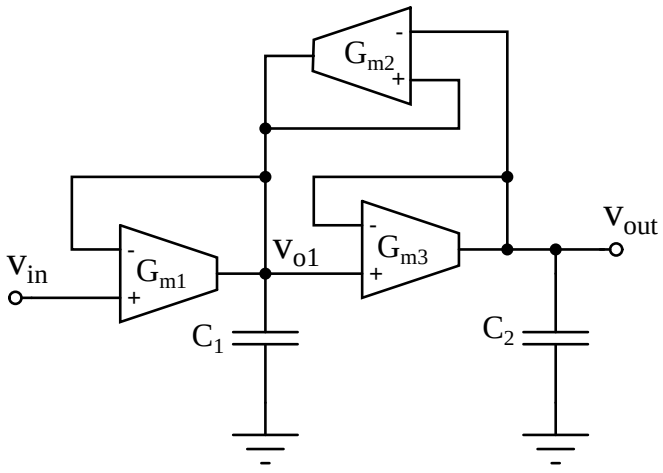


Figure 5.1: Schematic of a Cochlea filter.

The transfer function of the circuit in Fig. 5.1 can be written as

$$\frac{V_{out}}{V_{in}} = \frac{G_{m1}G_{m3}/C_1C_2}{s^2 + \left(\frac{G_{m1}C_2 + G_{m3}C_1 - G_{m2}C_2}{C_1C_2}\right)s + \left(\frac{G_{m1}G_{m3}}{C_1C_2}\right)} \tag{5.1}$$

where G_{m1}, G_{m2} and G_{m3} are the transconductances and C_1 and C_2 are the integrating capacitors. Comparing (5.1) with the transfer function of a second order low-pass prototype filter given in (5.2), the cut-off frequency ω_o and the quality factor Q of the filter can be written as shown in (5.3) and (5.4) respectively.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \tag{5.2}$$

where

$$\omega_o = \sqrt{\frac{G_{m1}G_{m3}}{C_1C_2}} \tag{5.3}$$

$$Q = \frac{\sqrt{G_{m1}G_{m3}(C_1/C_2)}}{(G_{m1} - G_{m2}) + G_{m3}(C_1/C_2)} \tag{5.4}$$

It is clear from the expressions (5.3) and (5.4) that the filter can be tuned for the desired bandwidth ω_o and quality factor Q by a proper choice of transconductances and capacitances. Another important point that can be noted is that, for a given set of G_{m1}, G_{m3}, C_1 and C_2 i.e. for a given ω_o, the filter Q can be easily and independently tuned for a high value by tuning G_{m2}. For active transconductors, the transconductance (gate or body) can be tuned by tuning the bias current. Therefore, Q of the Cochlea filter has high sensitivity to variations in the tuning transconductor G_{m2} . This is illustrated in the following subsection along with a comparison made to the conventional biquad circuit presented in chapter 2.

5.2.1 Sensitivity of Quality Factor

For the ease of analysis, the following assumptions are made,i.e. G_{m1}=G_{m3}=G_m and C_1=C_2. The expression for Q in (5.4) boils down to-

$$Q = \frac{G_m}{2G_m - G_{m2}} \tag{5.5}$$

The sensitivity of Q with respect to G_{m2} is

$$S^Q_{G_{m2}} = \frac{G_{m2}}{Q} \times \frac{\partial Q}{\partial G_{m2}} \tag{5.6}$$

$$= -\frac{G_{m2}/G_m}{2-(G_{m2}/G_m)} \tag{5.7}$$

The variation of $S^Q_{G_{m2}}$ with respect to G_{m2}/G_m is shown in Fig. 5.2. The sensitivity of Q

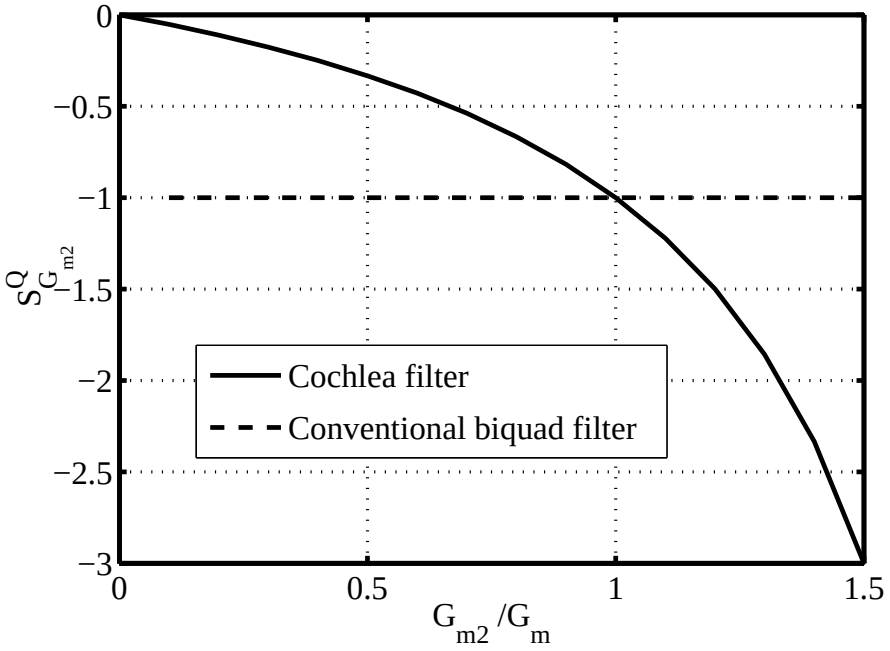


Figure 5.2: Comparison of $S^Q_{G_{m2}}$ in Cochlea filter and conventional biquad filter.

is an exponential function of G_{m2}. In comparison, the sensitivity of Q in a conventional biquad is independent of the tuning transconductor (see G_{m2} in Fig. 2.3). It can be

shown mathematically, that $S_{G_{m2}}^{Q}$ for the conventional biquad is -1. The high sensitivity of the Q in Cochlea is useful since, the application demands gain enhancement near the low-pass band-edge.

5.3 TRANSCONDUCTOR DESIGN

The Cochlea filter requires differential-input, single ended output transconductors. Bulk input transconductors are preferred when operating on low power supply voltage. If implemented on a standard n-well CMOS process, it becomes imperative to use PMOS input transistors. The schematic of the transconductor is shown in Fig. 5.3(a) and its symbol in Fig. 5.3(b). It has pseudo-differential architecture with a NMOS current mirror load.

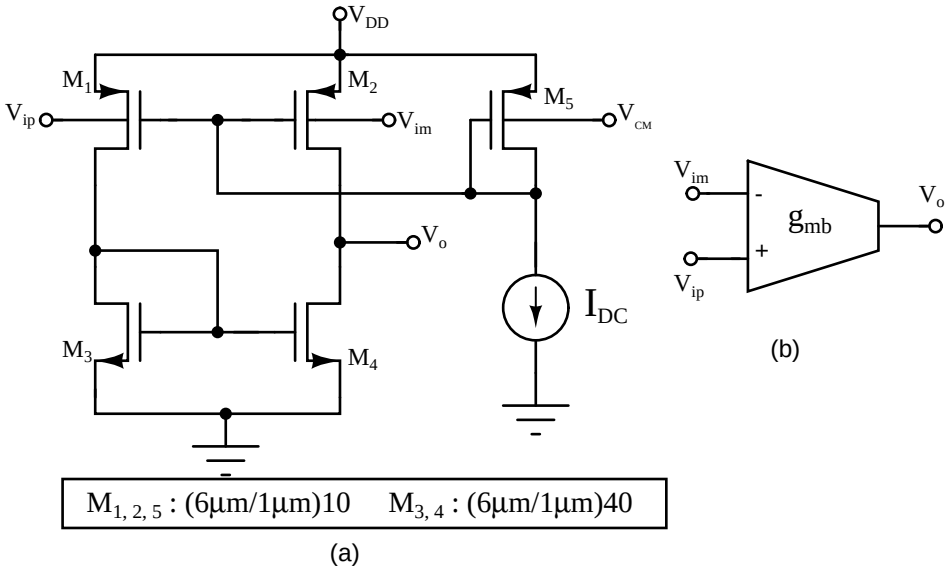


Figure 5.3: Bulk driven transconductor: (a) Schematic. (b) Symbol.

v_{ip} and v_{im} are differential inputs and v_o is the single ended output. M_1 and M_2 are the PMOS input transistors and M_3 and M_4 form NMOS current mirror load. Gates of M_1 and M_2 are biased to carry quiescent current of $2\,\mu$A. Bulk-transconductance of the circuit is designed for approximately $10\,\mu$S by sizing the input transistors. If the

constant current source I_{DC} is independent of process, temperature and voltage variation, the bulk-transconductance of M_1 and M_2 is found to remain intact with overall percentage variation less than 7.25%. A constant current generator circuit, presented in Chapter 3, is used to generate the bias for the transconductors. Designed transconductor is found to have a DC gain of 23.76 dB and UGB of 11.65 MHz.

5.4 FILTER IMPLEMENTATION

The Cochlea filter shown in Fig. 5.1 is realized using the designed bulk-driven transconductor. The filter is designed to have a Butterworth response with a bandwidth of 500 kHz. A fully differential architecture has been used for the filter due to the inherent merits of differential operation. For the given transconductance of 10 μS, the intended integrating capacitors C_1 and C_2 are computed using (5.3) and (5.4), and are found to be 4.56 pF and 2.279 pF respectively. The finite DC gain of the transconductor

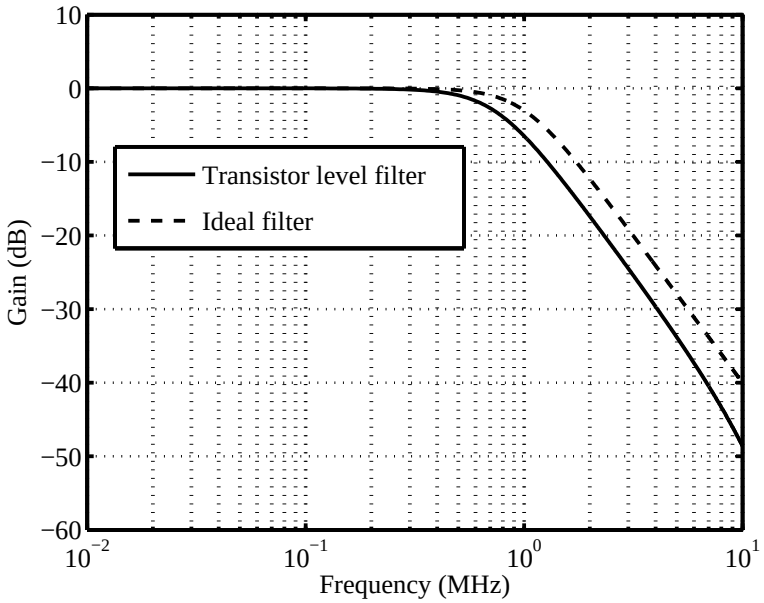


Figure 5.4: Magnitude response of the transistor level filter before design centering.

and the parasitics cause deviation in the response as shown in Fig. 5.4, hence calls for the design centering process.

In the design centering process followed in chapter 2, modeling the transconductor was quite easy as one required to find only the input/output resistance of the transconductor. The parasitic capacitance at every integrating node was estimated during the design centering. However, the transconductor in Fig. 5.3 has an internal node formed at the gates of M_3 and M_4 and this node plays a role in the transconductor action. It is necessary to take this effect into account while design centering the filter. This can be achieved by a careful model of the transconductor.

5.4.1 Model of the Transconductor

Every transconductor in the filter, has unity feedback architecture with output connected to one of the input terminals. The small-signal equivalent circuit of the first transconductor (G_{m1} in Fig. 5.1) is drawn in Fig. 5.5 where the effect of each transistor parasitics is considered. g_{mb1} and g_{mb2} are the bulk-transconductance of transistors M_1 and M_2.

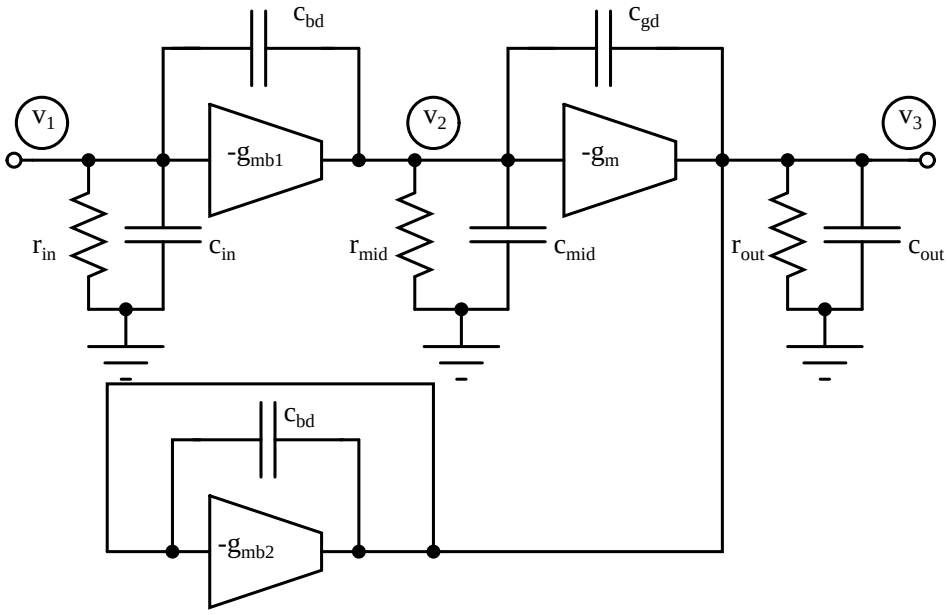


Figure 5.5: Small-signal equivalent circuit of bulk driven transconductor in unity feedback configuration.

g_m is the gate transconductance of transistor M_4.The effective resistance and capacitance at each node are also shown in the figure. Input node, intermediate node and the

output node are the three integrating nodes. The voltage at these nodes are taken as the state variables required to define the state-space model of the filter.

5.4.2 State Space Model of Cochlea Filter

The complete filter is found to have six state variables. The locations of the state variables are shown in Fig. 5.6 by drawing circles around the voltages V_1-to-V_6. Note that, the ideal Cochlea filter shown in Fig. 5.1, has only two state variables (second order system) i.e. voltage at the two integrating nodes. The non-ideality of the transconduc-

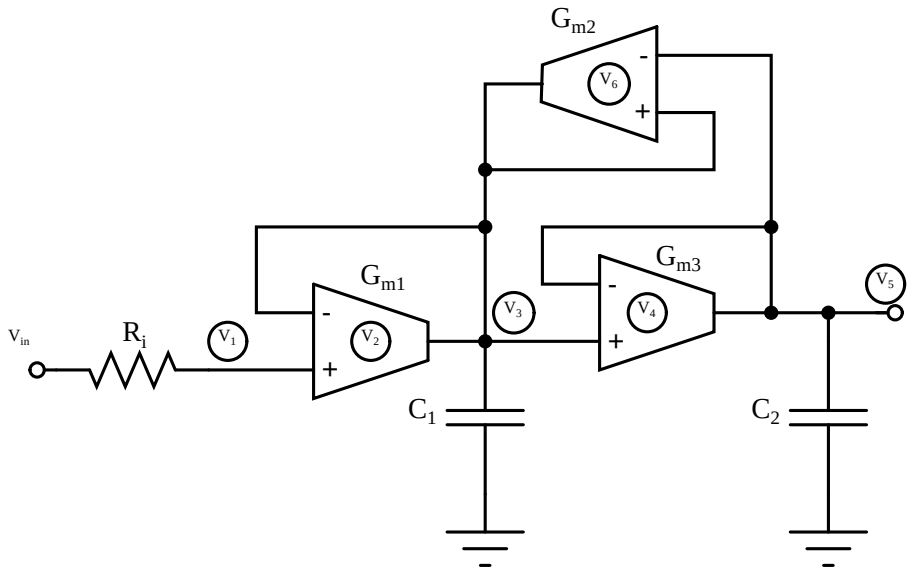


Figure 5.6: Cochlea filter circuit highlighting the location of state variables.

tor, results in four additional state variables for the same filter. The source resistance R_i is used as dummy resistor, included in Fig. 5.6 to enable the state space representation. The effect of this resistor is neglected as resistance value is chosen to be 0.001 Ω. Fig. 5.7 shows the small-signal equivalent circuit of the second order Cochlea filter. The capacitors C_1 and C_2 are the intended capacitors to be placed. The state-space model of the Cochlea filter is then derived from the small-signal equivalent circuit. The small-signal circuit shown Fig. 5.7 is modeled using descriptor state-space equations as given in (5.8) and (5.9). Since there is no feed-forward path from input to the output, **D** matrix

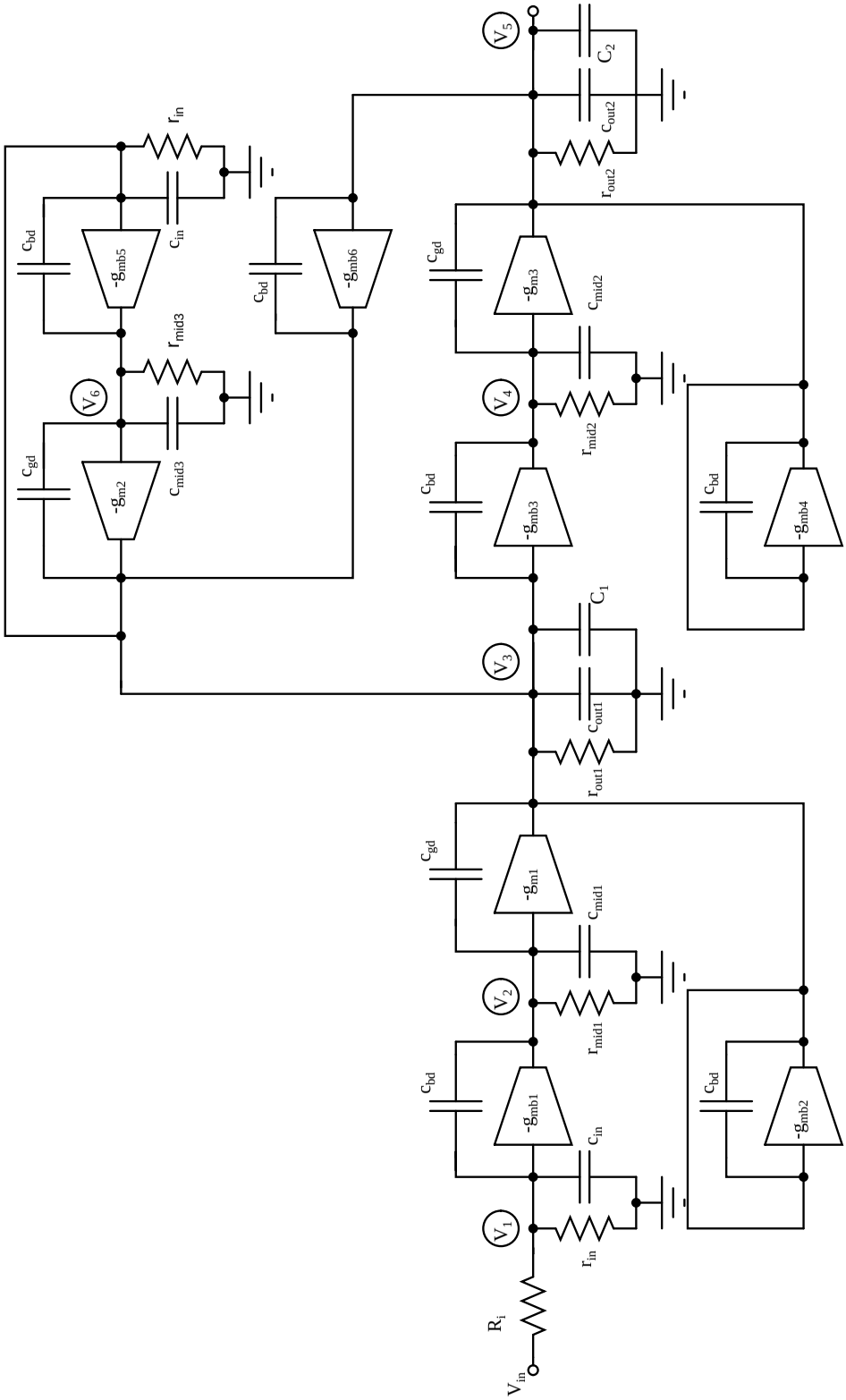


Figure 5.7: Small-signal equivalent circuit of the filter showing all the state variables

is a null matrix and is not shown.

$$\mathbf{H}\dot{x}(t) = \mathbf{A}x(t) + \mathbf{B}u(t) \tag{5.8}$$

$$y(t) = \mathbf{C}x(t) \tag{5.9}$$

where,

$$x = [V_1\ V_2\ V_3\ V_4\ V_5\ V_6]^T \tag{5.10}$$

$$u = [V_{in}] \tag{5.11}$$

$$y = [V_5] \tag{5.12}$$

Dimensions of the matrices are given below.

dim[**H**] = 6×6, dim[**A**] = 6×6, dim[**B**]= 6×1, dim[**C**] = 1×6.

The output node is V_5. Hence, **C** = [0 0 0 0 1 0].

Matrices of the descriptor state equation can be viewed as follows.

- **H**: Shows the capacitive coupling among the state variables and is derived based on (M.N.V.Prasadu, 2006).
- **A** : Shows the resistive coupling among the state variables.
- **B** : Shows the resistive coupling of the state variables with the input.

The state-space matrices for the Cochlea filter from Fig. 5.7 are written as follows.

$$\mathbf{H} = \begin{bmatrix} C_{11} & -c_{bd} & 0 & 0 & 0 & 0 \\ -c_{bd} & C_{22} & -c_{gd} & 0 & 0 & 0 \\ 0 & -c_{gd} & C_{33} & -c_{bd} & -c_{bd} & (-c_{bd}-c_{gd}) \\ 0 & 0 & -c_{bd} & C_{44} & -c_{gd} & 0 \\ 0 & 0 & -c_{bd} & -c_{gd} & C_{55} & 0 \\ 0 & 0 & (-c_{gd}-c_{bd}) & 0 & 0 & C_{66} \end{bmatrix} \tag{5.13}$$

where,

$$
\begin{aligned}
C_{11} &= c_{in} + c_{bd} \\
C_{22} &= c_{mid1} + c_{bd} + c_{gd} \\
C_{33} &= 3c_{in} + 2c_{out1} + 3c_{bd} + 2c_{gd} + C_1 \\
C_{44} &= c_{bd} + c_{gd} + c_{mid2} \\
C_{55} &= c_{out2} + 3c_{in} + c_{bd} + c_{gd} + C_2 \\
C_{66} &= c_{mid3} + c_{gd} + c_{bd}
\end{aligned}
$$

$$
\mathbf{A} = \begin{bmatrix}
G_{11} & 0 & 0 & 0 & 0 & 0 \\
-g_{mb1} & G_{22} & 0 & 0 & 0 & 0 \\
0 & -g_{m1} & G_{33} & 0 & -g_{mb6} & -g_{m2} \\
0 & 0 & -g_{mb3} & G_{44} & 0 & 0 \\
0 & 0 & 0 & -g_{m3} & G_{55} & 0 \\
0 & 0 & -g_{mb5} & 0 & 0 & G_{66}
\end{bmatrix} \tag{5.14}
$$

where,

$$
\begin{aligned}
G_{11} &= -\frac{1}{R_i} - \frac{1}{R_{in}} \\
G_{22} &= -\frac{1}{R_{mid1}} \\
G_{33} &= -3\frac{1}{R_{in}} - \frac{1}{R_{out1}} - \frac{1}{R_{out3}} - g_{mb2} \\
G_{44} &= -\frac{1}{R_{mid2}} \\
G_{55} &= -\frac{1}{R_{out2}} - g_{mb4} \\
G_{66} &= -\frac{1}{R_{mid3}}
\end{aligned}
$$

$$\mathbf{B} = \begin{bmatrix} -\frac{1}{R_i} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{5.15}$$

The parasitic resistance, parasitic capacitance and transconductance values are obtained from the DC operating point analysis of the filter. To validate the model, response of the state-space model is compared with that of the transistor level filter for one set of intended integrator capacitors C_1 and C_2. Figure 6.3 shows the accuracy of the model. It can be seen that the model of the filter closely matches with the transistor level filter, however there is a small deviation found in the stop band.

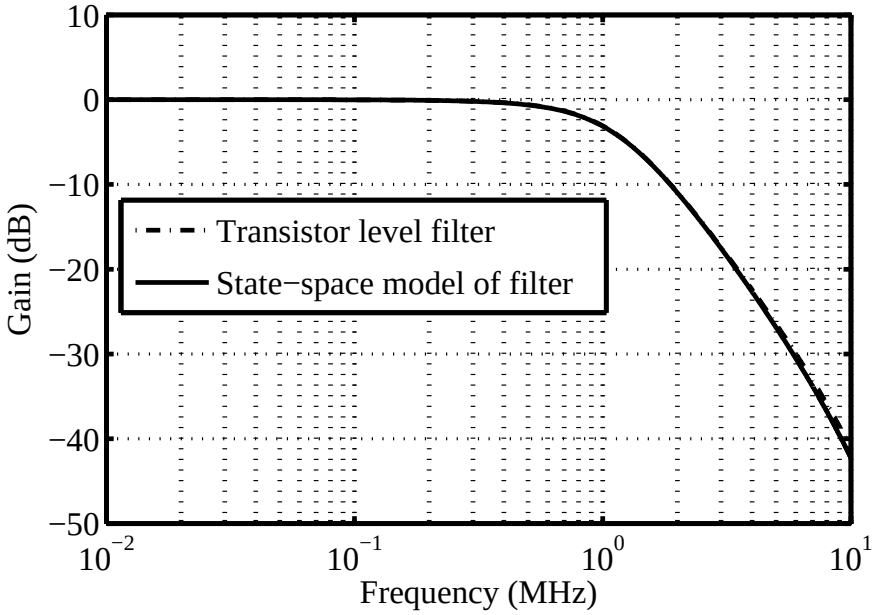


Figure 5.8: Comparing the magnitude response of state-space model with the transistor level filter.

5.5 PERFORMANCE OF THE FILTER

The filter is design centered using the state-space model. But, unlike in the method outlined in chapter 2, the required values of the intended capacitors are obtained by optimizing the filter model for ideal second-order Butterworth response. These capacitors are directly plugged into the transistor level filter to get the final response. The mag-

nitude response of the design centered transistor level filter is shown in Fig. 5.9. The deviation in the filter response from the ideal is due to the fact that the design centering process attempts to optimize a sixth order system to a second order response. The optimization can yield accurate result if and only if, the effect of parasitic poles and zeros are negligible in the band of interest.

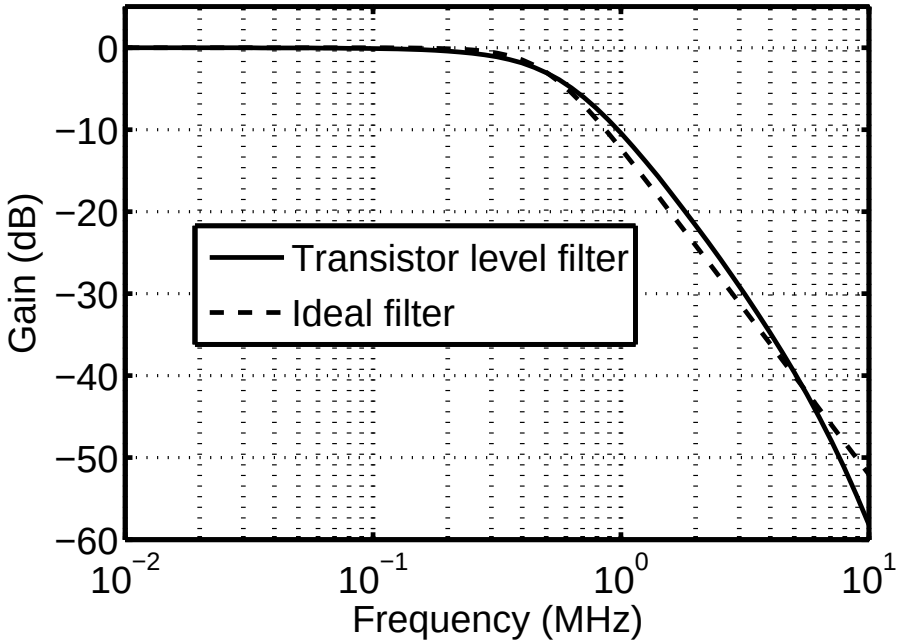


Figure 5.9: Magnitude response of transistor level filter vs ideal.

The simulated output noise power spectral density of the filter is shown in Fig. 5.10. At low frequency, it is dominated by 1/f noise while the thermal noise dominates near the band-edge.

Filter is simulated for an in-band tone of 450 kHz. 1% Total harmonic distortion is observed for an input peak-to-peak differential voltage of 170 mV. Dynamic range of the filter is found to be 51 dB. The dynamic range is calculated as the ratio of rms differential input voltage at 1% total harmonic distortion (THD) to input referred rms noise over the frequency range of 1 Hz to 5 MHz. The performance parameters of the filter are listed in Table 5.1.

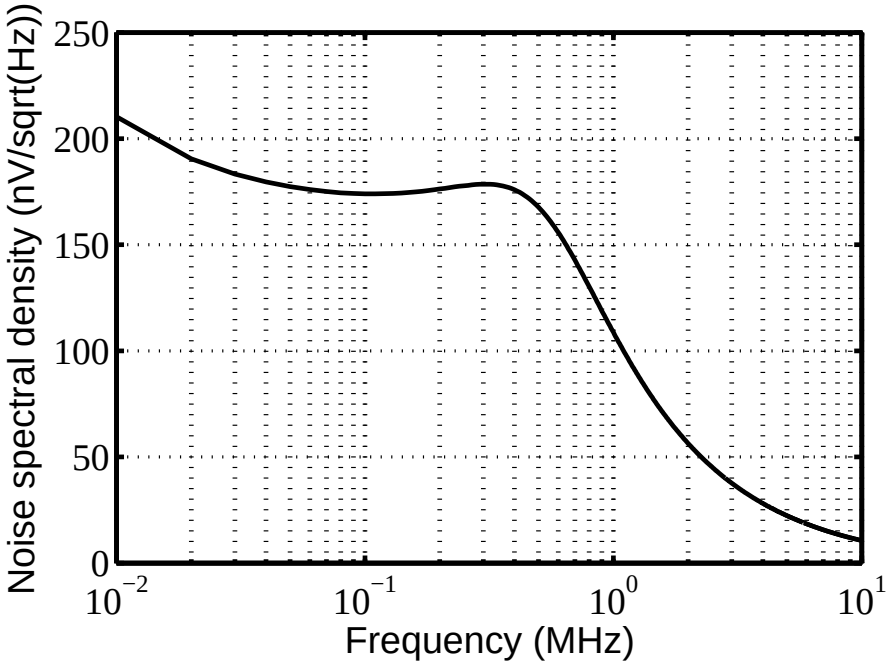


Figure 5.10: Output noise spectral density of the filter.

Table 5.1: **Performance parameters of Cochlea low-pass filter.**

Parameters of the filter	**Simulated values of Cochlea filter**
Supply [V_{DD}]	0.5
Technology [μm]	0.18
Cutoff frequency [kHz]	500
Power dissipation [μW]	20
Input noise [μV_{rms}]	207.50
Input [V_{pp} mV]@ 450 kHz for 1 % THD	170
Dynamic range [dB]	51

Simulations are carried out to test the robustness of the design for process corners, $\pm$10% change in supply voltage from nominal 0.5 V and temperature variations in the range of 0-70^{o}C. Fig. 5.11 shows the normalized magnitude response for all five process corners at room temperature and nominal supply voltage. It is observed that the change in bandwidth is less than $\pm$0.9% .

Figure 5.12 shows the normalized magnitude response for $\pm$10 % change in supply voltage at room temperature and typical corner. It is observed that the change in bandwidth is less than $\pm$7.14% at room temperature. The normalized magnitude re-

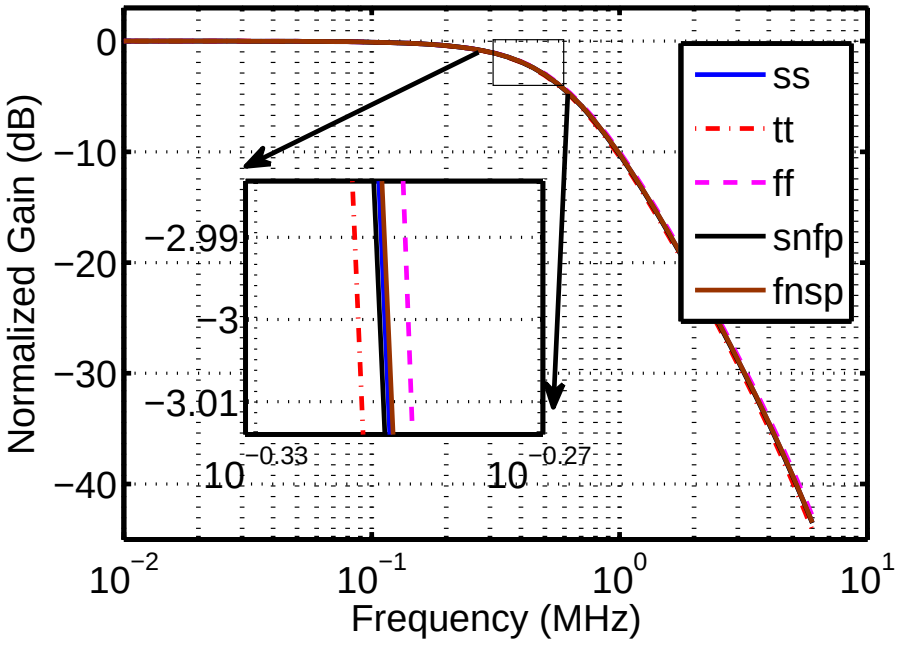


Figure 5.11: Magnitude response across process corners.

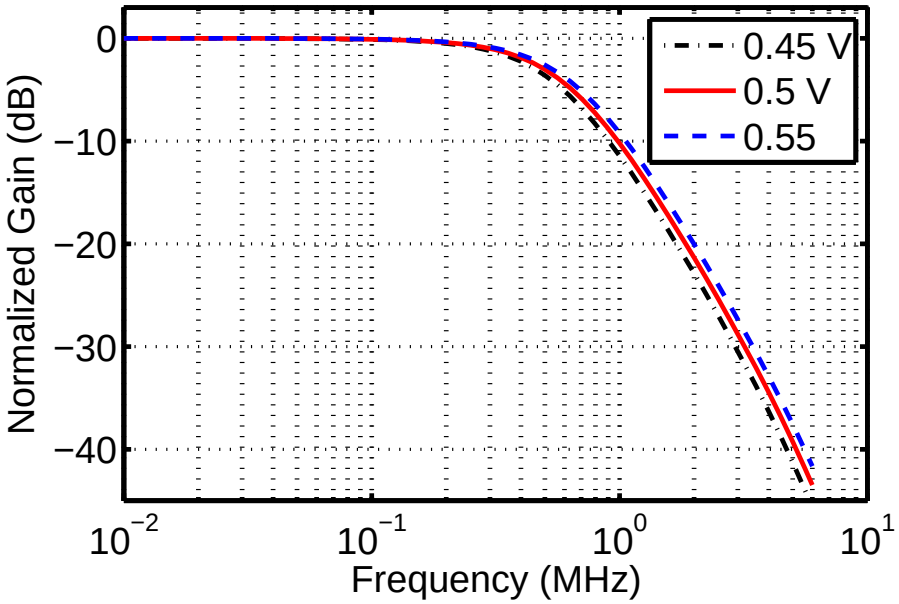


Figure 5.12: Magnitude response variations for ±10 % change in supply voltage at room temperature.

sponse for 0-70°C change in temperature at nominal supply voltage and typical corner is shown in Fig. 5.13. The change in bandwidth observed is less than ±6.5%.

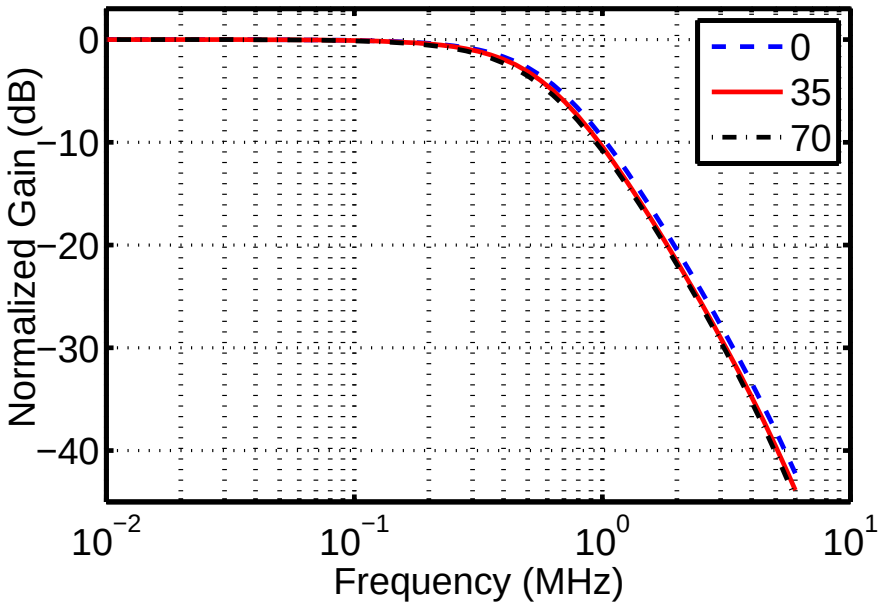


Figure 5.13: Magnitude response for change in temperature in the range of 0-70°C at typical corner and nominal supply voltage.

The performance of the designed filter is compared with some of the low voltage filters found in literature in Table 5.2. The distortion in (Chatterjee et al., 2005; Zhang and El-Masry, 2007; Carrillo et al., 2008, 2010) is computed for an in-band tone near the band-edge and so is in this work. The distortion measurement is done for a tone at 450 kHz. The FOM is computed using the same formula as given in (4.3) presented in chapter 4. The filter is found to be one of the filters offering lowest FOM.

Table 5.2: **Comparison of the present work with those available in the literature.**

Reference	**Bandwidth [kHz]**	**Order [n]**	**Supply Voltage [V]**	**Power [μW]**	Q_{max}	**Dynamic range@1 % THD [dB]**	**Topology**	**Tech-nology [μm]**	**FOM [fJ]**
(Chatterjee et al., 2005)	135	5	0.5	1100	6.2	56.6[1]	Active-RC	0.18	0.58
(Zhang and El-Masry, 2007)	1050	3	1.8	4070	1.99	45[2]	G_m-C	0.18	20.53
(Carrillo et al., 2008)	17.5	2	1	45	0.89	63.71[3]	G_m-C	0.35	0.62
(Carrillo et al., 2010)	10	2	1.5	648	0.707	62.6 [3]	G_m-C	0.35	25.18
Present work	500	2	0.5	19.8	0.707	51[4]	G_m-C	0.18	0.225

[1]Ratio of input @100 kHz for 1 % THD to integrated input noise, [2]Ratio of input @1 MHz for 1 % THD to integrated input noise, [3]Ratio of input @1 kHz for 1 % THD to integrated input noise, [4]Ratio of input @450 kHz for 1 % THD to integrated input noise.

5.6 LIMITATION ON BANDWIDTH SCALING

For a silicon Cochlea, the frequency band of interest is the audio band (20 Hz-20 kHz). The highest bandwidth of the second order low-pass filter required for silicon cochlea realization is 20 kHz. However, in this research, along with designing Cochlea filter in standard CMOS process for operation on 0.5 V supply it is also explored the limit to which the bandwidth can be pushed. In this section, a mathematical analysis has been carried out to postulate the maximum limit on scaling the bandwidth of the Cochlea filter.

The frequency response of a G_m-C filter can be scaled in two ways (Pavan and Tsividis, 2000).

- Constant-capacitance scaling: all transconductances and conductances are scaled by a constant factor, while keeping all the capacitances constant.
- Constant-transconductance scaling: all capacitances are scaled by a constant factor, while the transconductances and conductances are kept constant.

Let us take a Cochlea filter having Butterworth response and 20 kHz bandwidth. For the ease of design, let us say, we take the bulk transconductance of 10 μS. Assuming ideal transconductors, the capacitors C_1 and C_2 required are 112.5 pF and 56.25 pF respectively. If the bandwidth of the filter is to be increased without the increase in power, one need to go for constant transconductance scaling. Therefore, to scale up the bandwidth by factor α, all the capacitances must be scaled down by the same factor. Scaling the capacitor is not straight-forward as one need to account for the parasitic capacitances of the transconductor and layout which remain constant. Only option, the designer is left with, is to tweak the intended integrating capacitors which is physically placed at the integrating nodes so that the total capacitance at every node is scaled. Therefore, the minimum effective capacitance at any node is limited by parasitics, thus posing an upper limit on the achievable bandwidth. Figure 5.14 shows a transconductor,

with input parasitic capacitance at each input denoted as $c_{i,par}$ and the parasitic capacitance at the output denoted as $c_{o,par}$. When this transconductor is used in the Cochlea

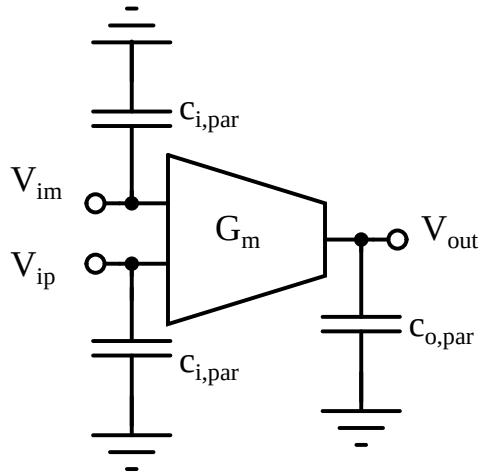


Figure 5.14: Differential-in single ended output transconductor with input and output parasitics.

filter, total parasitic capacitance appearing at each of the two nodes is given by (5.16) and (5.17) and the same has been shown in Fig. 5.15.

$$c_{1,par} = 3c_{i,par} + 2c_{o,par} \tag{5.16}$$

$$c_{2,par} = 2c_{i,par} + c_{o,par} \tag{5.17}$$

For scaling the bandwidth by α, both C_1 and C_2 should be scaled by factor $1/\alpha$. Therefore, intended integrating capacitances to be put at the two nodes, denoted by $C_{1,int}$ and $C_{2,int}$ respectively, can be computed from (5.18) and (5.21).

$$C_{1,int} = \frac{C_1}{\alpha} - c_{1,par} \tag{5.18}$$

$$C_{2,int} = \frac{C_2}{\alpha} - c_{2,par} \tag{5.19}$$

Noting that $C_1 = \dfrac{C_2}{Q^2}$ and writing $c_{1,par} = (1+x)c_{2,par}$ whare $x = \dfrac{(c_{ip}+c_{op})}{(2c_{ip}+c_{op})}$, (5.18)

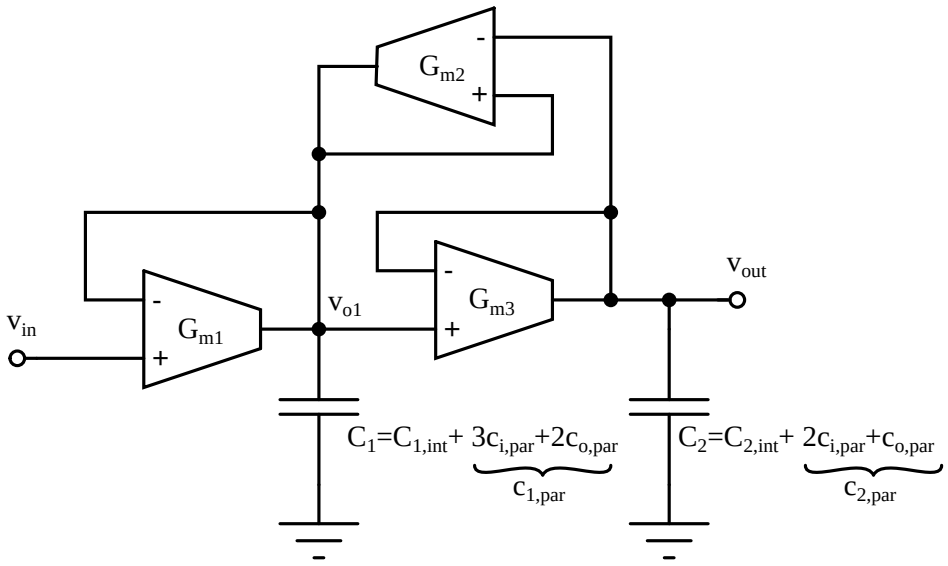


Figure 5.15: Cochlea filter showing the net capacitance at each integrating node.

and (5.21) can be re-written in the form

$$C_{1,int} = \frac{1}{Q^2}\left[\frac{C_2}{\alpha} - Q^2(1+x))c_{2,par}\right] \tag{5.20}$$

$$C_{2,int} = \frac{C_2}{\alpha} - c_{2,par} \tag{5.21}$$

The maximum value of α, is the α for which either $C_{1,int}$ or $C_{2,int}$ become zero. Or in other words,

$$\alpha_{max} = min\left[\left(\frac{1}{(1+x)Q^2}\frac{C_2}{c_{2,par}}\right), \frac{C_2}{c_{2,par}}\right] \tag{5.22}$$

$$= min\left[\frac{C_1}{c_{1,par}}, \frac{C_2}{c_{2,par}}\right] \tag{5.23}$$

From (5.23) it can be seen that if $Q > \sqrt{\frac{c_{2,par}}{c_{1,par}}}$, the node-1 parasitic will determine α_{max} otherwise node-2 parasitic decides α_{max}. However, the following points may be noted for deciding on α_{max}.

- In the analysis, it is assumed that the only non-ideality of the transconductor has the parasitic capacitances.

- In presence of finite input/output resistance, the scaling factor that can be achieved will be much less than α_{max} obtained from (5.23). Because, sufficient margin must be provided for $C_{1,int}$ and $C_{2,int}$ so as to allow for an effective design centering.
- Due to the presence of inter-node coupling capacitance (c_{bd}), again some margin is necessary to allow effective design centering.

For the Cochlea filter architecture taken in this work, the parasitic capacitances are about $c_{1,par}$=0.6 pF and $c_{2,par}$=0.4 pF. α_{max} computed from (5.23), for C_1 and C_2 of 112.5 pF and 56.25 pF respectively, is 141. This amounts a maximum bandwidth of 141×20 kHz = 2.82 MHz. Allowing a factor of safety of $five - six$ for the effective design centering in presence of all non-idealities, the bandwidth of the filter is chosen to be 500 kHz in the present work.

To emphasize the effect of scaling, the filter bandwidth is scaled down to 20 kHz (f_o) using constant transconductance scaling. Figure 5.16 shows the magnitude response of the Cochlea filter scaled to bandwidth of 20 kHz for the same power. It is noted that response matches closely with that of ideal Butterworth response.

5.7 *Q* TUNING

The Cochlea filter offers very high sensitivity for Q which is outlined in section 5.2.1. To illustrate this with the designed filter, the bias current of the Q-tuning transconductor G_{m2} is tuned above and below the nominal value of 2 μA. The response of the filter is plotted in Fig. 5.17 by scaling the bias current of G_{m2} by factor n with n=1 corresponding to nominal current of 2 μA. It can be clearly seen that the Cochlea filter can be programmed for Q-tuning. Such a Q-tuning finds its application in silicon Cochlea used in hearing aid (Watts et al., 1992; Lyon, 1998; Sarpeshkar et al., 1998).

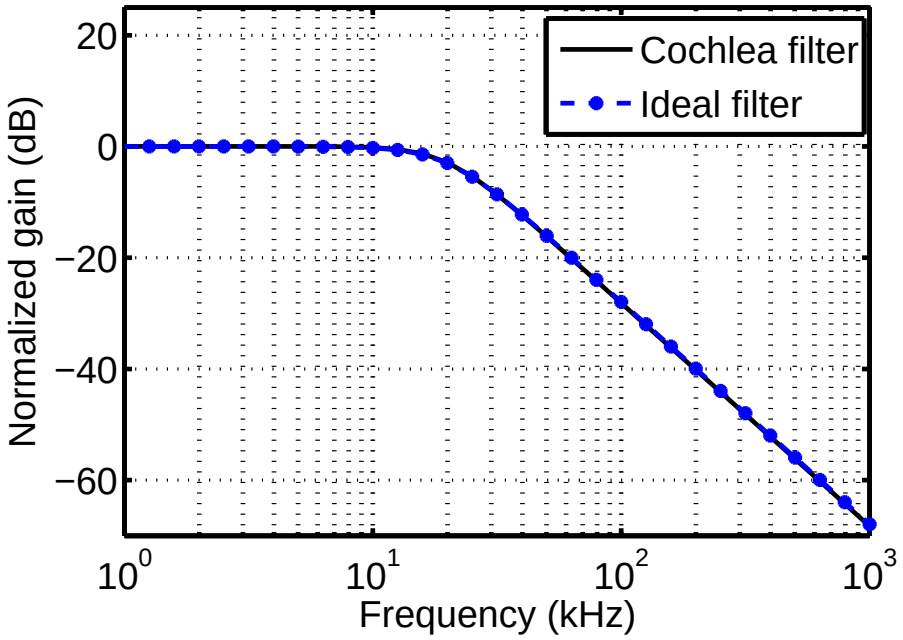


Figure 5.16: Magnitude response of 20 kHz bandwidth transistor level filter vs ideal.

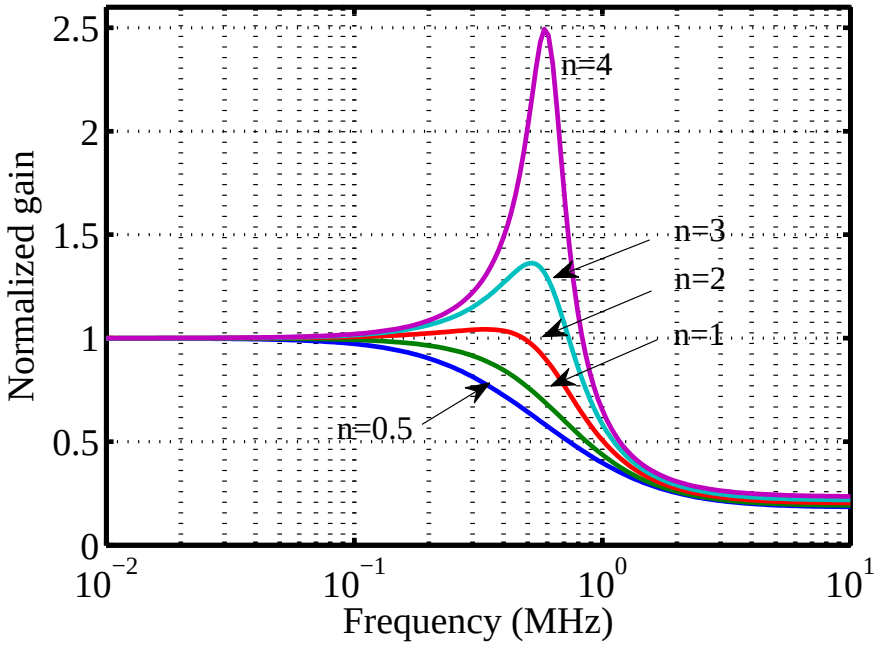


Figure 5.17: Illustration of filter *Q*-tuning by varying the bias current of G_{m2} by factor *n*.

CHAPTER 6

TWO-PORT ABCD PARAMETER BASED MODELING OF FILTERS FOR DESIGN CENTERING

6.1 INTRODUCTION

In a typical system-On-Chip (SOC), analog and RF front end exist along with the digital circuits. Analog components play an important role in integrated circuits. According to Electronic Design Automation (EDA) magazine on March 21,2005 (Graeb, 2007), analog components use, on average, 20% of the integrated circuits area and also reported that 75% of all integrated circuits would contain analog components. At the same time, the analog components require around 40% of the integrated circuits design effort and are responsible for about 50% of the design re-spins. Analog design automation is needed to improve the design quality and reduce the design effort, as more and more analog circuits are being integrated into ICs along with digital circuits. These requirements drive the designers to rely heavily on CAD tools in order to reduce the time-to-design and errors in designing/modeling circuits.

Like any design cycle, the design of analog circuits (amplifiers, filters etc.) starts with a set of specifications. An architecture is then chosen to meet the specifications. The initial design of the circuit, typically, assumes ideal devices/elements. With this assumption, a basic schematic is designed using CAD tools. However, the actual results form the schematic, when technology specific circuit elements are used, will deviate from the ideal. In CMOS circuits, the deviation is normally attributed to finite $g_m r_o$

product of transistors and parasitic capacitors. It becomes necessary to *design center* the filter to achieve a response that is in close match with the desired response even in presence of non-idealities.

One such design-centering technique used for integrated continuous-time filters is presented in (Laxminidhi and Pavan, 2007). This paper presents a simple design centering technique for integrated continuous-time transconductor-capacitor (G_m-C) filters. Due to the fully-differential architecture, chosen for the filter, the parasitic capacitance's appearing at the integrating nodes with-respect-to small-signal ground have the dominating effect on the response. The effect of any inter-node parasitic capacitance is made small by design and a careful layout technique. The above assumptions make the design centering process simple which is evident from the paper. However, when the filter has a single ended architecture, for example Cochlea architecture (Lyon and Mead, 1988), the above assumption may not be valid if the internode capacitance is a significant fraction of the integrating capacitor.

A course model is used for design centering the filter in (Laxminidhi and Pavan, 2007) and is arrived using state-space approach. The state-space model of the filter is arrived by writing down the small-signal equivalent circuit. Transconductor is modeled as an equivalent circuit consisting of a transconductance (g_m), output conductance g_o, input parasitic capacitance C_{in} and output parasitic capacitance C_p as shown in Fig. 6.1(a). It is to be noted that while modeling, the effect of overlap capacitance's is neglected and is assumed that all parasitic capacitance appear in parallel with the integrating capacitors. If C_n is the capacitance value to be present at a given node for a desired frequency response, it is clear from the Fig. 6.1(a) that the capacitance to be inserted (C_i) at that node can be easily found by subtracting the total parasitic capacitance appearing at that node from C_n. In presence of gate overlap capacitance (C_c), the equivalent circuit of the transconductor can be drawn as in Fig. 6.1(b). In such a case the state-space model of the filter used in (Laxminidhi and Pavan, 2007) will not be accurate enough due to

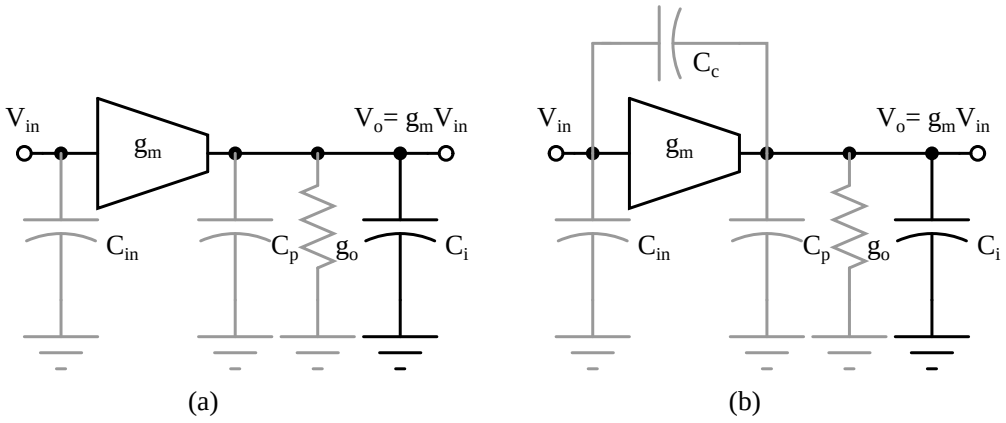


Figure 6.1: Equivalent circuit of non ideal transconductor (a) Without gate-overlap capacitance. (b) With gate-overlap capacitance.

following reasons- (a) possible frequency dependent Miller effect (b) addition of parasitic poles/zeros. It is not possible to adopt the design centering technique laid down in (Laxminidhi and Pavan, 2007) as it is. In this work an attempt is made to address this issue, especially in the regime of low voltage design.

With the reduced supply voltage for low voltage applications, voltage headroom issue due to higher threshold voltage can be critical. The transistors may be operating in weak inversion or in sub-threshold region. In such a scenario, while modeling circuits one need to consider the sub-threshold effects. This may not be feasible always if accurate sub-threshold models are not available for the MOS transistors. Therefore, the simple design centering technique presented in (Laxminidhi and Pavan, 2007) for filter operating at 3.3 V supply, that use state-space model may not be suitable for circuits operating at low voltage if one needs to consider sub-threshold effects and other parasitic poles and zeros.

Two-port parameter based representation is one of the methods used to model a linear system. This method can be readily adopted to model continuous-time filters as they are assumed to be linear for small-signal. Two-port transmission line parameter (ABCD parameter) model is one such method that can be effectively used for cascaded networks. This method is simple and has couple of advantages over other methods. Re-

cent publications (Elwakil, 2010; Choma and Chen, 2007) showed that there is increase in the application of two-port transmission line approach for better understanding of circuits.

In this chapter a two-port transmission parameter based modeling of filter is presented. A Cochlea Butterworth low-pass filter operating on 0.5 V supply voltage presented in the chapter 5 is used as the test-vehicle to explore the merits of two-port transmission parameter based modeling over state-space based approach for design centering the filter, specially when using CAD tools. The proposed technique is compared with the technique presented in (Laxminidhi and Pavan, 2007), henceforth referred as conventional method.

6.2 MODEL USING CONVENTIONAL METHOD

The Cochlea filter presented in Chapter 5 is redrawn in Fig. 6.2 for completeness. C_x and C_{out} are the effective integrating capacitors. Each capacitor is a combination of two components as shown in the figure viz. effective parasitic capacitance ($c_{x,par}$ and $c_{o,par}$) and the intended capacitor ($C_{x,int}$ and $C_{o,int}$). Intended capacitors are the capacitors explicitly placed at the two nodes. The required value of C_x and C_{out} are computed for Butterworth response and 500 kHz bandwidth assuming ideal conditions. But non-idealities of the OTA like parasitic capacitance, finite output impedance and finite input impedance cause the frequency response to deviate from the Butterworth response. In order to analyze the limitations of the conventional design centering process, the Cochlea filter is first modeled in a manner similar to that given in (Laxminidhi and Pavan, 2007).

Figure 6.2 is a simple schematic of the filter. At the intermediate node x, r_x is the effective resistance seen and C_x is the effective capacitance seen at this node. Similarly r_{out} and C_{out} are the effective resistance and capacitance at the output node. The state-

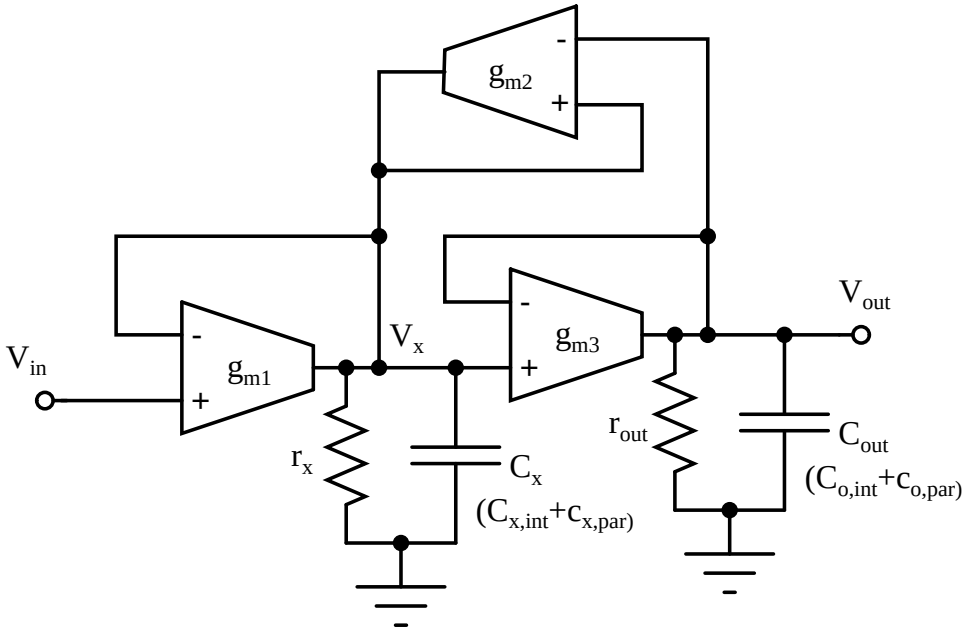


Figure 6.2: Equivalent circuit of the Cochlea filter considering the effect of finite input and output impedance of the transconductor.

space model of this filter is given by (6.1) and (6.2).

$$\dot{x}(t) = \mathbf{A}x(t) + \mathbf{B}V_{in}(t) \tag{6.1}$$

$$y(t) = [0\ 1]\,x(t) \tag{6.2}$$

where,

$$x(t) = [V_x\ V_{out}]^T \tag{6.3}$$

$$\mathbf{A} = \begin{bmatrix} \dfrac{(g_{mb2} - g_{mb1} - \dfrac{1}{r_x})}{C_x} & -\dfrac{g_{mb2}}{C_x} \\ \dfrac{g_{mb3}}{C_{out}} & -\dfrac{(g_{mb3} + \dfrac{1}{r_{out}})}{C_{out}} \end{bmatrix} \tag{6.4}$$

$$\mathbf{B} = \begin{bmatrix} \dfrac{g_{mb1}}{C_x} & 0 \end{bmatrix}^T \tag{6.5}$$

Note that all the transconductances g_{m1}-g_{m3} are replaced by g_{mb1}-g_{mb3} since the transconductors under consideration are body-driven. All the required resistances and transconductance values are taken from DC operating point analysis of the transconductor. Though for the transistor level circuit, parasitic capacitances are considered as separate entities, for the model they are not. For the model, C_x and C_{out} are considered as single entities and the parasitic capacitances can be absorbed into them.

The filter is design centered using the approach proposed in (Laxminidhi and Pavan, 2007). For the sake of completeness, the design centering process is briefly outlined as follows. Here, C_x and C_{out} are are represented as a vector $\mathbf{C} = [C_x\ C_{out}]$. Similarly $\mathbf{C_{int}} = [C_{x,int}\ C_{o,int}]$ and $\mathbf{c_{par}} = [c_{x,par}\ c_{o,par}]$.

1. Frequency response of the transistor level filter is obtained by inserting known set of intended integrating capacitors $\mathbf{C_{int}}$, say $\mathbf{C_{int:fil}}$. A best choice for initial set of $\mathbf{C_{int:fil}}$ will be the set that is computed assuming ideal transconductors.
2. The model is now tuned (optimized), by tweaking its $\mathbf{C}$, to match the response of the transistor level filter. Let the optimized set of capacitors be $\mathbf{C_{m1}}$.
3. If the model is accurate, the optimized set of capacitors from the model can be used to estimate the parasitics $\mathbf{c_{par}}$ of the transistor level filter. i.e. $\mathbf{c_{par}} = \mathbf{C_{m1}} - \mathbf{C_{int:fil}}$. Note, in step-1, if we set $\mathbf{C_{int:fil}} = [0\ 0]$ then $\mathbf{c_{par}} = \mathbf{C_{m1}}$.
4. Estimate the capacitors in the model required to get a response close to ideal. Let the capacitors required be $\mathbf{C_{m2}}$.
5. For the transistor level filter to offer a response close to ideal, it should have the same set of capacitors $\mathbf{C_{m2}}$ at its nodes. Knowing the parasitic capacitors at the nodes, the required intended capacitors that needs to be put in the transistor level circuit can be easily calculated.

Steps 1-3 are carried with initial set $\mathbf{C_{int:fil}} = [0\ 0]$ i.e. with no intended integrating capacitors in transistor level circuit. Fig. 6.3 and Fig. 6.4 shows the magnitude and phase response of the conventional (state-space) model of the filter compared with that of transistor level filter. The frequency response of the model is in deviation from that of the transistor level. This indicates that the model fails to estimate the filter parasitics accurately. The reason for this is that the model is a second order system

where as the transistor level filter is a higher order system with additional poles/zeros due to body-drain junction capacitance and the parasitic poles and zeros added due to the intermediate node of the transconductor (refer to Fig. 5.3 in chapter 5).

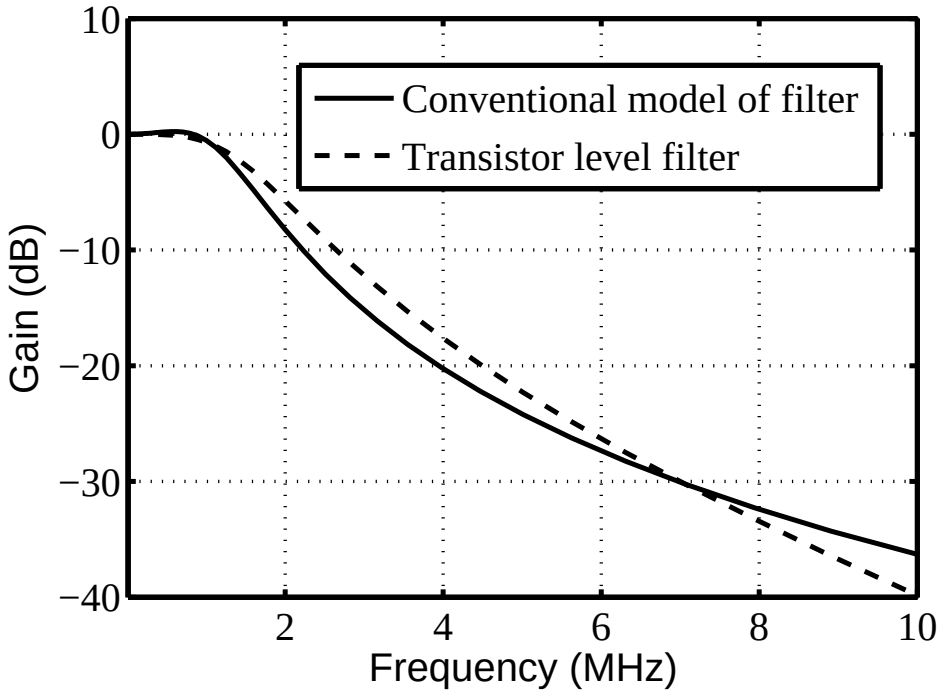


Figure 6.3: Magnitude response of state-space model and transistor level filter after estimating the parasitic capacitors.

For better accuracy of model, the inter node capacitances, parasitic poles and zeros are required to be taken into account. Every transconductor in the filter needs to be modeled accurately. The transconductor designed in this work, has an intermediate node formed at the common-drain point of M_1 and M_3 (refer Fig. 5.3). Also there exists a body-drain junction capacitors due to M_1 and M_2. An accurate state-space model for the Cochlea filter, considering the non-idealities, has been derived in chapter 5. The same may be used for design centering the filter. However, the following limitation can be observed for such a modeling method. Actual order of the state-space matrix can be more than that of the ideal situation, if there are intermediate nodes in the transconductor; for example, the transconductor used in the Cochlea filter. As the filter order increases, writing state-space model will require too much of designers attention and

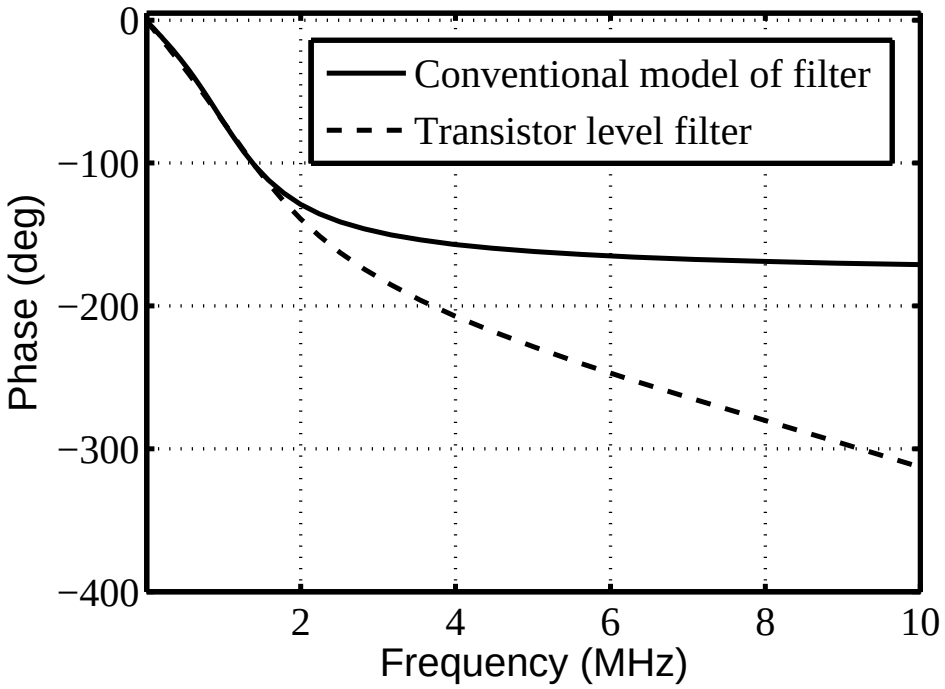


Figure 6.4: Phase response of state-space model and transistor level filter after estimating the parasitic capacitors.

time. Often, this may lead to error in modeling.

For the Cochlea filter architecture considered in this work and for similar architectures, there is need for a method to model the filter as accurate as possible and at the same time keeping it simple for designers. A close look at the architecture of the filter reveals that, the filter can be considered as cascade of several two-port networks. It is a well known fact that two-port transmission line (ABCD) parameter representation is the best suited two-port network model to represent cascaded two-port networks. It is worth exploring the usefulness of transmission line parameter modeling for the filter as an alternative to state-space model.

6.3 MODEL USING ABCD-PARAMETER APPROACH

The Cochlea filter shown in Fig. 6.2 can be viewed as four individual two-port networks connected in cascade as shown in Fig. 6.5. Individual two-port networks are named

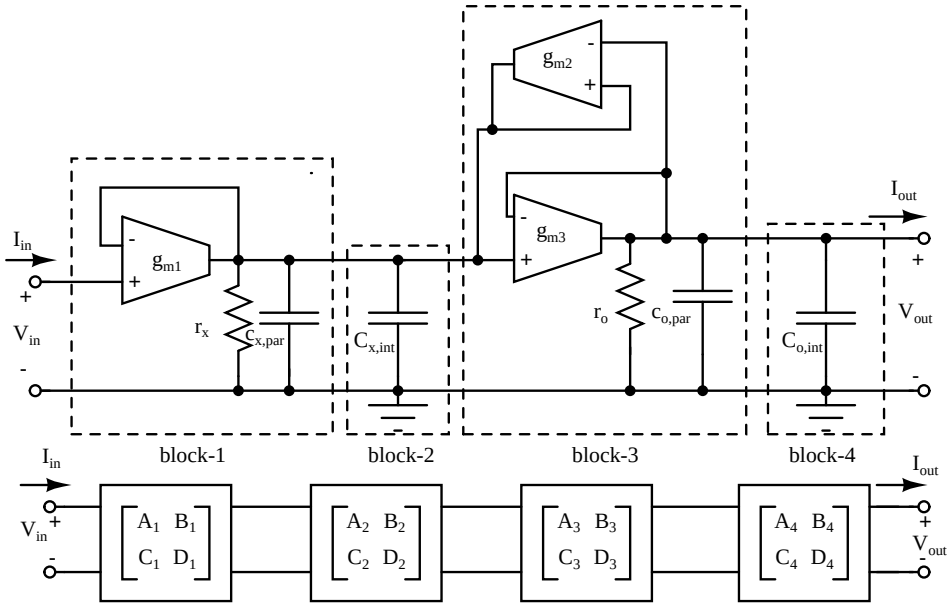


Figure 6.5: Cochlea filter represented in the form of cascaded two-port networks and their respective ABCD parameters connected in cascade form.

block-1 to block-4 in the figure. Note that, intended capacitors $C_{x,int}$ and $C_{o,int}$ are taken as individual two-port blocks (*block-2* and *block-4*), while parasitics of transconductors are absorbed into respective blocks (*block-1* and *block-3*). In Fig. 6.5, each block is also represented by its two-port ABCD parameters. When ABCD-parameters are used to represent linear two-port networks, the ABCD model of the cascade network can be easily obtained by multiplying ABCD matrix of individual blocks i.e. if A_i, B_i C_i and D_i are the ABCD parameters of i^{th} block in Fig. 6.5, the entire filter can be represented using ABCD-parameters as in (6.6).

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} \begin{bmatrix} A_4 & B_4 \\ C_4 & D_4 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \tag{6.6}$$

ABCD-parameter representation of blocks 2 and 4 is simple and can be written as in (6.7) and (6.8).

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_{x,int} & 1 \end{bmatrix} \tag{6.7}$$

$$\begin{bmatrix} A_4 & B_4 \\ C_4 & D_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_{o,int} & 1 \end{bmatrix} \tag{6.8}$$

For finding the ABCD matrix elements of blocks 1 and 3, one need to run four simulations on each block. Fig. 6.6 shows the simulation set-up required to find ABCD parameters of a given block. The simulations required are small-signal AC analysis over a frequency grid of interest. The procedure for finding these parameters is outlined as follows.

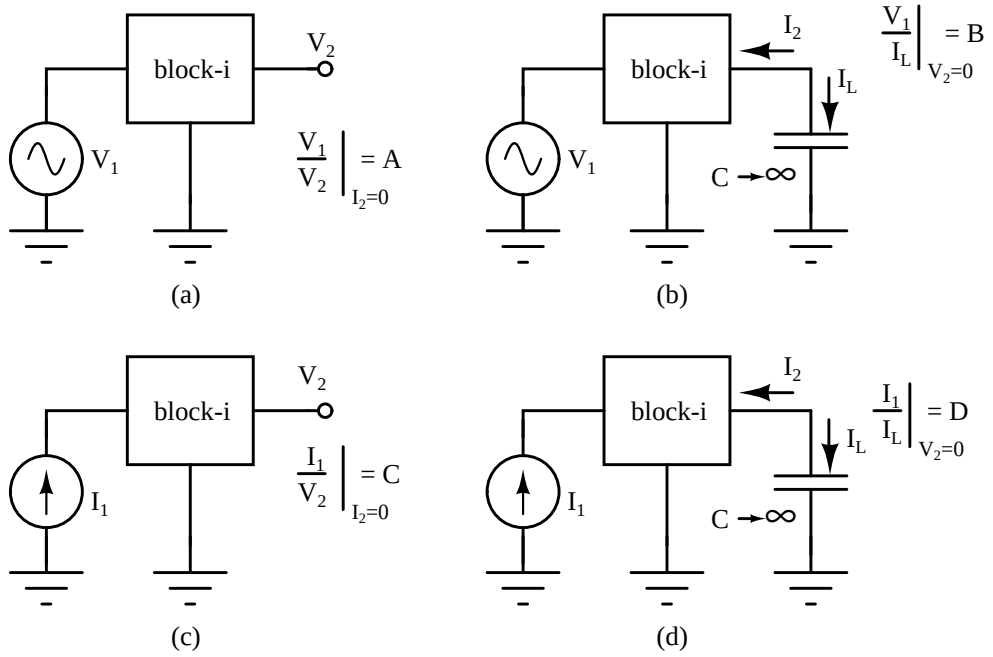


Figure 6.6: Simulation setup to determine *ABCD* parameters of i^{th} block (a) *A*-parameter. (b) *B*-parameter. (c) *C*-parameter. (d) *D*-parameter.

To find parameter A:

- By definition, $A = \left[\frac{V_1}{V_2}\right]_{I_2=0}$ i.e. the ratio of port-1 voltage (input voltage) to the port-2 voltage (output voltage) with the port-2 open circuit.
- The test setup shown in Fig. 6.6(a) is used to find *A*.
- AC simulations are run for a given frequency grid over a DC operating point with voltage as the input at port-1 and with port-2 open circuit.

- The voltage gain V_2/V_1 will yield a vector $1/A$ having a length equal to that of the frequency grid.
- Parameter A can be computed by taking element-by-element reciprocal of the vector $1/A$. Note that, simulators generally provide options to plot V_1/V_2 (i.e. input/output) in which case, this last step can be avoided.

To find parameter B:

- $B = -\left[\frac{V_1}{I_2}\right]_{V_2=0}$ i.e. the ratio of port-1 voltage (input voltage) to the port-2 current (output current) with the port-2 short circuit.
- The test setup shown in Fig. 6.6(b) is used to find B. Note that, a large capacitor (few tens of farads) placed at the port two offers very low reactance in the frequency grid of interest, thus acting as a short circuit. The capacitor offers short circuit without affecting DC operating point.
- AC simulations are run with voltage as input at port-1.
- The gain I_L/V_1 will yield a vector $1/B$ having a length equal to that of the frequency grid used for the simulation.
- Parameter B is the element-by-element reciprocal of the vector $1/B$.

To find parameter C:

- By definition, $C = \left[\frac{I_1}{V_2}\right]_{I_2=0}$ i.e. the ratio of port-1 current (input current) to the port-2 voltage (output voltage) with the port-2 open circuit.
- The test setup shown in Fig. 6.6(c) is used to find C.
- AC simulations are run for the same frequency grid over a DC operating point with current as input to port-1 and with port-2 open circuit.
- The gain V_2/I_1 will yield a vector $1/C$ having a length equal to that of the frequency grid.
- Parameter C is then computed by taking element-by-element reciprocal of the vector $1/C$.

To find parameter D:

- $D = -\left[\frac{I_1}{I_2}\right]_{V_2=0}$ i.e. the ratio of port-1 current to the port-2 current with the port-2 short circuit.
- The test setup shown in Fig. 6.6(d) is used to find D. The large capacitor at the port two acts as a short circuit without affecting DC operating point.
- AC simulations are run with current as input to port-1.
- The current gain I_L/I_1 is equal to $1/D$.
- Parameter D is the element-by-element reciprocal of the vector $1/D$.

The above exercise is carried out for the blocks 1 and 3 to find their ABCD parameters. These parameters are then taken to *MATLAB*, along with the parameters of blocks 2 and 4, as vectors corresponding to the frequency grid of interest. The ABCD matrix of the the filter is then computed. A pseudo-code for computing the ABCD matrix of the filter, assuming a frequency grid of length N, is outlined as follows.

```
  % Pseudo-code for computing the ABCD matrix
  % of the filter
  % w= frequency grid in rad/sec;
for i = 1 to N
  % Form the ABCD matrix of all blocks (1 to 4)
  % for 'i'th frequency
     [block1] = [A1(i) B1(i); C1(i) D1(i)];
     [block2] = [1  0;  j*w(i)C_{x,int} 1];
     [block3] = [A3(i) B3(i); C3(i) D3(i)];
     [block4] = [1  0;  j*w(i)C_{o,int} 1];
  % Compute the ABCD matrix of the filter
  % for 'i'th frequency
    ABCD_filter= [block1]*[block2]*[block3]*[block4];
  % A paramter of the filter for 'i'th frequency
    A_parameter_of_filter(i) = ABCD_filter(1,1);
```

```
end
  % Transfer function of the filter
    TF(jw)=1./A_parameter_of_filter
```

The transfer function of the filter is computed from the *A*-parameter of the filter i.e. $TF(j\omega) = 1/A_{fil}(j\omega)$ where, $A_{fil}(j\omega)$ is *A*-parameter of the filter.

Notice that the filter model has been derived directly from simulations and no paper work is necessary as unlike in the conventional method. The designers attention is only required to run the necessary simulations. Also, this technique can be readily applied to model the post layout extracted filter, if some care is taken to lay the filter in blocks.

The frequency response obtained from the ABCD-parameter based model of the filter and the transistor level filter are compared in Fig. 6.7 and Fig. 6.8 (magnitude and phase). The responses are obtained for one set of intended integrating capacitors. It can be inferred that, the model response is in a good match with transistor level filter response for the entire range of frequency. With the use of CAD tools, the complexity involved in modeling the filter with ABCD-parameter approach is found to be minimal, even with increase in the order of the filter.

6.4 DESIGN CENTERING USING PROPOSED METHOD AND CONVENTIONAL METHOD

After the filter is modeled, then it needs to be design centered to get response close to ideal. The design centering process is outlined as follows.

- Optimize the model to get a response close the ideal by tuning the intended integrating capacitors.
- The optimized set of capacitors are then put in the transistor level filter. If the model is having a good accuracy, the response of the transistor level filter will be the optimum and no further iterations are necessary (unlike in the case of conventional method).

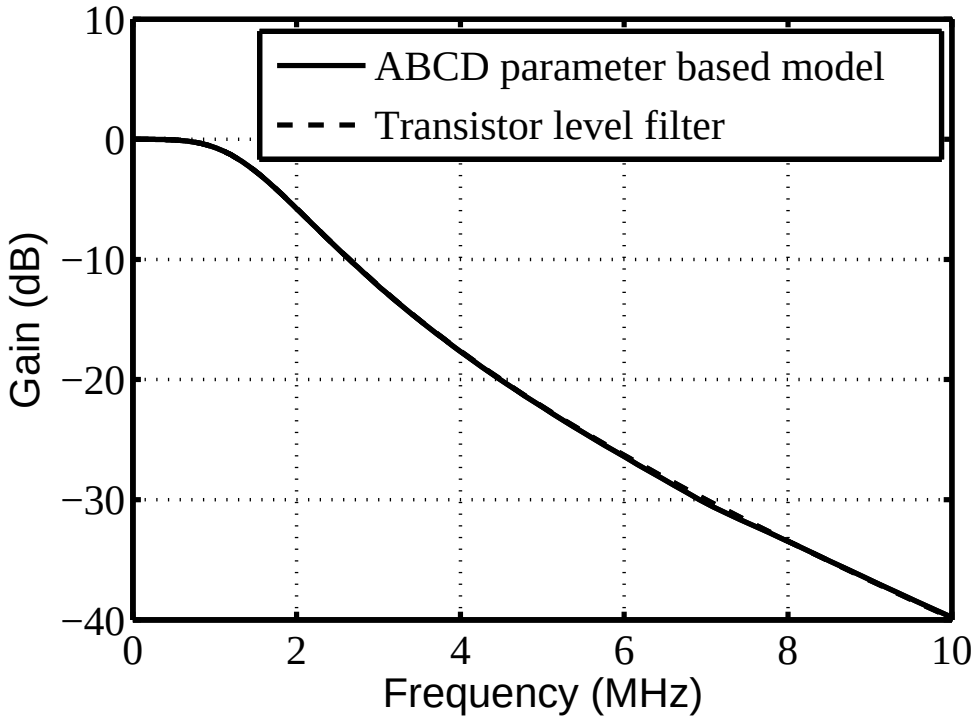


Figure 6.7: Magnitude response of ABCD parameter based model and transistor level filter.

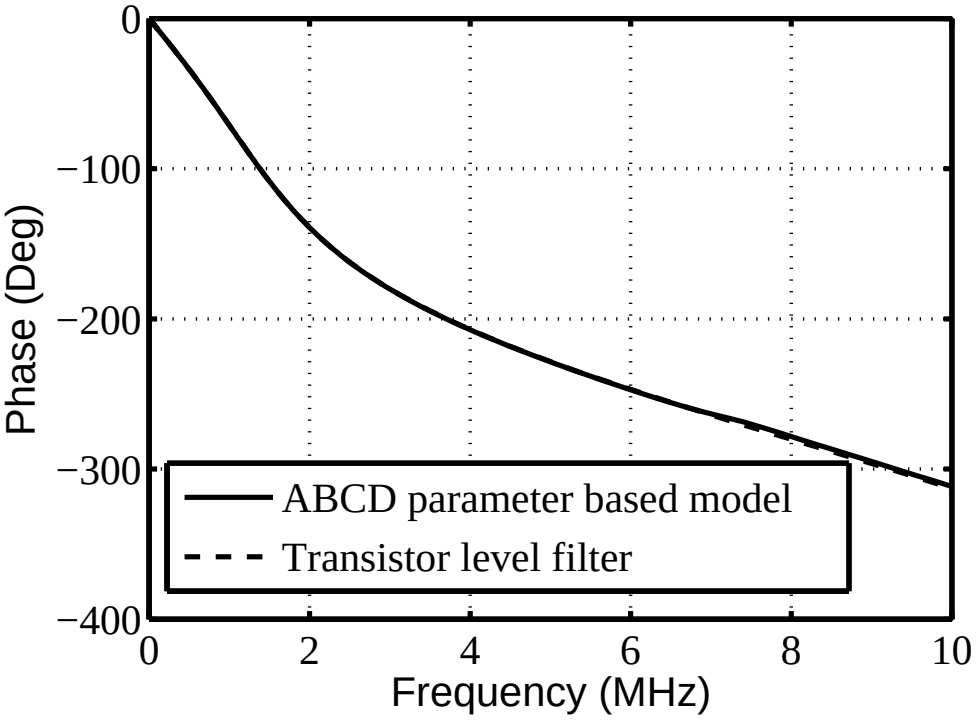


Figure 6.8: Phase response of ABCD parameter based model and transistor level filter.

The filter is design centered using both the state-space model based approach and ABCD-parameter based approach. The responses of the transistor level filter obtained after design centering using both the techniques are plotted in Fig. 6.9 along with the ideal. From the Fig. 6.9 it can be seen that near the band-edge, the proposed two-port

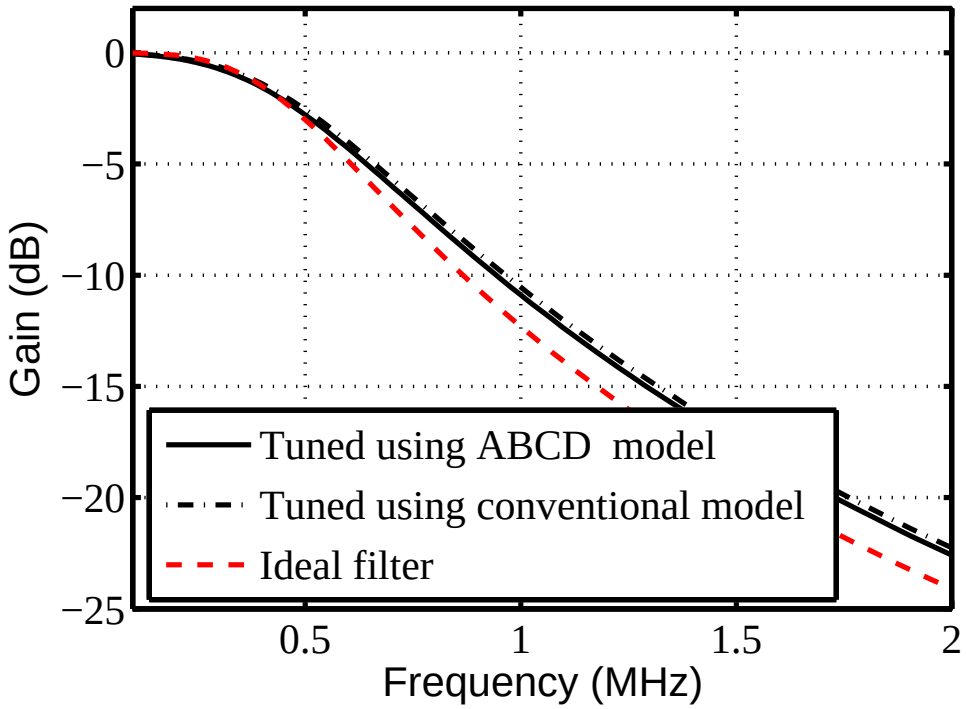


Figure 6.9: Magnitude response of transistor level filter tuned using ABCD based model and conventional model.

model based approach of design centering gives better accuracy than the state-space based approach. It is almost impossible to achieve perfect tuning even with two port based modeling due to the fact that the whole process of design centering here, attempts to match the response of a higher order filter (due to parasitics) to that of a ideal second order filter.

In order to highlight the effectiveness of the proposed modeling technique over conventional method, a percentage error in the magnitude response, defined as given in (6.9).

$$Percentage\ error = \left(\frac{gain_{ideal} - gain_{actual}}{gain_{ideal}} \right) \times 100 \tag{6.9}$$

is plotted in Fig. 6.10. In the pass-band, both the techniques offer similar error. However, in the stop band, the proposed ABCD parameter model based approach is found to be effective. The the maximum error is found to be 20 % for the proposed technique, while for that obtained using state-space approach, it is 25 %.

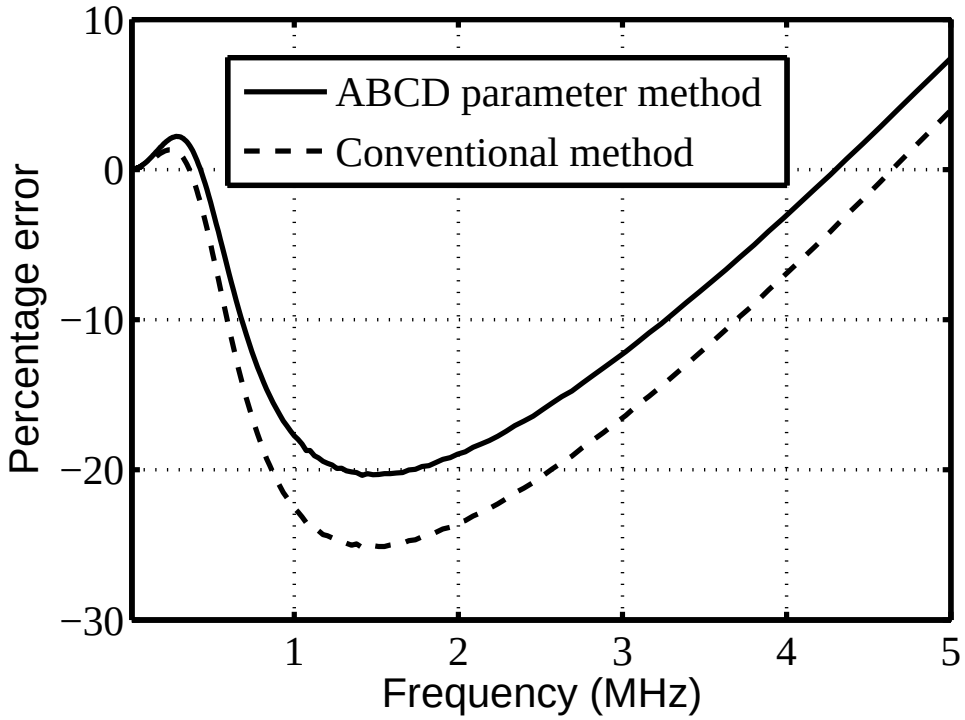


Figure 6.10: Percentage error with respect to ideal for transistor level filter tuned with ABCD parameter based model and conventional model.

The phase error ($\phi_{ideal} - \phi_{actual}$), is also plotted in Fig. 6.11 for the completeness. Ideally the phase error is expected to be zero if the response matches with ideal. It can be seen that the proposed technique offers smaller phase error in the pass-band when compared to the conventional method. In the stop-band, the phase error increases for both the techniques. This is expected since the actual filter is of higher order than the ideal.

The same filter is design centered for a bandwidth of 1 MHz frequency using both the models and the percentage error in the magnitude response as given in (6.9) is plotted in Fig. 6.12. Pass-band error remains same. However, in the stop band, the

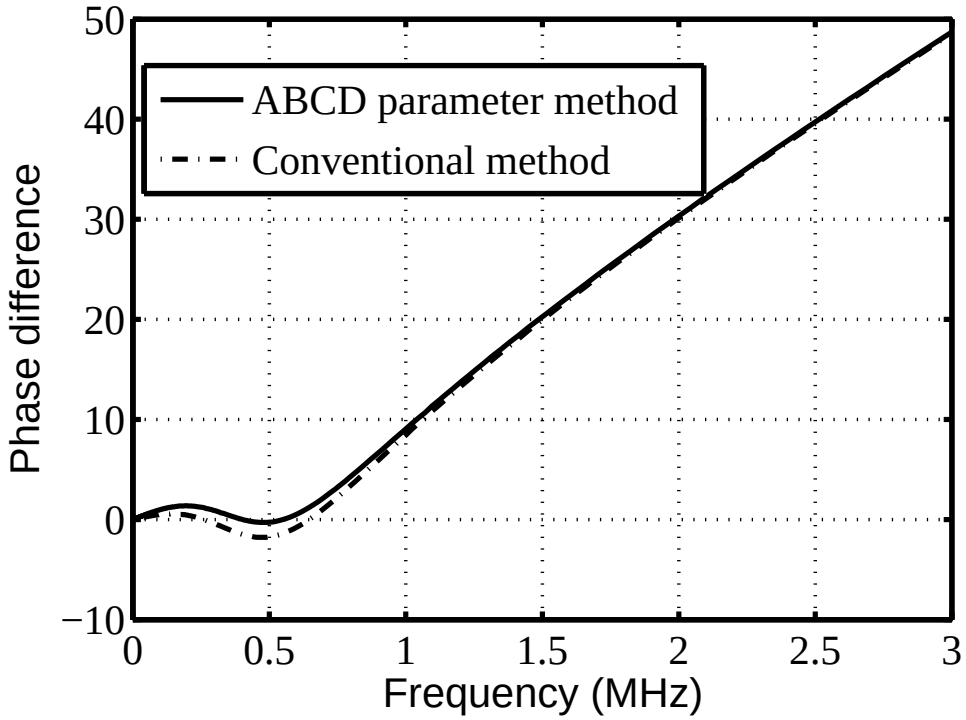


Figure 6.11: Deviation in phase of transistor level filter tuned with ABCD based model and state-space model from ideal.

proposed ABCD parameter model based approach is found to be effective and increase in error is found more for state-space approach compared to proposed approach. The maximum error is found to be 22 % for the proposed technique, while for that obtained using state-space approach, it is 33 %. This shows that the accurate model helps to minimize the deviation in the frequency response from the desired ideal response.

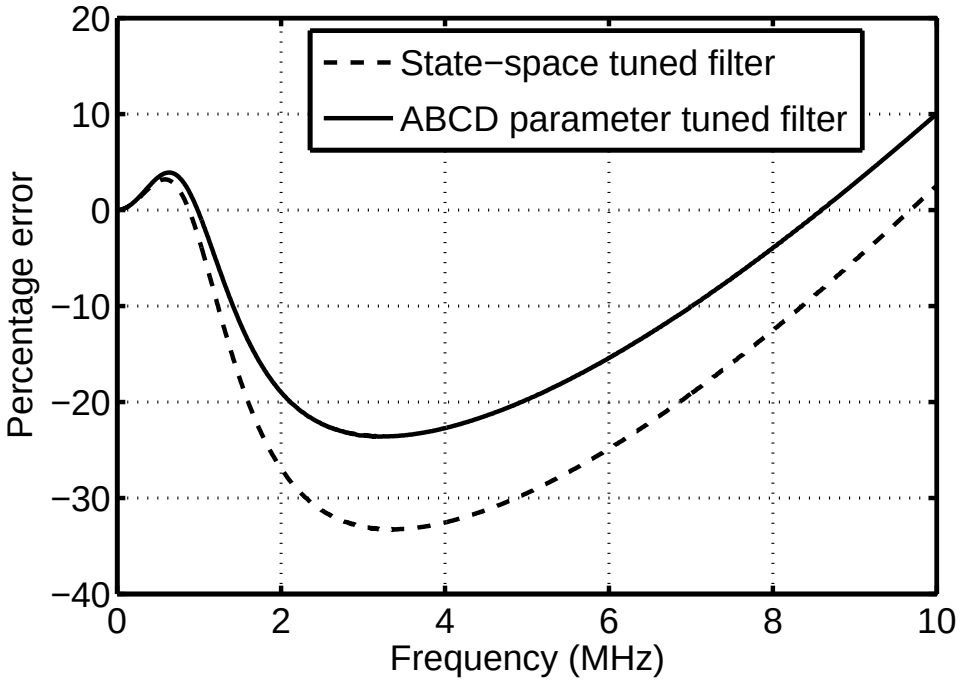


Figure 6.12: Percentage error with respect to ideal for transistor level filter tuned with ABCD parameter based model and conventional model for 1 MHz bandwidth.

CHAPTER 7

CONCLUSIONS AND FUTURE DIRECTIONS

7.1 CONCLUSIONS

The thesis addressed the issues in designing continuous-time G_m-C filters for 0.5 V operations. A fourth order filter was successfully fabricated on silicon using 0.18 μm n-well standard CMOS process. The designed filter offered 1 MHz bandwidth, the highest till date among the reported low voltage filters realized on silicon and operating on supply voltage less than 1 V. The lowest FOM (0.355 fJ) when compared to the similar works, indicated that the energy efficiency was not compromised in the process of achieving the necessary bandwidth. It was also shown that the bulk-driven transconductors can effectively be used for realizing the transconductors in the low voltage regime.

Two schemes were proposed for biasing the transconductors to keep the transconductance (gate-transconductance and/or bulk-transconductance) within limits across process, voltage and temperature variations. Simulation results showed that the proposed circuit is very effective in minimizing the variations in transconductance. With $\pm$10% change in supply voltage, the bulk-transconductance variations are less than $\pm$ 4.7% and $\pm$ 0.44% respectively for the two schemes at room temperature and five process corners. However, with the temperature, the bulk-variation is found to be slightly on the higher side but superior compared to the conventional circuit. The results shown are supported by a strong mathematical analysis. The analytical results are in good match with that of the simulated. It is concluded that the proposed fixed-bias circuits will serve the purpose well for low voltage analog circuits operating on supply voltage down to 0.5 V.

Design of a low-pass second order Butterworth filter with Cochlea architecture for operation on 0.5 V was also successfully demonstrated on schematic. Again, it was shown that a filter of 500 kHz bandwidth is realizable in 0.18 μm n-well standard CMOS process. Simulations showed that the designed filter has a dynamic range of 51 dB with power dissipation of 20 μW at 0.5 V supply voltage. The FOM of 0.225 fJ achieved by this filter is again stands as testimony for its energy efficiency.

A two-port transmission-line parameter based modeling technique was proposed for accurately modeling the filter which can be used for design centering the filters. It was shown through simulation results that proposed approach has a relatively good accuracy when compared to the conventional state-space approach. However, the two-port based approach are not suitable/applicable to all classes of filters especially where it is not possible to realize the filter as cascade of two-port networks.

7.2 FUTURE DIRECTIONS

The transconductance obtained from the bulk driven transconductor is very small compared to the gate driven transconductor. The input transistors in bulk driven technique can be made to operate in weak inversion or in sub-threshold operation by proper body bias/ gate bias. With this, the body transconductance can be made very small. Such technique can be used to explore the possibility of designing sub-hertz filters. Such filters find its application in the analog front end for detecting Seismic activities, structural health monitoring. Low power of such filters make them suited for deploying in wireless sensor networks.

Silicon cochlea find its applications in cochlea implants, hearing aids and front-ends of speech recognition systems. The cochlea filter designed in this work can be extended to realize the complete silicon cochlea. Low power nature of this filter make them best suited for such biomedical applications. Cochlea filters can be connected as a

bank having different bandwidths in the range of audio frequency in decreasing order of bandwidth. This can be achieved either by up scaling the capacitors or down scaling the transconductors. The filters along with the Q tuning can be used to realize low power silicon cochlea.

Since designing analog circuits for low voltage application is challenging, the scope of research for designing analog circuit is un-ending. Any analog circuit which can be thought of, is worthwhile to be tried for sub-1 V applications.

APPENDIX A

PIN DETAILS OF THE G_m-C LOW-PASS FILTER CHIP

Pin details of the packaged fourth-order G_m-C low-pass filter chip designed in this research is shown in Fig. A.1. The filter die is packaged in 44 pin JLCC package. The chip has a die size of 1.525×1.525 mm^2. The chip has three designs. Each design is chosen to have independent pins for power, input, output and ground pins. This enables testing of each design independently and without unwanted interference for the neighbouring designs on the chip. Only the design of interest is powered while the others are kept off.

The pin details of the chip along with its functions are given in Table A.1. The G_m-C filter has Eighteen dedicated pins. Each pin is named as per their functionality, followed by name of the designs to which those pin belongs so that they can be identified with their design. Pins corresponding the G_m-C filter have their name ending with '_VMH'. completeness,

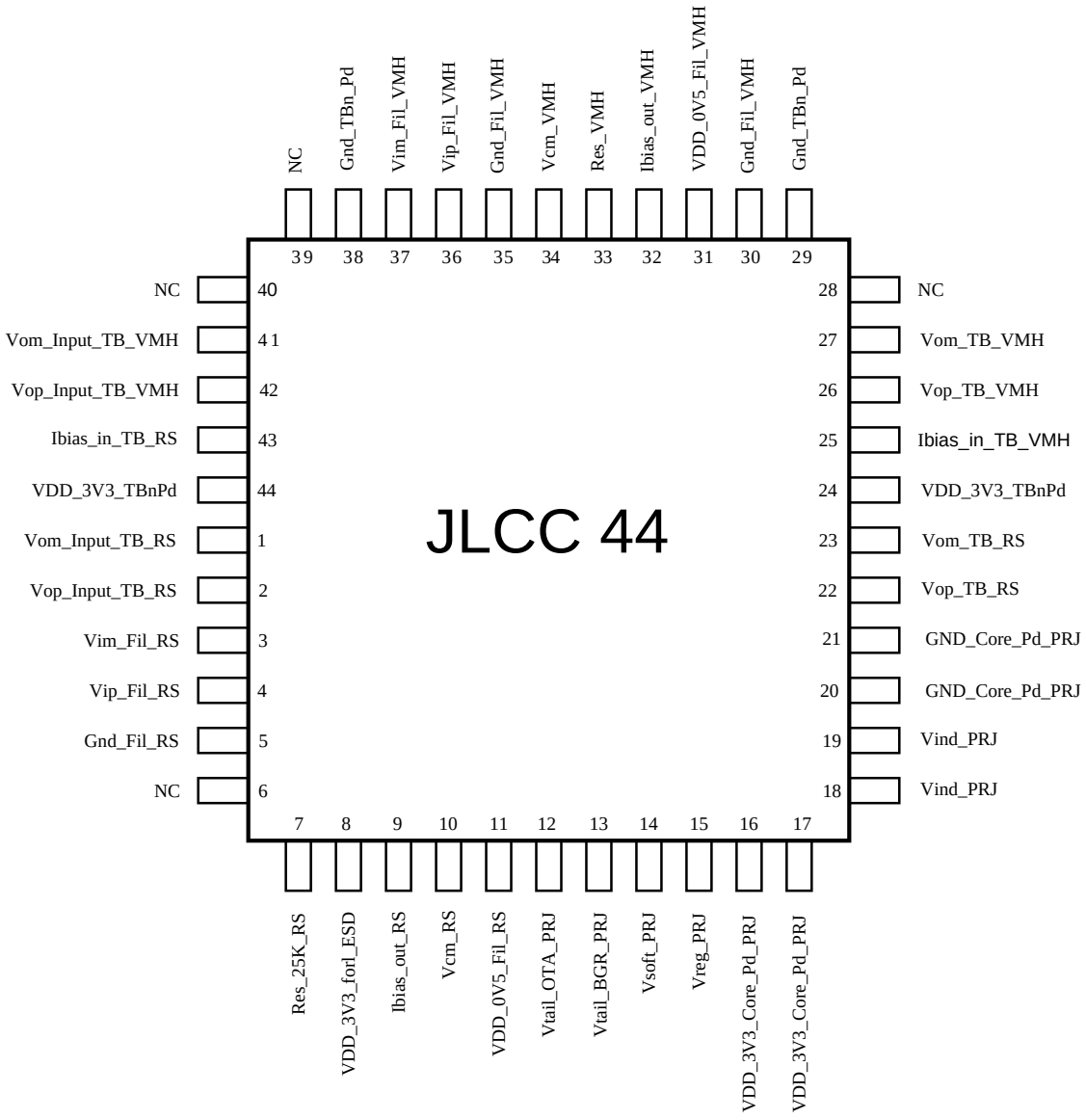


Figure A.1: Pin-out details of the packaged chip.

Table A.1: **Pin details of the packaged chip.**

Pin Number	**Pin name**	**Functionality**
8	VDD_3v3_for_ESD	3.3 V supply voltage for ESD Pad.
44,24	VDD_3v3_TBnPd	3.3 V supply voltage for Test buffer.
31	VDD_0v5_Fil_VMH	0.5 V supply voltage for Filter.
34	Vcm_VMH	0.25 V Common mode input voltage for Filter.
29, 38	GND_TBnPd	Top pack Ground.
30, 35	Gnd_Fil_VMH	Filter ground.
33	Res_VMH	An off-chip resistance connected to tune the bias current.
36 37	V_{ip} _Fil_VMH V_{im} _Fil_VMH	Filter differential input.
6, 28,39 and 40	NC	No Connection left open
26 27	V_{om} _TB_VMH V_{op} _TB_VMH	Filter path differential output.
40 41	V_{om} _Inputl_TB_VMH V_{op} _Inputl_TB_VMH	Direct path differential output.
25	I_{bias} _in_TB_VMH	Input bias current for the Test buffer.
32	I_{bias} _out_VMH	A test pin, where the transconductor bias current is brought out.
43	I_{bias} _in_TB_RS	Input bias current for the Test buffer.
5	Gnd_Fil_RS	RS Filter ground.
3 4	V_{im} _Fil_RS V_{ip} _Fil_RS	Filter path differential input for Filter.
1 2	V_{om} _Inputl_TB_RS V_{op} _Inputl_TB_RS	Direct path differential output.
23 22	V_{om} _TB_RS V_{op} _TB_RS	Filter path differential output.
7	RES_25K_RS	An off-chip resistance connected between this pin and ground for Filter.
10	Vcm_RS	Common mode input voltage for Filter (0.25 V).
9	I_{bias} _out_RS	A test pin.
11	VDD_0v5_Fil_RS	RS Filter 0.5 V power supply.
20, 21	GND_core_Pd_PRJ	PRJ circuit Ground.
16,17	VDD_3v3_Pd_PRJ	3.3V supply voltage for circuit.
12	Vtail_OTA_PRJ	Vtail for PRJ circuit.
13	Vtail_BGR_PRJ	Vtail for PRJ circuit.
14	Vsoft_PRJ	Vsoft for PRJ circuit.
15	Vreg_PRJ	Regulated output for PRJ circuit.
18,19	Vsoft_PRJ	Vsoft for PRJ circuit.

APPENDIX B

LM 334 BASED CURRENT SINK

An off-chip current sink for 100 μA required to generate the necessary bias for the test-buffers is designed using LM334 from National Semiconductors. It is a three terminal adjustable current source/sink. A current source/sink circuit using LM334 is shown in Fig. B.1.

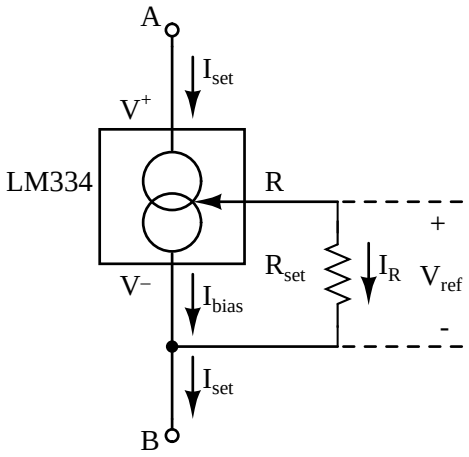


Figure B.1: LM 334 IC terminal details.

The three terminals of LM334 are named V^+, R and V^-. LM334 generates a constant voltage V_{ref} between R and V^- for a given temperature, which is approximately given by 214μV/° K. An external resistance R_{set} sets the current I_R between the terminals R and V^-. I_{bias} is the bias current required by the IC for its operation. Therefore the current I_{set} by the current source is given as

$$I_{set} = \frac{V_R}{R} + I_{bias} \tag{B.1}$$

The bias current I_{bias} depends on I_R. A typical ratio $\frac{I_{set}}{I_{bias}}$ is about 18 for 2 μA $< I_{set}$ $< 1\,mA$. Using this value, in B.1, the resistance R_{set} required to generate a given I_{set} at

room temperature (300^o K) can be simplified to

$$R_{set} = \frac{68\,mV}{I_{set}} = \frac{68\,mV}{100\,\mu A} = 680\,\Omega. \tag{B.2}$$

This resistance is connected between the the terminals R and V^-. This acts as current sink of magnitude $100\,\mu$A sinking a current from terminal A as shown in the Fig. B.1.

APPENDIX C

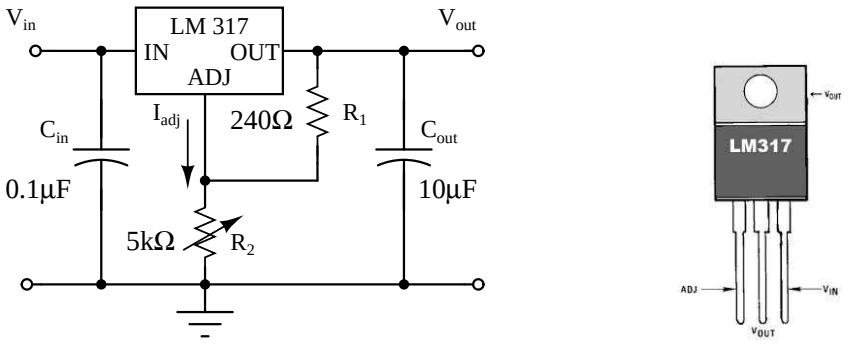
POWER SUPPLY DESIGN

The designed filter needs three individual dedicated power supplies for characterizing the filter chip.

1. 3.3 V : power supply for test buffer.
2. 0.5 V : power supply for the filter.
3. 0.25 V : input common mode voltage.

C.1 3.3 V POWER SUPPLY

3.3 V power supply is derived using an adjustable voltage regulator LM317 from National Semiconductors. The schematic of the voltage regulator circuit for generating 3.3 V is shown in Fig. C.1. The LM317 has a sourcing capacity of 1.5 A which is well in excess of the requirements of test-buffer.



(a) (b)

Figure C.1: (a) Circuit diagram of LM317 based voltage regulator. (b) Pin details of LM317.

The output voltage V_{out} of the regulator is given by

$$V_{out} = 1.25\left(1+\frac{R_2}{R_1}\right)+I_{adj}R_2 \tag{C.1}$$

Since I_{adj} is less than $100\,\mu$A, the second term in (C.1) can be made negligible by a proper choice of R_2. Ratio R_2/R_1 is chosen such that the output V_{out} is 3.3 V. C_{in} and C_{out} are the by-pass capacitors.

C.2 0.5 V POWER SUPPLY

Fig. C.2 shows the circuit designed to derive a regulated 0.5 V supply. The voltage regulator IC LM317 generates a regulated 1.25 V. This voltage is scaled down to 0.5 V using potential divider network. The potential divider is made adjustable by using a potentiometer. This allows the voltage adjustable by $\pm$10% around the nominal 0.5 V.

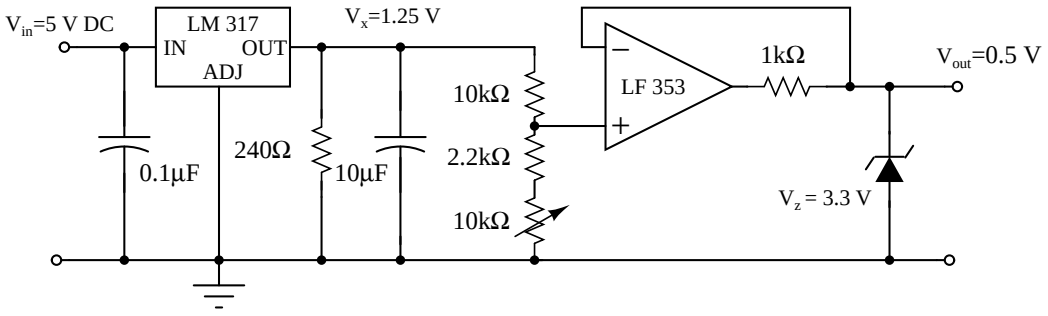


Figure C.2: Schematic of power supply circuit to generate 0.5 V.

The divided voltage is then buffered using an opamp based unity gain amplifier. A low noise opamp LF353 has for the buffer. A protection is provided at the output node, by connecting a 3.3 V zener diode across the output. This protects the chip against any accidental increase in the supply voltage beyond 3.3 V (and beyond 0.7 V in reverse). This is necessary since the buffer is operated on $\pm$6 V supply.

C.3 0.25 V POWER SUPPLY

The common mode reference voltage of 0.25 V is derived from the designed 0.5 V power supply. Fig. C.3 shows the circuit diagram. The circuit works similar to that of 0.5 V supply. It is to be noted that, input common mode reference will always be a function of filter supply. Or in other words, $V_{cm,ref} = V_{DD}/2$.

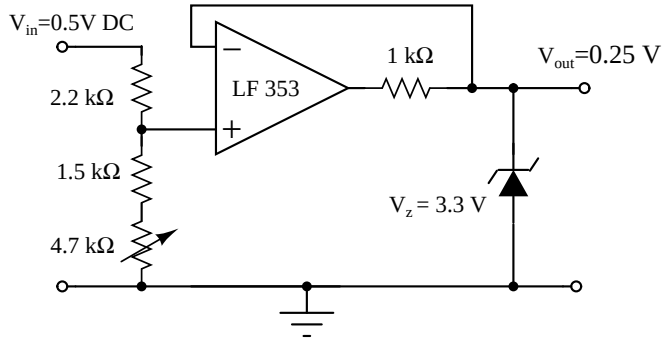


Figure C.3: Schematic of the circuit to generate 0.25 V.

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LIST OF PAPERS BASED ON THE THESIS

Journal Publications

1. **Vasantha M.H. and Tonse Laxminidhi**, "Two-Port Transmission Line Parameters Approach for Accurate Modeling and Design Centering of Integrated Continuous-Time Filters", *International Journal of Advanced Computer Research* (ISSN (print): 2249-7277, ISSN (online): 2277-7970) Volume-2, Number-4, Issue-6, pp:156-162 December 2012.
2. **Vasantha M.H. and Tonse Laxminidhi**,"Fixed Transconductance Bias Circuit for Low-Voltage Gate/Bulk Driven Transconductors", *International Journal of Circuits, Systems, and Computers, World Scientific publishing*, Communicated.

Conference Publications

1. **Vasantha M.H. and Tonse Laxminidhi**, "20 μW, 500 kHz Continuous-Time Low-Pass Filter in 0.18 μm CMOS Process",in proceedings of *Second International Engineering Symposium -IES 2012 (KU-MIT-NITK Joint Symposium)*, March 5–7, 2012, pp. E1-3-1–E1-3-6.
2. **Vasantha M.H. and Tonse Laxminidhi**, "A 0.5 V, 20 μW Pseudo-differential 500 kHz $G_m - C$ Low-Pass Filter in 0.18 μm CMOS Technology", in proceedings of *IEEE International Conference on Devices, Circuits and Systems (ICDCS–2012)*, March 15-16, 2012, pp. 76–79.
3. **Vasantha M.H. and Tonse Laxminidhi**, "0.5 V, 36 μW $G_m - C$ Butterworth Low Pass Filter in 0.18μm CMOS process", in proceedings of *The Fourth IEEE Asia Symposium on Quality Electronic Design (ASQED– 2012)*, July 11–12, 2012, pp. 82–85.
4. **Vasantha M.H. and Tonse Laxminidhi**, "0.5 V, Low Power, 1 MHz Low Pass Filter in 0.18 μm CMOS Process", in proceedings of *IEEE Third International Symposium on Electronic System Design*, Dec 18–21, 2012, pp.33–37.
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