INTEGRATED ACTIVE-RC CONTINUOUS TIME FILTERS FOR LOW VOLTAGE AND LOW POWER APPLICATIONS

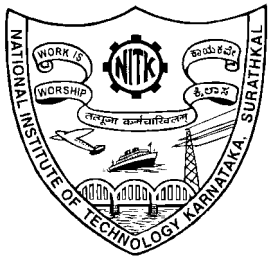
Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

REKHA S.



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November 2014

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **INTEGRATED ACTIVE-RC CONTINUOUS TIME FILTERS FOR LOW VOLTAGE AND LOW POWER APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Doctor of Philosophy*** is a ***bona fide report of the research work carried out by me***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to *certify* that the Research Thesis entitled **INTEGRATED ACTIVE-RC CONTINUOUS TIME FILTERS FOR LOW VOLTAGE AND LOW POWER APPLICATIONS**, submitted by **Rekha S.** (Register Number: EC08P01) as the record of the research work carried out by her, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of ***Doctor of Philosophy***.

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This thesis is
dedicated to
my dear **parents**

ACKNOWLEDGEMENTS

I would like to express my profound gratitude and deep regards to my research advisor Dr. Laxminidhi T. I thank him for the constant, exemplary guidance and support he has provided throughout the course of this research work. His immense knowledge about circuits and the passion for circuit simulation made me accomplish this. I owe my deepest gratitude to him, also for bringing this thesis in the present form. Words are not enough to express my indebtedness to him, for all the guidance, support and help.

I owe my heartfelt gratitude to Prof. Muralidhar Kulkarni, Head, Department of Electronics and Communication Engineering for the constant support, help and encouragement. I am indebted to him for his inspiring and kind words. I am thankful to Prof. Sumam David, Head of the department of E&C Engg. during my enrollment for Ph.D. program, for her support and help. My sincere thanks to Dr. G. S. Punekar, Prof. M. C. Narasimhan, RPAC members, for their invaluable suggestions during every step of my progress in the research work. I also would like to thank my co-researcher Mr. Vasantha M. for his help and support throughout the research work. I am deeply indebted to him for his help during the layout design, PCB design, testing the chip etc. I take this opportunity to thank Dr. Ramesh Kini for his help during my course work and also for helping me with cadence tools. I am grateful to Mr. Kiran kumar lad for helping me to install different softwares in my computer. My special thanks to my colleagues Dr. Aparna P. and Mrs. Kalpana Bhat for their constant moral support and help.

I would like to thank the Department of Information Technology, MCIT, Govt. of India, for the tool support provided to carry out this research work under SMDP-VLSI project.

I would like to thank Mr. Rathish and Mr. Ashok for helping in populating the printed circuit board and also for providing other help. I thank Mr. Sanjeeva poojary for making arrangements for in-time purchase of components for testing the fabricated chip. I am very grateful to Mr. Thilak for maintaining servers in VLSI lab and helping me to run the simulations smoothly. My special thanks to Mrs. Pushpalatha, Mrs. Prabha, Mrs. Sowmya, Mrs. Asha, Mrs. Jeevitha, Mr. Subrahmanya Karanth and Mr. Sheik Mohammad for extending their help whenever I needed their assistance. I also take this opportunity to thank all the faculty and staff of E&C department, NITK Surathkal. I also thank the staff in Academic, Admission and Cash sections of NITK for their assistance.

My heartfelt thanks to my husband Dr. M. S. Bhat for his support and help throughout this research work. Words are not enough to express my gratitude to my beloved

daughter Ms. Shraddha Chaitanya who has been a constant source of inspiration to me. Many times during this research work, roles of mother and daughter were interchanged and the mental support I got from her is invaluable. I am deeply indebted to her.

I recall with immense gratitude the unconditional love and support rendered by my parents and my sisters in my education and in my career throughout. It is my profound duty to thank the almighty for his grace without which I would not have been able to come all this way.

I would like to dedicate my thesis to my parents as a token of love and gratitude.

(Rekha S.)

ABSTRACT

This research proposes a couple of continuous-time analog filters with other accessories for low voltage and low power applications. The proposed designs are targeted to operate on a power supply voltage of 0.5 V. The research focuses on designing continuous-time filters using standard n-well devices in 180 nm CMOS process. Initial part of the thesis outlines the design of a fifth order continuous time active-RC low pass Chebyshev filter which has been used as the test-vehicle. A Bulk driven, pseudo-differential, feed-forward compensated Operational Transconductance Amplifier (OTA) has been proposed which is used as the building block of the filter. The filter, having a bandwidth of 477 kHz (3 Mrad/sec), along with all the necessary accessories such as common mode feedback (CMFB) circuit, bias generating circuits and test buffers is realized on silicon from United Microelectronics Corporation (UMC). The post-silicon results reveal that the filter offers a bandwidth of 750 kHz with a Dynamic range of 46.33 dB at 0.5 V supply. The filter on silicon is found to offer higher bandwidth than designed for. The thesis presents justification for this observed deviation. The filter has the highest bandwidth and also the highest energy efficiency when compared with filters of same category found in the literature. A Figure of Merit (FOM) of 0.2 fJ stands as testimony for the energy efficiency of the proposed filter.

The parasitics of OTA always put check on the maximum realizable filter bandwidth. The thesis presents a mathematical analysis of the effect of these parasitics on the filter response for a particular case of feed-forward compensated OTA. A first order active-RC filter has been taken for study. The maximum realizable bandwidth of the filter has

been quantified as a function of frequency beyond which the OTA parasitics dominate, order of the filter and the desired minimum attenuation. The mathematical analysis is found to match well with the results of transistor level filter.

The thesis also proposes four low power Common-mode Feedback (CMFB) circuits targeted for the pseudo-differential transconductor for operation on 0.5 V supply. All the proposed circuits offer high impedance (capacitive) with power consumption as low as 50 nW when used for a transconductor which consumes 10 μW. The absolute maximum deviation offered by these circuits over the nominal common-mode voltage of 0.25 V is found be 2.5% across process and temperature.

An ultra low power fifth order Chebyshev filter is presented in the last part of the thesis. A feed-forward OTA architecture is proposed which uses CMOS inverter as the basic transconductor. The fifth order filter is designed in 180 nm CMOS technology to validate the proposed OTA. Power consumption of this filter, offering a bandwidth of 150 kHz, is as low as 21.79 μW when operating on 0.5 V. The simulated filter offers a dynamic range of 54.15 dB. Further, this concept has been extended to realize a filter in 90 nm n-well CMOS process. The ideas are validated using a second order Butterworth biquad filter. It is found that the bandwidth can be as high as 5 MHz while offering a dynamic range of 55.78 dB and consuming a power of 58.76 μW when operating on 0.5 V power supply.

KEYWORDS: Low-power; Low-voltage; Feed-forward compensated OTA; Continuous-time filter; Design centering; OTA non-idealities; CMFB circuits; CMOS inverter based transconductor.

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ABBREVIATIONS

SoC	System on Chip
CMOS	Complementary Metal Oxide semiconductor
PMOS	P-channel Metal Oxide semiconductor
NMOS	N-channel Metal Oxide semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ITRS	International Technology Roadmap for Semiconductors
LOP	Low Operating Power
UMC	United Microelectronics Corporation
G_m-C	Transconductor - Capacitor
CMFB	Common mode feedback
OTA	Operational Transconductance Amplifier
FF-OTA	Feed-forward Operational Transconductance Amplifier
Op-amp	Operational Amplifier
PLL	Phase Locked Loop
THD	Total Harmonic Distortion
LTI	Linear Time Invariant
SA	Spectrum Analyser
VNA	Vector Network Analyser
VCO	Voltage Controlled Oscillator
Q	Quality Factor
VGA	Variable Gain Amplifier
DIP	Dual in-line Package
FOM	Figure of Merit

NOTATIONS

f	Frequency in Hz
ω	Angular frequency in radians per sec
g_m	Small signal transconductance of the MOSFET
g_{mb}	Small signal Bulk-transconductance of the MOSFET
C_{gg}	Intrinsic gate capacitance of the MOSFET
C_{bd}	Bulk-drain intrinsic capacitance of the MOSFET
C_{gd}	Gate-drain intrinsic capacitance of the MOSFET
C_{ox}	Gate oxide capacitance per unit area
L	Channel length of the MOSFET
W	Channel width of the MOSFET
V_{GS}	Gate-source voltage of the MOSFET
V_{DS}	Drain-source voltage of the MOSFET
V_{BS}	Bulk-source voltage of the MOSFET
k	Boltzmann Constant
T	Absolute temperature
q	Electronic charge
V_{TH}	Threshold voltage of the MOSFET
V_T	Volt equivalent of Temperature

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Over the past several decades, the phenomenal growth of semiconductor industry is driven by technology scaling. Scaling has resulted in improved chip performance, increased transistor density and reduced power consumption (Chang *et al.*, 2010). Although, reliability issues dictate the supply voltages to scale with device dimensions (Mead, 1994), aggressive supply voltage scaling for a given technology node is driven by the lower power consumption requirements. The supply voltage scaling is demanded by digital circuits since their dynamic power is proportional to square of the supply voltage. In a typical system-on-chip (SoC), analog and RF front end exist along with the digital circuit and integrated to consume power efficiently (Brock and Rajamani, 2003). As more and more applications find their way into portable battery operated systems, SoC designs have become very complex and lower power has become a mandatory requirement. Although scaling has resulted in improved performance in digital circuits, analog designs benefit only marginally, as minimum sized transistors suffer from noise and offset problems. It is a real challenge for analog designers to design efficient analog circuits to satisfy low power requirements without compromising on the dynamic range (Enz and Vittoz, 1996). In the present day technology, analog front-end is present in almost all SoCs that are used for processing real world signals (Iwai, 2009).

It is an observed trend that, with technology scaling, the threshold voltage (V_{TH}) of a MOSFET does not scale with the same proportion as the power supply voltage (Thompson *et al.*, 1998; Bohr, 2009). This is indeed due to a design decision where the primary reason is to keep the sub-threshold currents (Iwai, 2009) and noise margins

in check. Table 1.1 shows the V_{TH} values for different processes across three different vendors (Mosis, 2011). It can be seen that the threshold voltage does not scale with the same factor as technology.

Table 1.1: V_{TH} values for various process technologies

Vendor	**Feature size** (μ**m**)	V_{TH}	
		NMOS	**PMOS**
IBM	0.5	0.66	-0.47
	0.35	0.41	-0.37
	0.25	0.6	-0.44
	0.18	0.44	-0.43
	0.13	0.4	-0.43
	0.09	0.38	-0.43
	0.065	0.39	-0.43
ONSemiconductor	1.5	0.77	-0.91
TSMC	0.35	0.58	-0.79
	0.25	0.53	-0.52
	0.18	0.5	-0.49

At supply voltages below 1 V, it is challenging to design CMOS analog circuits using standard analog design techniques, as the transistors fail to operate in strong inversion. Both the NMOS and PMOS require at least V_{TH} in order to be biased in moderate inversion. To meet this requirement, a supply voltage of atleast 2 V_{TH} is needed (Blalock *et al.*, 1998). But low power requirements of today's designs call for aggressive power supply reduction mainly from the digital design perspective (Rajput and Jamuar, 2001; Shouli and Sanchez-Sinencio, 2000). In such cases, when analog circuits co-exist with the digital on a single die, many circuit techniques have been reported in the literature such as voltage boosting, floating gate approach (Hasler and Lande, 2001; Berg *et al.*, 2001; Rajput and Jamuar, 2001), using the bulk driven weakly inverted devices (Chatterjee *et al.*, 2005; Carrillo *et al.*, 2011; Lasanen *et al.*, 2000; Von Arnim *et al.*, 2005; Vlassis, 2012) etc. to address the issue of low voltage and relatively higher V_{TH}. Voltage boosting circuits are effective only for light/negligible load applications. They become complex as the load increases. In addition, this technique is prone to ripple and the resulting switching noise can have a serious effect on the performance of analog circuits which the voltage booster powers. Floating gate approach is an effective

method where the V_{TH} of the MOSFET is tuned using multiple gate inputs. However, this technique requires additional process steps and therefore is not economical. In the bulk driven technique, the signal is applied to the bulk-terminal of the transistor which modulates the current flow through the transistor whereas the biasing is done through gate of the device. With this approach, it is possible to have both positive and negative bias voltages $(\text{body-source voltage}\, V_{BS})$ for the devices thus offering tunability of V_{TH}. A forward bias of source body junction would reduce $|V_{TH}|$ of the transistor. This increases the achievable signal swing which would help to increase the dynamic range of the circuit. The concept of body biasing was found to be useful for low voltage digital circuits (Narendra *et al.*, 2004; Von Arnim *et al.*, 2005; Tschanz *et al.*, 2002; Chen *et al.*, 1996). In analog circuits, this concept was proposed by A. Guzinski and others (Guzinski *et al.*, 1987) in 1987. A bulk driven OTA was proposed in the paper. The research thereon led to many analog circuits such as transconductors, filters, phase locked loops (PLLs) etc. at sub-1 V power supply for example (Chatterjee *et al.*, 2005) is a break-through in realizing continuous time filters for 0.5 V operations.

One of the important modules in any analog front-end is continuous time filter used for antialiasing, noise filtering etc. Basic building block of the analog filter is an integrator. There are two basic approaches followed, in integrated circuits, for realizing integrators namely Active-RC and Transconductor-Capacitor ($G_m - C$). Active-RC approach has a better linearity and dynamic range over $G_m - C$ filter counter-parts for a given power dissipation. Active-RC filters can be realized using Operational Amplifiers (op-amps) or Operational Transconductance Amplifiers (OTAs). OTAs are attractive when compared to op-amps as the latter demand a large power for their low resistance output stage (Wheatley and Wittlinger, 1969; Tsividis, 1994; Sanchez-Sinencio and Silva-Martinez, 2000). However, the OTAs can only be used with a careful design as outlined in (Tsividis, 1994). One of the demerits of active-RC filters is that it is slow when compared to $G_m - C$ filters. This is because the OTAs are operated in closed loop. The conventional Miller compensation used to stabilize the loop makes the system even slower owing to the charging/discharging time of the compensating capacitor. Increase

in speed can be achieved only at the expense of increased gain-bandwidth product of the OTA which in-turn demands increased power. The requirement of large gain-bandwidth product for the op-amp has been an impediment for pushing the bandwidth of the filter (realized using such OTAs) to its limits for a given power.

Another issue is that in order to get a good filter response, the DC gain of the OTA must be as high as possible (Nauta, 1992). To achieve this, transconductors are cascaded necessitating a compensation for stable operation when used in a closed loop. Use of conventional Miller compensation is found to degrade the gain-bandwidth product of the OTA. This limitation can be overcome by using a feed-forward frequency compensation technique (Harrison, 2002) which pushes the gain-bandwidth product of the OTA to a higher value (Harrison and Weste, 2002). This technique is found to be quite effective and efficient for realizing high frequency filters without trading off with the power (Thandri and Silva-Martinez, 2003; Laxminidhi *et al.*, 2009). The block schematic of a fully differential feed-forward compensated OTA is shown in Figure 1.1. g_{m1}, g_{m2} and g_{m3} are fully differential transconductors. The cascade connection of g_{m1} and g_{m2} forms the forward path responsible for the high DC gain and the parallel path formed by g_{m3} forms the feed-forward path which introduces a left half s-plane zero offering the necessary stability. A simplified single ended model of the feed-forward compen-

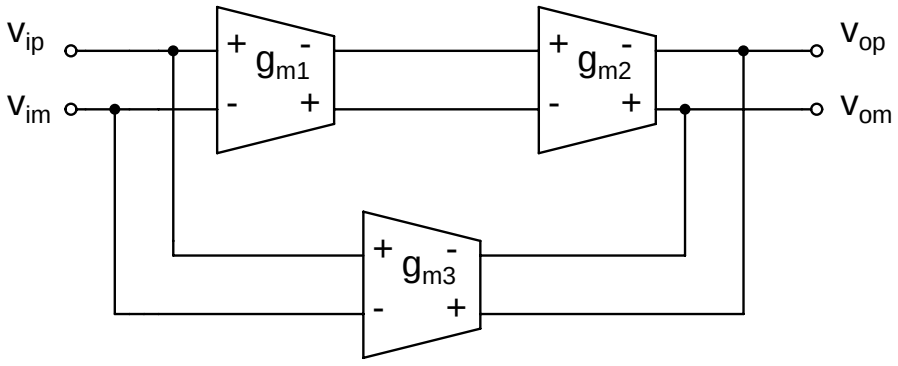


Figure 1.1: Schematic of a feed-forward compensated OTA

sated OTA is shown in Figure 1.2 where the non-idealities of the transconductors such as finite input/output resistance and the parasitic capacitance are grouped together into

r_1, r_2, c_1 and c_2. The corresponding transfer function can be written as given in (1.1).

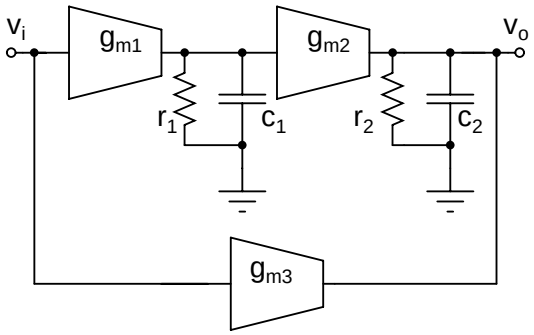


Figure 1.2: Single ended model of feed-forward compensated OTA

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}r_1r_2\left[1+\frac{s}{\omega_z}\right]}{\left[1+\frac{s}{\omega_{p1}}\right]\left[1+\frac{s}{\omega_{p2}}\right]} \tag{1.1}$$

where $\omega_{p1} = \frac{1}{r_1c_1}$, $\omega_{p2} = \frac{1}{r_2c_2}$, $\omega_z = \frac{\omega_{p1}g_{m1}g_{m2}r_1}{g_{m3}}$.

The feed-forward path thus introduces a left half s-plane zero at $s = -\omega_z$ which improves the phase margin of the OTA without compromising the bandwidth.

The International Technology Roadmap for Semiconductors (ITRS) in its 2012 update (2013 update is yet to be released) (ITRS, 2012) predicts that power supply voltage of relatively high performance applications such as mobile applications, laptop computers will be around 0.5 V in 2020. The main motive for this aggressive scaling of supply voltage is to reduce the dynamic power of digital logic circuits. Such low power logic category is termed as Low Operating Power (LOP) in ITRS documentation. A graph of supply voltage for LOP as predicted by ITRS is redrawn in Figure 1.3.

With such a scaling being predicted, it is necessary to come up with analog circuits to work on such low supply voltages for SoC applications. This has been one of the key motivations for this research. The main focus of the research is to design integrated continuous time filters along with some of the necessary accessories in standard CMOS (n-well) process operating on a power supply voltage of 0.5 V. In addition, the filters

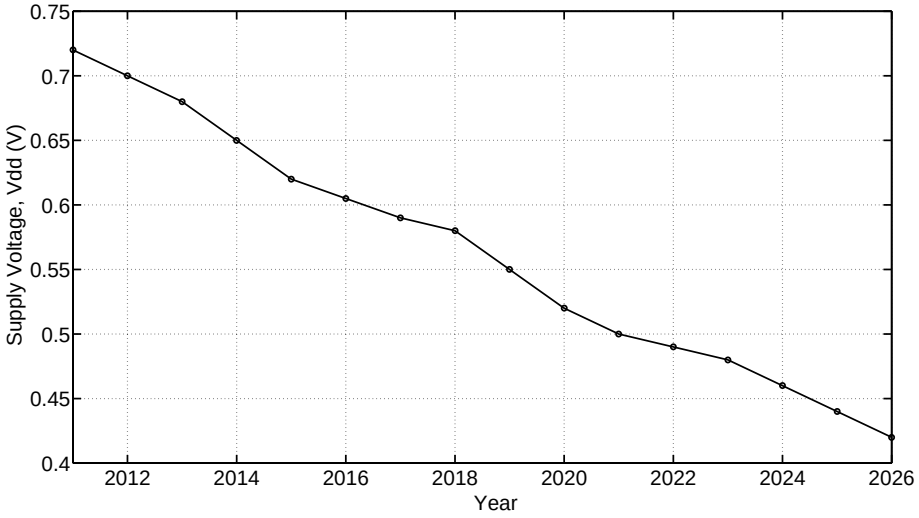


Figure 1.3: Scaling trend of supply voltage with year

are designed for low power operation. The filters proposed in this research find their applications as anti-aliasing and smoothing filters. Such filters with bandwidths ranging from a few kilohertz to a few megahertz find their applications in analog front-ends as well as baseband filters in wireless communication systems (Porret *et al.*, 2001).

One of the key contributions of this research is a low power energy efficient continuous-time active-RC filter in a 180 nm standard n-well CMOS process which is targeted to operate on supply voltage of 0.5 V. Since the process is standard n-well, the proposed design is economical too. It is to be noted that designing analog circuits in standard CMOS process is quite challenging for operation on 0.5 V when compared to designing circuits on twin-well or triple-well process. In twin-well/triple-well process, the designers have lots of liberty since they have independent control over each of the transistors. The main motive of this research is to obtain a fairly good performance from the filter designed in standard CMOS process. The OTAs are realized to have feed-forward compensation thereby eliminating the additional power required to charge/discharge the large Miller capacitance. A fifth order Chebyshev low pass filter is designed as a test-vehicle using 180 nm process from United Microelectronics Corporation (UMC). The filter bandwidth is chosen to be 477 kHz (3 Mrad/sec) with a pass-band ripple of 1 dB.

The designed filter is realized on silicon through Europractice.

Parasitic capacitances associated with the transistors and the layout directly affect the response of the filter. Therefore, to have a desired response, either the bandwidth of the filter must be sufficiently smaller than the frequency at which the reactance of the parasitic capacitances has significant influence on the response, or the parasitics have to be made sufficiently small so that they do not affect the filter response. The filter bandwidth is the specification where the designer does not have a choice. The parasitics, on the other hand, are in designer's hand. However, there is a limitation since there are other factors to which the designer is also required to pay attention. For example, in the case of low voltage circuits, the designer may be forced to use large sized transistors in order to obtain good matching between the transistors. In such a situation, designer will not be in a position to minimize the parasitic capacitances. The parasitic capacitances thus limit the maximum achievable bandwidth for a given transistor size. Thus a need is felt for analyzing the effect of parasitics (resistances and capacitances) of the OTA on the filter performance. In this research an attempt has been made in this direction. A mathematical analysis has been carried out for a first order active-RC low pass filter built using the feed-forward compensated OTA (FF-OTA). The results are then generalized for any filter of order-n built using such FF-OTAs. The analytical results are found to have a very good correlation with that obtained for transistor level filters through simulations.

Fully differential operation has become a de-facto choice for realizing analog circuits. It offers superior dynamic range and rejection of common-mode and power supply noise over its single-ended counterpart. These merits have motivated the designers to opt for differential operation. For a fully differential OTA used in filters, it is required to set the output common-mode DC of the filter to a reference. Often, the output common-mode is set equal to the input common-mode of the OTA. This is important, specially in active-RC filters, to avoid unnecessary direct currents that may result due to unequal common-mode voltages between the input and output nodes. A dedicated

common-mode feedback (CMFB) circuit is commonly used to set the output common-mode voltage to a reference value. Though there are a few number of common-mode feedback circuits available in literature, they are suited only for circuits having sufficient voltage headroom. Therefore, it is found that there is a need for effective and efficient common-mode feedback circuits for low voltage applications and the same has been addressed in this research. A total of four CMFB circuits are proposed in this thesis. The proposed circuits are power efficient and offer high input impedance. The circuits are designed and characterized on a 180 nm standard CMOS technology node from UMC and they are tested for a bulk driven pseudo differential transconductor.

In 1992, Bram Nauta proposed a CMOS inverter based architecture for realizing continuous time $G_m - C$ filters (Nauta, 1992). The simplicity of the architecture is the key feature in addition to reduced power when compared to the conventional source-coupled differential transconductor based filters. Though this idea is validated by Nauta on 3 μm CMOS process operating on 2.5-10 V supply, this architecture is a potential candidate for realizing low voltage filters. This fact has been exploited in a couple of designs (Vlassis, 2012; Arya *et al.*, 2013). It is felt that, if this concept is extended to realize the OTA, merits of active-RC filters can be exploited. In addition, all the designs available in the literature which work on 0.5 V use twin-well/triple-well process. In this research, an active-RC filter is proposed using CMOS inverter based OTAs for operation on 0.5 V supply. A fifth order Chebyshev low pass filter has been designed in 180 nm standard CMOS process. Also, a biquad filter has been designed in 90 nm standard CMOS process to see the performance gain of this method with technology scaling.

1.2 PRIOR WORK

The literature lists many continuous time filter designs, most of them use $G_m - C$ architectures. Inspite of having potential advantages such as lower power dissipation, good linearity, good dynamic range etc., active-RC filter designs are found to be taken

a back-seat. A summary of different architectures for OTA and filters can be found in (Geiger and Sanchez-Sinencio, 1985; Sanchez-Sinencio and Silva-Martinez, 2000). The first integrated continuous time $G_m - C$ filter reported in 1978 in (Moulding and Wilson, 1978) uses bipolar technology for color television receivers. Another $G_m - C$ filter based on bipolar technology was designed in 1982 by (Voorman *et al.*, 1982). Such filters found their applications in analog front end of Pulse Code Modulators and viewdata modems. Later, continuous time filters for read channel applications were reported in early 90s and they employ tunable bandwidth. (Khoury, 1991) reports the design of a $G_m - C$ filter with a tunable bandwidth of 6-15 MHz in a 5 V, 0.9 μm CMOS process. The filter offered a dynamic range of 55 dB and used a voltage controlled oscillator (VCO) based master-slave tuning circuit for bandwidth tuning. (De Veirman and Yamasaki, 1992) presents a 2-10 MHz tunable fifth order equiripple linear phase filter operating at 5 V supply. The design shows how a careful one time frequency trim and use of DC current through an external precise resistor can avoid master-slave tuning in filters with moderate Qualty factor (Q). The filter offered a dynamic range of 49 dB with a THD of less than 1 % at 2 V_{pp}. The work presented by (Alini *et al.*, 1992) was a second order low-pass filter in 2 μm BiCMOS technology. The cut-off frequency of the filter was tunable in the range 8-32 MHz and the Q was 2. This design used a fully differential BiCMOS transconductor using a MOS transistor. The filter had a dynamic range of 72 dB for -40 dB total harmonic distortion (THD) at a power supply voltage of 5 V.

(Nauta, 1992) reported a very high frequency low-pass $G_m - C$ filter tunable in the range 22-98 MHz in 3 μm CMOS process. This filter uses a CMOS inverter based transconductor circuit. This work also presents a circuit for automatically tuning the quality factors of integrated filters. (Gopinathan *et al.*, 1999) reported an approach to design a high speed low voltage programmable continuous time filters with an embedded variable- gain amplifier (VGA). The filter has a seventh order equiripple response with bandwidth tunable in the range 30-100 MHz in a 0.25 μm CMOS process and it uses a power supply voltage of 2.5 V. (Pavan *et al.*, 2000) presented a fourth or-

der Butterworth $G_m - C$ filter in 0.25 μm CMOS process with bandwidth tunability from 60-350 MHz. In this work, constant capacitance scaling is employed to allow the frequency scalability without affecting the noise performance and frequency response shape. This filter, operating at 3.3 V power supply, has a dynamic range of 54 dB. (Harrison and Weste, 2002) presented a fifth order elliptic opamp-RC filter in 0.18 μm CMOS process. The filter has a cut-off frequency of 350 MHz with a power supply of 1.8 V and achieves a 0.5 V_{pp} signal swing at -40 dB THD. They used feed-forward frequency compensation technique to achieve high frequency filtering. The design is power efficient since it avoids the conventional Miller compensation. They also presented a 500 MHz opamp-RC filter in 0.18 μm CMOS process in (Harrison and Weste, 2003). It is seen in both these filters that the shape of the frequency response varies when the bandwidth of the filter is varied over its tuning range. (Pandey *et al.*, 2006) presented a fourth order linear phase OTA based low-pass filter. It has a cut-off frequency of 550 MHz and the design was fabricated in 0.35 μm CMOS process. Supply voltage used for this design was $\pm$1.65 V. The achieved dynamic range was only 40 dB for a THD of -40 dB.

(Zhang *et al.*, 2008) has presented a third order elliptic low-pass $G_m - C$ filter using a bulk driven CMOS triode based fully balanced OTA in 0.18 μm CMOS process. The filter operates on 1.8 V supply voltage and exhibits a dynamic range of 45 dB. The filter presented by (Carrillo *et al.*, 2008) also uses a $G_m - C$ architecture and has a biquadratic response with a cut-off frequency of 17.5 kHz. It is a power efficient design with a power dissipation of 45 μW. It reported that the filter exhibits a dynamic range of 63.7 dB for 1 % THD. The filter uses a bulk driven transconductor and operates with a power supply voltage of 1 V. (Carrillo *et al.*, 2010) also presented a second order low-pass $G_m - C$ filter having a cut-off frequency of 10 kHz with a power supply voltage of 1.5 V. In this work, the response of a bulk driven MOS input stage over the input common mode voltage range is experimentally evaluated. A scheme to automatically control the gate bias voltage of a bulk driven differential pair is proposed to optimize the design tradeoff between the effective input transconductance and the input current.

However, the design is not power efficient. The work presented by (Carrillo *et al.*, 2011) is suited to low voltage operation. They have presented a $G_m - C$ second order low-pass tunable filter with a cut-off frequency as high as 3 MHz with a power supply of 1.2 V. The OTA used to design the filter has bulk driven input stage with improved DC gain and bandwidth capability. This design was implemented in 0.35 μm CMOS technology and is reported to have a dynamic range of 70 dB. This work is also a power efficient design consuming a power of 382 μW.

Filters discussed above are some of the important contributions found in the literature. All the filters cited above use supply voltages in excess of 1 V. However, when filters for sub-1 V operation are considered, there are only a few designs that are reported in the literature. A $G_m - C$ filter with bulk driven inputs is presented in (Grech *et al.*, 2005) which is designed to operate on 0.9 V power supply in n-well CMOS process.

A significant break through in the filter design for 0.5 V supply voltage operation has been seen in 2005. A first filter for operation on 0.5 V supply is presented in (Chatterjee *et al.*, 2005). An Active-RC fifth order elliptic low-pass filter with a 135 kHz cut-off frequency is presented in this paper. The design is fabricated in 0.18 μm triple-well CMOS process for operation on 0.5 V. The realized filter uses gate-input OTAs. The filter consumes 1100 μW when operating on 0.5 V supply. The use of triple-well process enabled the control over transistor threshold voltage for both NMOS and PMOS transistors through body bias tuning. Such tuning along with additional circuits, used to achieve necessary performance, is found to increase the complexity of OTA.

A CMOS inverter based tunable transconductor has been presented in (Vlassis, 2012) for 0.5 V operation based on the work presented in (Nauta, 1992). The transconductor presented here uses triple-well devices to achieve the tunability but at the expense of cost. An extension of this work resulted in a filter and is presented in (Arya *et al.*, 2013). In this paper, a third order tunable $G_m - C$ filter operating at 0.5 V is presented. The filter cut-off frequency is made tunable using a tunable transconductor. The filter

is designed in a triple-well 0.13 μm CMOS process. The simulation results presented in the paper reveal that the filter exhibits a cut-off frequency of 970 kHz and a dynamic range of 63.13 dB. In (Trakimas and Sonkusale, 2009), a butterworth low pass filter was designed for 10 kHz bandwidth with a power supply of 0.5 V in 180 nm technology. However, the paper does not reveal the filter design rather explains only the design of OTA.

It is inferred from the above literature survey that any further improvement in filter design for low voltage operation either in terms of bandwidth or power or dynamic range or the energy efficiency can be a significant contribution to the field of analog circuits. This research is an outcome of the effort in this direction.

1.3 THESIS ORGANIZATION

This thesis presents the design of analog filters with their accessories for low voltage applications and targeted to operate on a power supply voltage down to 0.5 V. The rest of the thesis is organized as follows.

Chapter 2 explains the design and layout of the fifth order low pass active-RC Chebyshev ladder filter that has been designed to validate the FF-OTA designed for low voltage operation. Transistor level realization of each block of the filter and the necessary accessories are explained in detail. The chapter also explains the procedure followed for design centering the filter in presence of parasitics. A detailed mathematical model of the filter is also presented which has been derived for design centering the filter.

Chapter 3 presents the results of the filter that has been realized on silicon. It also explains the design of test buffers and the test set-up used to characterize the test-chip. The results of the chip are also compared with the relevant filters found in the literature.

Chapter 4 is dedicated for the analysis of the effect of OTA parasitics on the filter response. This chapter gives a detailed mathematical analysis of the effects of FF-

OTA parasitics on active-RC filters and outlines a method to evaluate the achievable bandwidth for a given filter order when using FF-OTA.

In chapter 5, common mode feedback (CMFB) circuits for low voltage pseudo differential transconductor are proposed. A comparison of the performance of the proposed circuits is also presented in this chapter.

In chapter 6, a CMOS inverter based FF-OTA has been presented. The FF-OTA is used to design a continuous time filter. The simulated performance of the filter is presented and compared with the similar filters found in the literature. A mathematical analysis has been presented in support of the use of n-well devices for CMOS inverters when they are operating in sub-threshold region. The performance of the FF-OTA is evaluated for two technology nodes viz. 180 nm and 90 nm.

Chapter 7 gives conclusions and suggestions for future work.

CHAPTER 2

DESIGN AND IMPLEMENTATION OF A FIFTH ORDER ACTIVE-RC FILTER

To validate the idea of the design of continuous time filters for low voltage and low power applications, a fifth order active-RC Chebyshev filter is designed in 180 nm CMOS process. Keeping in mind the cost implications, it is chosen to propose the designs in standard CMOS process. The filter bandwidth is chosen to be 477 kHz (3 Mrad/sec) with a pass-band ripple of 1 dB. The filter has a fully differential architecture because of its inherent advantages over single ended counterpart.

The basic building block of any continuous time filter is the integrator. For active-RC realization of an integrator, OTA has become the de-facto choice for the analog designers due to its power efficient nature when compared to Op-amp. The large compensating capacitor (Miller capacitor) demanded by the OTA in feedback always found to limit the bandwidth of the OTA and hence the filter. Feed-forward compensation technique has emerged as an alternative since it offers compensation without trading the bandwidth. The OTAs proposed in this work, therefore, are also designed to have feed-forward compensation.

This chapter discusses the design of bulk-driven OTAs for 0.5 V supply operation. The OTAs are then used to realize the filter. The so designed filter is realized on silicon. This chapter details the complete filter design along with required accessories. The specifications of the filter are summarized below.

- Filter response type : Chebyshev
- Filter order (n) : 5
- 3-dB bandwidth (f_o) : 477 kHz

- Realization : Ladder
- Architecture : Active-RC
- Supply voltage (V_{DD}) : 0.5 V
- Technology : 180 nm standard CMOS process from UMC

2.1 BULK DRIVEN TRANSCONDUCTOR

Feed-forward compensated OTA is realized using transconductors as shown in Figure 1.1 in chapter 1. It is a common practice to use source coupled differential pair to realize transconductors. But due to the limitations on overhead when operating with low supply voltages, often designers are forced to use pseudo differential architecture (Rezzi *et al.*, 1995). And, so is the case in this work. The transconductors use bulk input transistors.

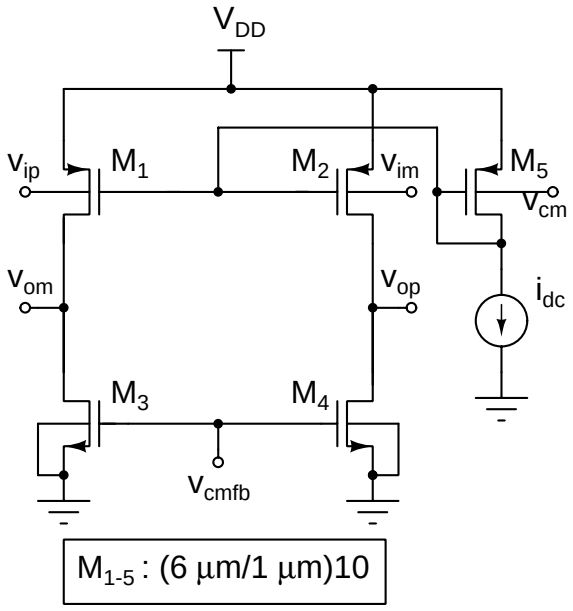


Figure 2.1: Pseudo differential bulk-driven transconductor

Figure 2.1 shows the schematic of the pseudo differential transconductor designed in this research. In the figure, v_{ip} and v_{im} are the differential inputs and, v_{op} and v_{om} are the differential outputs. M_1 and M_2 are the input transistors operating in saturation. M_3 and

M_4 are the NMOS loads and they operate in weak inversion. Gates of M_1 and M_2 are biased to carry a quiescent current of 10 μA using a diode connected PMOS transistor (M_5). Gates of M_3 and M_4 are biased with a common mode feedback voltage which sets the output common mode voltage. A detailed analysis of the designed common mode feedback circuit is given section 5.1.2 of chapter 5. The input and output common mode voltages of the transconductor are fixed at 0.25 V. The drain current of NMOS transistor operating in sub-threshold region is given in 2.1 (Taur and Ning, 1998).

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) V_T^2 e^{(V_{GS}-V_{TH})/(mV_T)} (1 - e^{-V_{DS}/V_T}) \tag{2.1}$$

where V_T is the volt equivalent of temperature and is about 26 mV at room temperature. In (2.1), the drain current can be assumed to be independent of V_{DS} if V_{DS} is higher by atleast 5 times that of V_T i.e. $(1 - e^{-V_{DS}/V_T}) \approx 1$. The drain-source voltage (V_{DS}) of M_3 and M_4 (in Figure 2.1) is at output common mode voltage ($V_{DS,3,4}$=250 mV). Hence the above assumption is valid and the drain current can be assumed to be independent of V_{DS}. I_{DS} remains constant for a given V_{GS} and therefore, NMOS transistors M_3 and M_4 act as current source loads.

A careful look at the circuit reveals that the body-drain junction capacitance of input transistors appears between input and output terminals of the transconductor. A single ended small signal equivalent circuit of the transconductor can be drawn as shown in Figure 2.2. In the figure, g_{mb} is the transconductance of bulk driven transistor (M_1 or M_2). C_{in} and C_{out} are the effective capacitances (parasitic) at input and output and, R_{in} and R_{out} are the effective input and output resistances. C_{bd} is the effective body-drain junction capacitance (M_1 or M_2) between the input and the output.

The differential voltage gain of the transconductor can be written as,

$$\frac{V_{op} - V_{om}}{V_{ip} - V_{im}} = \frac{g_{mb} r_{out} \left[1 - \frac{C_{bd}}{g_{mb}} s\right]}{1 + r_{out}(C_{out} + C_{bd}) s} \tag{2.2}$$

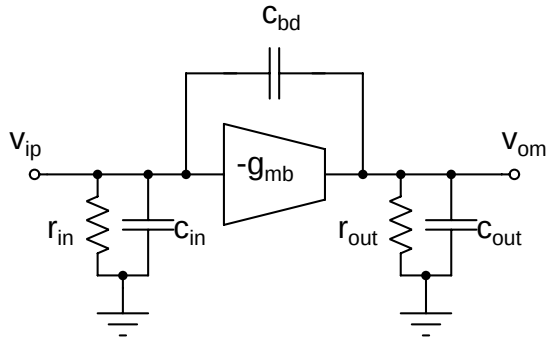


Figure 2.2: Single ended small signal model of the transconductor

It can be seen that there exists a right half *s*-plane zero at g_{mb}/C_{bd}. This zero adds excess phase lag to the transconductor and can pose instability to the OTA when in closed loop.

We propose a scheme to compensate for the effect of C_{bd}. Here, the differential nature of the circuit has been exploited to cancel/minimize the effect. The idea behind the circuit is the following. If a capacitance equal to C_{bd} is placed between v_{ip} and v_{op} in Figure 2.1 (similarly between v_{im} and v_{om}), the signal coupling from input to output and vice-versa get effectively canceled. This is possible since the signals that are coupling to a node are differential in nature. A simple modification for the transconductor which attempts to compensate for this effect is proposed in Figure 2.3. It uses two dummy transistors M_{1d} and M_{2d} which are connected between v_{ip} and v_{op} and, v_{im} and v_{om} respectively. These transistors are maintained in cut-off by using reverse bias across gate and source terminals. It is to be noted that the proposed scheme will only attempt to compensate for the capacitance but will not cancel the coupling effect altogether.

Frequency response of the transconductor is plotted in Figure 2.4 for both with and without the proposed compensation scheme. It is evident from the figure that the transconductor with compensation offers a first order response with a roll-off of -20 dB/dec. Without the compensation, the phase lag exceeds 90° and the magnitude response is pulled upwards beyond a frequency of around 130 MHz, thus clearly indicating the effect of right half *s*-plane zero. Designed transconductor provides a DC gain

of 19.5 dB, 3-dB bandwidth of 3.41 MHz, unity gain bandwidth (UGB) of 31.4 MHz. Bandwidth of the transconductor with compensation scheme is seen to degrade slightly when compared with that without compensation. This is expected since the dummy transistor adds some additional capacitance to the output capacitance.

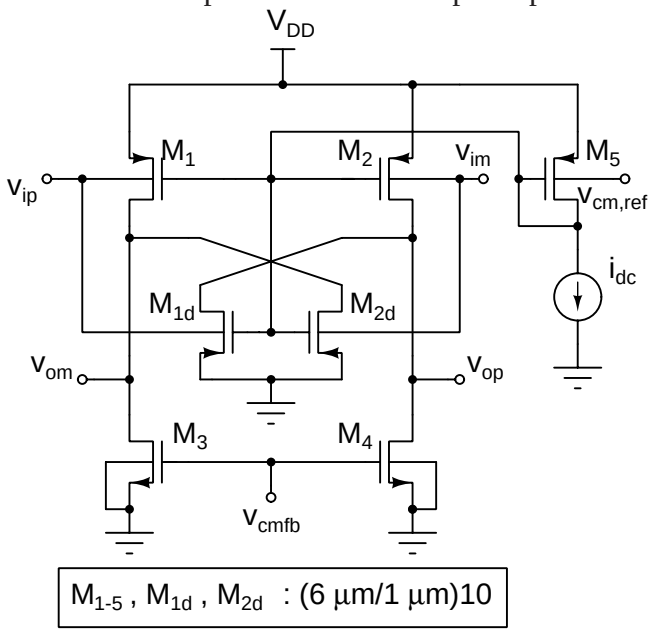


Figure 2.3: Proposed schematic of the transconductor to compensate for the effect of C_{bd} of input transistors.

2.2 FEED-FORWARD COMPENSATED OTA

The bulk driven transconductors are used to realize the OTA as shown in Figure 1.1. Note that, the transconductance g_m shown in the figure should be replaced by the bulk-transconductance g_{mb} since the transconductor action is due to the bulk-transconductance of input transistors. Three transconductors are used to realize the OTA; two in the forward path and one in the feed-forward path. The OTA requires only two CMFB circuits. Since the outputs of second stage transconductor and the feed-forward transconductor are common, only one CMFB circuit would suffice for these two transconductors.

Figure 2.5 shows the DC input-output characteristic of feed-forward OTA.

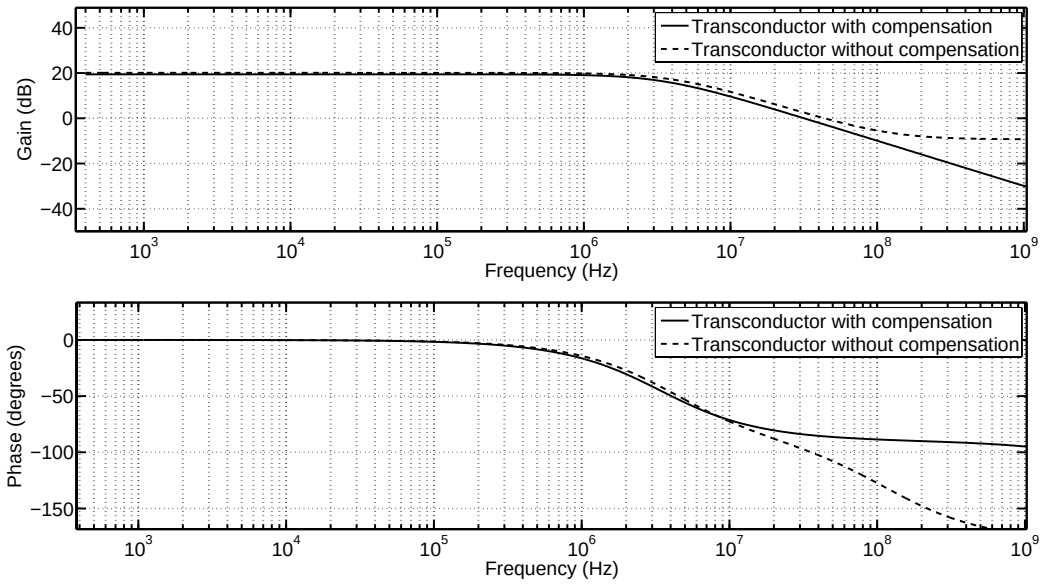


Figure 2.4: Frequency response of transconductor with and without the proposed scheme for compensating for the effect of C_{bd}.

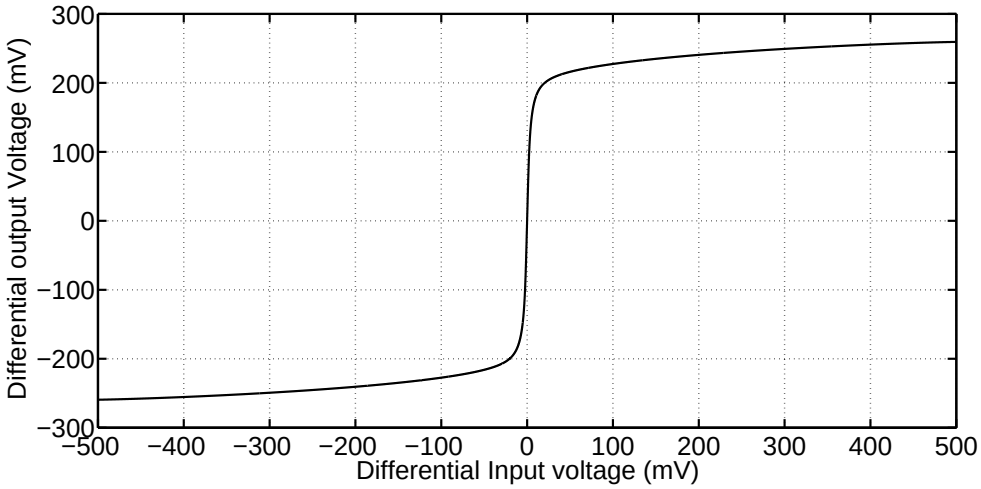


Figure 2.5: Input-output characteristic of feed-forward OTA

Frequency response of the OTA is plotted in Figure 2.6 for a capacitor load of 1 pF. The OTA has an open loop DC gain of 33.76 dB, 3-dB bandwidth of 670 kHz and UGB of 7.94 MHz. It has a phase margin of 49.3° and gain margin of 67.82 dB. If resistive loads are considered, the phase margin is sure to be improved owing to the increase in the damping. With no load on the OTA, the 3-dB bandwidth and UGB are found to be

1 MHz and 17.9 MHz respectively. The OTA is stable with a phase margin of 70.94° and a gain margin of 57.33 dB under no load condition. It is to be noted that, if it were a Miller compensation, for the same UGB of 17.9 MHz, the 3-dB bandwidth would have been only 367 kHz. Thanks to the feed-forward compensation.

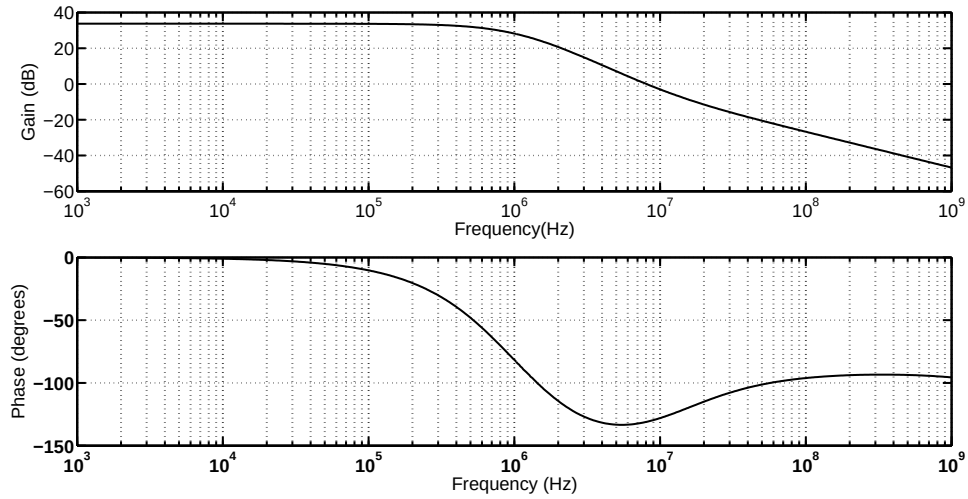


Figure 2.6: Frequency response of feed-forward OTA with 1 pF load

Table 2.1 lists the parameters of OTA. A comparison of performance parameters of the designed OTA with other low voltage OTAs found in literature is drawn in Table 2.2. It can be seen that, in terms of UGB, power and noise, the designed OTA performs better than those found in the literature. It is to be noted that, the gain-bandwidth product (GBW) of this OTA is 32.66 MHz. For OTAs with Miller compensation, GBW is approximately the same as UGB.

2.2.1 Small-signal model of the OTA

A single ended small signal equivalent circuit of the differential feed-forward OTA is shown in Figure 2.7. r_1, c_1 and r_2, c_2 represent the effective impedance seen with respect to small signal ground at the intermediate node in the forward path and the output respectively. The capacitor c_c represents the effective coupling capacitance appearing between the input and output terminals of the transconductor. Note that c_c takes into ac-

Table 2.1: Parameters of OTA

Parameter		**Simulated values of OTA**
Supply [V]		0.5
Open loop DC Gain [dB]		33.76
3 dB Bandwidth [kHz]	No load	1050
	1 pF capacitive load	669
UGB [MHz]	No load	17.9
	1 pF capacitive load	7.94
Phase margin[$^\circ$]	No load	70.94
	1 pF capacitive load	49.3
Gain margin [dB]	No load	57.33
	1 pF capacitive load	67.82
Power [μW]		45.33
Technology [μm]		0.18
Input referred noise [$nV/\sqrt{Hz}$]	@ 10kHz	135.96
	@ 1MHz	62.24

Table 2.2: Comparison with other low voltage OTA designs found in literature

Reference	**Supply [V]**	**DC Gain [dB]**	**UGB [MHz]**	**Power [μW]**	**Technology [μm]**	C_L **[pF]**	**Input referred noise @ 10 KHz** $\left[\frac{nV}{\sqrt{Hz}}\right]$	**Input referred noise @ 1 MHz** $\left[\frac{nV}{\sqrt{Hz}}\right]$
(Chatterjee *et al.*, 2005)	0.5	52	2.5	110	0.18	20	220	90
(Lasanen *et al.*, 2000)	1	70	0.2	5	0.35	7	260	–
(Blalock *et al.*, 1998)	1	49	1.3	300	2	22	181	43.6
(Lehmann and Cassia, 2001)	0.8	53	0.8	–	0.5	20	–	–
(Stockstad and Yoshizawa, 2002)	0.9	79	0.006	0.5	2.5	12	–	–
(Ferri and Sansen, 1996)	1.3	84	1.3	460	0.7	15	–	–
This work	**0.5**	**33.76**	**7.94**	**45.33**	**0.18**	**1**	**135.96**	**62.24**

count the capacitance which remains as residue after compensating for the body-drain junction capacitance of input transistors of the transconductor.

The voltage transfer function of the OTA can be written as in (2.3).

$$\frac{V_o}{V_i} = \frac{{g_{mb}}^2 r_1 r_2 \left[1 - \frac{sc_c}{g_{mb}}\right]\left[1 + \frac{(c_1 + c_c)s}{g_{mb}}\right]}{r_1 r_2 (c_1 c_2 + 2c_c c_1 + 2c_c c_2 + 3{c_c}^2)s^2 + (r_1 c_1 + r_2 c_2 + c_c r_1 + c_c r_2 + g_{mb} r_1 r_2 c_c)s + 1} \tag{2.3}$$

There are two zeros, one on the left half of s-plane $\left(\text{at } s = \frac{-g_{mb}}{c_1 + c_c}\right)$ and the other on the right half of s-plane $\left(\text{at } \frac{g_{mb}}{c_c}\right)$. The left half s-plane zero is introduced by the feed-forward transconductor thus providing stability to the OTA. Effect of the right half

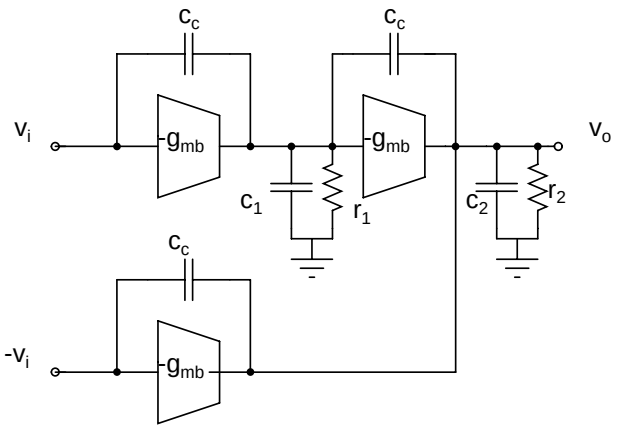


Figure 2.7: Single ended small signal model of feed-forward OTA

s-plane zero on the stability is made minimum by design.

Figure 2.8 compares the frequency responses of the transistor level OTA and of its model (Figure 2.7). The model derived here finds its use for design centering the filter which will be discussed in section 2.5.

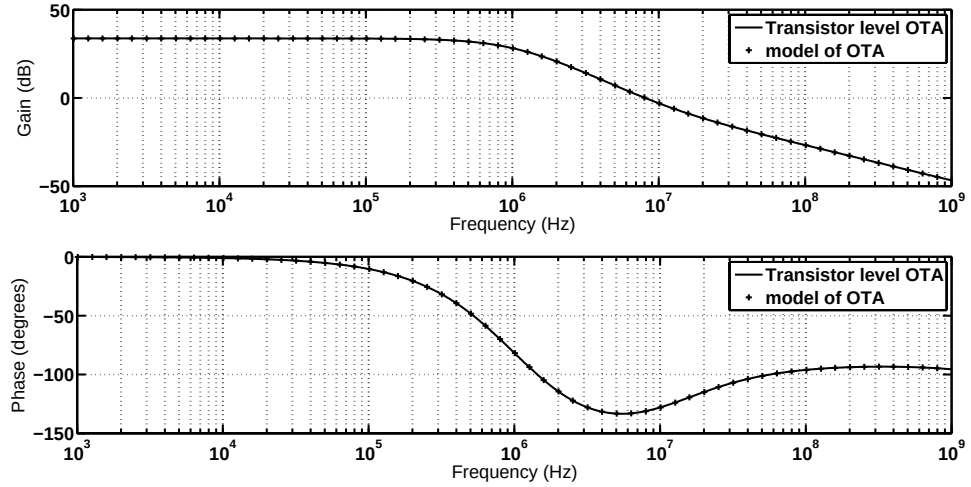


Figure 2.8: Frequency response of feed-forward OTA

2.3 FILTER REALIZATION

A fifth order Chebyshev low pass filter is designed using the feed-forward compensated OTAs. The filter is derived from the singly terminated LC ladder architecture whose prototype is shown in Figure 2.9 (Laxminidhi *et al.*, 2009). The element values shown are for 1 Ω terminating resistance and a band edge of 1 rad/sec.

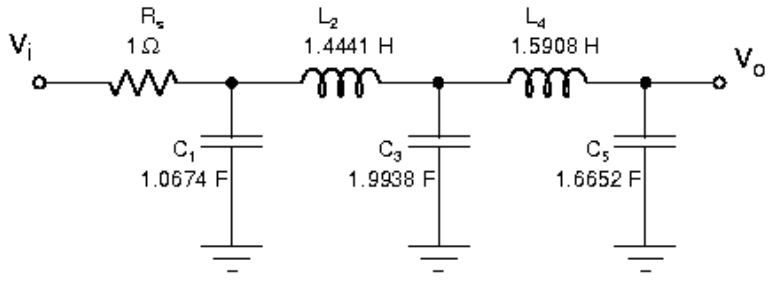


Figure 2.9: Prototype of LC ladder filter

An active-RC realization of the prototype LC ladder can be derived by first converting the LC ladder into a $G_m - C$ filter which in turn is achieved by emulating inductors using gyrator-capacitor architecture. The so obtaining $G_m - C$ filter is then converted into an equivalent active-RC filter. The active-RC ladder filter prototype is shown in Figure 2.10. In the figure, all resistors are of value 1 Ω. Capacitors C_1, C_3 and C_5 have same values as shown in Figure 2.9. The values of capacitors C_2 and C_4 are same as that of L_2 and L_4 in Figure 2.9 i.e. C_2 =1.4441 F and C_4 =1.5908 F. This active-RC prototype filter is then scaled to the desired terminating resistance and cut-off frequency.

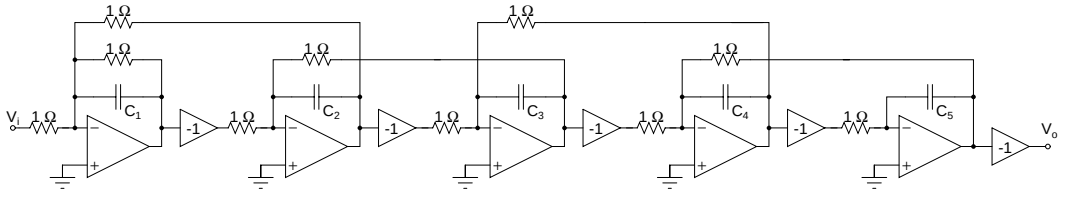


Figure 2.10: Singly terminated ladder filter

2.3.1 Frequency and Impedance scaling

The filter is chosen to have a band-edge of 3 Mrad/sec (477 kHz). The band-edge of the ladder filter is well below the 3-dB bandwidth of the OTA. The terminating resistance is chosen to be 100 kΩ. The terminating resistor is chosen such that after scaling, the desired capacitance values are less than 10 pF. To scale the filter for impedance and frequency, the following transformation is used for resistor and capacitor.

- Every resistor in Figure 2.10 is multiplied by a factor equal to R_{des} where R_{des} is the desired source impedance.
- Every capacitor in Figure 2.10 is multiplied by a factor $1/(R_{des}\omega_{des})$ where ω_{des} is the desired bandwidth.

For the filter in this work $R_{des} = 100\,\text{k}\Omega$ and $\omega_{des} = 3$ Mrad/sec. The values of resistors and capacitors after scaling are given below.

$$R = 100\,\text{k}\Omega; \quad C_1 = 3.558\text{ pF}; \quad C_2 = 4.814\text{ pF};$$
$$C_3 = 6.646\text{ pF}; \quad C_4 = 5.302\text{ pF}; \quad C_5 = 5.551\text{ pF}.$$

It is common among analog designers to opt for fully differential operation due to its inherent merits. Therefore, the filter realized in this thesis also chosen to have fully differential architecture. Figure 2.11 shows the fully differential filter. There are a couple of things to observe in the figure.

- Though all the integrating resistors in Figure 2.10 are assumed to have same values, in Figure 2.11 they are given separate names R_d, R_{12}, R_{23}, R_{34}, R_{45}, R_{21}, R_{32}, R_{43} and R_{54}. This is done only to ease the filter design centering which will be discussed in section 2.5.
- A resistor has been put in series with every integrating capacitor. These resistors, denoted as R_z, help to cancel/minimize the effect of right-half *s*-plane zero when OTA is used in place of opamps. A detailed analysis has been given in Appendix A.

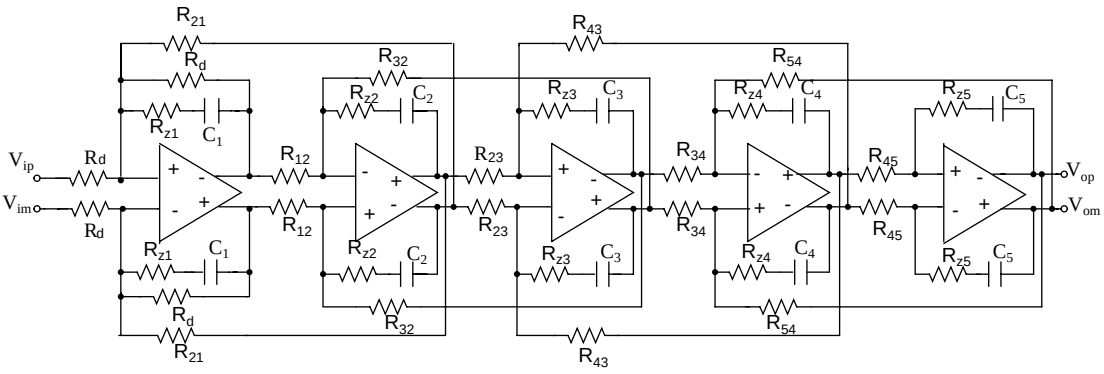


Figure 2.11: Schematic of the fully differential fifth order active-RC Chebyshev filter.

2.3.2 Node scaling

Node scaling maximizes the dynamic range of the filter. In the ladder filter, it is possible that the swing at intermediate integrating nodes is higher than that of the output node. In such a case, the linearity of the filter will be limited by the integrators connected to those nodes. Therefore to maximize the linearity, it is preferred not to allow any node to swing beyond the expected swing of the output. Or in other words the gains from input to each of the integrating nodes is not allowed to be more than the gain from input to the output node. Similarly, if the gain from input to any intermediate integrating node is very small, it implies that the next stage may have to offer a large gain. Then there is a risk of noise of the previous stage also getting amplified thus reducing the dynamic range. Therefore, all the intermediate integrating nodes are scaled to have a gain from the input close to that of the output but less than the output.

Node scaling is done by adjusting integrating capacitors and integrating resistors in such a way that total transfer function remains unaltered. The swing at a particular node can be reduced by decreasing the effective impedance at that node, i.e., by increasing the integrating capacitance at the node by a factor α. In order that this scaling does not affect the next stage, all the integrating resistors that are driven by this stage are reduced by the same factor α (this process ensures that the current supplied to the next integrator is independent of scaling).

When scaling, it is also important to ensure that matching between the resistors is not lost; because as seen in Figure 2.11 the resistors also feed the current back to the previous stage. It is extremely important that the resistors connected to the summing nodes are also matched in addition to differential resistors. Therefore, it is wise to use integer values for α. The integrating resistors are realized as combination of unit resistors R_{int} =100 kΩ.

The response of the node scaled filter is shown in Figure 2.12 where the gain at each integrating node is plotted. The capacitor and resistor values after the node scaling are given below.

$C_1 = 3.558$ pF; $C_2 = 9.628$ pF; $C_3 = 6.646$ pF;

$C_4 = 10.604$ pF; $C_5 = 5.551$ pF;

$R_d = R_{12} = R_{32} = R_{34} = R_{54} = R_{int}$

$R_{21} = R_{23} = R_{43} = R_{45} = R_{int}/2$ (two units of R_{int} in parallel)

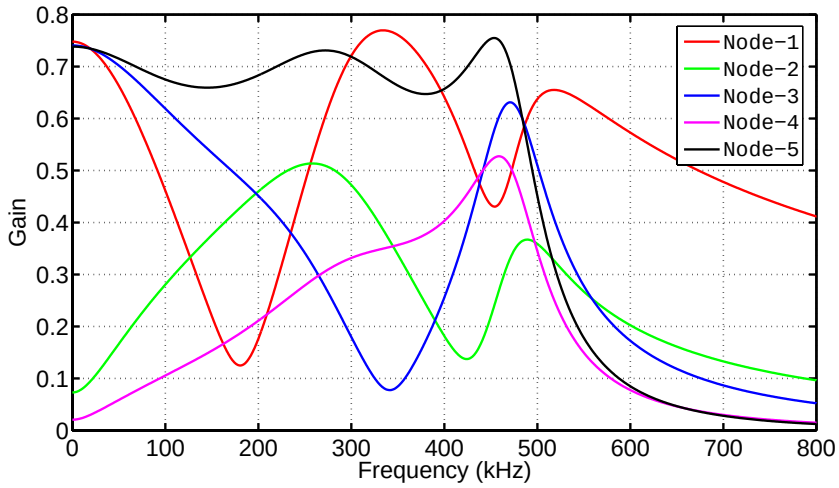


Figure 2.12: Response of the filter after node scaling (Node-*i* represents output of i^{th} OTA from left).

It is necessary to see that after node scaling any reduction in integrating capacitor will not load the OTAs. Therefore, the total bias current of the OTA output stage should be sufficient enough to drive the resistive loads for the highest signal swing expected

without the loss of linearity. Note that the transconductor is designed to have a bias current of 10 μA. Even with rail-to-rail swing at any node, the maximum current an OTA has to source/sink is found to be only 2.5 μA, thus ensuring sufficient margin for the transistor currents.

2.4 BIAS GENERATION AND DISTRIBUTION

The transconductors of the OTA are biased using a constant current source of 10 μA as shown in Figure 2.3. The constant current source is generated on chip by a constant current generating circuit and is distributed to all the transconductors. It is to be noted that, current distribution is preferred over voltage distribution for analog integrated circuits specially when the transconductors are located far away from the bias generating circuit.

The simple scheme to generate a constant current is shown in Figure 2.13. A negative feedback loop sets the current source to a constant value $I_{BIAS} = I_{ref} = V_{ref}/R_{ext}$ where, V_{ref} is a constant voltage and R_{ext} is a thermally stable off-chip resistor. This current is required to be distributed to all the transconductors using current mirrors.

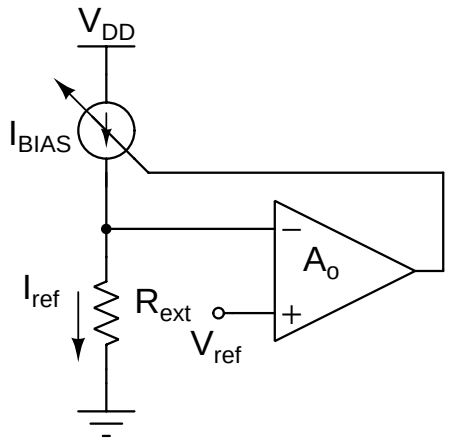


Figure 2.13: Constant current generator circuit.

With low supply voltages, the mirroring accuracy can be very poor which can result

in transconductor bias current to have a significant deviation from the desired I_{BIAS}. To mitigate this, an effective bias distribution scheme is used. The schematic of the circuit is shown in Figure 2.14.

The current source to be tuned in Figure 2.13 is realized using a transistor M_{f1}. The transistor M_{f1} is sized equal to that of input transistors $M_{1,2}$ of the transconductor. M_{f2} and M_5 are also sized equal. Similar to the simple current generating scheme, the negative feedback loop sets the current (I_{BIAS}) in M_{f1} equal to V_{ref}/R_{ext}. The error amplifier is realized using a simple pseudo-differential amplifier with a current-mirror load as shown in the inset of Figure 2.14. The bias distribution scheme mirrors the current generated in M_{f1} almost accurately to the transconductor (i.e. to the transistors $M_{1,2}$ of the transconductor). The current mirroring scheme, used here, acts in such a way that any error arising due to mismatch in mirroring is effectively canceled. This can be explained as follows. The feedback loop has a current mirror formed by M_{f1} and M_{f2}. Due to the V_{DS} mis-match, $I_{D,f2} \neq I_{D,f1}$. Let us say, $I_{D,f2} = I_x = I_{BIAS}/\alpha$. This current is then distributed through M_{f4}, M_{f5},... to all the transconductors. The whole arrangement is such that V_{DS} of M_{f3}, M_{f4}, M_{f5} ... are all made equal. For example, $V_{DS,f3} = V_{DS,f4}$ since M_{f2} and M_5 have equal size (or in other words equal current density). This arrangement forces the transistor M_5 to carry a current I_x ($= I_{BIAS}/\alpha$). In the transconductor, the current in M_5 is mirrored to $M_{1,2}$, but with an error. This error is equal and opposite to that between M_{f1} and M_{f2}. As a result, the current in $M_{1,2}$ will be exactly equal to that of M_{f1}, or in other words, $I_{D,1} = I_{D,2} = I_{BIAS}$.

In the present design, V_{ref} is fixed at V_{cm}, common mode reference voltage and the off-chip resistance of 25 kΩ is used for a constant current of 10 μA. The error amplifier has a DC gain of 35.55 dB and a bandwidth of 270 kHz.

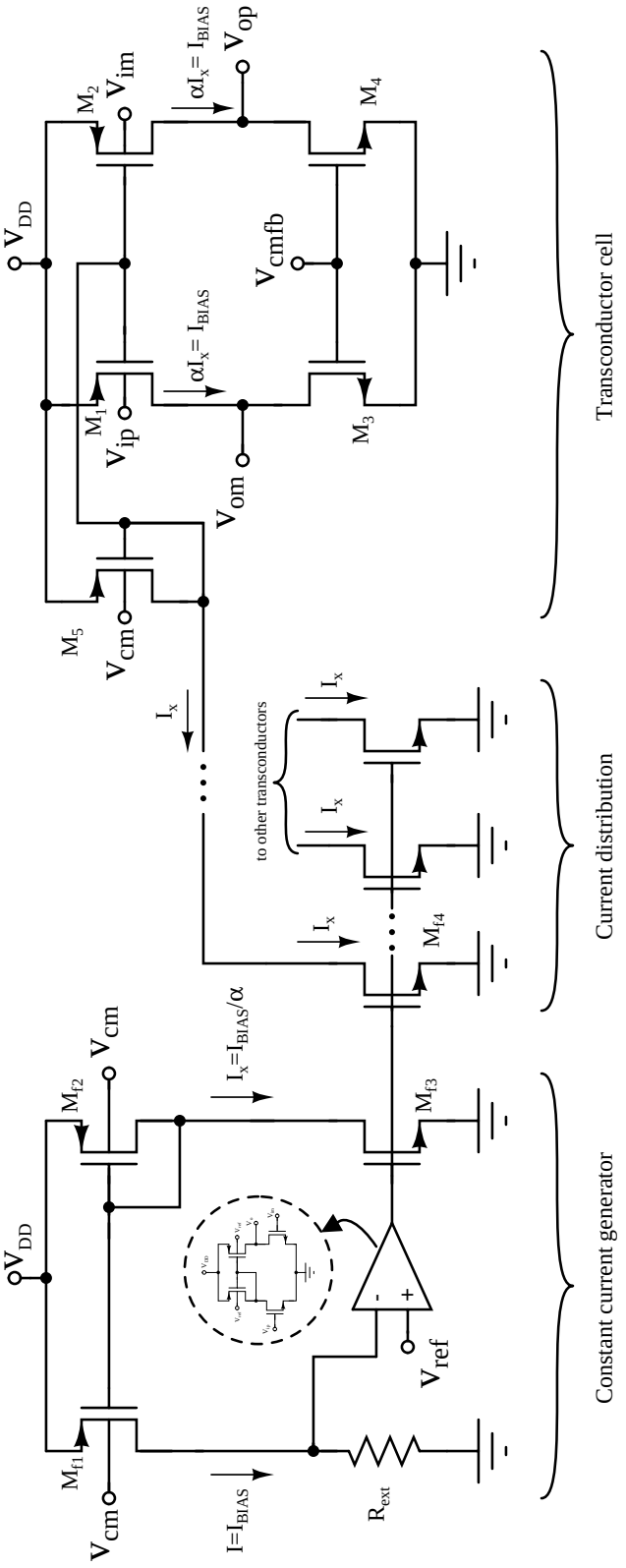


Figure 2.14: Constant current bias generator circuit with current distribution scheme.

2.5 DESIGN CENTERING THE FILTER

While designing the filter in the initial phase of the design, values of integrating capacitors and resistors are computed assuming that the OTA is ideal. But non-idealities of the OTA like parasitic capacitance, finite gain, finite bandwidth, finite output impedance, finite input impedance cause the frequency response to deviate from the ideal response. It is evident from the small signal model of the transconductor shown in Figure 2.2 that the transconductor offers parasitic capacitances and resistances both at its output and input. With these parasitics, filter performance will deviate from the nominal and steps should be taken to ensure that the variations in the response are within tolerable bounds. Since the filter transfer function is a function of every integrating capacitor and resistor used, the frequency response can be brought back to ideal by tuning these capacitors and resistors. This process is called the 'design centering'. The design centering procedure used for the filter in this work has been explained in this section.

Design centering the filter using cad tool is found to be time intensive (Laxminidhi and Pavan, 2007) since the optimization process involves computation of filter frequency response for every tweak in the optimizing parameters (resistors and capacitors). In (Laxminidhi and Pavan, 2007), a design centering technique for $G_m - C$ filters has been proposed based on the space mapping method. Here, the filter is optimized in a model space of the filter and the results are interpreted in actual filter space. This approach is proved to be time efficient. With some modification the same approach can also be employed to design center active-RC filters. Such a method has been followed for design centering the filter designed in this research.

The space mapping technique demands the filter to be modeled. Higher the accuracy of the model, fewer will be the number of design centering iterations. State space model is a good choice since the filter can be modeled easily and the MATLAB tool can be used effectively for optimizing the filter in model space. Hence the filter is modeled using state equations in this research. MATLAB built-in optimization routine,

fminsearch is used to minimize the error between the frequency response of state space model and that of the ideal by tuning the integrating capacitors and resistors. Optimized values of resistors and capacitors are then used in the transistor level filter. If the model is accurate, the optimized component values when put in actual filter would give a response close to ideal. This tuning is done once and not in real time. The design centering process ensures that the response at the nominal process corner with nominal supply and temperature is indeed near to ideal for a finite gain OTA with parasitics.

2.5.1 State Space model of the filter

State space model is a mathematical model of a physical system as a set of input, output and state variables related by first order differential equations. The most general state space representation of a Linear Time Invariant (LTI) system with p inputs, q outputs and n state variables is written in the following form:

$$\dot{x}(t) = \mathbf{A}x(t) + \mathbf{B}u(t) \tag{2.4}$$

$$y(t) = \mathbf{C}x(t) + \mathbf{D}u(t) \tag{2.5}$$

dim[**A**]= $n \times n$, dim[**B**]= $n \times p$, dim[**C**]= $q \times n$, dim[**D**]= $q \times p$, $\dot{x}(t) = \dfrac{dx(t)}{dt}$.
$\dot{x}(t)$ is called the 'state vector', $y(t)$ is called the 'output vector', $u(t)$ is called the 'input (or control) vector', $\mathbf{A}$ is the 'state matrix', $\mathbf{B}$ is the 'input matrix', $\mathbf{C}$ is the 'output matrix', $\mathbf{D}$ is the 'feed-through (or feed-forward) matrix'. If the circuit nodes are coupled capacitively, we need to use Descriptor state equations which are in the following form.

$$\mathbf{H}\dot{x}(t) = \mathbf{A_d}x(t) + \mathbf{B_d}u(t) \tag{2.6}$$

$$y(t) = \mathbf{C}x(t) + \mathbf{D}u(t) \tag{2.7}$$

where $\mathbf{A} = \mathbf{H^{-1}A_d}$ and $\mathbf{B} = \mathbf{H^{-1}B_d}$.

For the filter in this work, ideally there are only five state variables. However, the non-ideal OTA increases the number of state-variable to twenty. The locations of these

state variables are shown in Figure 2.15. Each OTA is associated with four state variables. Referring to the first OTA in figure, one state variable is due to the capacitor at the input terminal of OTA (v_1), one (v_2) at the intermediate node of the forward path of OTA, one (v_3) at the output terminal due to output capacitor and the last (v_4) at the junction between the C_1 and R_z. A small signal model of the first stage of OTA with integrating capacitor C_1 and R_{z1} is shown in Figure 2.16. The locations of four state variables ($v_1 - v_4$) associated with this OTA are highlighted by circling the voltages.

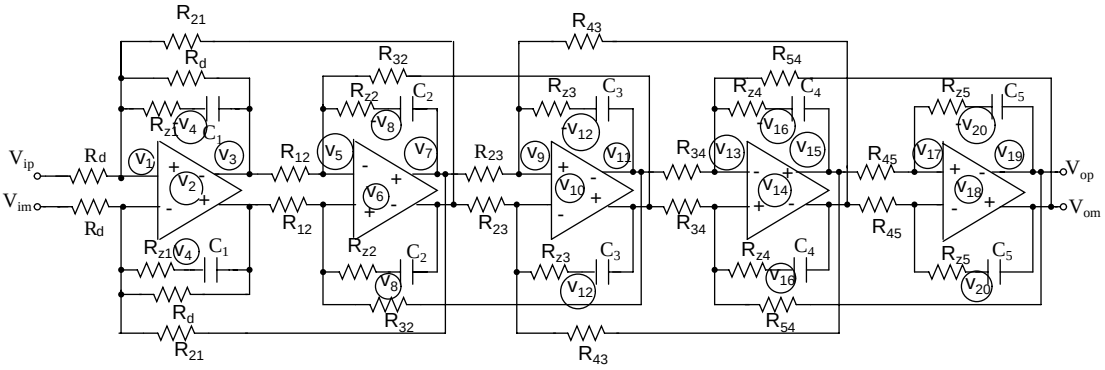


Figure 2.15: Schematic of the filter with state variables marked

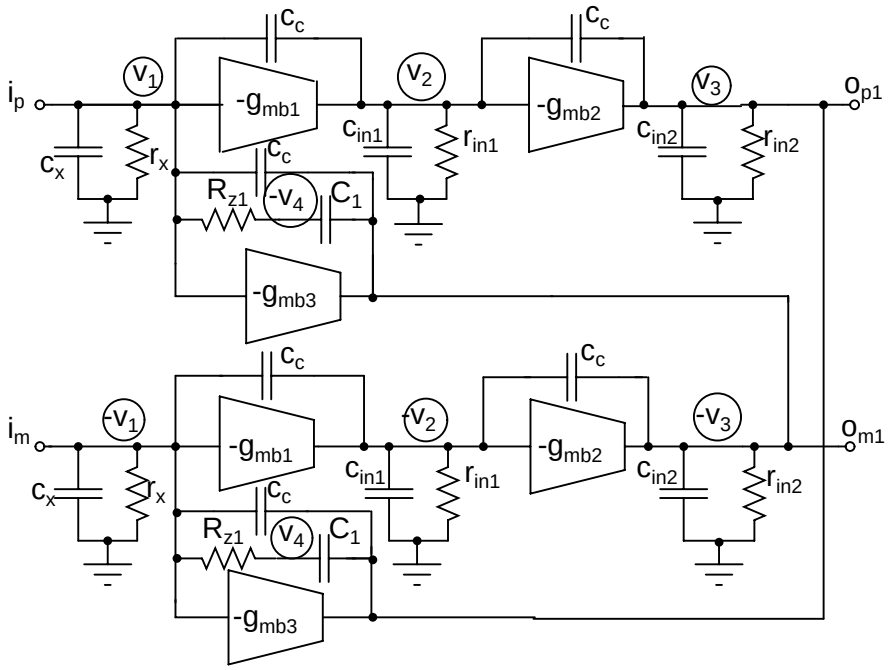


Figure 2.16: Model of the first stage of the 5th order filter

A, B, C, D matrices of the filter

The state space equations of the filter, given by equations (2.6) and (2.7) can be expanded as follows. The D matrix is a null matrix as there is no feed-forward path from input to the output.

$$\begin{bmatrix} \mathbf{H}_{11} & \mathbf{H}_{12} & \mathbf{H}_{13} & \mathbf{H}_{14} & \mathbf{H}_{15} \\ \mathbf{H}_{21} & \mathbf{H}_{22} & \mathbf{H}_{23} & \mathbf{H}_{24} & \mathbf{H}_{25} \\ \mathbf{H}_{31} & \mathbf{H}_{32} & \mathbf{H}_{33} & \mathbf{H}_{34} & \mathbf{H}_{35} \\ \mathbf{H}_{41} & \mathbf{H}_{42} & \mathbf{H}_{43} & \mathbf{H}_{44} & \mathbf{H}_{45} \\ \mathbf{H}_{51} & \mathbf{H}_{52} & \mathbf{H}_{53} & \mathbf{H}_{54} & \mathbf{H}_{55} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}_1} \\ \dot{\mathbf{x}_2} \\ \dot{\mathbf{x}_3} \\ \dot{\mathbf{x}_4} \\ \dot{\mathbf{x}_5} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_{d_{11}} & \mathbf{A}_{d_{12}} & \mathbf{A}_{d_{13}} & \mathbf{A}_{d_{14}} & \mathbf{A}_{d_{15}} \\ \mathbf{A}_{d_{21}} & \mathbf{A}_{d_{22}} & \mathbf{A}_{d_{23}} & \mathbf{A}_{d_{24}} & \mathbf{A}_{d_{25}} \\ \mathbf{A}_{d_{31}} & \mathbf{A}_{d_{32}} & \mathbf{A}_{d_{33}} & \mathbf{A}_{d_{34}} & \mathbf{A}_{d_{35}} \\ \mathbf{A}_{d_{41}} & \mathbf{A}_{d_{42}} & \mathbf{A}_{d_{43}} & \mathbf{A}_{d_{44}} & \mathbf{A}_{d_{45}} \\ \mathbf{A}_{d_{51}} & \mathbf{A}_{d_{52}} & \mathbf{A}_{d_{53}} & \mathbf{A}_{d_{54}} & \mathbf{A}_{d_{55}} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \mathbf{x}_3 \\ \mathbf{x}_4 \\ \mathbf{x}_5 \end{bmatrix} + \begin{bmatrix} \mathbf{B}_{d_1} \\ \mathbf{B}_{d_2} \\ \mathbf{B}_{d_3} \\ \mathbf{B}_{d_4} \\ \mathbf{B}_{d_5} \end{bmatrix} \mathbf{u} \tag{2.8}$$

$$\mathbf{y} = \begin{bmatrix} \mathbf{C}_{11}\mathbf{C}_{22}\mathbf{C}_{33}\mathbf{C}_{44}\mathbf{C}_{55} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \mathbf{x}_3 \\ \mathbf{x}_4 \\ \mathbf{x}_5 \end{bmatrix} \tag{2.9}$$

where,

$$\mathbf{x}_1 = [v_1\ v_2\ v_3\ v_4]^T \tag{2.10}$$

$$\mathbf{x}_2 = [v_5\ v_6\ v_7\ v_8]^T \tag{2.11}$$

$$\mathbf{x}_3 = [v_9\ v_{10}\ v_{11}\ v_{12}]^T \tag{2.12}$$

$$\mathbf{x}_4 = [v_{13}\ v_{14}\ v_{15}\ v_{16}]^T \tag{2.13}$$

$$\mathbf{x}_5 = [v_{17}\ v_{18}\ v_{19}\ v_{20}]^T \tag{2.14}$$

$$\mathbf{u} = [v_{ip}] \tag{2.15}$$

$$\mathbf{y} = [v_{19}] \tag{2.16}$$

The dimensions of the sub matrices are given below.

dim[$\mathbf{H}_{ij}$] = 4×4, dim[$\mathbf{A}_{d_{ij}}$] = 4×4, dim[$\mathbf{B}_{di}$]= 4×1, dim[$\mathbf{C}_{ii}$] = 1×4. The output node is v_{19}. Hence, $\mathbf{C}_{ii}$ = [**0**] for i = 1,2,3,4. $\mathbf{C}_{55}$= [0 0 1 0]

The descriptor state equations can be viewed as follows.

- **H**: Shows the capacitive (or inductive) coupling among the state variables.
- $\mathbf{A}_d$: Shows the resistive coupling among the state variables.
- $\mathbf{B}_d$: Shows the resistive coupling of the state variables with the input.

Most of the sub matrices given in equation (2.8) are null matrices.

- $\mathbf{H}_{ij}$ = $[\mathbf{0}]_{4\times4}$, $i \neq j$, if there is no capacitive coupling between states $\mathbf{x}_i$ and $\mathbf{x}_j$.
- $\mathbf{A}_{d_{ij}}$ = $[\mathbf{0}]_{4\times4}$, $i \neq j$, if there is no resistive coupling between states $\mathbf{x}_i$ and $\mathbf{x}_j$.
- $\mathbf{B}_{d_i}$ = $[\mathbf{0}]_{4\times1}$, if there is no resistive coupling between states $\mathbf{x}_i$ and input.

First row of equation (2.8) shows how the set of nodes represented by $\mathbf{x}_1$ are coupled to other nodes. The first integrator is coupled to the input and second integrator through resistors. Hence, the first row of equation (2.8) can be simplified as

$$\mathbf{H_{11}}\dot{\mathbf{x_1}} = \mathbf{A}_{d_{11}}\mathbf{x_1} + \mathbf{A}_{d_{12}}\mathbf{x}_2 + \mathbf{B}_{d_1}v_i \tag{2.17}$$

Note that, $\mathbf{A}_{d_{13}}$, $\mathbf{A}_{d_{14}}$ and $\mathbf{A}_{d_{15}}$ are null matrices since 3rd, 4th and 5th stages are not coupled to the first stage. Also, $\mathbf{B}_{d_2}$-$\mathbf{B}_{d_5}$ are null vectors since the input couples only to the first stage.

While writing the state space equations, the following convention is maintained.*The net capacitive current flowing out of a node is equal to the net resistive current coming into the node*. Referring to the filter shown in Figure 2.15 and the small signal model

shown in Figure 2.16, the state space matrices of first integrator can be written as follows.

$$\mathbf{H}_{11} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_1 & c_x + 2c_c & -c_c & c_c & 0 \\ v_2 & -c_c & c_{in1} + 2c_c & -c_c & 0 \\ v_3 & c_c & -c_c & c_{in2} + 2c_c + C_1 & -C_1 \\ v_4 & 0 & 0 & -C_1 & C_1 \end{array}\right) \tag{2.18}$$

$$\mathbf{A}_{d_{11}} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_1 & -\frac{1}{R_{21}} - \frac{2}{R_d} - \frac{1}{R_{z1}} - \frac{1}{r_x} & 0 & -\frac{1}{R_d} & -\frac{1}{R_{z1}} \\ v_2 & -g_{mb1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_3 & g_{mb3} - \frac{1}{R_d} & -g_{mb2} & -\frac{1}{r_{in2}} - \frac{1}{R_d} - \frac{1}{R_{12}} & 0 \\ v_4 & -\frac{1}{R_{z1}} & 0 & 0 & -\frac{1}{R_{z1}} \end{array}\right) \tag{2.19}$$

$$\mathbf{A}_{d_{12}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_1 & 0 & 0 & -\frac{1}{R_{21}} & 0 \\ v_2 & 0 & 0 & 0 & 0 \\ v_3 & \frac{1}{R_{12}} & 0 & 0 & 0 \\ v_4 & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.20}$$

$$\mathbf{B}_{d_1} = \left(\begin{array}{c|c} & v_i \\ \hline v_1 & \frac{1}{R_d} \\ v_2 & 0 \\ v_3 & 0 \\ v_4 & 0 \end{array}\right) \tag{2.21}$$

State space equation and the corresponding matrices for second integrator are as follows.

$$\mathbf{H_{22}}\dot{\mathbf{x_2}} = \mathbf{A}_{d_{21}}\mathbf{x}_1 + \mathbf{A}_{d_{22}}\mathbf{x}_2 + \mathbf{A}_{d_{23}}\mathbf{x}_3 \tag{2.22}$$

$$\mathbf{H_{22}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_5 & c_x + 2c_c & -c_c & c_c & 0 \\ v_6 & -c_c & c_{in1} + 2c_c & -c_c & 0 \\ v_7 & c_c & -c_c & c_{in2} + 2c_c + C_2 & -C_2 \\ v_8 & 0 & 0 & -C_2 & C_2 \end{array}\right) \tag{2.23}$$

$$\mathbf{A}_{d_{21}} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_5 & 0 & 0 & \frac{1}{R_{12}} & 0 \\ v_6 & 0 & 0 & 0 & 0 \\ v_7 & -\frac{1}{R_{21}} & 0 & 0 & 0 \\ v_8 & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.24}$$

$\mathbf{A}_{d_{22}}$ is similar to $\mathbf{A}_{d_{11}}$ except for the fact that there is no local feedback (R_d) for the second integrator.

$$\mathbf{A}_{d_{22}} = \left(\begin{array}{c|cccccccc} & \multicolumn{4}{c}{v_5} & \multicolumn{2}{c}{v_6} & \multicolumn{2}{c}{v_7} & v_8 \\ \hline v_5 & -\frac{1}{R_{12}} & -\frac{1}{R_{z2}} & -\frac{1}{r_x} & -\frac{1}{R_{32}} & \multicolumn{2}{c}{0} & \multicolumn{2}{c}{0} & -\frac{1}{R_{z2}} \\ v_6 & \multicolumn{4}{c}{-g_{mb1}} & \multicolumn{2}{c}{-\frac{1}{r_{in1}}} & \multicolumn{2}{c}{0} & 0 \\ v_7 & \multicolumn{4}{c}{g_{mb3}} & \multicolumn{2}{c}{-g_{mb2}} & -\frac{1}{r_{in2}} - \frac{1}{R_{21}} - \frac{1}{R_{23}} & & 0 \\ v_8 & \multicolumn{4}{c}{-\frac{1}{R_{z2}}} & \multicolumn{2}{c}{0} & \multicolumn{2}{c}{0} & -\frac{1}{R_{z2}} \end{array}\right) \tag{2.25}$$

$\mathbf{A}_{d_{23}}$ is similar to $\mathbf{A}_{d_{12}}$ and it can be obtained by replacing R_{12} and R_{21} with R_{23}

and R_{32} respectively.

$$\mathbf{A}_{d_{23}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_5 & 0 & 0 & -\dfrac{1}{R_{32}} & 0 \\ v_6 & 0 & 0 & 0 & 0 \\ v_7 & \dfrac{1}{R_{23}} & 0 & 0 & 0 \\ v_8 & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.26}$$

For the third integrator, the state space equation can be written as follows.

$$\mathbf{H_{33}}\dot{\mathbf{x_3}} = \mathbf{A}_{d_{32}}\mathbf{x}_2 + \mathbf{A}_{d_{33}}\mathbf{x}_3 + \mathbf{A}_{d_{34}}\mathbf{x}_4 \tag{2.27}$$

$$\mathbf{H_{33}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_9 & c_x + 2c_c & -c_c & c_c & 0 \\ v_{10} & -c_c & c_{in1} + 2c_c & -c_c & 0 \\ v_{11} & c_c & -c_c & c_{in2} + 2c_c + C_3 & -C_3 \\ v_{12} & 0 & 0 & -C_3 & C_3 \end{array}\right) \tag{2.28}$$

$$\mathbf{A}_{d_{32}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_9 & 0 & 0 & \dfrac{1}{R_{23}} & 0 \\ v_{10} & 0 & 0 & 0 & 0 \\ v_{11} & -\dfrac{1}{R_{32}} & 0 & 0 & 0 \\ v_{12} & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.29}$$

$\mathbf{A}_{d_{33}}$ is similar to $\mathbf{A}_{d_{22}}$ and it can be obtained by replacing R_{12}, R_{32}, R_{21}, R_{23} and

R_{z2} with R_{23}, R_{43}, R_{32}, R_{34} and R_{z3} respectively.

$$\mathbf{A}_{d_{33}} = \left(\begin{array}{c|cccccccc} & v_9 & & & & v_{10} & v_{11} & & v_{12} \\ \hline v_9 & -\frac{1}{R_{23}} & -\frac{1}{R_{z3}} & -\frac{1}{r_x} & -\frac{1}{R_{43}} & 0 & 0 & & -\frac{1}{R_{z3}} \\ v_{10} & & -g_{mb1} & & & -\frac{1}{r_{in1}} & 0 & & 0 \\ v_{11} & & g_{mb3} & & & -g_{mb2} & -\frac{1}{r_{in2}} - \frac{1}{R_{32}} - \frac{1}{R_{34}} & & 0 \\ v_{12} & & -\frac{1}{R_{z3}} & & & 0 & 0 & & -\frac{1}{R_{z3}} \end{array}\right) \tag{2.30}$$

$\mathbf{A}_{d_{34}}$ is similar to $\mathbf{A}_{d_{23}}$ and it can be obtained by replacing R_{32} and R_{23} with R_{43} and R_{34} respectively.

$$\mathbf{A}_{d_{34}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_9 & 0 & 0 & -\frac{1}{R_{43}} & 0 \\ v_{10} & 0 & 0 & 0 & 0 \\ v_{11} & \frac{1}{R_{34}} & 0 & 0 & 0 \\ v_{12} & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.31}$$

State space equation of fourth integrator is as follows.

$$\mathbf{H_{44}}\dot{\mathbf{x_4}} = \mathbf{A}_{d_{43}}\mathbf{x}_3 + \mathbf{A}_{d_{44}}\mathbf{x}_4 + \mathbf{A}_{d_{45}}\mathbf{x}_5 \tag{2.32}$$

$$\mathbf{H_{44}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{13} & c_x + 2c_c & -c_c & c_c & 0 \\ v_{14} & -c_c & c_{in1} + 2c_c & -c_c & 0 \\ v_{15} & c_c & -c_c & c_{in2} + 2c_c + C_4 & -C_4 \\ v_{16} & 0 & 0 & -C_4 & C_4 \end{array}\right) \tag{2.33}$$

$$\mathbf{A}_{d_{43}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_{13} & 0 & 0 & \frac{1}{R_{34}} & 0 \\ v_{14} & 0 & 0 & 0 & 0 \\ v_{15} & -\frac{1}{R_{43}} & 0 & 0 & 0 \\ v_{16} & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.34}$$

$\mathbf{A}_{d_{44}}$ is similar to $\mathbf{A}_{d_{33}}$ and it can be obtained by replacing R_{23}, R_{43}, R_{32}, R_{34} and R_{z3} with R_{34}, R_{54}, R_{43}, R_{45} and R_{z4} respectively.

$$\mathbf{A}_{d_{44}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{13} & -\frac{1}{R_{34}} - \frac{1}{R_{z4}} - \frac{1}{r_x} - \frac{1}{R_{54}} & 0 & 0 & -\frac{1}{R_{z4}} \\ v_{14} & -g_{mb1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_{15} & g_{mb3} & -g_{mb2} & -\frac{1}{r_{in2}} - \frac{1}{R_{43}} - \frac{1}{R_{45}} & 0 \\ v_{16} & -\frac{1}{R_{z4}} & 0 & 0 & -\frac{1}{R_{z4}} \end{array}\right) \tag{2.35}$$

$\mathbf{A}_{d_{45}}$ is similar to $\mathbf{A}_{d_{34}}$ and it can be obtained by replacing R_{43} and R_{34} with R_{54}

and R_{45} respectively.

$$\mathbf{A}_{d_{45}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{13} & 0 & 0 & -\dfrac{1}{R_{54}} & 0 \\ v_{14} & 0 & 0 & 0 & 0 \\ v_{15} & \dfrac{1}{R_{45}} & 0 & 0 & 0 \\ v_{16} & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.36}$$

For the final stage, the state space equation can be written as follows.

$$\mathbf{H_{55}}\dot{\mathbf{x_5}} = \mathbf{A}_{d_{54}}\mathbf{x}_4 + \mathbf{A}_{d_{55}}\mathbf{x}_5 \tag{2.37}$$

$$\mathbf{H_{55}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{17} & c_x + 2c_c & -c_c & c_c & 0 \\ v_{18} & -c_c & c_{in1} + 2c_c & -c_c & 0 \\ v_{19} & c_c & -c_c & c_{in2} + 2c_c + C_5 & -C_5 \\ v_{20} & 0 & 0 & -C_5 & C_5 \end{array}\right) \tag{2.38}$$

$$\mathbf{A}_{d_{54}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{17} & 0 & 0 & \dfrac{1}{R_{45}} & 0 \\ v_{18} & 0 & 0 & 0 & 0 \\ v_{19} & -\dfrac{1}{R_{54}} & 0 & 0 & 0 \\ v_{20} & 0 & 0 & 0 & 0 \end{array}\right) \tag{2.39}$$

$$\mathbf{A}_{d_{55}} = \left(\begin{array}{c|ccccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{17} & -\frac{1}{R_{45}} - \frac{1}{R_{z5}} - \frac{1}{r_x} & 0 & 0 & -\frac{1}{R_{z5}} \\ v_{18} & -g_{mb1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_{19} & g_{mb3} & -g_{mb2} & -\frac{1}{r_{in2}} - \frac{1}{R_{54}} & 0 \\ v_{20} & -\frac{1}{R_{z5}} & 0 & 0 & -\frac{1}{R_{z5}} \end{array}\right) \tag{2.40}$$

and

$$\mathbf{C}_{55} = (\,0\;0\;1\;0)$$

The final descriptor state space equations for the filter are given below.

$$\begin{bmatrix} \mathbf{H}_{11} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{H}_{22} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{H}_{33} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H}_{44} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H}_{55} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}_1} \\ \dot{\mathbf{x}_2} \\ \dot{\mathbf{x}_3} \\ \dot{\mathbf{x}_4} \\ \dot{\mathbf{x}_5} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_{d_{11}} & \mathbf{A}_{d_{12}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{A}_{d_{21}} & \mathbf{A}_{d_{22}} & \mathbf{A}_{d_{23}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{d_{32}} & \mathbf{A}_{d_{33}} & \mathbf{A}_{d_{34}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A}_{d_{43}} & \mathbf{A}_{d_{44}} & \mathbf{A}_{d_{45}} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A}_{d_{54}} & \mathbf{A}_{d_{55}} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \mathbf{x}_3 \\ \mathbf{x}_4 \\ \mathbf{x}_5 \end{bmatrix} + \begin{bmatrix} \mathbf{B}_{d_1} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \mathbf{u} \tag{2.41}$$

$$\mathbf{y} = \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{C}_{55} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \mathbf{x}_3 \\ \mathbf{x}_4 \\ \mathbf{x}_5 \end{bmatrix} \tag{2.42}$$

Frequency response of the filter can be obtained from $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ matrices using MATLAB built-in routines $ss2tf$ and $freqs$.

2.5.2 Design centering procedure

All small signal parameters of the OTA including parasitic capacitances are computed using DC operating points and necessary simulations. Once all the small signal parameters are found, the model is derived using the state space equations as explained in the previous sub-section. The model is now ready to be tuned to offer a desired response. Since the integrating resistors, integrating capacitors and zero compensating resistors can be set to the desired value, it is easy to tune the filter by tuning these parameters. MATLAB built-in optimization routine, *fminsearch* which employs the Nelder-Mead simplex optimization process is used in this work to minimize the error between actual and the desired frequency responses. The steps followed for design centering the filter are outlined as follows.

- For the given biasing conditions, DC analysis is done on the transistor level filter to obtain the operating point of OTAs. The necessary small signal parameters of all the OTAs are obtained.
- The filter is simulated to obtain the frequency response (for the desired frequency grid) for a given set of Integrating resistors R_{int}, Integrating capacitors [C_1 C_2 C_3 C_4 C_5] and R_z. Let us denote this optimization vector as $\mathbf{k}$ =[C_1 C_2 C_3 C_4 C_5 R_z R_{int}]. A good choice for the initial $\mathbf{k}$ would be that corresponding to the values which are computed assuming ideal OTA i.e. the values obtained after node scaling the filter.
- Small signal parameters of the OTA are used in the state-space model of the filter.
- The frequency response of the model is obtained for the same frequency grid and the initial optimization vector $\mathbf{k}$, in order to ensure that the model is accurate.
- Optimization routine $fminsearch$ is run on the model to fit the response of the model to the ideal filter response. This minimizes the error between the ideal and the actual frequency response. The error function is made a function of $\mathbf{k}$.
- The final optimized $\mathbf{k}$ is put back into transistor level filter. Since the model is sufficiently accurate, the response of the transistor level filter will also be close to the ideal.

Values of the optimizing parameters of the design centered filter are as follows.

$C_1 = 1.44$ pF; $C_2 = 2.67$ pF; $C_3 = 2.40$ pF;

$C_4 = 2.49$ pF; $C_5 = 1.40$ pF;

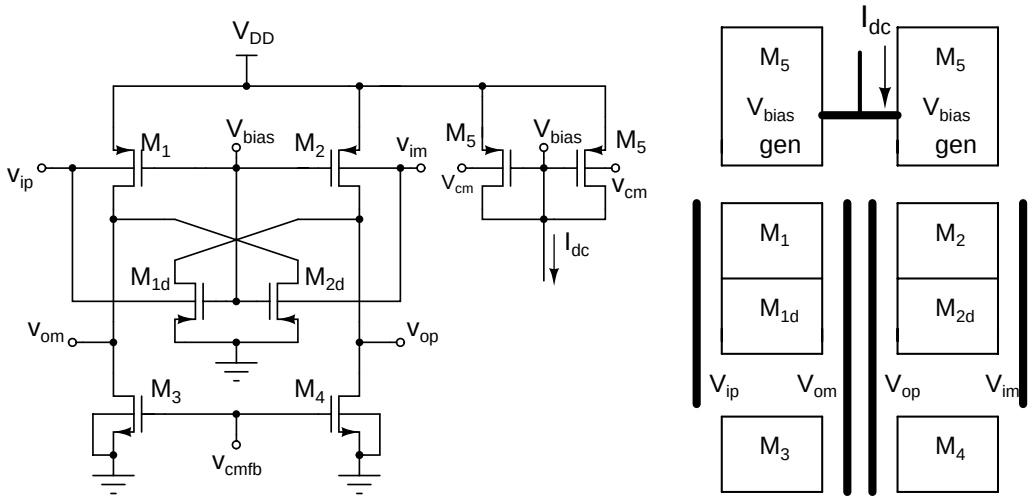
$R_{int} = 326.94$ kΩ; $R_z = 10.19$ kΩ

2.6 LAYOUT OF THE FILTER

The filter uses differential architecture. Therefore, it is important to ensure that there exists a very good match between the transconductors, OTAs and resistors. A well planned layout is mandatory to achieve satisfactory operation in presence of random mismatches in the fabricated circuit. This section discusses the layout plan used for the filter.

Since the transconductor is the building block of OTA, it is laid out first. Figure 2.17 shows the floorplan of the layout of transconductor along with the corresponding schematic. The symmetry of the schematic is maintained for the layout also. But, the diode connected transistor M_5 used to generate the bias for the current sources of the transconductor is not symmetric. However, by splitting M_5 into two halves, symmetry can be achieved even for M_5. The same has been followed in the floorplan as shown in the figure. All horizontal routing has been done using *metal-1* and *metal-3*, while all the vertical routing is done using *metal-2* and *metal-4*. The same convention has been followed for the complete filter.

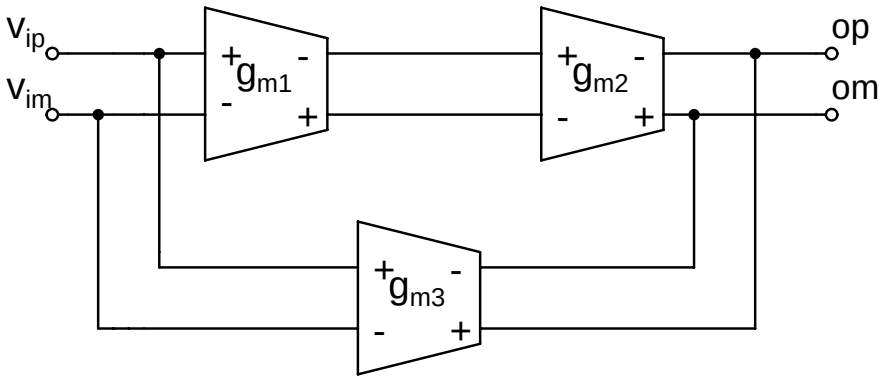
The scheme used to draw the layout of the OTA is shown in Figure 2.18. Three transconductors (first, second and feed-forward) are arranged and connected to each other as shown. The interconnection between the metal lines is accomplished by placing a via. Black bubbles in Figure 2.18(b) show these interconnections. While connecting two wires using via, both the wires are extended beyond the junction uniformly. This ensures that the interconnect parasitic coupling capacitances on the differential lines are equal (Pavan, 1999).



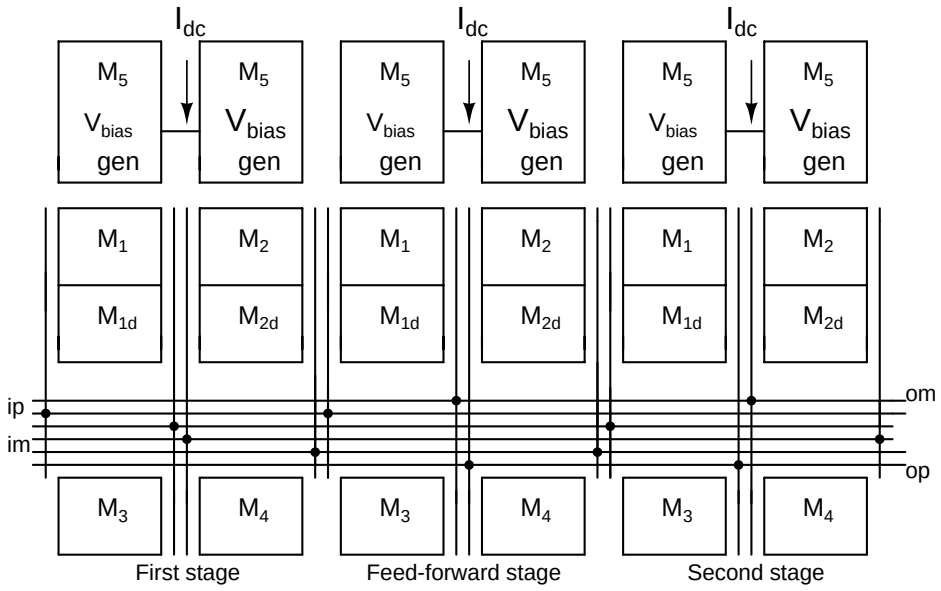
(a) Schematic (b) Floorplan

Figure 2.17: Layout of the unit transconductor (a) Schematic (b) Layout floorplan

The complete scheme of the filter layout is shown in Figure 2.19. Each OTA cell is represented by a simple block with input (ip and im) and output (op and om) lines. The integrating capacitors are realized using the Metal-Insulator-Metal (MIM) capacitors available in the UMC technology and are represented by simple boxes coloured gray in the Figure 2.19. The integrating resistors and the zero compensating resistors are realized using high resistivity poly resistors available in the UMC technology and they are represented by boxes coloured black in the figure. Routing between the consecutive blocks is also shown. Figure also shows the fully differential schematic of the filter. The schematic is drawn here to have one-to-one correspondence with the layout. Figure 2.20 shows the screenshot of the complete layout of the filter. The layout also includes accessories such as CMFB circuits, the constant current generating circuit (used to bias the transconductors) and the associated bias distribution circuit. The total area of the filter is 0.65 mm^2. The parasitics of the interconnects are extracted and the simulations are run on the layout extracted netlist.



(a) Schematic



(b) Floorplan

Figure 2.18: OTA layout (a) Schematic (b) Floorplan of the layout

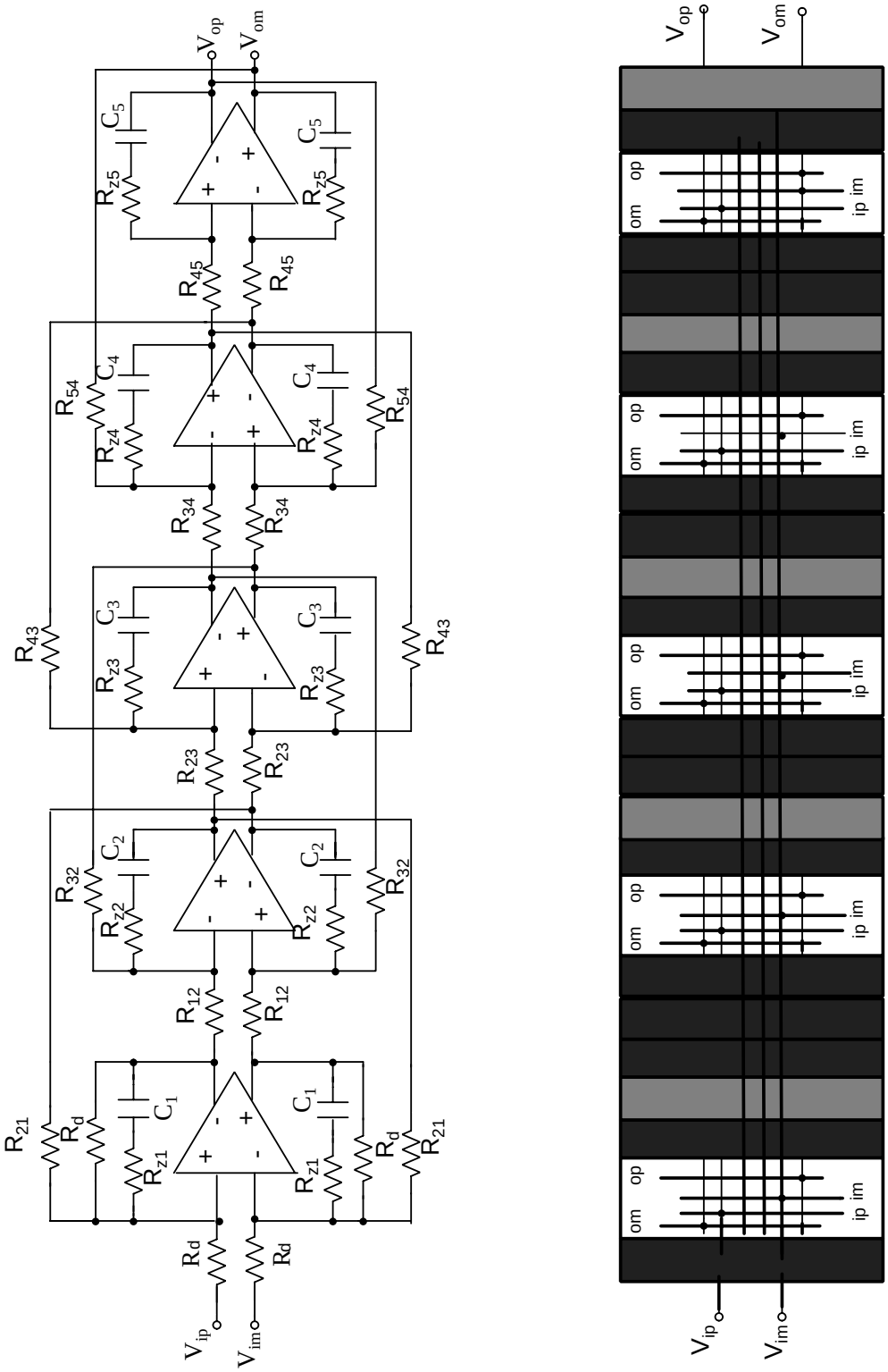


Figure 2.19: Schematic and Floorplan of the filter

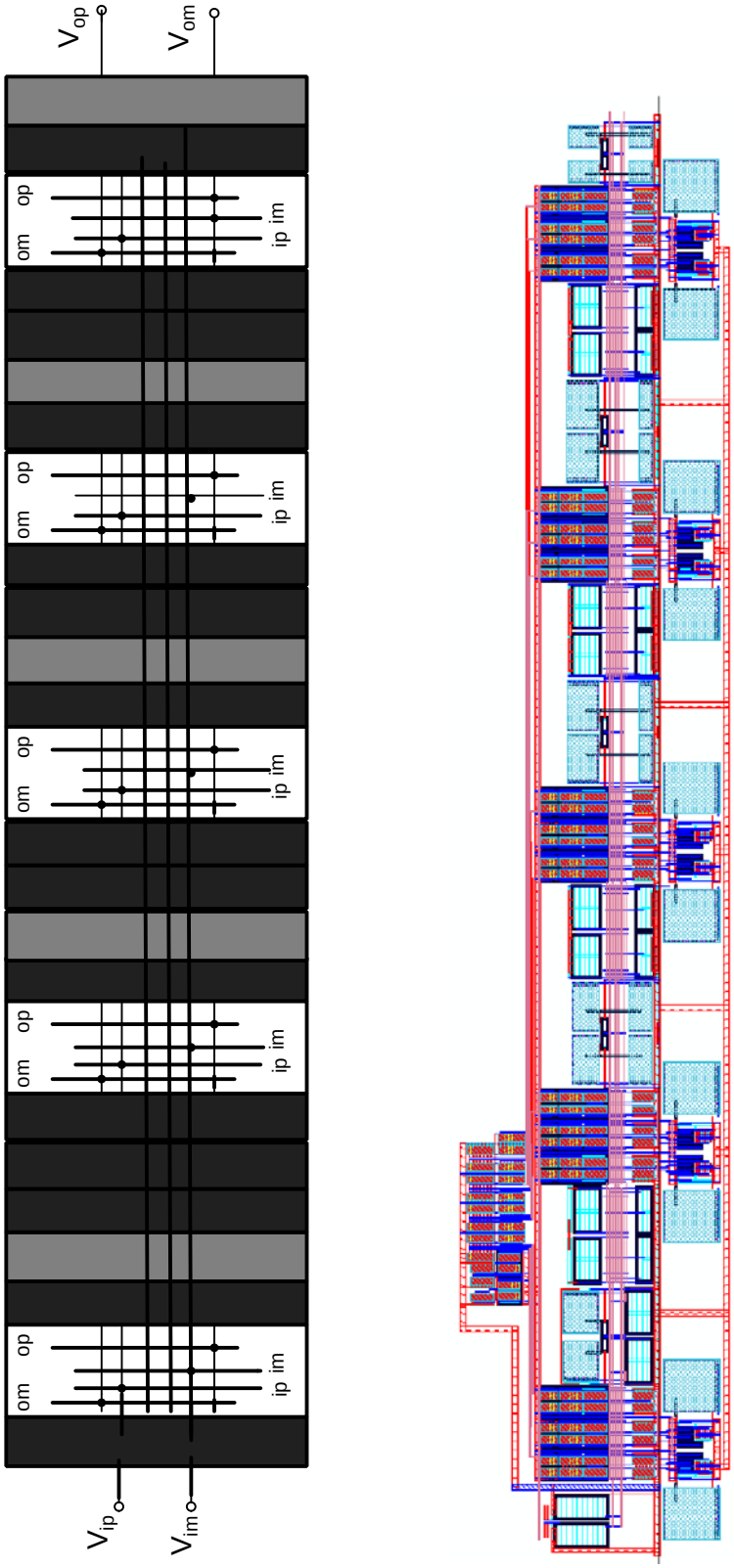


Figure 2.20: Floorplan and layout of the filter

2.6.1 Design centering the layout extracted netlist

Though the schematic is design centered before the layout, interconnect parasitics affect the response of the layout extracted filter. Therefore, the filter requires to be design centered again in presence of layout parasitics. The procedure remains the same. However, the model should be updated by including the layout parasitics which can be obtained from the extracted netlist.

2.7 SIMULATION RESULTS

The complete filter is simulated for the frequency response. Figure 2.21 shows the normalized magnitude response of the filter at nominal supply voltage of 0.5 V, room temperature and nominal process corner. When compared with the ideal, the passband response has a good match with the ideal. However, the stop band tends to deviate from the ideal beyond about 1 MHz where the filter attenuation is above 50 dB. This deviation can be attributed to the parasitic poles of the filter. Note that, the actual filter is found to be the order of twenty and the design centering process tries to fit the response to a filter of fifth order.

The performance of the filter is summarized in Table 2.3.

Table 2.3: Parameters of the filter - simulated

Supply Voltage	0.5 V
Technology	180 nm CMOS
Filter type	5th order Chebyshev,low pass
3 dB bandwidth	477 kHz
Power	250 μW
Integrated output noise (in the range 40 kHz-600 kHZ)	510 μV rms
V_{in-pp} differential for THD=-40 dB	768 mV
Dynamic Range for THD=-40 dB	50.96 dB

Simulations are also done to test the performance of the filter against temperature

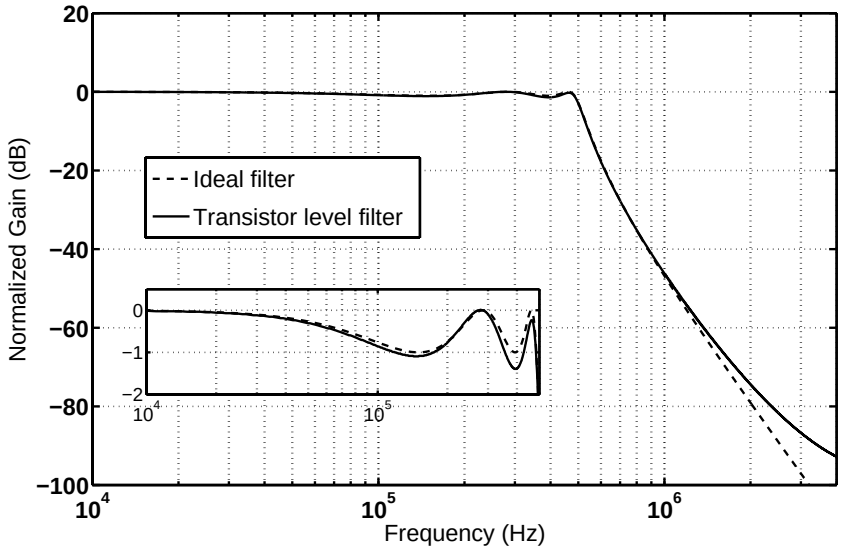


Figure 2.21: Magnitude response of the filter

variations in the range 0-80°C. The Figure 2.22 shows the filter response at nominal supply voltage and nominal process corner. The change in the band edge is only ±2.5%.

Figure 2.23 shows the filter response for supply voltage variations in the range ±10% over the nominal 0.5 V at room temperature and typical corner. Figure 2.24 shows the filter response for five corners at nominal supply voltage and room temperature. There is only a ±2% variation in the band edge of the filter across corners.

Figure 2.25 shows the integrated output noise of the filter versus frequency. At low frequencies, the output noise is dominated by 1/f noise; the small flat region in the passband of the filter is a result of white noise. The later peaking at around 480 kHz is a result of the filter topology and transfer function. The observed 1/f noise corner is about 310 kHz. The OTAs contribute to the noise at lower frequencies while the filter resistors dominantly contribute beyond the 1/f noise corner frequency.

The designed low-pass fifth-order Chebyshev active-RC filter is fabricated using UMC 180 nm CMOS process. The filter is fabricated on silicon at *IMEC*, Belgium

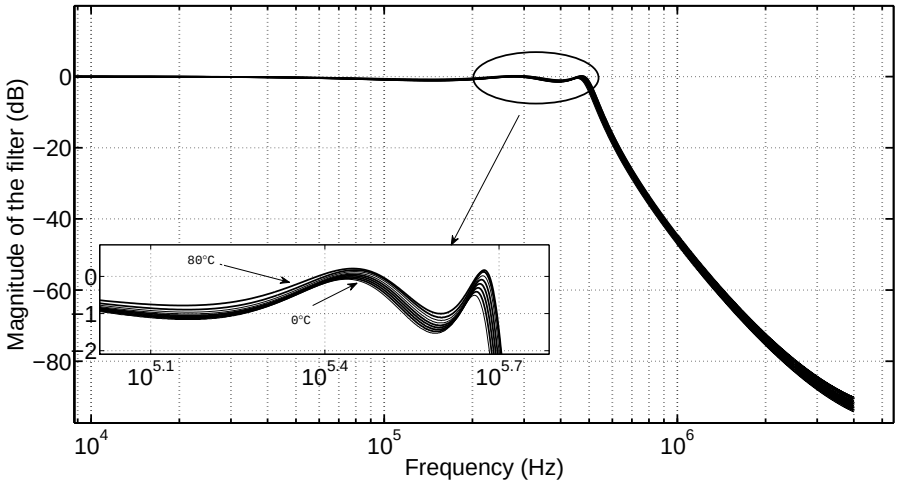


Figure 2.22: Magnitude response of the filter across temperature in the range 0-80°C

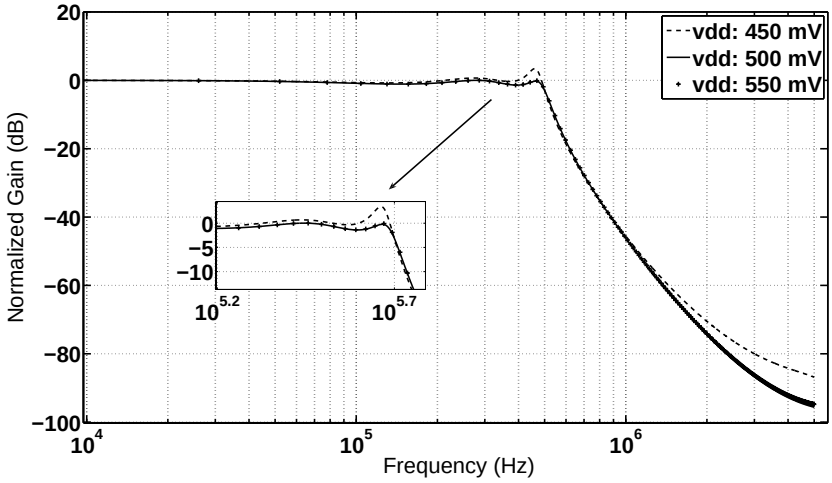


Figure 2.23: Magnitude response of the filter for V_{DD} variations (0.5 V$\pm$10%)

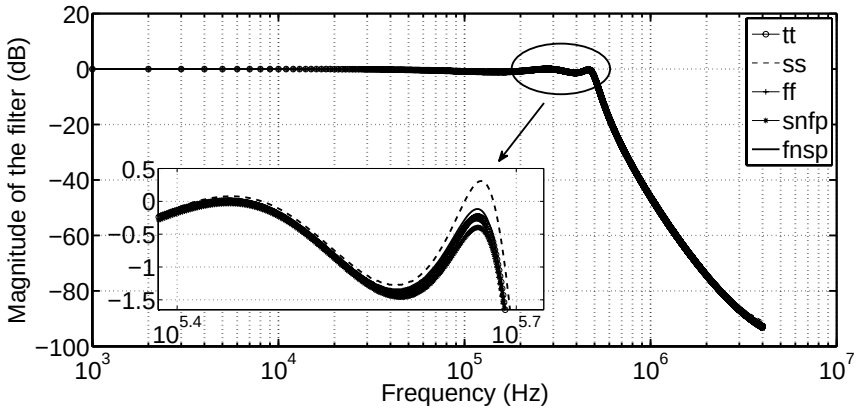


Figure 2.24: Magnitude response of the filter for different corners

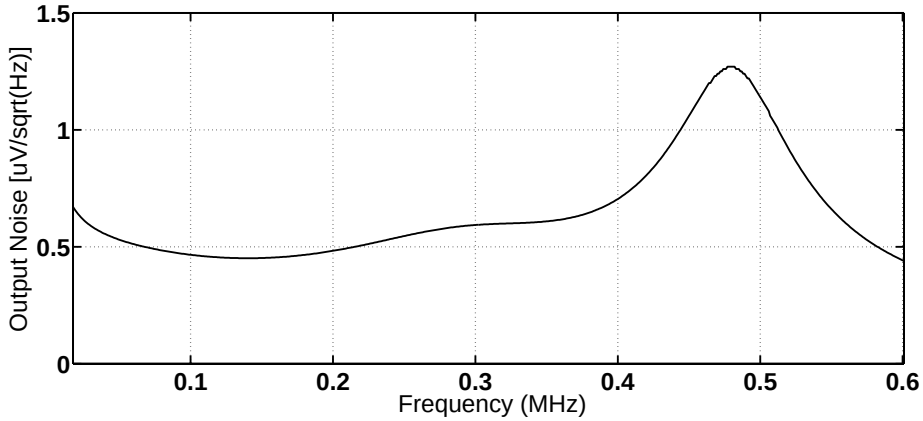


Figure 2.25: Output noise of the filter

through *EUROPRACTICE*. The results of the fabricated filter are presented in the next chapter.

CHAPTER 3

CHARACTERIZATION OF ON-CHIP FILTER

Characterization of integrated continuous time filters require the filter output signal to be brought out of the chip for measurements. But typically, the filters are not designed to drive large capacitive loads offered by the IC package or the 50 Ω load offered by the measuring instruments such as Vector Network Analyzer (VNA) / Spectrum Analyzer (SA). It is common to use buffers to drive such large loads. However, when characterizing the filter in packaged chips, effects of the test-buffers and the package parasitics must be de-embedded from the filter response. The characterizing procedure must be able to measure the filter response very effectively. A simple technique is proposed in (Nauta, 1992) to characterize packaged integrated filters. This technique is accurate enough for characterizing low frequency filters where the package parasitics can be considered to have negligible effect on the measured stop-band characteristic of the filter. For the filter designed in this work, this approach has been used. Figure 3.1 shows the test-setup used for characterizing the fabricated filter.

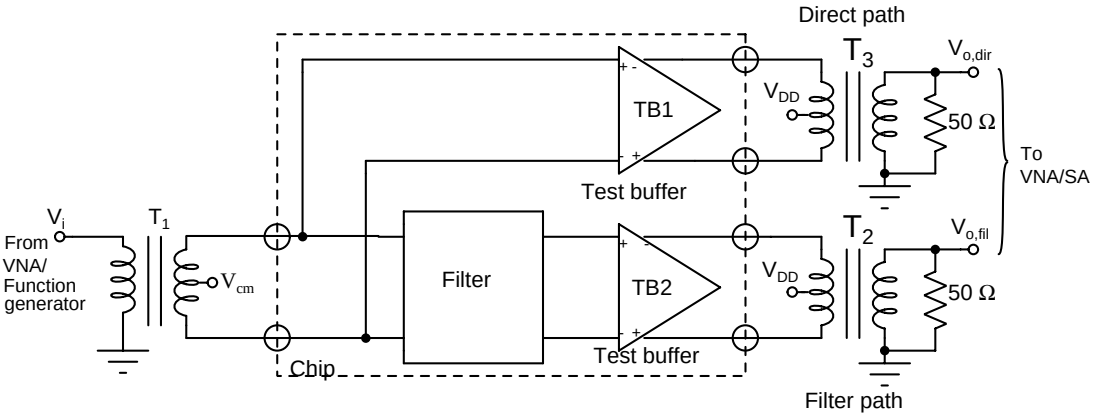


Figure 3.1: Test set-up for on-chip filter characterization

The filter to be tested is assumed to be fully differential. Transformer T1 converts

the single ended excitation from the test equipment into a fully differential signal to be fed to the filter differential inputs. Since the filter is not designed to drive the external loads, two nominally identical on-chip test buffers TB1 and TB2 are used. These test buffers are biased by sufficiently large currents so that they are able to drive the external loads. They are activated only during characterization. TB1 senses the input of the filter and forms the direct measurement path while TB2 senses the output of the filter and forms the filter measurement path. Transformers T2 and T3 convert the test buffer outputs into single ended signals that are measured by the test instruments. The test buffers, IC package and board parasitics have a frequency response that must be de-embedded in order to obtain the true filter response. While characterization, following assumptions are made (Laxminidhi, 2007).

1. TB1 and TB2 are matched.
2. The measurement paths at the outputs of TB1 and TB2 are identical.
3. The input impedance of TB1 and TB2 are negligible.
4. The reverse transmissions of the filter, TB1 and TB2 are negligible in the frequency range of interest.
5. Signal feed-through from input of the chip to the output of the chip due to package parasitics is negligible in the frequency range of interest.

The block diagram representation of the test set-up is shown in Figure 3.2. H_{in} is

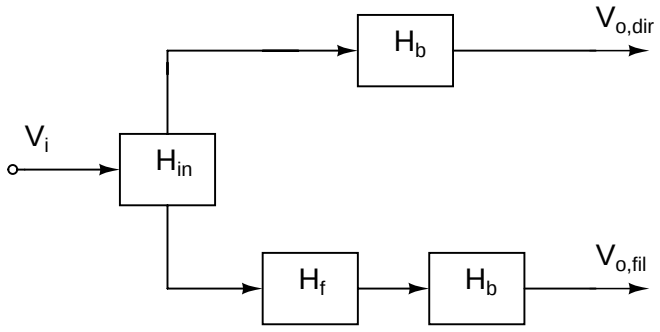


Figure 3.2: Block diagram of the test setup

the transfer function of the input path, i.e. from v_i to the input of the filter. H_f is the

filter transfer function and H_b is the transfer function from the test buffer input to the final output (outputs of T2 and T3 in Figure 3.1). From the block diagram, frequency response of the filter can be written as in (3.1).

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} \tag{3.1}$$

SA or VNA can be used to measure $H_f(f)$. If magnitude response is only of interest SA can be used to measure $V_{o,fil}(f)$ and $V_{o,dir}(f)$ independently and $H_f(f)$ can be computed from $V_{o,fil}(f)$ and $V_{o,dir}(f)$. If VNA is used for measurements, S-parameters of the filter path and the direct path can be measured from which the filter response can be obtained. Assuming a good impedance match, it can be shown that

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} = \frac{S_{21,fil}(f)}{S_{21,dir}(f)} \tag{3.2}$$

This technique has been found to be a standard for characterizing the filters over the years.

3.1 TEST BUFFER DESIGN

Figure 3.3 shows the schematic of the test buffer designed to drive external loads. It is designed to operate on 3.3 V supply since linearity of buffer should be maintained at a level much higher than that of the filter. The buffer has fully differential architecture and has two stages. The first stage is a source follower formed by the input transistors M_1 and M_2, and the second is a differential amplifier (source-coupled differential pair) converting analog output to a proportional current. The source follower stage serves two purposes. One, it offers a capacitive load to the filter. The sizes of the input transistors are made small so that they offer small capacitance and this small capacitance can be taken into account while design centering the filter. Second, the source follower acts as a level shifter raising the output common-mode DC of the filter (which is 0.25 V) to

about 1.6 V such that the differential amplifier of the second stage will have sufficient headroom to offer the desired linearity.

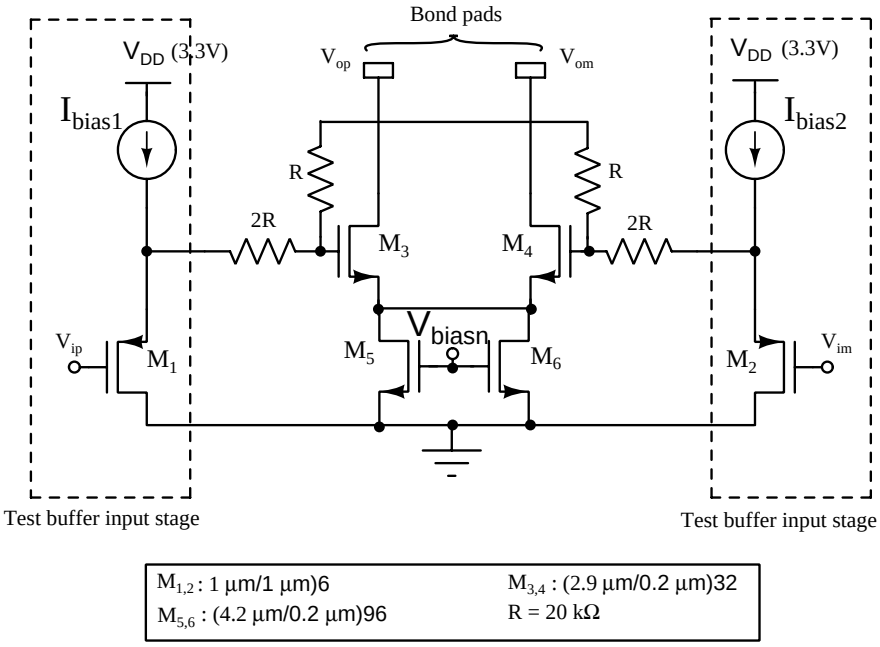


Figure 3.3: Schematic of Test buffer

The differential amplifier is formed by the transistors M_3 and M_4 along with the tail-current source transistors M_5 and M_6. Transistors M_3 and M_4 are sized so that they have a large gate overdrive voltage while they are made to carry large currents of approximately 15 mA. This is important because distortion of the test buffer must be small when compared to that introduced by the filter. However, since the filter is designed to work at a differential swing of 1 V peak-to-peak, the achievable gate overdrive is not sufficient to keep the distortion of the buffer below the desired limits of -60 dB. Thus, to achieve the necessary buffer linearity, the output of the first stage is attenuated by a factor of three using a resistive potential divider, before feeding it to the next stage. Note that this potential divider is differential and hence operates only on output signal.

Figure 3.4 shows the biasing circuit used to bias the test buffers. An off-chip current of 100 μA, generated using the IC LM 334, is used as the reference. Detailed circuit

diagram of 100 μA current generation is given in Appendix B. In Figure 3.4, transistors M_a and M_b form the current sources (I_{bias1} and I_{bias2} respectively) for the input stage of test-buffer circuit of Figure 3.3. The bias voltage (V_{biasn}) for the tail-current source of the second stage of the test buffer is generated by transistors $M_c - M_j$.

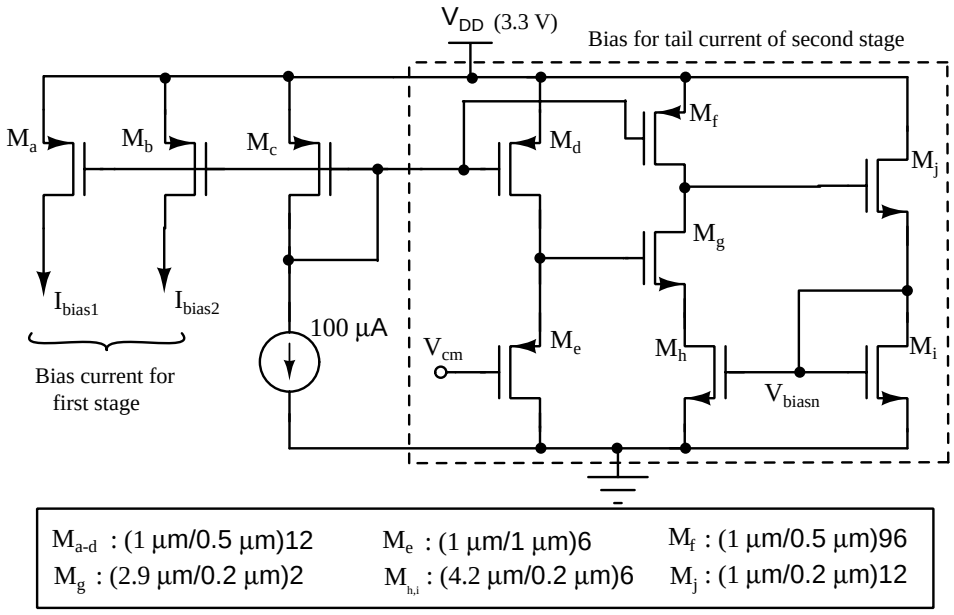


Figure 3.4: Biasing circuit for test buffer

3.2 CHIP DETAILS

Proposed filter is fabricated using UMC 180 nm CMOS process through Europractice. Size of the die is 1.5 mm$\times$1.5 mm (2.25 mm^2) of which the Active-RC filter occupies an area of 0.65 mm^2. The die-photograph and the top level layout of the fabricated chip is shown in Figure 3.2. Highlighted area shows the Active-RC filter designed in this work. The chip is packaged in a 44-pin J-leaded chip carrier (JLCC) package. The pinout of the packaged chip and the functionality of the pins are given in Appendix C. Figure 3.5 shows the bonding diagram used for packaging.

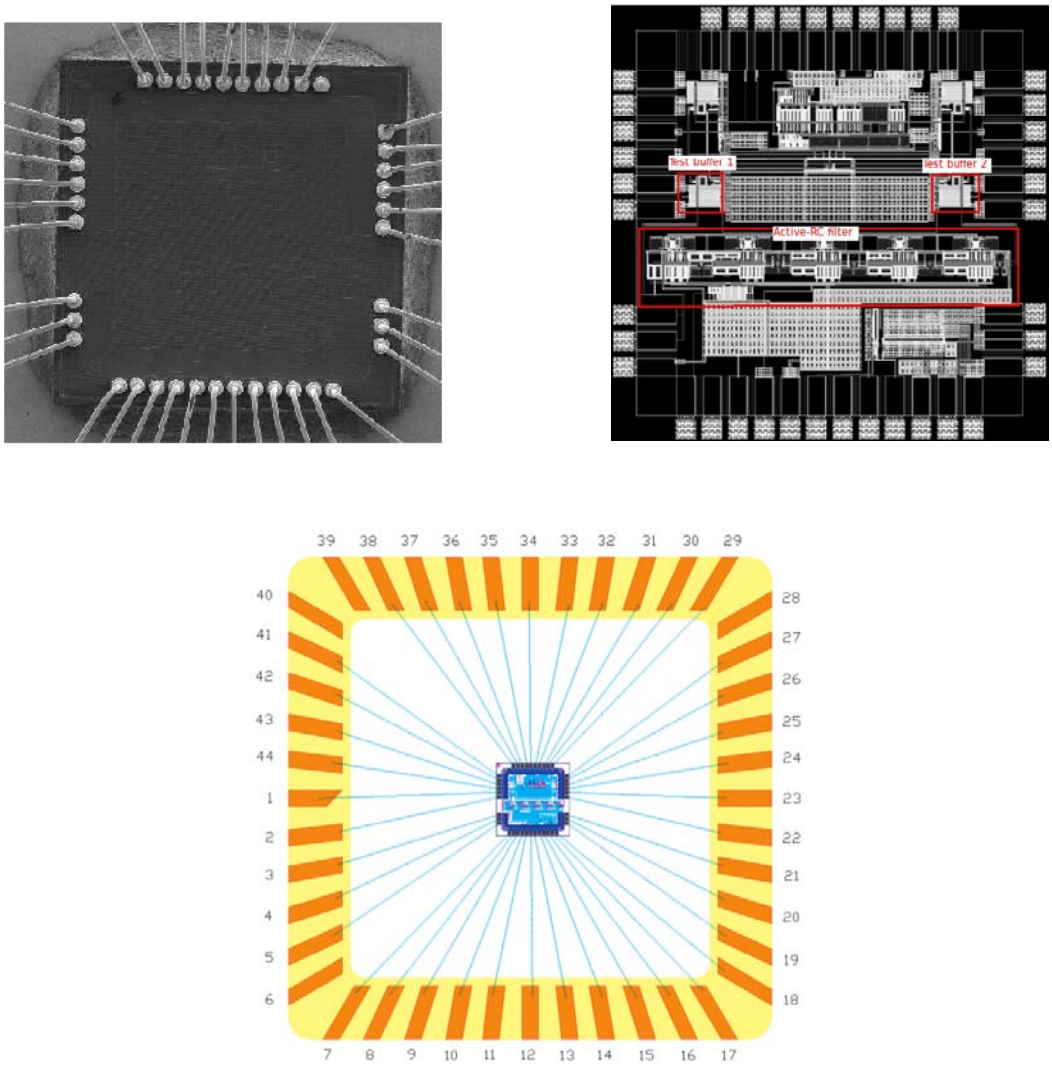


Figure 3.5: Bonding diagram for packaging the die.

3.3 DESIGN OF TEST BOARD

A two layered printed circuit board (PCB) is designed and fabricated to characterize the filter chip. The board measured $3.4'' \times 4.2''$ in size. A photograph of the populated PCB is shown in Figure 3.6. The baluns T1-T3, referring to Figure 3.1, are realized from a wide-band transformers ADT1-6WT from Mini-Circuits. They have a frequency range of 0.03-150 MHz with an insertion loss of 3 dB.

Decoupling capacitors are used at each power pin in order to decouple the supply

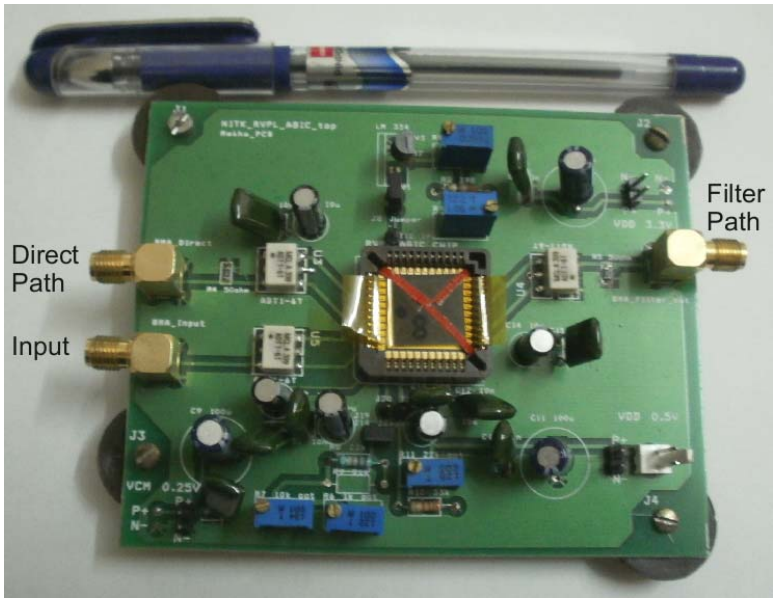


Figure 3.6: Photograph of the two layered PCB populated with all the components.

voltage from any interference and/or noise which can couple through parasitics. A 10 μF electrolytic capacitor (for suppressing low frequency noise) and a 10 nF polyester film capacitor (for decoupling high frequency noise) are placed very close to each power pin. The same has been followed for common-mode reference voltage too.

The board has one LM334 based current sink circuit to sink a current of 100 μA from the chip to generate the bias for the test-buffer circuit inside the chip.

3.4 POWER SUPPLY DESIGN

The chip requires three regulated voltages viz 0.5 V to power the filter (V_{DD}), 0.25 V as common-mode reference voltage for the filter (V_{cm}) and 3.3 V for the test buffer (V_{DD1}). An adjustable laboratory power supply is sufficient for 3.3 V. But, for 0.5 V and 0.25 V it is not advisable to use such a power supply, for the reason that a small change in any adjustment (intentional or accidental) can change the voltage by a large percentage. Therefore, a dedicated regulated power supply has been designed for 0.5 V and 0.25 V. The details of the power supply circuits are given in Appendix D.

3.5 MEASURED RESULTS

The test-board explained in the previous section is used to characterize the chip. Figure 3.7 shows the measured magnitude response of the filter and is also compared with the ideal. Though the filter is designed for a bandwidth of 477 kHz, the fabricated filter is found to have a bandwidth of 750 kHz, an increase by a factor of about 1.57. The ideal response plotted in the figure is obtained by matching the ideal stop-band to the filter stop-band. It is to be noted that the filter offers a fifth order roll-off (-30 dB/octave) as expected. An analysis has been done to find the possible reason for increase in the bandwidth of the filter chip and is presented at the end of this chapter.

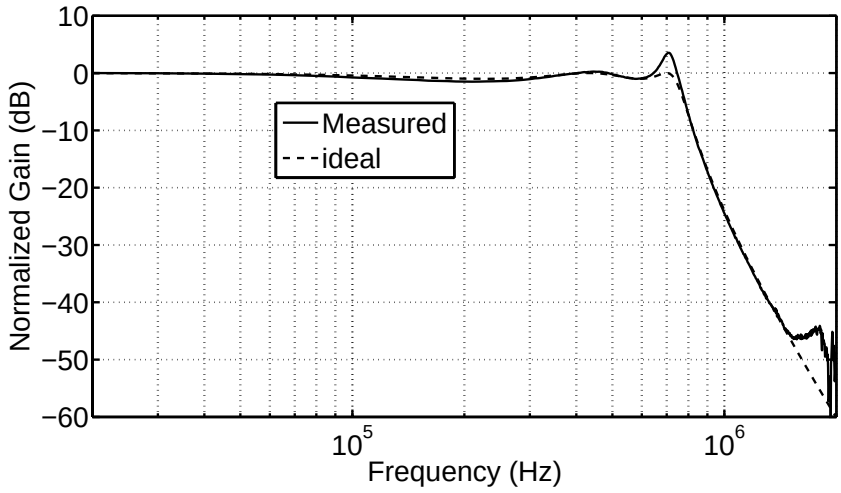


Figure 3.7: Normalized magnitude response of the filter.

To check the repeatability of the design, response of eighteen samples of the fabricated chip is plotted in Figure 3.8. It is evident that the fabricated chips offer a very good repeatability with a $\pm 2\%$ variation in bandwidth.

The voltage noise spectral density measured at the output of the filter is plotted in Figure 3.9. At low frequencies, the output noise is dominated by $1/f$ noise. As expected, the output noise power spectral density has a shape of filter frequency response. The OTAs contribute to the noise at lower frequencies while the filter resistors dominantly contribute beyond the $1/f$ noise corner frequency. The rms output noise when integrated

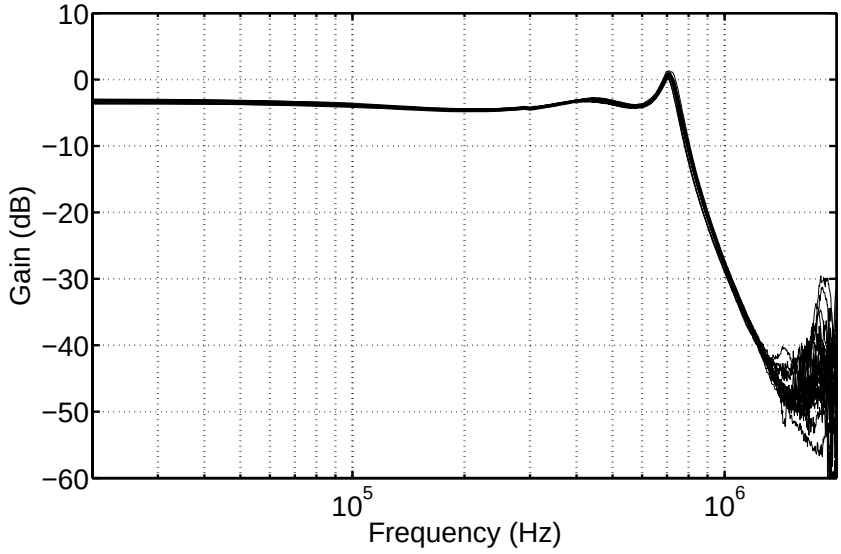


Figure 3.8: Magnitude response of eighteen samples of the filter chip.

upto 1 MHz is found to be 851 μV.

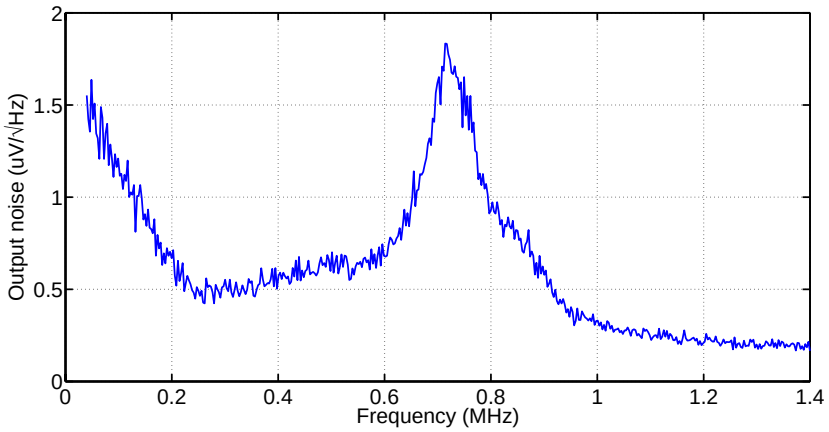


Figure 3.9: Output noise power spectral density of the filter.

3.5.1 Distortion Performance

The filter is tested for distortion performance for an in-band tone at 250 kHz. Figure 3.10 shows the Total Harmonic Distortion (THD) of the filter for a set of a differential peak-to-peak input voltage. Here, the tone is selected to have 250 kHz so that filter

will have third harmonic component as the dominant harmonic at the output while the higher order harmonics are naturally rejected by the filter characteristics.

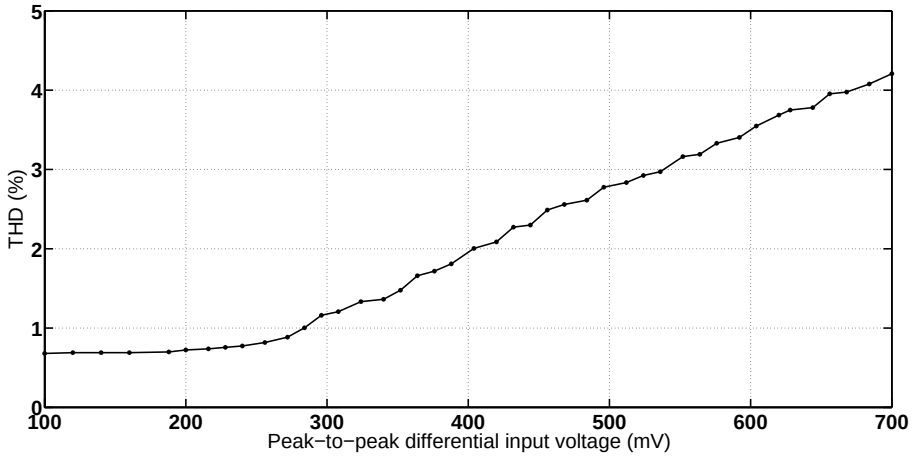


Figure 3.10: Total Harmonic distortion of the filter as a function of the input differential voltage at 250 kHz

When the filter is tested for an in band tone at 550 kHz, a THD of 1% is observed for a differential peak-to-peak input voltage of 768 mV. Dynamic range of the filter is found to be 46.33 dB and is computed as the ratio of the rms differential input voltage offering 1% THD for a tone of 550 kHz (near the band-edge) to the input referred rms noise over the frequency range of 40 kHz to 1 MHz. The performance of the filter is summarized in Table 3.1.

Table 3.1: Parameters of the filter - Measured

Supply Voltage	0.5 V
Technology	180 nm CMOS
Filter type	5th order Chebyshev,low pass
3 dB bandwidth	750 kHz
Power	305 μW
Integrated output noise	851 μV rms
V_{in-pp} differential for THD=-40 dB	768 mV
Dynamic Range for THD=-40 dB	46.33 dB

The filter is compared with some of the low-voltage filters (gate/bulk driven) found in the literature and the comparison is given in Table 3.2. All the filters that are com-

pared here are realized on silicon. For a fair comparison, the dynamic range is computed as the ratio of the rms differential input voltage that offers 1% THD for a tone of 550 kHz (near the band-edge) to the input referred rms noise over the frequency range of 40 kHz to 1 MHz. Note that, for $G_m - C$ filters in (Carrillo *et al.*, 2010) and (Carrillo *et al.*, 2011), the linearity has been measured for tone at a frequency much below the bandwidth. At frequencies much below the filter bandwidth, the distortion offered by $G_m - C$ filters are typically small since the distortion currents of the transconductors cancel each other (Pavan *et al.*, 2000). A Figure of Merit (FOM) (Laxminidhi *et al.*, 2009) has been used for the comparison and is given in (3.3).

$$FOM = \frac{P_{diss}}{pQ_{max}f_oDR^2} \tag{3.3}$$

where P_{diss} is the power dissipation, p is the number of filter poles, f_o is the filter cut-off frequency, Q_{max} is the maximum quality factor of the filter poles and DR is the dynamic range. A lower FOM indicates a more power efficient design. It is to be noted that there are a very few sub-1 V filters available in the literature that are realized on silicon.

The following points may be observed in the table for the filter chip.

- Q_{max} of the filter is estimated to be 9.34. This is done since the filter chip shows peaking in the response near the band-edge. Q_{max} is estimated by tuning the poles and zeros of the fifth order filter so as to get a response close to the measured response of the chip. Thanks to the *fminsearch* routine of the MATLAB. Owing to the increased Q, FOM of the filter chip is computed for Q_{max} =9.34.
- For the simulated response, Q_{max} is 5.55 (since the filter is tuned to match the ideal response).
- Power of the filter chip is found to be 20% in excess of that of simulated. The off-chip resistor R_{ext} which sets the bias current of transconductors is fixed at a value (25 kΩ) same as that used for the simulated filter.
- It is interesting to note that the measured linearity is same as that of the simulated. This is expected since the reduction in the integrating capacitors (in the filter chip) will not affect the load on the OTAs. Also, while finding linearity of the filter chip and the layout extracted netlist, ratio of exciting tone to bandwidth is maintained constant as can be seen in the note given below Table 3.2.

- Dynamic range of the filter chip is smaller than expected from the simulation. This is due to the fact that the actual integrating capacitors in place in the chip are smaller than that in the layout extracted netlist.
- The FOM of the filter chip, however, is comparable to the simulated.

Table 3.2: Comparison with some published filters

Reference	**Bandwidth [MHz]**	**Order**	**Supply Voltage [**V]	**Power [μW]**	Q_{max}	**Input [mVrms] for 1% THD**	**Dynamic Range[dB] (for THD$\approx$ -40 dB)**	**Topology**	**Tech. [μm]**	**FOM (fJ)**
(Chatterjee *et al.*, 2005)	0.135	5	0.5	1100	6.2	50	56.6[1]	Active-RC	0.18	0.58
(Zhang *et al.*, 2008)	1.05	3	1.8	4070	1.99	282.8	45[2]	Gm-C	0.18	20.53
(Carrillo *et al.*, 2010)	0.010	2	1.5	648	0.707	166.1	62.6[3]	Gm-C	0.35	25.18
(Carrillo *et al.*, 2011)	3	2	1.2	382	0.707	636.4	69.6[4]	Gm-C	0.35	0.009
This work- Measured	**0.750**	**5**	**0.5**	**305**	**9.34**	**271.5**	**46.33**[5]	**Active-RC**	**0.18**	**0.202**
(Simulated)	(0.477)			(250)	(5.55)	(271.5)	(50.96[6])			(0.149)

[1]Ratio of input at 100 kHz to integrated input noise for the range 1 kHz-150 kHz
[2]Ratio of input at 1 MHz to integrated input noise for the range 1 Hz-1 MHz
[3]Ratio of input at 1 kHz to integrated input noise for the range 10 Hz-10 kHz
[4]Ratio of input at 1 kHz to integrated input noise for the range 100 Hz-4 MHz
[5]Ratio of input @ 550 kHz to integrated input noise for the range 40 kHz-1 MHz
[6]Ratio of input @ 350 kHz to integrated input noise for the range 40 kHz-600 kHz

3.6 REASON FOR INCREASE IN THE MEASURED BANDWIDTH OF THE FILTER CHIP

The measured bandwidth of the filter is found to be about 750 kHz in contrast to 477 kHz for which the filter is designed. An analysis has been done to find the reason for this deviation and to justify. Following points may be noted with respect to the design.

- No Q tuning loop has been used in the filter which is normally used to fix the time constant of the filter to the desired against the process, voltage and temperature variations.
- The filter also does not use any dedicated servo loop to fix the integrating resistors.

As a first step in the analysis, the possible reasons for increase in the bandwidth are listed. The following may be thought of as possible reasons for increase in the bandwidth.

1. The integrating resistors after fabrication are less than the expected nominal value by a factor of 1.57.
2. The integrating capacitors after fabrication are less than the expected nominal value by a factor of 1.57.
3. Both the integrating resistors and capacitors are less than the expected such that their product is less than the nominal by a factor of 1.57.

Let us consider the first case i.e. all the integrating resistors are decreased by a factor of 1.57 while all the capacitances remain unaltered. In such a case, from the properties of time-scaled electrical networks (Pavan and Tsividis, 2000), the integrated noise should remain unaltered. Also with the decrease in integrating resistors, the load on the OTA increases. This should result in the degradation in the linearity offered by the filter. A comparison of pre and post fabrication results of the filter (Table 2.3 and Table 3.1) reveal that the integrated output noise (mean-squared value) is scaled up by an approximate factor of 2.9 (rms noise increases to 850 μV from 500 μV). Also, the

linearity offered by the filter remains approximately equal as can be seen in Table 3.2. This clearly indicates that increase in the bandwidth seen from the filter chip is not due to any change in integrating resistors; in other words, the integrating resistors in the filter chip are almost same as that expected. This inference also leads to the conclusion that the reason-3 enumerated above (i.e. Both the integrating resistors and capacitors are less than the expected such that their product is less than the nominal by a factor of 1.57) is also not true.

Let us now assume that all the integrating capacitors are decreased by a factor 1.57 while fabricating. If this is the case, then one would expect the integrated noise at the filter output to increase by a factor of approximately 1.57. Also, the filter linearity should not be affected since the load on the OTAs is only decided by the integrating resistors and not by the capacitors. From Table 3.2, the linearity of the filter indeed is not changed after fabrication. By comparing Table 2.3 and Table 3.1, it can be seen that the integrated output noise has been increased by a factor approximately equal to 2.9. The additional factor of 1.8 (i.e. 2.9/1.57) can be attributed to the $1/f$ noise of the filter chip and the peaking of the filter response near the band-edge (Refer Figure 2.25 and Figure 3.9).

From the above analysis it is confirmed that there is a possibility of integrating capacitors being less than what is expected. To validate this, the extracted netlist of the filter is carefully observed. Surprisingly, the extraction tool, while extracting the netlist, is found to extract a parasitic capacitance in parallel to every integrating capacitor (realized using MIM capacitors) of the filter. A detailed information about error in the extracted netlist is given in Appendix E. A consolidation of the extraction error is given in Table 3.3 where the value of five MIM capacitors that are used as integrating capacitors and the corresponding parasitic capacitances extracted (by the tool) in parallel with the MIM capacitors are listed. As can be seen from the table, for every MIM capacitor used as integrating capacitor, a parasitic capacitance of 56% of MIM capacitance is extracted and is found to be independent of the value of MIM capacitor. A 56% of

parasitic capacitance is unlikely to happen in reality.

Table 3.3: MIM capacitor and the extracted parasitic capacitor at the five integrating nodes

Capacitor	**MIM Capacitor** C_{MIM} in pF	**Extracted Parasitic** C_{par} in pF	**Percentage** $\left(\frac{C_{par}}{C_{MIM}} \times 100\right)$
C_1	0.961	0.540	56
C_2	1.700	0.955	56
C_3	1.517	0.856	56
C_4	1.565	0.882	56
C_5	0.742	0.423	57

While design centering the filter in the layout phase, the MIM capacitors are sized such that in the presence of parasitic capacitances, the filter response is indeed the desired. i.e. the total integrating capacitance which takes part in signal filtering includes the MIM capacitor and the 56% parasitic capacitance. If the extraction of this 56% parasitic capacitance by the tool is wrong, the effective integrating capacitances that the filter chip is going to have will be only due to the MIM capacitors; in other words, the integrating capacitance present in each node after fabrication will be 1.56 times smaller than what is expected. This will result in an enhancement of bandwidth by a factor of 1.56 and the same has been observed in the measured filter response.

The measured response is also found to peak near the band edge by about 3.5 dB as can be seen in the Figure 3.7. This can be attributed to the fact that the filter is design centered in presence of parasitics, not only 56% additional capacitance but also the parasitics of OTA and layout. In the absence of parasitics (56%) of MIM capacitors, the frequency response will be de-tuned and will result in Q-enhancement.

To justify both the bandwidth scaling and peaking in the filter response, the extracted netlist of the filter is modified by removing the 56% parasitic capacitance appearing at every integrating node and the response of this modified netlist is obtained. The so obtained response is plotted in Figure 3.11 and compared with the measured response and the design centered filter response before fabrication. It can be seen that with the parasitics removed, the bandwidth scales as expected and the response peaks by about

2 dB. The additional 1.5 dB peaking observed in the measured response is attributed to the secondary effects.

Note that the bandwidth of the filter with MIM parasitics removed is about 3% in excess of the measured response. This is expected since the filter chip will surely have some parasitics across each MIM capacitance and can be inferred that this is about 3%.

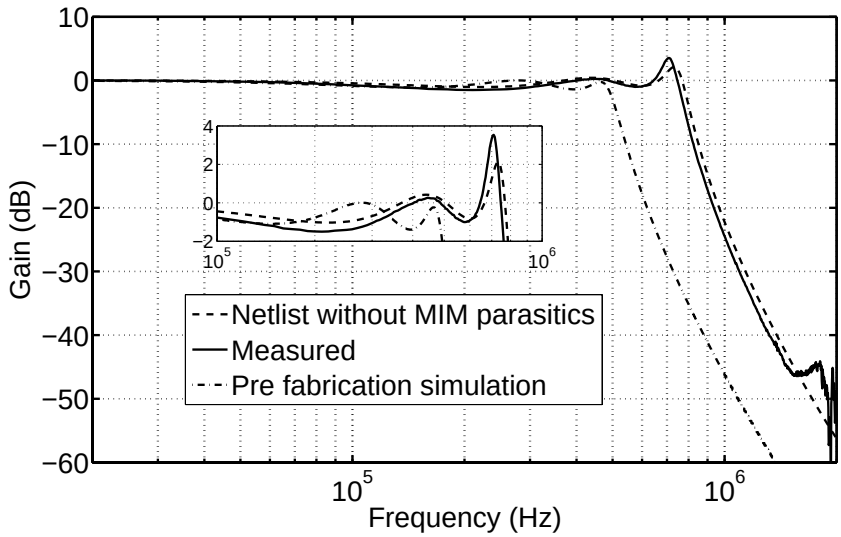


Figure 3.11: Magnitude response of the filter (extracted netlist) with parasitic capacitances, appearing across the integrating MIM capacitors, removed.

CHAPTER 4

STUDY OF THE EFFECT OF PARASITICS OF FEED-FORWARD COMPENSATED OTA ON ACTIVE-RC FILTERS

Parasitic capacitances are inherent to the transistors and layout. These parasitics can affect the frequency response of the filter significantly if they are of the order close to the integrating capacitors. In the case of low voltage circuits, where pseudo differential circuits are preferred, the designers are often forced to use large sized transistors in order to obtain good matching between the transistors; resulting in increased parasitic capacitance. In such cases, there is always a limit on the maximum achievable bandwidth without compromizing on the desired stop band performance.

This chapter analyzes the effect of parasitics of a feed-forward compensated OTA on a first order active-RC low pass filter. The results are then extended to filters of any order.

4.1 ACTIVE-RC INTEGRATOR

Integrator is the basic block of any filter. A lossy integrator can be viewed as a first order filter. Therefore an active-RC integrator is considered for the initial analysis in this chapter. A general schematic of an active-RC integrator is shown in Figure 4.1. Single ended circuit is shown for simplicity. All circuit elements are represented as admittances, in the figure. The admittance y_1 represents the integrating resistor. Admittance y_2 represents the feedback path; a capacitor for an integrator and a combination of capacitor and resistor in parallel for a first order filter. y_a and y_b are the input and

output admittances of the feed-forward OTA appearing due to the parasitic capacitance and resistance at the input and output nodes (nodes ‘a’ and ‘b’ respectively). G_m is the transconductance of the OTA.

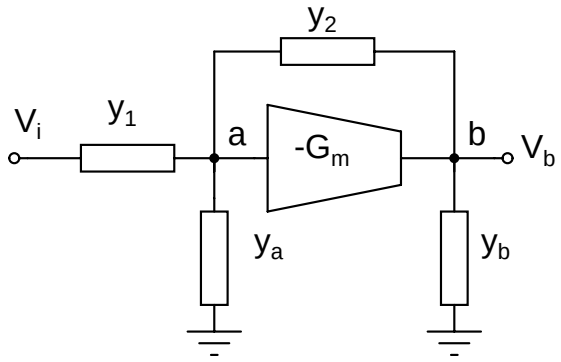


Figure 4.1: Single ended integrator topology

The transfer function of this circuit can be derived as follows. Applying Kirchhoff’s current law, equations for the current at nodes ‘a’ and ‘b’ can be written as in (4.1) and (4.2).

$$V_a y'_a = V_i y_1 + V_b y_2 \tag{4.1}$$

$$V_a(y_2 - G_m) = V_b y'_b \tag{4.2}$$

where y'_a and y'_b are the net admittances at nodes ‘a’ and ‘b’ respectively and are given by following equations.

$$y'_a = y_1 + y_2 + y_a \tag{4.3}$$

$$y'_b = y_2 + y_b \tag{4.4}$$

The OTA considered in this analysis is the feed-forward compensated OTA presented in chapter 2. A single ended equivalent small-signal model of the OTA is re-

drawn in Figure 4.2 for completeness. The effective input capacitance c_a and input resistance r_a of the OTA are absorbed into y_a in Figure 4.1. Similarly, the c_b and r_b are absorbed into y_b. c_{int} and r_{int} represent the impedance at the intermediate node. The effective transconductance G_m (w.r.t. Figure 4.1) of the OTA can be written as in (4.5).

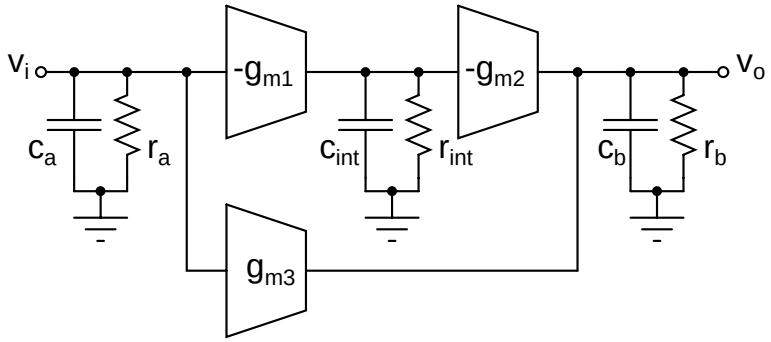


Figure 4.2: Small signal model of the Feed-forward OTA

$$G_m = \frac{g_{m1} r_{int} g_{m2}}{1 + r_{int} c_{int} s} + g_{m3} \tag{4.5}$$

Using the above two equations (4.1) and (4.2), the transfer function of the integrator can be written in the form as in (4.6).

$$\frac{V_b}{V_i} = -\frac{y_1}{y_2}\left[\frac{1}{1 - F(s)}\right] \tag{4.6}$$

where,

$$F(s) = \frac{y'_a y'_b}{y_2(y_2 - G_m)} \tag{4.7}$$

All the variables in (4.6) are functions of complex frequency 's'. If $F(j\omega)$ approaches

zero, then (4.6) reduces to the form shown in (4.8), in the Fourier domain.

$$\frac{V_b(j\omega)}{V_i(j\omega)} = -\frac{y_1(j\omega)}{y_2(j\omega)} \tag{4.8}$$

This is the transfer function of an ideal OTA with $G_m(j\omega)$ tending to infinity. So, we can denote $1/(1 - F(j\omega))$ as a non-ideality factor (NIF) which must approach to one or in other words $F(j\omega)$ must be negligible compared to unity. It is clear that $F(j\omega)$ is frequency dependent which in-turn is decided by y_a, y_b and G_m. Therefore for a given OTA, there is a range of frequency over which the integrator can be expected to work satisfactorily.

4.2 FIRST ORDER LOW PASS FILTER AND MATHEMATICAL ANALYSIS

The analysis put forward in the last section can be directly applied to a first order active-RC filter. A single ended schematic of the filter with unity passband gain is shown in Figure 4.3. OTA parasitics are not shown for simplicity. The filter is designed for a cut-off frequency of 380 kHz (assuming ideal filter), with R = 290 kΩ and C = 1.44 pF. The only reason for choosing these values is that for the fifth order active-RC filter presented in chapter 2, the first stage is a first order low pass filter if the feedback from the second stage is not considered. The values of R and C are from the design centered filter.

The ideal transfer function of the filter is as given in (4.9).

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1}{1 + j\omega CR} \tag{4.9}$$

Knowing the parasitics of OTA obtained using simulations (as explained in chapter 2), NIF can be easily computed using the MATLAB. The magnitude and phase of the

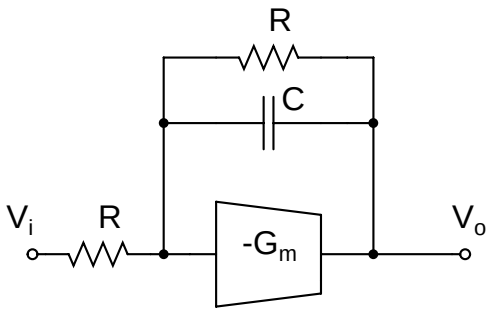


Figure 4.3: Single ended schematic of the low pass filter

NIF for the first order filter are plotted in Figure 4.4. Ideally one needs $|NIF|$ = 1 and phase of (NIF) = 0. In Figure 4.4, it can be seen that it is not so and is frequency dependent. At DC, NIF is not unity (about 0.978 i.e. -0.185 dB). This error is due to the finite DC-gain of the transconductors and is not a serious issue since it is only going to scale the magnitude response of the filter without affecting the phase response. At low frequencies, both magnitude (in dB) and phase of NIF are observed to be flat and almost same as that for DC. For frequency beyond 1 MHz, $|NIF|$ is found to increase and is highly frequency dependent. Similarly in the phase plot of NIF, the phase is close to zero at low frequencies. At 1 MHz, the excess phase lag introduced by NIF is about 3° and is found to increase for frequencies beyond 1 MHz.

To validate this analysis, the transistor level first order filter is simulated, the response of which is plotted in Figure 4.5. It can be clearly seen that the transistor level filter response too is in deviation beyond 1 MHz justifying the mathematical analysis.

This mathematical analysis, also strongly supports the frequency response of the fifth order Chebyshev filter presented in chapter 2. In the magnitude response of the simulated fifth order filter shown in Figure 2.21, it can be clearly seen that the magnitude response deviates from the ideal beyond 1 MHz. Thus it is clear that if the filter is to be designed for a given frequency range, then the OTA needs to be designed such that its parasitics have minimum effect on the filter response. Or for a given OTA and the distortion performance, there is always a limit on the maximum bandwidth of the filter that can be realized using that OTA.

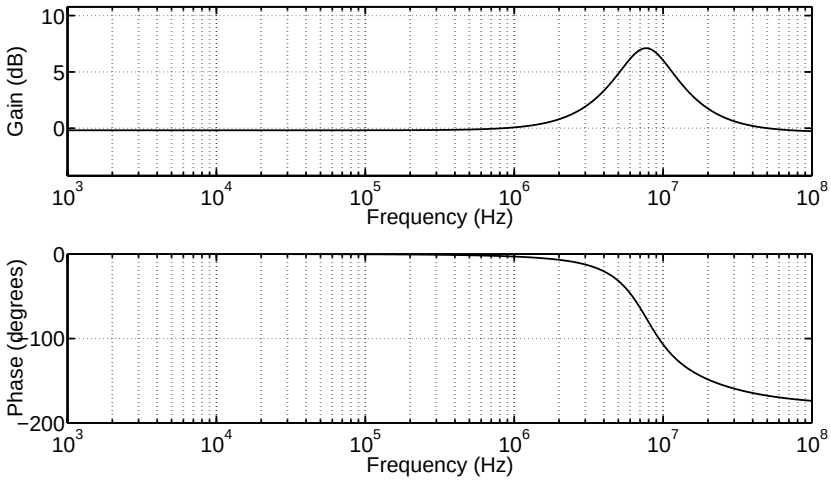


Figure 4.4: Plot of NIF as a function of frequency

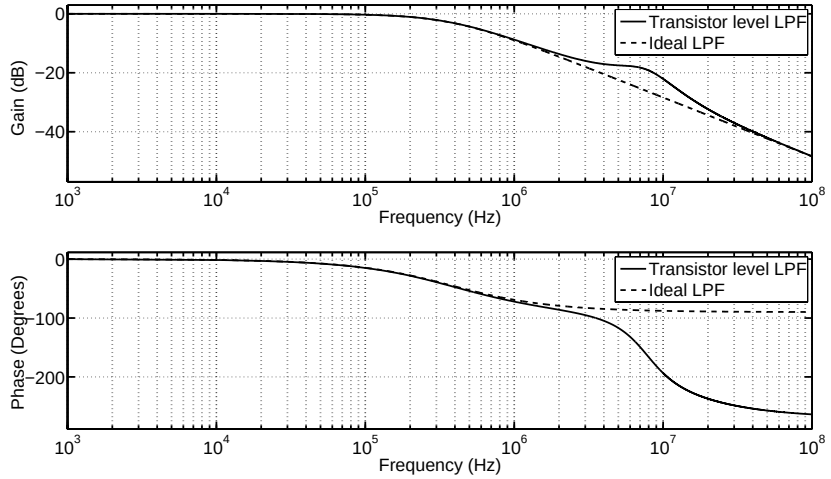


Figure 4.5: Frequency response of the first order filter

4.3 GENERALIZATION

This section tries to generalize the mathematical analysis for active-RC filters built using feed-forward OTA. Here, the OTA is assumed to be an independent entity being i.e. it is assumed that the OTA has been already designed in accordance with the power requirements and distortion performance requirements (selection of the bias current and transconductance). It is also assumed that the transistors of the OTA are sized for the

desired transconductance and the matching requirements. With this assumption, capacitors, resistors and the transconductors of the OTA (referring to the Figure 4.2) are fixed. Therefore, the designer now has to find the maximum bandwidth of the filter that can be realized. The maximum filter bandwidth that can be realized depends on the desired bandwidth, order of the filter and the desired stop-band performance of the filter. The Figure 4.6 highlights this statement.

In the Figure 4.6, ω_{NIF} represents the frequency beyond which the NIF is considered to affect the filter response. $H_{min,1}$ and $H_{min,2}$ indicate the desired stop band attenuation performance for the two cases. Considering $H_{min,1}$, the maximum realizable bandwidth for a first order filter n =1 is smaller than for n =2. For a given order the maximum realizable bandwidth reduces with decrease in H_{min} (increase in the stop-band attenuation). The maximum realizable bandwidth for a given ω_{NIF}, order n and H_{min} can be approximated to (4.10).

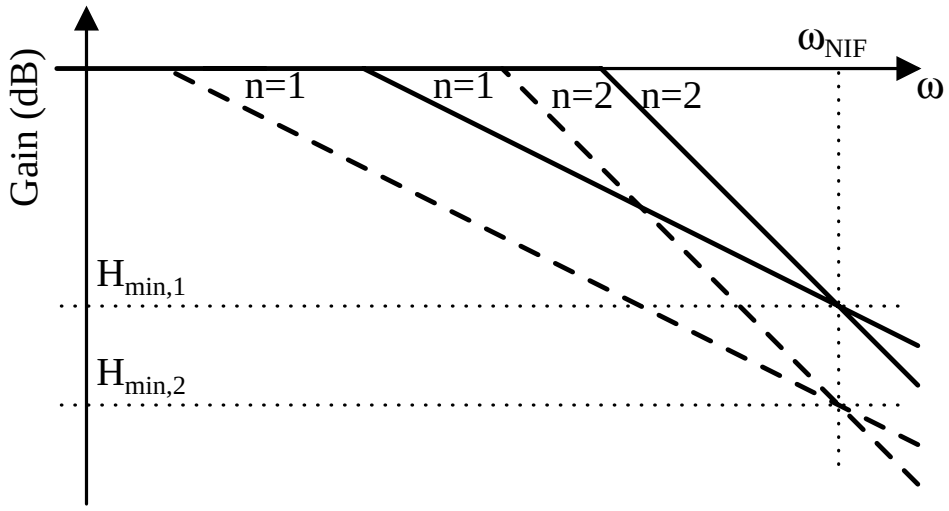


Figure 4.6: Maximum realizable filter bandwidth for a given OTA

$$\omega_{o,max} \approx \omega_{NIF} \times 10^{(H_{min}/20n)} \tag{4.10}$$

If the OTA is designed for a given distortion performance, the load on the OTA cannot be increased/scaled without the increase in power. This implies that the integrating

resistors of the filter are fixed. Therefore, if ω_{NIF} is estimated using the equations outlined in the section 4.1, the achievable filter bandwidth can be estimated using (4.10). However, it is interesting to see that, strictly, ω_{NIF} is in turn a function of $\omega_{o,max}$. This is because, ω_{NIF} is a function of integrating capacitor and resistor. One simple solution would be to estimate ω_{NIF} assuming that the integrating capacitor is of the order of parasitic capacitors i.e. $C = max(c_a, c_b)$ or smaller. This will give a good estimate for ω_{NIF} from which the $\omega_{o,max}$ can be computed. With the design centering process in place there is a scope for tuning the response atleast to some extent if not to a large extent.

The next chapter proposes a few common-mode feedback circuits for low voltage transconductors.

CHAPTER 5

LOW POWER CMFB CIRCUITS FOR PSEUDO DIFFERENTIAL TRANSCONDUCTOR

For fully differential active-RC filters, it is required that the common-mode DC of each integrating node be kept at a reference value. This is important, since it avoids unnecessary inter-node direct currents. Since, the output of the OTAs form the integrating nodes of the filter, the common-mode DC can be set by setting the output common-mode of OTAs. CMFB circuits are commonly used for this task.

A block diagram of a CMFB circuit used for a fully differential amplifier is shown in Figure 5.1 (Pramod and Laxminidhi, 2010). Common mode output voltage of the differential amplifier is sensed and averaged by a common-mode detector. Detected common-mode $(V_{cm,d})$ is compared with the common-mode reference voltage $(V_{cm,ref})$ using an error amplifier. Amplifier error is used to adjust the bias currents of the transistors, through a negative feedback action, in the differential amplifier and hence the common-mode voltage is maintained.

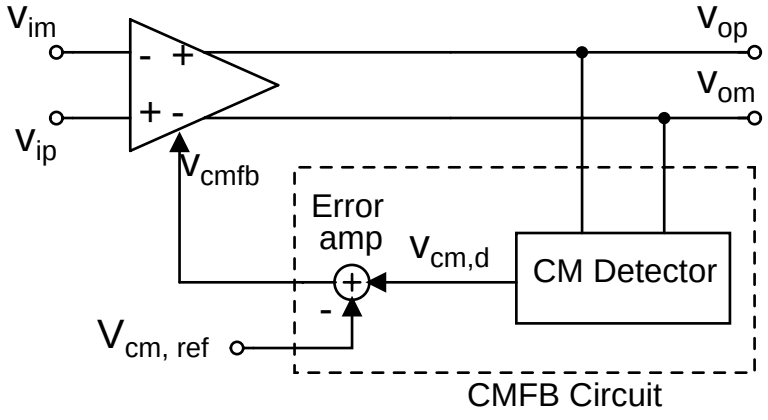


Figure 5.1: Block diagram of a fully differential amplifier with CMFB circuit

This chapter proposes a few CMFB circuits for pseudo differential bulk-driven transconductors to be operated on power supplies as low as 0.5 V. Though there are a few number of common-mode feedback circuits available in literature, they are suited only for circuits having sufficient voltage headroom. Therefore, it is found that there is a need for effective and efficient common-mode feedback circuits for low voltage applications. A total of four CMFB circuits are proposed in this chapter. The proposed circuits are power efficient and offer high input impedance. The circuits are designed and characterized on a 180 nm standard CMOS technology node from UMC and they are tested for a bulk driven pseudo differential transconductor presented in section 2.1 of chapter 2.

5.1 PROPOSED CMFB CIRCUITS

5.1.1 CMFB circuit I

Figure 5.2 shows the proposed circuit I. It is a very simple circuit to maintain common-mode voltage level. In Figure 5.2, v_{om} and v_{op} are the inputs to the CMFB circuit which come from the outputs of the transconductor. The transistors M_a and M_b convert the output voltages v_{op} and v_{om} to proportional currents. The sum of the drain currents of M_a and M_b is sensitive only to the output common-mode voltage of the transconductor. This current is mirrored at the drain of the transistor M_e using the current mirror formed by transistors M_d and M_e. Transistor M_c is driven by the common-mode reference voltage ($V_{cm,ref}$). The size of this transistor is made double of that of M_a and M_b so that the drain current of it equals the sum of drain currents of M_a and M_b. At the node V_{cmfb} (output node of the CMFB circuit), the drain current of M_c is compared with that of M_e. Any error between them, will generate a voltage V_{cmfb} which biases the NMOS loads of the transconductor (refer Figure 2.3), thus closing the loop. The negative feedback loop will act in such a way as to make the output common-mode

voltage of the transconductor equal to the common-mode reference voltage, $V_{cm,ref}$. The capacitor C_c and resistor R help to stabilize the common-mode loop.

When a differential signal along with the common-mode signal is applied to the inputs, depending on the magnitude of the differential signal, one of the transistors conducts more and the other conducts less by an approximately equal amount. Thus sum of the drain currents remains approximately equal to that in the case when only the common-mode input signal is applied.

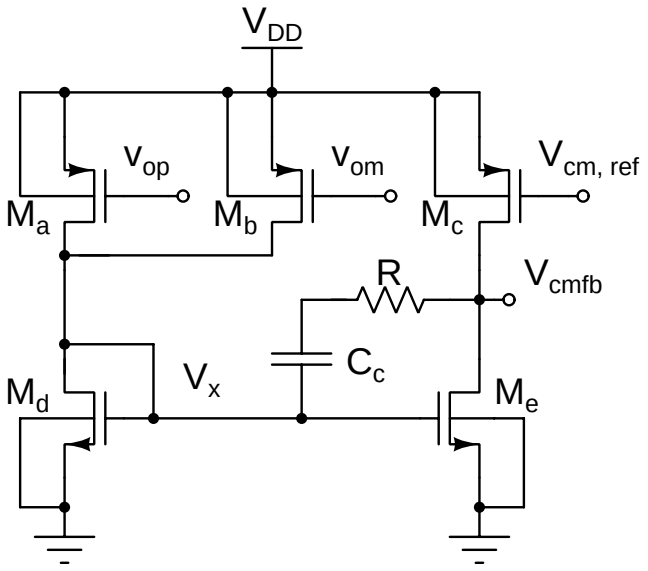


Figure 5.2: CMFB circuit I

Although the circuit I is very simple, it suffers from channel length modulation effect since it is operating on 0.5 V supply. A careful observation of this circuit along with the transconductor (in Figure 2.3) used in this work, reveal the following.

- For the transconductor in Figure 2.3, V_{cmfb} required at the gates of M_3 and M_4, to keep the output common-mode to $V_{cm,ref}$ (=0.25 V), is found to be as close as to 0.35 V which is in excess of 0.25 V.
- In Figure 5.2, the voltage V_x is found to be less than V_{cmfb} since M_a and M_b are operating in sub-threshold region. This results in an error in voltage to current conversion between $M_{a/b}$ and M_c and also results in mirroring error between the drain currents of M_d and M_e.

A systematic analysis to quantify the common-mode error resulting due to the mismatch in current mirror can be given as follows.

Drain currents of NMOS and PMOS transistors operating in sub-threshold region can be written in the form shown in (5.1) and (5.2)

$$I_n = A_n e^{C_n(V_{GS,n}-V_{TH,n})}(1-e^{-BV_{DS,n}}) \tag{5.1}$$

$$I_p = A_p e^{C_p(V_{SG,p}-|V_{TH,p}|)}(1-e^{-BV_{SD,p}}) \tag{5.2}$$

where,

$$A_{n/p} = \mu_{n/p} C_{ox} \left(\frac{W}{L}\right)_{n/p} (m-1)\left(\frac{kT}{q}\right)^2 \tag{5.3}$$

$$B = \frac{q}{kT} \tag{5.4}$$

$$C_{n,p} = \frac{q}{mkT} \tag{5.5}$$

m is the body-effect coefficient and its value lies between 1.1 and 1.4 (Taur and Ning, 1998).

For current mirror formed by transistors M_d and M_e in Figure 5.2, the ratio of their drain currents can be written, using (5.1) and (5.2), in the form,

$$\frac{I_d}{I_e} = \frac{1-e^{-BV_x}}{1-e^{-BV_{cmfb}}} \tag{5.6}$$

Similarly, the ratio of sum of the drain currents of M_a and M_b to the drain current of M_c can be written as follows.

$$\frac{I_a}{I_c} = e^{C_p(V_{cm,ref}-V_{cmo})}\frac{1-e^{-B(V_{DD}-V_x)}}{1-e^{-B(V_{DD}-V_{cmfb})}} \tag{5.7}$$

Here, it is assumed that the output common-mode settles to a value V_{cmo} instead of desired $V_{cm,ref}$. In steady state, the ratios in (5.6) and (5.7) are equal. Therefore, equating the two equations and defining the output common-mode error $V_{cm,error}$ as $V_{cm,ref}$ -

V_{cmo},

$$V_{cm,error} = \frac{1}{C_p} ln \left[\frac{1 - e^{-BV_x}}{1 - e^{-BV_{cmfb}}} \times \frac{1 - e^{-B(V_{DD} - V_{cmfb})}}{1 - e^{-B(V_{DD} - V_x)}} \right] \tag{5.8}$$

It can be seen that, the common-mode error largely depends on error between V_x and V_{cmfb}. If V_x is made approximately equal to the desired V_{cmfb} by some means, the systematic error resulting out of the inaccurate mirroring can be minimized to a large extent. The CMFB circuit II, presented in the next sub-section attempts to do this job.

5.1.2 CMFB circuit II

CMFB circuit II shown in Figure 5.3 is a modified version of circuit I and attempts to minimize the effect of channel length modulation. The negative feedback loop formed between the transistors M_d, M_f and M_g generate the voltage V_x to bias the transistors M_d and M_e. The transistor M_f is sized carefully so as to adjust V_{GS,M_f} such that V_y (=$V_x + V_{GS,M_f}$) becomes approximately equal to V_{cmfb}. This arrangement minimizes the mirroring error and hence the output common-mode error.

Similar to circuit I, when a differential signal along with the common-mode signal is applied to the inputs, sum of the drain currents of M_a and M_b remains approximately equal to that with only common-mode input signal.

5.1.3 CMFB circuit III

In the circuits I and II, ideally, it is assumed that the linearity of the transconductor is not affected by the CMFB circuit. But the currents generated by transistors M_a and M_b do not cancel each other when a differential signal is applied to the transconductor, thereby reducing the linearity of the transconductor. CMFB Circuit III, shown in Figure 5.4, attempts to mitigate this problem by suitably modifying the circuit II. CMFB cicuit III uses an additional circuit formed by transistrors M_{h-n}. Transistors M_{h-l} complement the original circuit (formed by transistors M_{a-e}) by offering NMOS input for

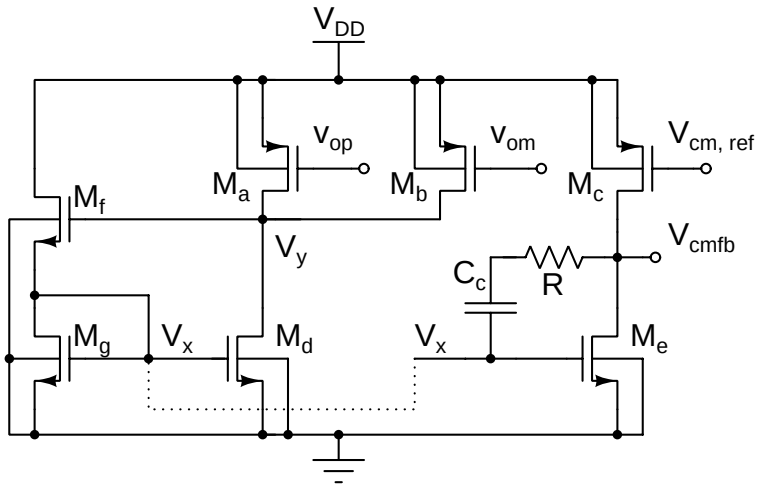


Figure 5.3: CMFB circuit II

the common-mode detection and attempt to cancel the effect of differential signal on the common-mode detection. Transistors M_m and M_n are used to minimize the effect of channel length modulation on common-mode detection and current mirroring error.

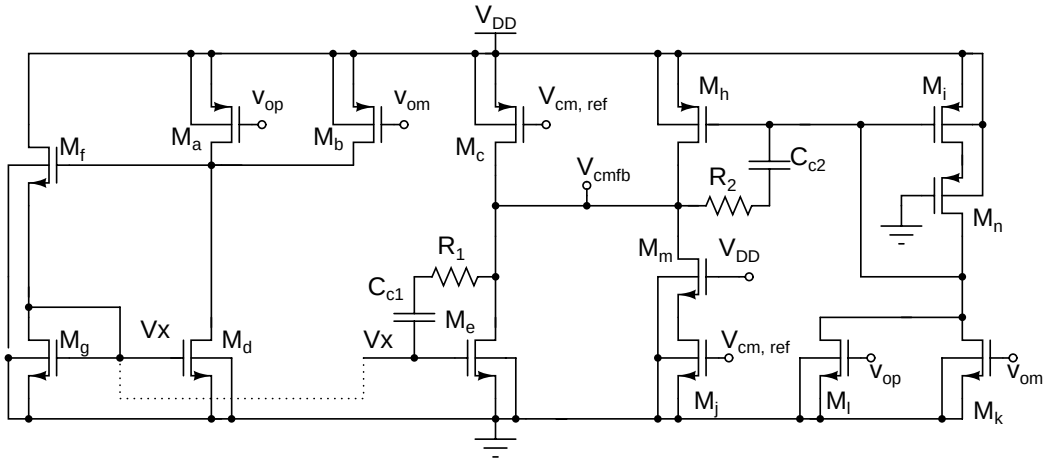
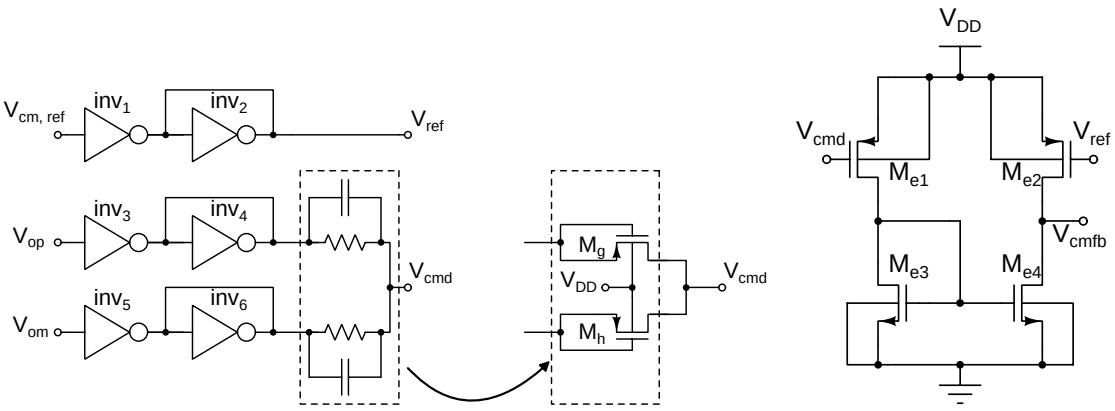


Figure 5.4: CMFB circuit III

5.1.4 CMFB circuit IV

Circuit IV shown in Figure 5.5 uses a different approach as compared to the circuits I-III discussed in earlier subsections. The approach uses CMOS inverters to detect output common-mode of the transconductor.



(a) Common mode detector (b) Error amplifier

Figure 5.5: CMFB circuit IV

inv$_3$-*inv*$_6$ along with transistors M_g and M_h form the common-mode detector. Inverters 3 and 5 are the common-mode sensing inverters and offer capacitive impedance for the transconductor. Inverters 4 and 6 have their outputs shorted to inputs. The arrangement reduces the gain of the common-mode circuit approximately to unity. This enhances the linearity of the sensing circuit and the entire CMFB circuit. Transistors M_g and M_h along with the capacitor form the average detector. The arrangement of M_g and M_h offer high resistance making the average detector predominantly capacitive. The common-mode voltage V_{cmd} detected at the common-drain node of M_g and M_h is compared with the reference, formed by inverters 1 and 2, using a simple error amplifier shown in Figure 5.5(b). The error amplifier output is fed back to the transconductor to complete the negative feedback loop. The loop acts in such a way as to set the output common-mode equal to the reference $V_{cm,ref}$.

5.2 SIMULATION RESULTS

The four proposed CMFB circuits are validated with the same pseudo differential bulk driven transconductor explained in section 2.1.

Figure 5.6 shows the performance of the proposed CMFB circuits for variation in temperature in the range 0 to 70°C. The following observations can be made.

- As expected CMFB II offers a lower common-mode error (≈1 mV) when compared to CMFB I (≈5 mV). Thanks to improved mirroring accuracy made possible by transistors M_f and M_g in Figure 5.3. CMFB III is found to have higher accuracy with error less than 0.5 mV.
- CMFB I, II and III offer a common-mode voltage almost independent of temperature.
- The common-mode error in case of CMFB IV is approximately 2.5 mV - 3.5 mV.

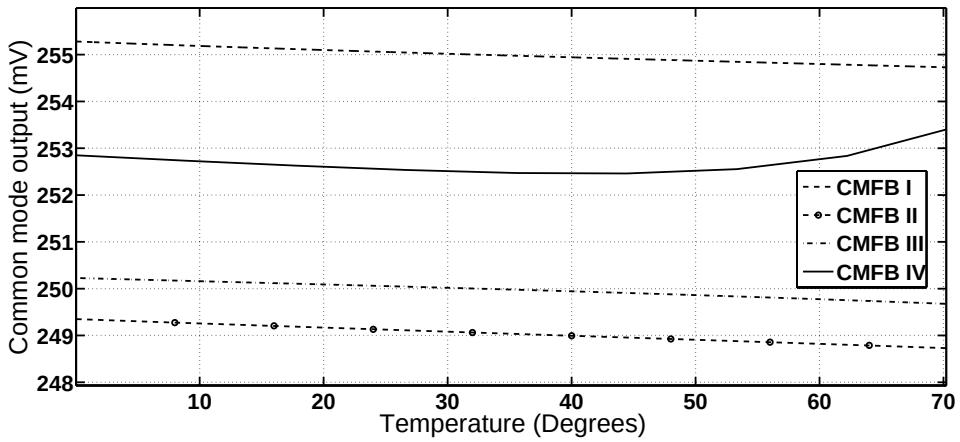
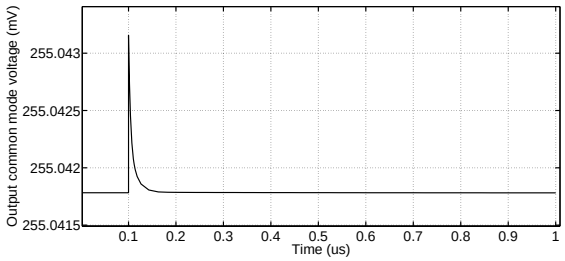


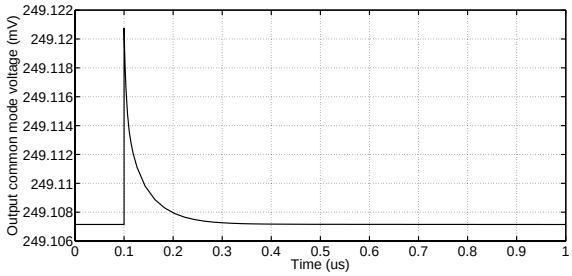
Figure 5.6: Variation of Common mode voltage with temperature

Figure 5.7 shows stability of the common-mode loop of four CMFB circuits for common-mode perturbation. The loops of all the circuits are made stable by the appropriate choice of compensating capacitors and resistors.

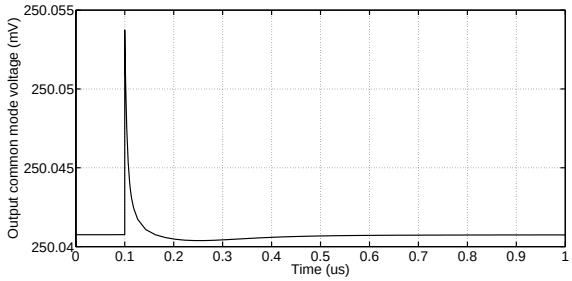
In Figure 5.8, the input admittance offered by the common-mode detector is plotted as a function of frequency in linear scale. It can be seen that the proposed circuits load the outputs of the transconductor capacitively for a wide frequency range as is evident from the straight line nature of graphs. The capacitance (C_{in} = slope/2π) offered by the proposed circuits is the order of femto farads. The values are listed in Table 5.1. CMFB III offers higher input capacitance (approximately two folds) compared to other three circuits. This is because the input of the CMFB III has NMOS transistors in



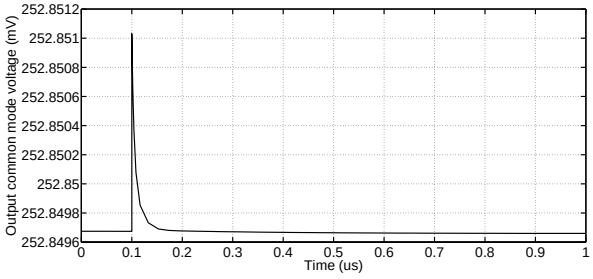
(a) CMFB I



(b) CMFB II



(c) CMFB III



(d) CMFB IV

Figure 5.7: Stability of common-mode loop for common-mode perturbation.

addition to PMOS transistors. It is to be noted that with a proper resizing of transistors, the capacitance offered by CMFB III can also be made close to that of other CMFB circuits.

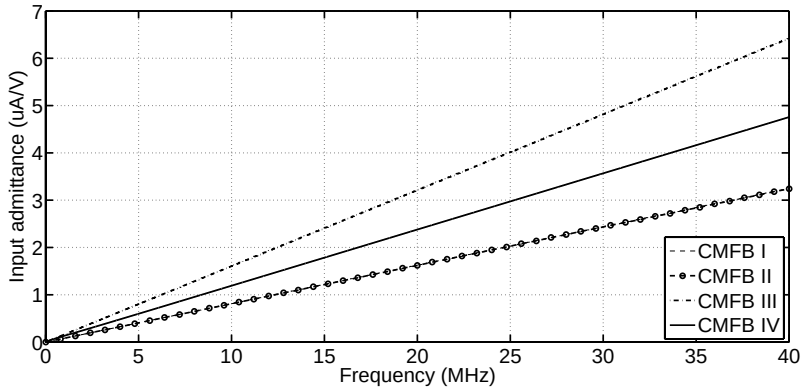


Figure 5.8: Input admittance of CMFB circuits as a function of frequency.

Figure 5.9 throws light on the effect of CMFB circuits on the linearity of the transconductor. Here, the differential output voltage of the transconductor is plotted as a function of differential input voltage in the presence of proposed CMFB circuits. As outlined in section 5.1.3, CMFB I and II are found to degrade the linearity of the transconductor while with CMFB III, the linearity is found to be improved. It can also be seen that the transconductor operated with CMFB IV has higher linearity compared to that with the other three circuits.

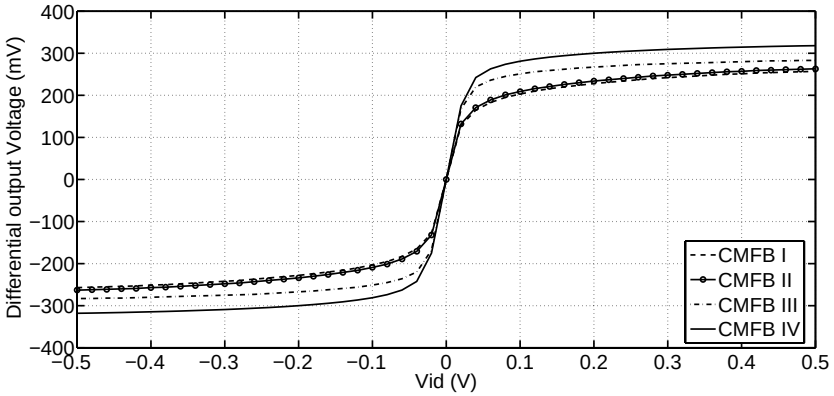


Figure 5.9: Differential output voltage versus differential input voltage

Figure 5.10 shows the time domain response showing the range of variation of the common mode output as a function of differential output for a frequency of 100 kHz. In this test, the output peak-to-peak voltage of all the transconductors are fixed at 200 mV by suitably adjusting the input peak-to-peak voltage. It is seen that CMFB I, CMFB

II and CMFB IV circuits offer very good performance with minimum common-mode variations (8.2, 6 and 7.8 mV peak-to-peak respectively) with an average common-mode close to the desired 250 mV. However, CMFB III is found to have about 30 mV peak to peak variation in common-mode which is high when compared to other circuits. This can be attributed to the fact that the circuit is bringing in the linearity by adjusting the output common-mode voltage. The reason for the observed common-mode variations with the differential output in all the four proposed circuits is that the loop gain of the common-mode loop is a function of the differential voltage. A robust common-mode loop that is independent of differential output is required to improve the common-mode behaviour.

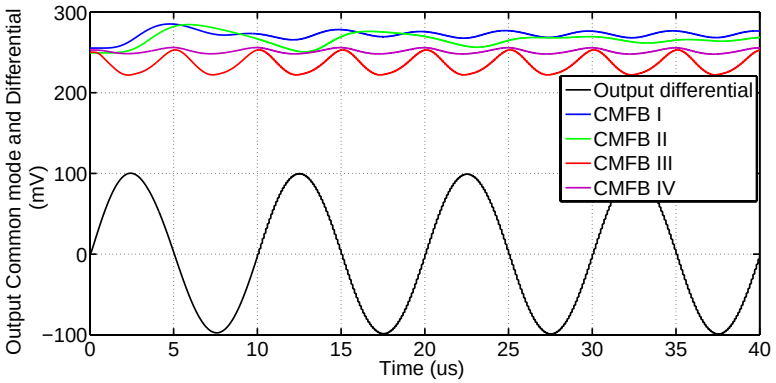


Figure 5.10: Time domain response showing the range of variation of common mode output as a function of differential output

Table 5.1 tabulates the power consumption of the proposed CMFB circuits and the capacitance offered by them. Note that, when compared to the power of the transconductor (10 μW) the power requirement on the common-mode circuit is found to be negligible.

DC analysis of the transconductor is performed for various process corners with the proposed CMFB circuits. Table 5.2 tabulates the common-mode output voltage of the transconductor over different process corners. All the proposed circuits are found to offer consistent performance across corners at nominal temperature and 0.5 V supply.

Table 5.1: Performance of proposed circuits

Circuit	**Power (nW) (CMFB)**	C_{in} **(fF)**
CMFB I	4	13
CMFB II	5	13
CMFB III	50	26
CMFB IV	41	19

Table 5.2: Performance of proposed circuits over different process corners

Circuit	**tt**	**ss**	**ff**	**snfp**	**fnsp**
CMFB I	255.3	256.1	254.6	254.9	255.8
CMFB II	249.3	249.9	248.8	237.4	251
CMFB III	250.2	250.5	250.1	248.4	250.7
CMFB IV	252.8	253.7	252.2	253.4	252.5

CHAPTER 6

ACTIVE-RC FILTERS USING CMOS INVERTERS

Active-RC filters demand a large DC gain for the OTAs if the filter DC gain is required to be close to ideal. Higher the DC gain, better will be the matching of the filter response to the ideal in the frequency range of interest. There are many techniques available in the literature which are targeted to increase the DC gain of the transconductors. A few of the gain boosting techniques such as cascode, folded-cascode are common for realizing high gain transconductors/OTAs. Also, a negative resistor based approach using a controlled positive feedback has also been found to be useful in increasing the DC gain. All such approaches are well suited for circuits where there is a sufficient voltage headroom. However, circuits operating on low supply voltages lack the necessary headroom for any cascode arrangement specially when using standard CMOS process. The designers are forced to use pseudo-differential architecture.

For a pseudo-differential transconductor with PMOS input, only PMOS transistors take active part in voltage to current conversion. The NMOS transistors act only as current sources. This results in a transconductor DC gain of $g_{mp}(r_{op}||r_{on})$, where g_{mp} is the transconductance (gate/body depending on where the input is connected) of the PMOS transistor, r_{op} and r_{on} are the output resistance of PMOS and NMOS transistors respectively. Similarly for the transconductor with NMOS input transistors, the DC gain will be $g_{mn}(r_{op}||r_{on})$. One method to improve the DC gain of the transconductor is to make both the NMOS and PMOS transistors to actively take part in the signal amplification, which means that tying the signal to both NMOS and PMOS transistors. This converts each leg of the pseudo-differential transconductor to CMOS inverters. Such a technique is first introduced by Nauta in (Nauta, 1992) where, he demonstrated a realization of $G_m - C$ filter using CMOS inverters. He also presents an approach to

enhance the common-mode rejection of transconductor by using a negative-resistance technique. However, the filter designed in 3 μm CMOS process had a leisure of sufficient headroom as it is operated on 10 V supply.

In this research, a feed-forward compensated OTA has been proposed using CMOS inverters for low supply voltage operation down to 0.5 V on a 180 nm standard CMOS process. The proposed OTA is used to realize a fifth order active-RC Chebyshev filter. The transistors in this work operate in sub-threshold region unlike those in (Nauta, 1992) where they are operated in strong-inversion region. A mathematical analysis has been carried out to justify the applicability of the transistors in such an architecture when the transistors are operated in sub-threshold region. The design is also extended to 90 nm CMOS process where a biquad filter has been designed.

6.1 CMOS INVERTER BASED TRANSCONDUCTOR

Schematic of the inverter based differential transconductor is shown in Figure 6.1(a). The architecture is same as that proposed in (Nauta, 1992).

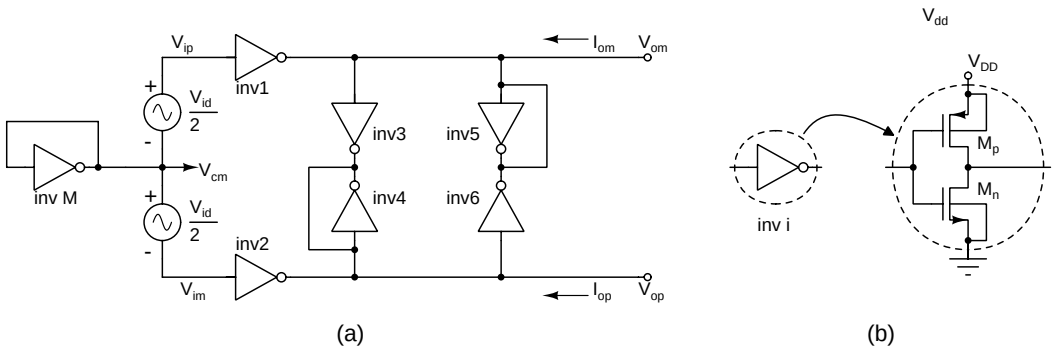


Figure 6.1: (a) Inverter based differential Transconductor (b) CMOS inverter

The inverter $inv\ M$ generates the input common-mode voltage for the transconductor. The input/output common-mode DC voltages are set at V_{DD}/2 i.e. 0.25 V. This inturn is achieved by sizing the NMOS and PMOS of the inverters. Once, the transistor sizes are fixed for $inv\ M$, all other inverters are chosen to have same current density.

Inverters $inv1$ and $inv2$ offer the basic transconductor action. Inverters $inv3 - inv6$ serve three purposes. One, they set the output common-mode DC of the transconductor; second, the arrangement offers a negative resistance at the output for differential signal thus enhancing the DC gain; third, the arrangement offers a low common-mode gain enhancing the common-mode-rejection-ratio (CMRR). A detailed analysis of the transconductor action is presented in the next section.

6.1.1 Transconductor Action

When the CMOS inverter shown in Figure 6.1(b) is operated on a supply (V_{DD}) of 0.5 V, both the PMOS and NMOS transistors will be operated in sub-threshold region. For a PMOS transistor operating in sub-threshold region, the instantaneous drain current $i_{D,p}$ (flowing out of the drain terminal) can be written as in (6.1).

$$i_{D,p} = A_p e^{B_p(v_{SG,p} - |V_{TH,p}|)}(1 - e^{-v_{SD,p}/V_T}) \tag{6.1}$$

where,

$$A_p = \mu_p C_{ox} \frac{W}{L}(m_p - 1)V_T^2 \tag{6.2}$$

$$B_p = \frac{1}{m_p V_T} \tag{6.3}$$

$V_T = kT/q$, the volt equivalent of temperature and m_p is the body-effect coefficient and its value lies between 1.1 and 1.4 (Taur and Ning, 1998). For $v_{SD,p} \geq 4V_T$, the current $i_{D,p}$ can be assumed to be independent of $v_{SD,p}$ i.e. $(1 - e^{-v_{SD,p}/V_T}) \approx 1$ and this is a reasonable assumption if the maximum swing at the output of the inverter is limited to about 150 mV above the common-mode voltage of 0.25 V. Then (6.1) can be simplified to (6.4) as follows.

$$i_{D,p} \approx A_p e^{B_p(v_{SG,p} - |V_{TH,p}|)} \tag{6.4}$$

Under biasing condition, with $v_{SG,p} = V_{SG,p} = V_{DD} - V_{cm}$, the DC bias current

$I_{D,p}$ can be written as in (6.5).

$$I_{D,p} \approx A_p e^{B_p(V_{SG,p}-|V_{TH,p}|)} \tag{6.5}$$

When a small signal voltage $v_{sg,p}$ is applied to the PMOS transistor, the instantaneous drain current $i_{D,p}$ can be obtained using,

$$i_{D,p} \approx I_{D,p}\, e^{B_p v_{sg,p}} \tag{6.6}$$

Using the Taylor series expansion, (6.6) can be approximated to

$$\begin{aligned} i_{D,p} &\approx I_{D,p}\,(1 + B_p v_{sg,p}) && (6.7)\\ &\approx I_{D,p} + I_{D,p} B_p v_{sg,p} && (6.8) \end{aligned}$$

Note that the above approximation is valid iff $v_{sg,p} << \sqrt{2} m_p V_T$. The second term in (6.8) can be considered as the small signal component of the drain current. i.e.

$$i_{d,p} \approx I_{D,p}\, B_p v_{sg,p} \tag{6.9}$$

Thus the small signal transconductance of the PMOS transistor is given by

$$g_{mp} \approx \frac{I_{D,p}}{m_p V_T} \tag{6.10}$$

A similar analysis for NMOS transistor will result in a small signal drain current flowing into the drain terminal as given in (6.11).

$$i_{d,n} \approx I_{D,n}\, B_n v_{gs,n} \tag{6.11}$$

The corresponding transconductance will be

$$g_{mn} \approx \frac{I_{D,n}}{m_n V_T} \tag{6.12}$$

For small signals, $v_{gs,n} = v_{in}$, the input voltage and $v_{gs,p} = -v_{gs,n}$. Also, $I_{D,p} = I_{D,n}$. Therefore, the effective transconductance of the CMOS inverter is

$$\begin{aligned} g_{m,eff} &\approx g_{mn} + g_{mp} && (6.13) \\ &\approx \frac{I_{D,n}}{V_T}\left(\frac{1}{m_n} + \frac{1}{m_p}\right) && (6.14) \end{aligned}$$

Inverters 3-6 in Figure 6.1 are used for controlling the output common mode and for enhancing the DC gain as stated earlier. A small signal equivalent circuit of Figure 6.1 is shown in Figure 6.2 indicating the small signal voltages and currents. Here, g_{mi} represents the effective transconductance of i^{th} inverter. An equivalent model of this figure is shown in Figure 6.3. $Inv4$ and $inv5$ act as resistances connected between the output nodes and the common mode voltage V_{cm}, thus offer small signal resistances $1/g_{m4}$ and $1/g_{m5}$ at the output nodes v_{op} and v_{om} respectively with respect to small-signal ground.

Applying KCL for the circuit in Figure 6.3,

$$i_{om} = g_{m1}v_{ip} - g_{m5}v_{om} - g_{m6}v_{op} \tag{6.15}$$

$$i_{op} = g_{m2}v_{im} - g_{m4}v_{op} - g_{m3}v_{om} \tag{6.16}$$

For common mode signals, (6.15) and (6.16) can be written as follows.

$$i_{om,cm} = g_{m1}v_{icm} - g_{m5}v_{ocm} - g_{m6}v_{ocm} \tag{6.17}$$

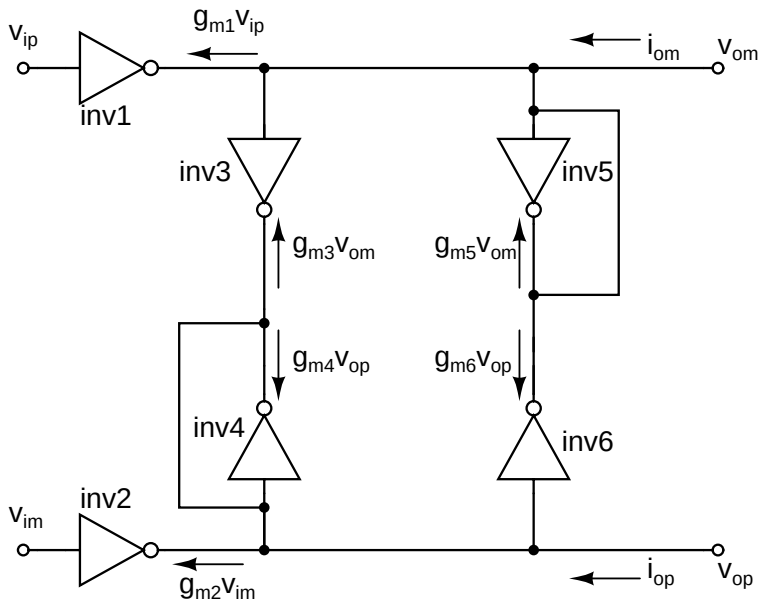


Figure 6.2: Small signal equivalent circuit of Figure 6.1(a).

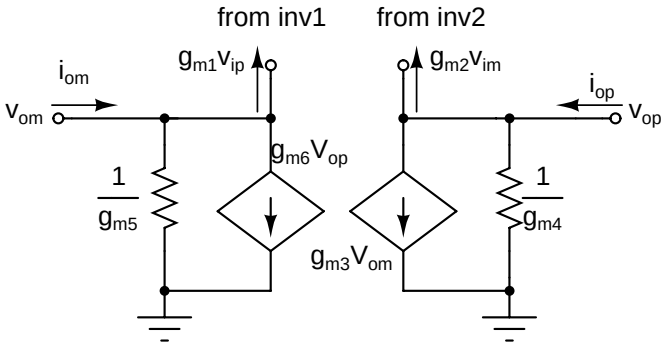


Figure 6.3: Small signal model of the part of the circuit formed by inverters 3-6.

$$i_{op,cm} = g_{m2}v_{icm} - g_{m4}v_{ocm} - g_{m3}v_{ocm} \tag{6.18}$$

where v_{icm} and v_{ocm} are the input common-mode and the output common-mode voltages respectively. From the equations (6.17) and (6.18), it can be seen that v_{om} node is virtually loaded with a resistance $1/(g_{m5} + g_{m6})$ and the v_{op} node is loaded with a virtual resistance $1/(g_{m3} + g_{m4})$ for common-mode signals. If differential-mode signals are considered, since v_{om} = -v_{op}, the output nodes v_{om} and v_{op} are virtually loaded with resistances $1/(g_{m5} - g_{m6})$ and $1/(g_{m4} - g_{m3})$ respectively. If the four inverters are per-

fectly matched, all the g_ms are equal. Thus the network formed by inverters 3-6 offers a low ohmic load for common mode signals and a high ohmic load (ideally infinite) for differential signals there by offering a common-mode rejection at the outputs.

A high ohmic load of the transconductor for differential signal also helps in realizing high DC gain. The DC gain of this transconductor can further be increased by loading the outputs v_{om} and v_{op} with a negative resistance for differential signals. This can be easily achieved by choosing $g_{m3} > g_{m4}$, g_{m5} = g_{m4} and g_{m6} = g_{m3} (Nauta, 1992). The transistors in $inv4$ and $inv5$ are sized smaller than those of $inv3$ and $inv6$ in order to have negative resistance at the output. This results in a DC gain enhancement of 21 dB to 27.78 dB in the transconductor designed in this work. However for an OTA it is necessary to have a sufficiently large DC gain. In (Nauta, 1992), it was suggested that the power supplies of inverters 4 and 5 can be tuned for enhancing the DC gain. This may not be acceptable for low voltage designs especially for designs presented in this work. Therefore, cascading of two transconductors is inevitable and can be easily achieved, thanks to the feed-forward compensation.

6.2 FEED-FORWARD COMPENSATED OTA

Schematic of a fully differential feed-forward compensated OTA realized using CMOS inverters is shown in Figure 6.4. Inverters 1-12 form the differential forward path and inverters 13 and 14 form the differential feed-forward path.

The research proposes active-RC filters using this OTA architecture in two process technologies viz. 180 nm and 90 nm.

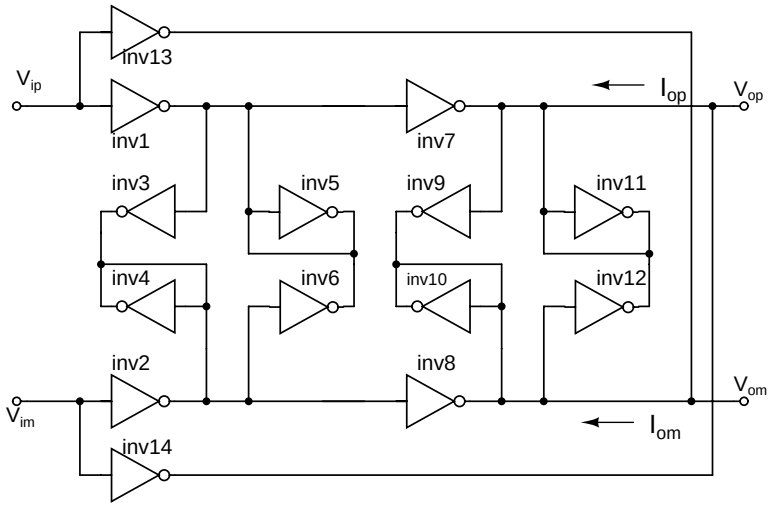


Figure 6.4: Fully differential feed-forward compensated inverter based OTA

6.3 FIFTH ORDER CHEBYSHEV LOW PASS FILTER IN 180 nm CMOS TECHNOLOGY

6.3.1 OTA performance

The OTA is designed in 180 nm CMOS process. The frequency response of the OTA is given in Figure 6.5. It offers an open loop DC gain of 51.3 dB with an UGB of 3.52 MHz. The OTA is stable with a phase margin of 52 °. The performance parameters of the OTA are tabulated in Table 6.1.

6.3.2 Fifth order Chebyshev low pass filter

A fifth order Chebyshev filter with 1 dB pass band ripple is designed using the feed-forward OTA. The bandwidth of the filter was chosen to be 150 kHz. The filter is derived from the singly terminated LC ladder architecture as outlined in chapter 2. A schematic of the filter is shown in Figure 6.6 for the ease of reading. A terminating resistance of 200 kΩ has been used.

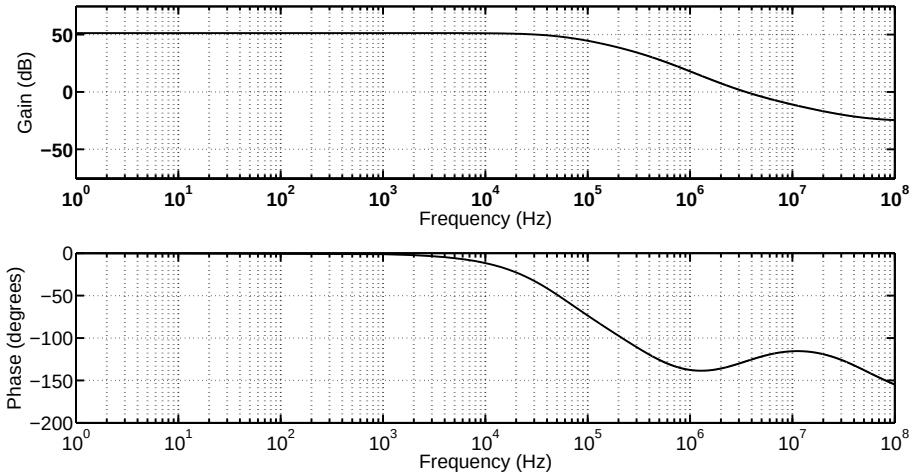
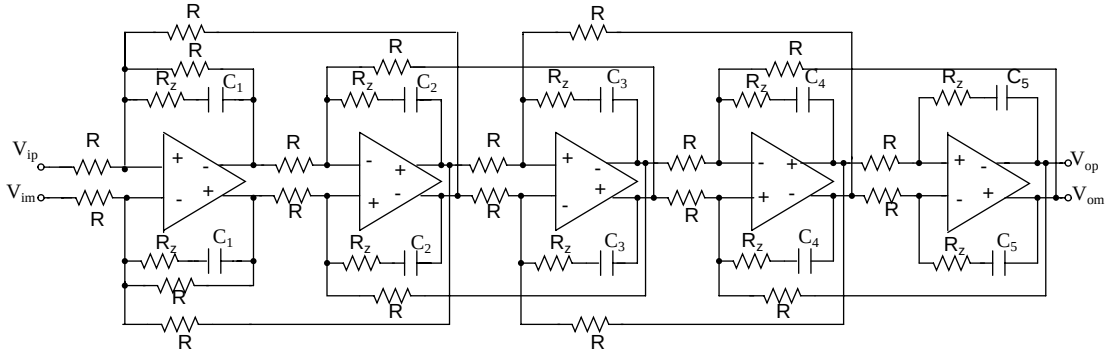


Figure 6.5: Frequency response of feed-forward OTA

Table 6.1: Parameters of the feed-forward OTA

Parameter		**Simulated values of OTA**
Supply [V]		0.5
Open loop DC Gain [dB]		51.30
3 dB Bandwidth [kHz]		52.9
UGB [MHz]		3.52
Phase margin[degrees]		52
Gain margin [dB]		25.5
Power [μW]		4.3
Technology [μm]		0.18
Input referred noise	@ 10kHz	123.36
$[nV/\sqrt{Hz}]$	@ 1MHz	48.29



R = 200 kΩ, R_z = 2.2 kΩ, C_1 = 5.66 pF, C_2 = 7.66 pF, C_3= 10.57 pF, C_4= 8.43 pF, C_5= 8.83 pF

Figure 6.6: Schematic of fifth order Chebyshev filter

6.3.3 Simulation Results

Figure 6.7 shows the frequency response of the transistor level filter and is compared with the ideal response.

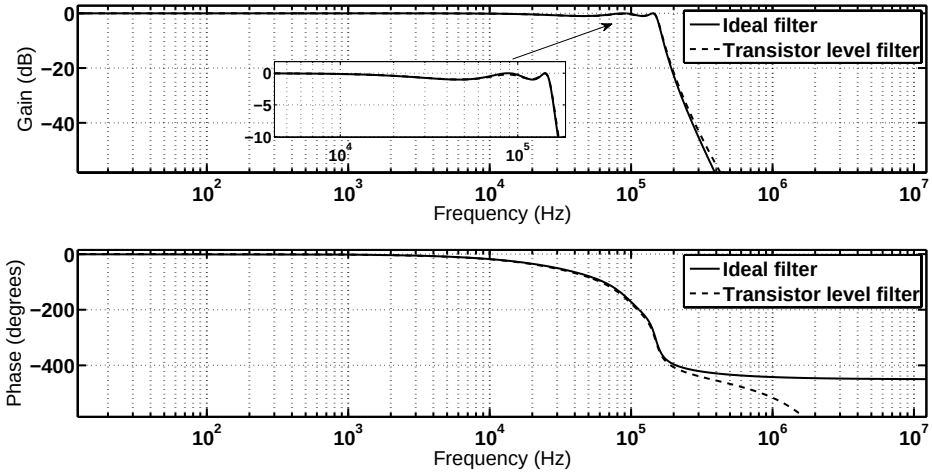


Figure 6.7: Frequency response of the filter

Figure 6.8 shows the integrated output noise of the filter versus frequency. At low frequencies, the output noise is dominated by 1/f noise; the small flat region in the passband of the filter is a result of white noise. The later peaking at around 150 kHz is due to the filter transfer function.

Table 6.2 summarizes the filter parameters. A comparison of performance parameters of the designed filter with other filters found in the literature is given in Table 6.3. The Figure of Merit (FOM) used for comparison is (Laxminidhi *et al.*, 2009) given in section 3.5. Designed filter offers lowest FOM which indicates that the design is energy efficient. Filter consumes 21.79 μW of power and has a dynamic range of 54.16 dB when operating at 0.5 V supply.

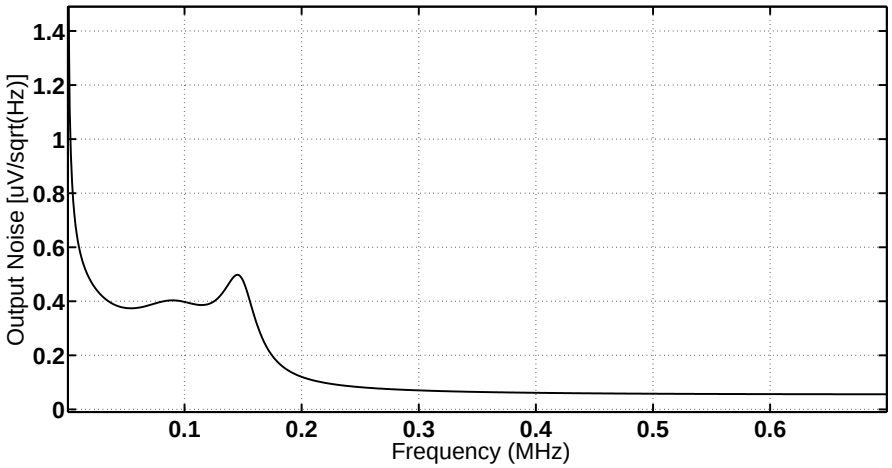


Figure 6.8: Filter output noise

Table 6.2: Parameters of the filter

Supply Voltage	0.5 V
Technology	0.18 μm CMOS
Filter type	5th order Chebyshev low pass
3 dB bandwidth	150 kHz
Power	21.79 μW
Integrated output noise	180.74 μV rms
V_{in-pp} differential for THD$\leq$-40 dB at 50 kHz	316 mV
Dynamic Range for THD=-40 dB	54.16 dB

Table 6.3: Comparison with some published filters

Reference	**Bandwidth [MHz]**	**Order**	**Supply Voltage** [V]	**Power [μW]**	Q_{max}	**Input [mVrms] for 1% THD**	**Dynamic Range[dB] (for THD$\sim$ -40 dB)**	**Topology**	**Tech. [μm]**	**FOM (fJ)**
(Chatterjee *et al.*, 2005)	0.135	5	0.5	1100	6.2	50	56.6[1]	Active-RC	0.18	0.58
(Zhang *et al.*, 2008)	1.05	3	1.8	4070	1.99	282.8	45[2]	Gm-C	0.18	20.53
(Carrillo *et al.*, 2008)	0.0175	2	1	45	0.89	530.3	63.7[3]	Gm-C	0.35	0.606
(Carrillo *et al.*, 2010)	0.010	2	1.5	648	0.707	166.1	62.6[4]	Gm-C	0.35	25.18
(Carrillo *et al.*, 2011)	3	2	1.2	382	0.707	636	69.6[5]	Gm-C	0.35	0.009
(Arya *et al.*, 2013)	0.9705	3	0.5	332	0.707	18.29	63.13[6]	Gm-C	0.13	0.078
This work	**0.150**	**5**	**0.5**	**21.79**	**5.55**	**111.72**	**54.16**[7]	**Active-RC**	**0.18**	**0.02**

[1]Ratio of input @ 100 kHz to integrated input noise for the range 1 kHz-150 kHz
[2]Ratio of input @ 1 MHz to integrated input noise for the range 1 Hz-1 MHz
[3]Ratio of input @ 1 kHz to integrated input noise for the range 1 Hz-18 kHz
[4]Ratio of input @ 1 kHz to integrated input noise for the range 10 Hz-10 kHz
[5]Ratio of input @ 1 kHz to integrated input noise for the range 100 Hz-4 MHz
[6]Ratio of input to integrated input noise for the range 1 kHz-1 MHz
[7]Ratio of input @ 50 kHz to integrated input noise for the range 1 kHz-160 kHz

6.4 SECOND ORDER BIQUAD FILTER IN 90 nm CMOS TECHNOLOGY

To investigate the performance of the proposed CMOS inverter based OTA with the technology scaling, a second order biquad filter is designed in 90 nm CMOS process. The performance of the OTA and the filter are given in this section.

6.4.1 OTA performance

Figure 6.9 shows the frequency response of the feed-forward OTA designed in 90 nm process. The OTA exhibits an open loop DC gain of 61.89 dB, UGB of 1.4 GHz and a phase margin of 52.85 °. Table 6.4 summarizes the parameters of the OTA. It consumes a power as low as 29.91 μW.

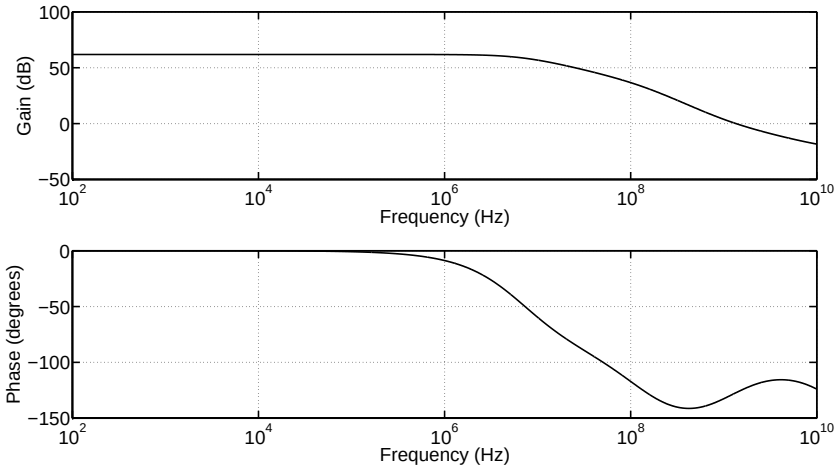


Figure 6.9: Frequency response of feed-forward OTA in 90 nm technology.

6.4.2 Second order Biquad filter

A second order butterworth biquad filter is designed using the feed-forward OTA for a band-edge of 5 MHz. The schematic of the fully differential active-RC filter is shown

Table 6.4: Parameters of feed-forward OTA.

Parameter		Simulated values of OTA
Supply [V]		0.5
Open loop DC Gain [dB]		61.89
3 dB Bandwidth [MHz]		6.78
UGB [MHz]		1357
Phase margin[degrees]		52.85
Gain margin [dB]		24.8
Power [μW]		29.91
Technology [μm]		0.09
Input referred noise	@ 100kHz	83.76
$[nV/\sqrt{Hz}]$	@ 10MHz	19.46

in Figure 6.10. Resistors and capacitors are the integrating resistances and integrating capacitances and their values for the desired band-edge are also given in the figure. The filter is laid out and a snap-shot of the same is shown in Figure 6.11.

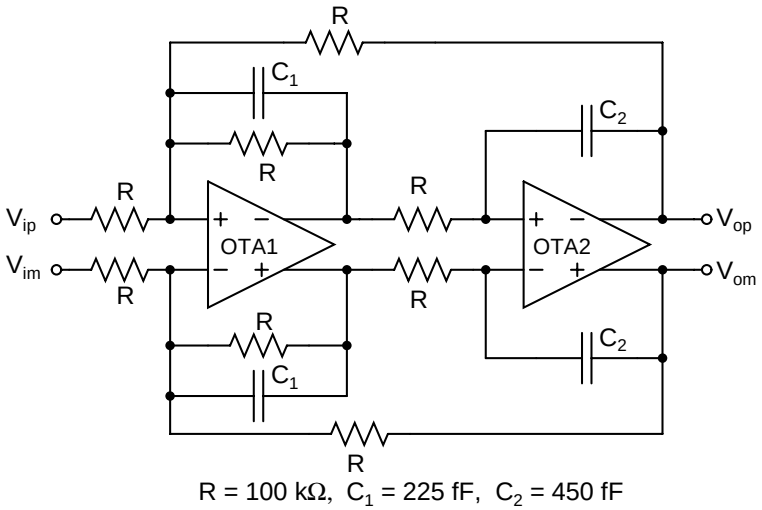


Figure 6.10: Schematic of Biquad filter.

6.4.3 Frequency Response and parameters of the biquad filter

Figure 6.12 shows the magnitude response of the layout extracted filter. The response indicates that a second order filter of 5 MHz bandwidth is realizable even with sub-

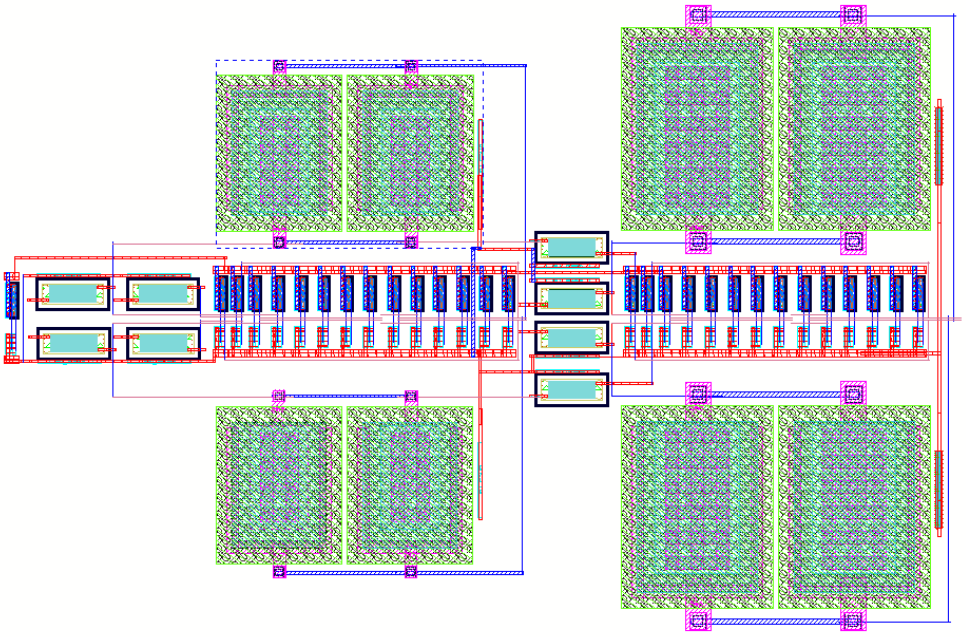


Figure 6.11: Layout of Biquad filter

threshold operation and operating on 0.5 V. Filter consumes 58.76 μW of power and has a dynamic range of 55.78 dB. Table 6.5 summarizes the filter parameters. A comparison of performance parameters of the designed filter with other filters found in the literature is given in Table 6.6. It can be noted that this filter has the highest bandwidth among similar filters operating on 0.5 V supply and has been achieved without the loss of FOM.

Table 6.5: Parameters of the filter

Supply Voltage	0.5 V
Technology	0.09 μm CMOS
Filter type	2nd order low pass biquad
3 dB bandwidth	5 MHz
Power	58.76 μW
Integrated output noise (in the range 50 kHz-10 MHz)	358.8 μV rms
V_{in-pp} differential for THD$\leq$-40 dB at 1.6 MHz	632 mV
Dynamic Range for THD=-40 dB	55.78 dB

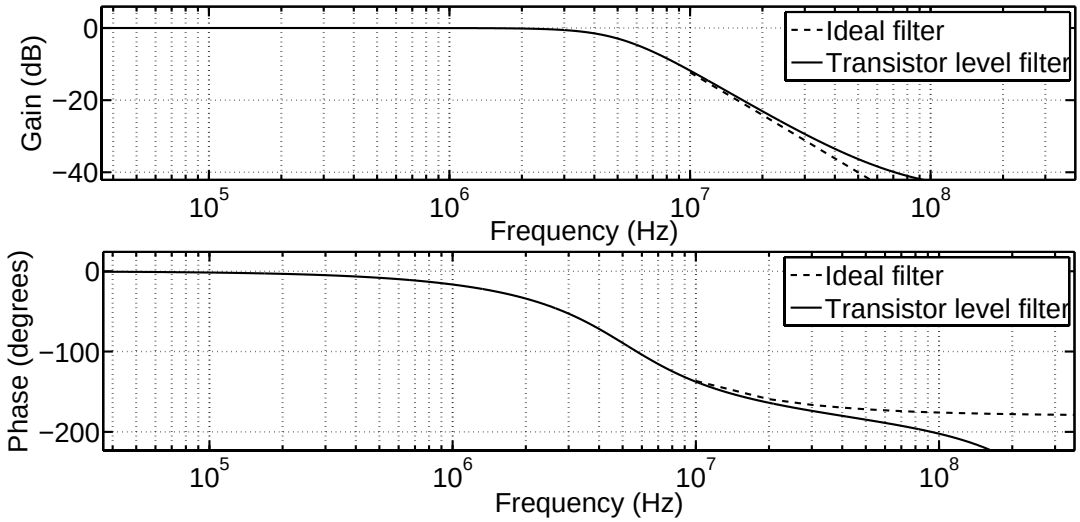


Figure 6.12: Frequency response of the biquad filter.

Table 6.6: Comparison with some published filters

Reference	**Bandwidth [MHz]**	**Order**	**Supply Voltage [**V]	**Power [μW]**	Q_{max}	**Input [mVrms] for 1% THD**	**Dynamic Range[dB] (for THD$\sim$ -40 dB)**	**Topology**	**Tech. [μm]**	**FOM (fJ)**
(Chatterjee *et al.*, 2005)	0.135	5	0.5	1100	6.2	50	56.6[1]	Active-RC	0.18	0.58
(Zhang *et al.*, 2008)	1.05	3	1.8	4070	1.99	282.8	45[2]	Gm-C	0.18	20.53
(Carrillo *et al.*, 2008)	0.0175	2	1	45	0.89	530.3	63.7[3]	Gm-C	0.35	0.606
(Carrillo *et al.*, 2010)	0.010	2	1.5	648	0.707	166.1	62.6[4]	Gm-C	0.35	25.18
(Carrillo *et al.*, 2011)	3	2	1.2	382	0.707	636	69.6[5]	Gm-C	0.35	0.009
(Arya *et al.*, 2013)	0.9705	3	0.5	332	0.707	18.29	63.13[6]	Gm-C	0.13	0.078
This work	**5**	**2**	**0.5**	**58.76**	**0.707**	**223.45**	**55.78**[7]	**Active-RC**	**0.09**	**0.022**

[1]Ratio of input @ 100 kHz to integrated input noise for the range 1 kHz-150 kHz
[2]Ratio of input @ 1 MHz to integrated input noise for the range 1 Hz-1 MHz
[3]Ratio of input @ 1 kHz to integrated input noise for the range 1 Hz-18 kHz
[4]Ratio of input @ 1 kHz to integrated input noise for the range 10 Hz-10 kHz
[5]Ratio of input @ 1 kHz to integrated input noise for the range 100 Hz-4 MHz
[6]Ratio of input to integrated input noise for the range 1 kHz-1 MHz
[7]Ratio of input @ 1.6 MHz to integrated input noise for the range 50 kHz-10 MHz

CHAPTER 7

CONCLUSIONS AND FUTURE DIRECTIONS

7.1 CONCLUSIONS

The thesis addressed the issues in designing low power active-RC filters for 0.5V operations using n-well standard CMOS process. A fifth order Chebyshev filter was successfully fabricated on silicon using 0.18 μm n-well standard CMOS process. The designed filter offered 750 kHz bandwidth, the highest till date among the reported for low voltage active-RC filters realized on silicon and operating on supply voltage less than 1V. The lowest FOM (0.202 fJ) when compared to the similar works, indicated that the energy efficiency was not compromised in the process of achieving the necessary bandwidth. The issue associated with low supply voltage and relatively higher threshold voltage was addressed by making use of bulk driven input devices and was shown that the bulk-driven transconductors can effectively be used for realizing the OTAs in the low voltage regime. Also, it was shown that feed-forward compensation too can be effectively used. The filter offered a dynamic range of 46.33 dB consuming a power of 305 μW. An extensive mathematical model of the filter is also presented which would help the designers to model the filter for design centering such active-RC filters.

A detailed analysis of the effects of OTA non-idealities such as finite input and output impedances on the performance of active-RC filters was presented for the case of FF-OTAs. A first order active-RC filter was taken as an example for the study. A non-ideality factor was defined to quantify the effect of non-idealities on the filter frequency response. It was shown that OTA non-idealities limit the maximum frequency beyond which the frequency response deviates from the ideal. The analytical results are found to have a very good correlation with that obtained for transistor level filters through

simulations. The maximum bandwidth (ω_{max}) which is realizable for any filter was quantified as a function of the frequency beyond which non-ideality factor deviates from the desired (ω_{NIF}), the desired stop-band attenuation expected and the order of the filter. A simple method to estimate ω_{NIF} was also given.

Four CMFB circuits were proposed for pseudo-differential transconductors for 0.5 V supply operation. These circuits help to maintain the output common-mode voltage of the transconductors to a reference voltage. All the proposed circuits offered high input impedance and very low power when compared with the transconductor; for the case considered in this work, it was less than 0.5%. Comparisons are also made with respect to input capacitance, power, linearity and steady state error. In overall, the CMFB circuit-IV was found to offer better performance when compared to other circuits.

A CMOS inverter based transconductor for realizing continuous time filters was found to be very effective, simple and power efficient. Use of such transconductors was proposed, in the last chapter of this thesis, for realizing FF-OTAs and then were extended to realize active-RC filters. This is first of its kind. A fifth order 150 kHz low pass Chebyshev active-RC filter was designed as the proof of concept and was targeted to operate on 0.5 V supply. This ultra low power filter, designed in 180 nm standard n-well CMOS process, consumes 21.79 μW. Further, a second order Butterworth biquad filter was designed in 90 nm CMOS technology. It was found that with technology scaling, the filter bandwidth can be as high as 5 MHz for the similar energy efficiency as that for the filter designed in 180 nm process.

7.2 FUTURE DIRECTIONS

In the bulk driven transconductor circuit, input devices can be made to operate in weak inversion or sub-threshold regions by the proper gate/body bias. However, the transconductance offered by the input transistors is very small compared to that of gate driven devices. This technique can be exploited to design circuits in sub-hertz frequency range.

As most of the bio-medical signals are in hertz and sub-hertz frequency range, the concept of bulk driven input transistors can be used to design filters as analog front end for biomedical implants that demand low voltage and low power.

In the filter realized in this research, dedicated servo loops are not used for fixing the filter time constants. This is because, the main focus of this research was to design filters for operation on 0.5 V supply using 180 nm standard CMOS process. It will be quite interesting to design on-chip servo loops to tune the filter response such as Q-tuning loops. In addition, resistor tuning technique can also be exploited. This would be quite challenging since the tuning circuit has to be designed to operate on 0.5 V.

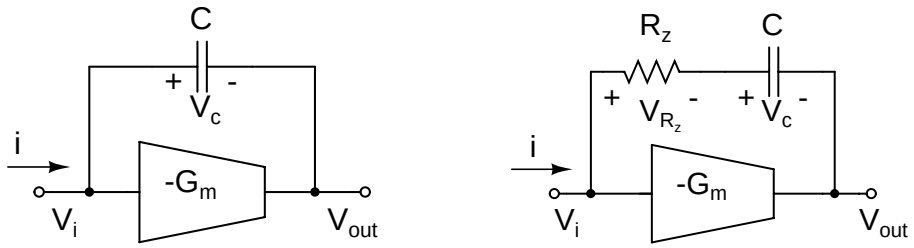
Since designing analog circuits for low voltage application is challenging, the scope of research for designing analog circuit is un-ending. Any analog circuit which can be thought of, is worthwhile to be tried for sub-1V applications.

APPENDIX A

RIGHT HALF *s*-PLANE ZERO CANCELLATION

Integrator realized using OTA will have a right half s-plane (RHP) zero. This reduces the phase margin and hence degrades the stability of the system. To compensate for the effect of this RHP zero, a resistor is connected in series with the integrating capacitor as shown in Figure A.1. A detailed analysis is given below.

A.1 OTA-C integrator without R_z



(a) (b)

Figure A.1: OTA-C integrator (a) without R_z (b) with R_z

Consider a OTA-C integrator shown in Figure A.1(a). Applying KVL,

$$V_{out} = -V_c + V_i \tag{A.1}$$

$$= -\frac{i}{sC} + \frac{i}{G_m} \tag{A.2}$$

$$= i\left[\frac{1}{G_m} - \frac{1}{sC}\right] \tag{A.3}$$

From equation (A.3), there exists a right half s-plane zero at

$$s = \left[\frac{G_m}{C}\right] \tag{A.4}$$

A.2 OTA-C integrator with R_z compensation

The circuit shown in Figure A.1(b) can be used to change the location of the zero by a proper choice of the compensating resistor R_z. Applying KVL to the Figure A.1(b),

$$\begin{aligned} V_{out} &= -V_c - V_{R_z} + V_i && \text{(A.5)} \\ &= -\frac{i}{sC} - iR_z + \frac{i}{G_m} && \text{(A.6)} \\ &= i\left[\left(\frac{1}{G_m} - R_z\right) - \frac{1}{sC}\right] && \text{(A.7)} \end{aligned}$$

It can be inferred from (A.7) that the right half plane zero can be eliminated if R_z is chosen equal to $1/G_m$. In reality, perfect cancellation is not possible. However, the zero can be pushed far away from the origin either on left half or right half of the s-plane.

APPENDIX B

CONSTANT CURRENT SINK DESIGN USING LM334 IC

An off-chip current sink for 100 μA, required to generate the necessary bias for test buffers, is designed using LM334 IC from National Semiconductors. It is a three terminal adjustable current source/sink. A basic current source/sink circuit using LM334 is shown in Figure B.1. The current source is built between node-A and node-B where A

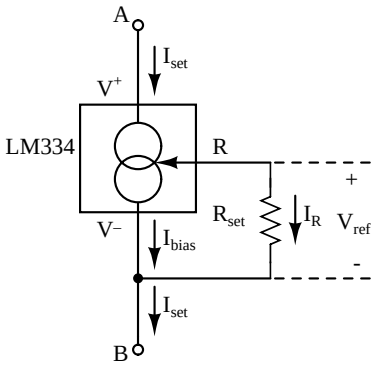


Figure B.1: LM 334 IC terminal details

is at higher potential than B. The three terminals of LM334 are named V^+, R and V^-. LM334 generates a constant voltage V_{ref} between R and V^- for a given temperature, which is approximately given by 214μV/K. At room temperature (300 K), this amounts to 64.2 mV. An external resistance R_{set} sets the current I_R between terminals R and V^-. I_{bias} is the bias current required by the IC for its operation. Therefore, the current set (I_{set}) by the current source is given as

$$I_{set} = \frac{V_R}{R} + I_{bias} \tag{B.1}$$

The bias current I_{bias} depends on I_R. A typical ratio $\frac{I_{set}}{I_{bias}}$ is about 18 for 2 μA $< I_{set} <$1 mA. Using this value in (B.1), the resistance R_{set} required to generate a given I_{set} at room temperature (300 K) can be simplified to

$$R_{set} = \frac{68\,\text{mV}}{I_{set}} \tag{B.2}$$

For I_{set} of 100 μA, the R_{set} required will be 680 Ω. Since the chip in this work requires a current sink, the terminal B of circuit in Figure B.1 is grounded and the terminal A is connected to the filter chip.

APPENDIX C

PIN DETAILS OF THE ACTIVE-RC FILTER CHIP

Pin details of the packaged fifth-order active-RC low-pass filter chip designed in this research is shown in Figure C.1. The filter die is packaged in 44 pin JLCC package. The chip has a die size of 1.525×1.525 mm^2. The chip has three designs. Each design is chosen to have independent pins for power, input, output and ground pins. This enables testing of each design independently and without unwanted interference for the neighbouring designs on the chip. Only the design of interest is powered while the others are kept off.

The pin details of the chip along with their functions are given in Table C.1. The active-RC filter has sixteen dedicated pins. Each pin is named according to its functionality, followed by the name of the design to whom that pin belongs to. Pins corresponding to the active-RC filter have their names ending with 'RS'.

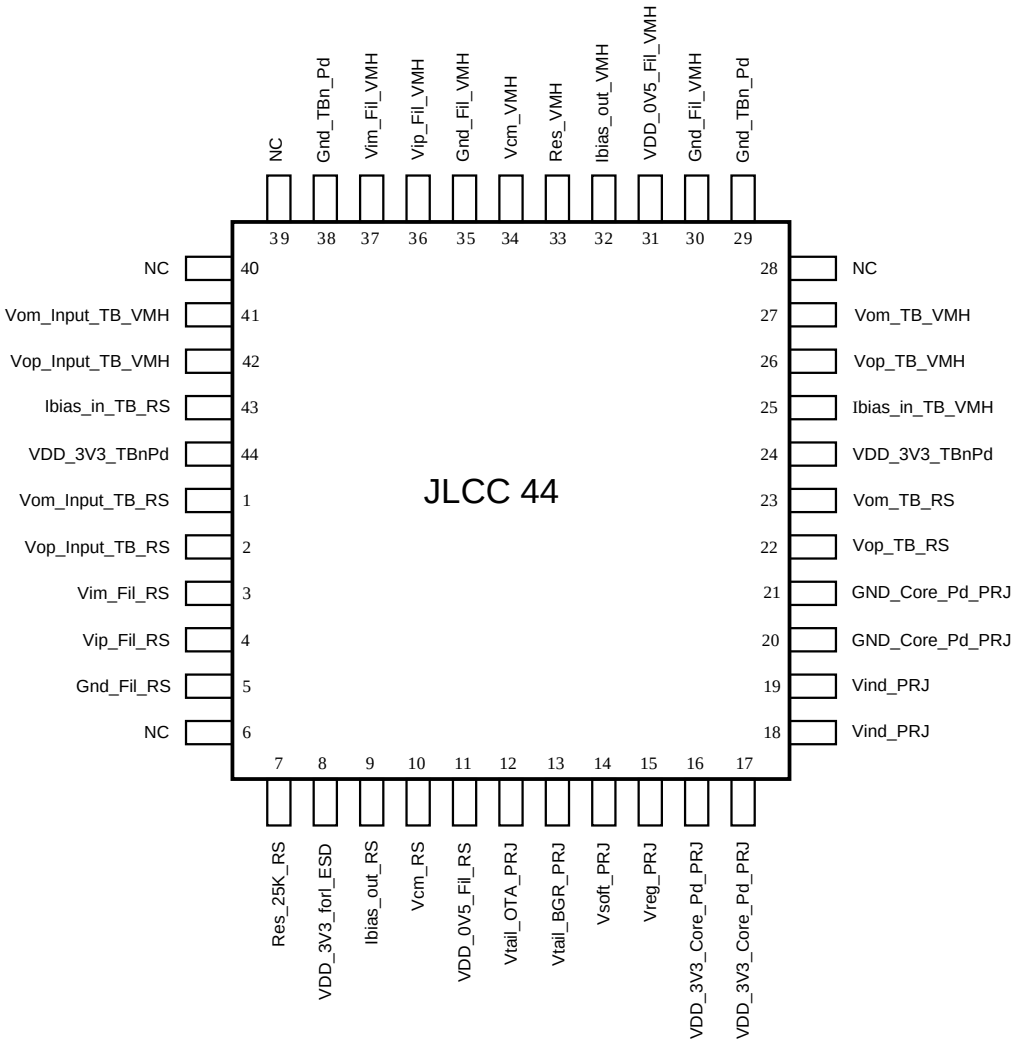


Figure C.1: Pin-out details of the packaged chip

Table C.1: Functionality of pins of complete chip

Pin Number	**Pin name**	**Functionality**
29, 38	GND_TBnPd	Top pack Ground
30, 35	Gnd_Fil_VMH	VMH Filter ground
20, 21	GND_core_Pd_PRJ	PRJ circuit Ground
5	Gnd_Fil_RS	RS Filter ground
44,24	VDD_3v3_TBnPd	Vdd 3.3V supply voltage for Test buffer
8	VDD_3v3_for_ESD	Vdd 3.3V supply voltage for ESD Pad
31	VDD_0v5_Fil_VMH	VMH Filter 0.5 V power supply
34	Vcm_VMH	Common mode input voltage for VMH Filter (0.25 V)
32	I_{bias} _out_VMH	A test pin, where the VMH transconductor bias current is brought out
33	RES_VMH	An external stable resistance connected between this pin and ground for VMH Filter
36 37	V_{ip} _Fil_VMH V_{im} _Fil_VMH	Filter path differential input for VMH Filter
6, 28,39 and 40	NC	No Connection, left open
26 27	V_{om} _TB_VMH V_{op} _TB_VMH	Filter path differential output for VMH
40 41	V_{om} _Inputl_TB_VMH V_{op} _Inputl_TB_VMH	Direct path differential output for VMH
25	I_{bias} _in_TB_VMH	Input bias current for the VMH Test buffer
43	I_{bias} _in_TB_RS	Input bias current for the RS Test buffer
3 4	V_{im} _Fil_RS V_{ip} _Fil_RS	Filter path differential input for RS Filter
1 2	V_{om} _Inputl_TB_RS V_{op} _Inputl_TB_RS	Direct path differential output for RS
23 22	V_{om} _TB_RS V_{op} _TB_RS	Filter path differential output for RS
7	RES_25K_RS	An external stable resistance connected between this pin and ground for RS Filter
10	Vcm_RS	Common mode input voltage for RS Filter (0.25 V)
9	I_{bias} _out_RS	A test pin, where the RS transconductor bias current is brought out
11	VDD_0v5_Fil_RS	RS Filter 0.5 V power supply
16,17	VDD_3v3_Tcore_Pd_PRJ	Vdd 3.3V supply voltage for PRJ circuit
12	Vtail_OTA_PRJ	Vtail for PRJ circuit
13	Vtail_BGR_PRJ	Vtail for PRJ circuit
14	Vsoft_PRJ	Vsoft for PRJ circuit
15	Vreg_PRJ	Regulated output for PRJ circuit
18,19	Vsoft_PRJ	Vsoft for PRJ circuit

APPENDIX D

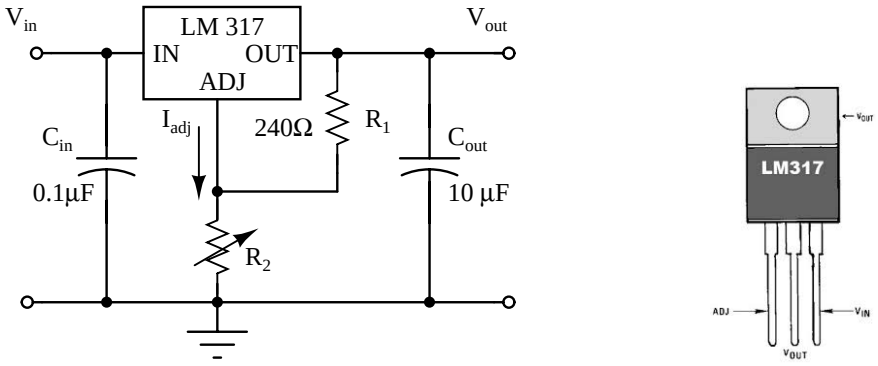
POWER SUPPLY CIRCUITS

The designed filter needs three individual dedicated power supplies for characterizing the filter chip.

1. 3.3 V : Power supply for test buffer
2. 0.5 V : Power supply for the filter
3. 0.25 V : Input common-mode voltage

D.1 3.3 V POWER SUPPLY

3.3 V power supply is derived using an adjustable voltage regulator LM317 from National Semiconductors. The schematic of the voltage regulator circuit for generating 3.3 V is shown in Figure D.1(a). The LM317 has a sourcing capacity of 1.5 A which is well in excess of the requirements of test-buffer.



(a) (b)

Figure D.1: (a) Circuit diagram of LM317 based voltage regulator. (b) Pin details of LM317.

The output voltage V_{out} of the regulator is given by

$$V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \tag{D.1}$$

Since I_{adj} is less than 100 μA, the second term in (D.1) can be made negligible by a proper choice of R_2. Ratio R_2/R_1 is chosen such that the output V_{out} is 3.3 V. C_{in} and C_{out} are the by-pass capacitors.

D.2 0.5 V POWER SUPPLY

Figure D.2 shows the circuit designed to derive a regulated 0.5 V supply. The voltage regulator IC LM317 generates a regulated 1.25 V. This voltage is scaled down to 0.5 V using potential divider network. The potential divider is made adjustable by using a potentiometer. This allows the voltage adjustable by $\pm$10% around the nominal 0.5 V. The divided voltage is then buffered using an op-amp based unity gain amplifier. A low noise op-amp LF353 has been used for the buffer. A protection is provided at the output node, by connecting a 3.3 V zener diode across the output. This protects the chip against any accidental increase in the supply voltage beyond 3.3 V (and beyond 0.7 V in reverse). This is necessary since the buffer is operated on $\pm$6 V supply.

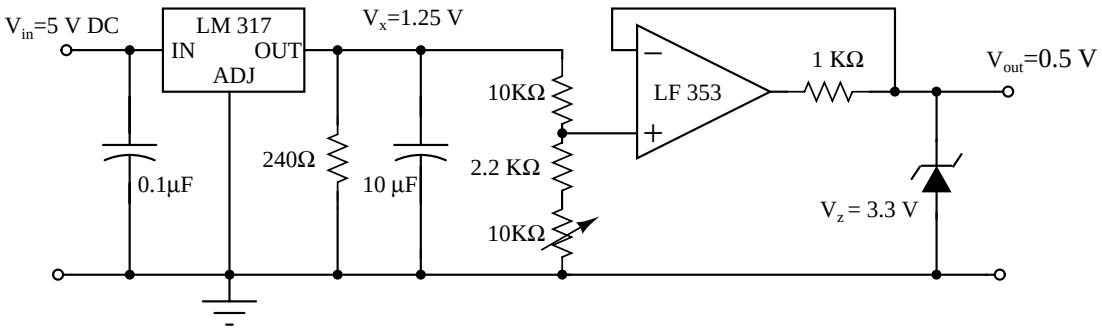


Figure D.2: Schematic of power supply circuit to generate 0.5 V.

D.3 0.25 V POWER SUPPLY

The common mode reference voltage of 0.25 V is derived from the designed 0.5 V power supply. Figure D.3 shows the circuit diagram. The circuit works similar to that of 0.5 V supply. It is to be noted that, input common mode reference will always be a function of filter supply. Or in other words, $V_{cm,ref} = V_{DD}/2$.

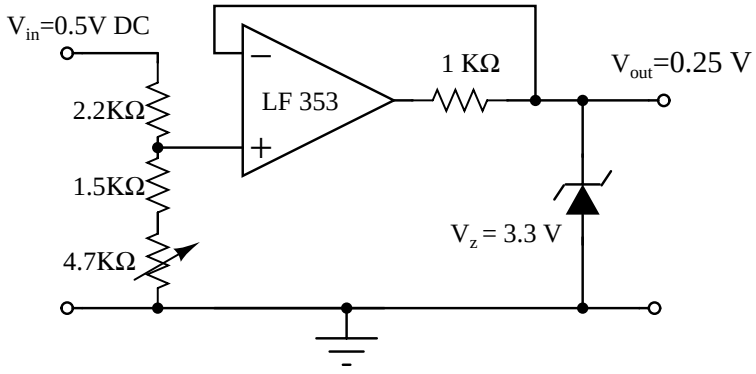


Figure D.3: Schematic of the power supply circuit to generate 0.25 V.

APPENDIX E

EXTRACTED NETLIST OF THE FILTER: ERROR IN EXTRACTION

In this appendix, the errors observed while extracting the MIM capacitors, used as integrating capacitors of the filter, are highlighted. Here, the netlist of the test-bench where both the schematic and layout extracted filters are simulated is used for highlighting the error in extraction. Figure E.1 shows the header of the extracted netlist. The following

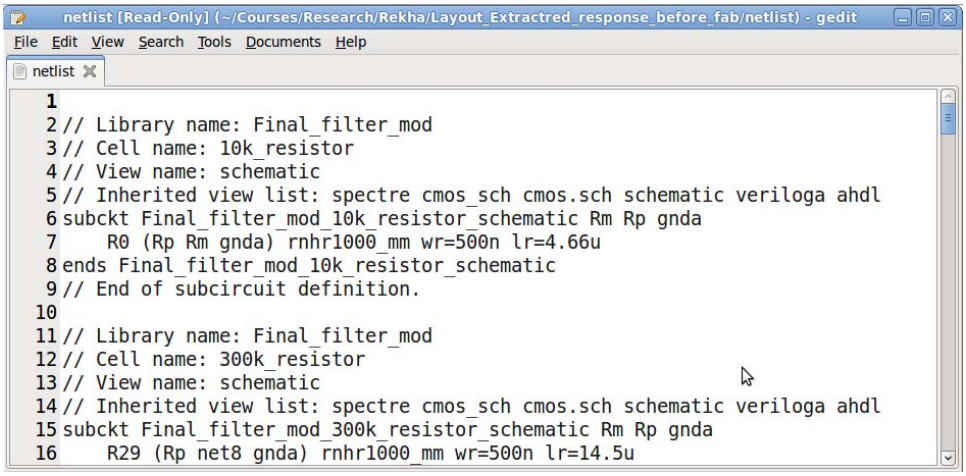


Figure E.1: Header of the extracted netlist of the filter test bench

conventions have been followed while naming the integrating nodes.

- Output of each OTA is the integrating node. There are five integrating nodes. The two outputs of the first differential integrator are named $vop1$ and $vom1$. Similarly the outputs of the second, third and fourth integrators are named. For the fifth integrator outputs are named as vop_filter and vom_filter since they form the differential output of the filter.
- Each fully differential integrator has two capacitors. Each capacitor appears between one of the outputs of the differential OTA (vop or vom) and the corresponding zero compensating resistor R_z (refer Figure 2.11).

- The nodes where R_z and the MIM capacitor meet in the integrators are named such that they have a prefix of Vrz. For example, the node $Vrz1p$ corresponds to the first integrator where the other terminal of the MIM capacitor (attached to this node) is connected to the OTA output $vop1$.

The above conventions are shown in Figure E.2 for the first integrator, for the ease of understanding. With these conventions, all the integrating capacitors (MIM and parasitic) can be easily identified in the netlist.

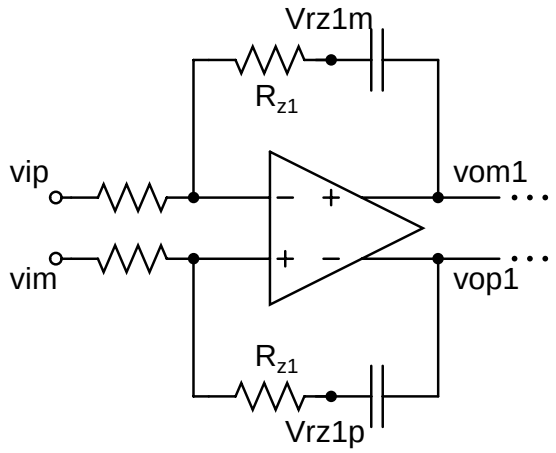


Figure E.2: Integrator schematic showing the naming convention followed for the nodes.

The section of the netlist showing the MIM capacitors in schematic and in the extracted netlist are shown in Figure E.3 and E.4 respectively. Let us now consider the error seen while extracting the MIM capacitors of the first integrator. One of the MIM capacitors is connected between the nodes $Vrz1p$ and $vop1$ and the other between $Vrz1m$ and $vom1$. Upon searching the netlist, an additional capacitor is found to exist between $Vrz1p$ and $vop1$ and similarly between $Vrz1m$ and $vom1$. The portions of the netlist highlighting these are shown in Figure E.5. It can be seen that the area of one MIM capacitor is 29.75$\times$32 sq.μm. This amounts to total capacitance of approximately 952 fF since MIM capacitors offer approximately 1 fF per sq.μm area. It can also be seen that a parasitic capacitance of 540 fF has been extracted by the extraction tool across the MIM capacitor which is about 57% of the MIM capacitor value.

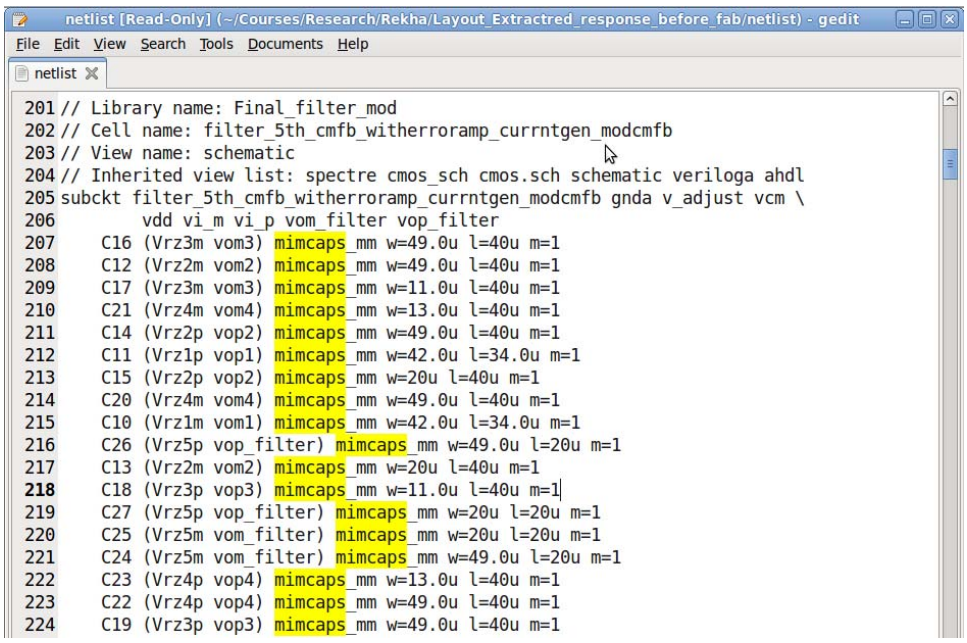


Figure E.3: Portion of the netlist showing the MIM capacitors used as integrating capacitors in the filter schematic.

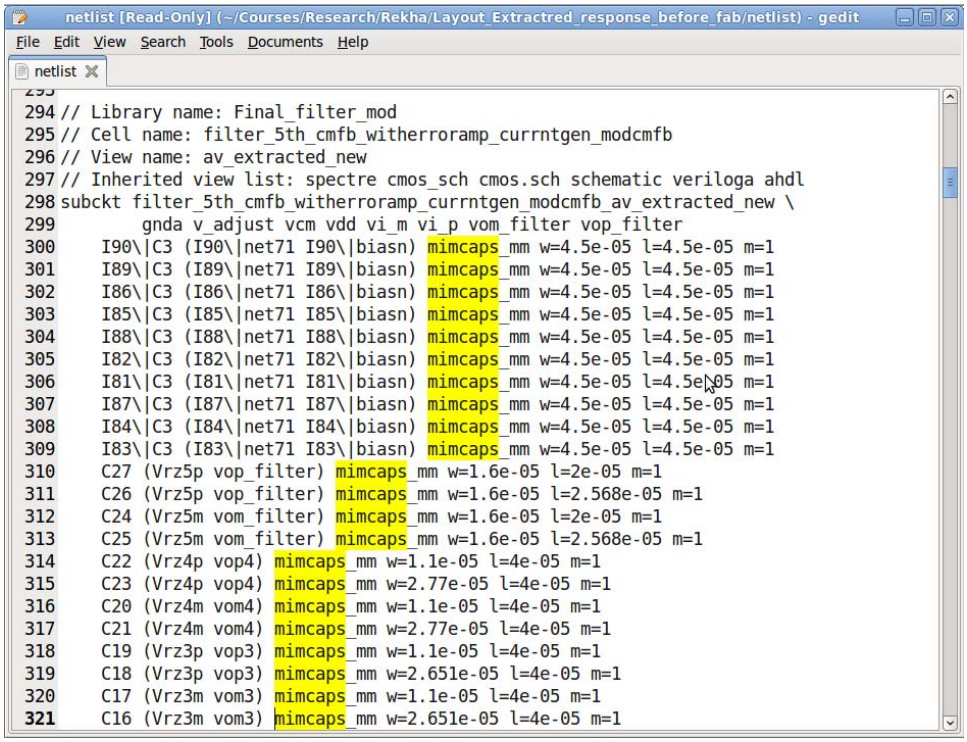


Figure E.4: Portion of the netlist showing the MIM capacitors used as integrating capacitors in the extracted view.

Similar observations can be made for all the MIM capacitors of remaining integrators. Snap shots of the portions of netlist highlighting this error in extraction are shown in Figure E.6-Figure E.9.

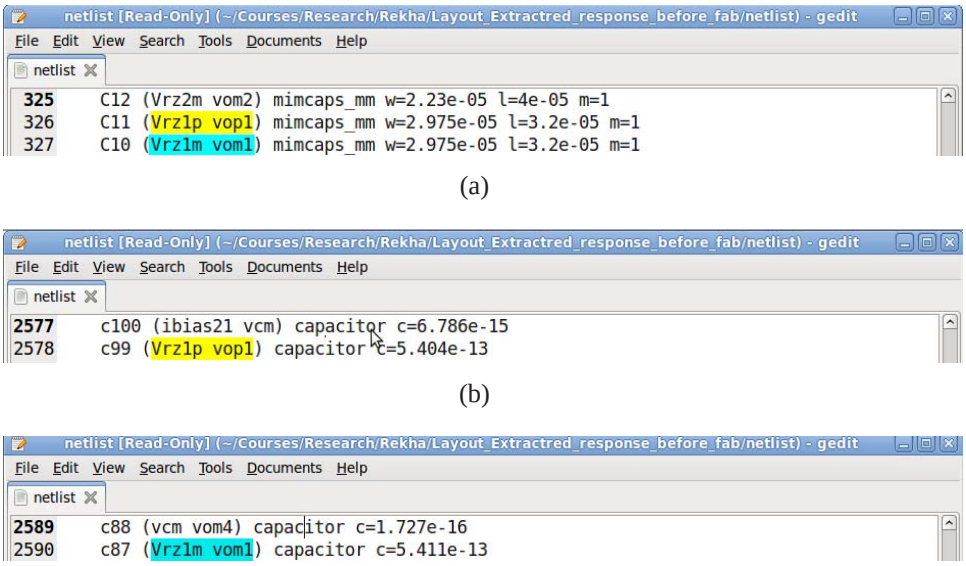
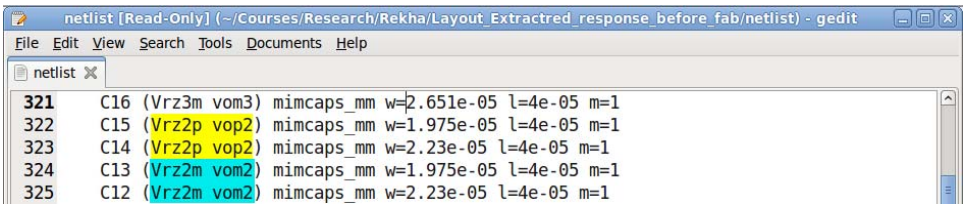
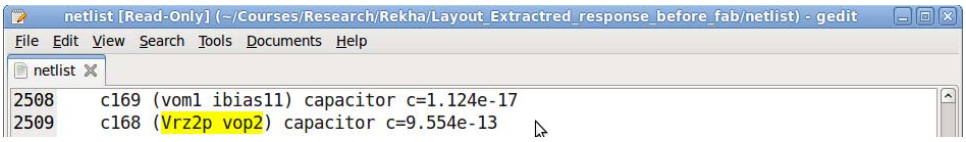


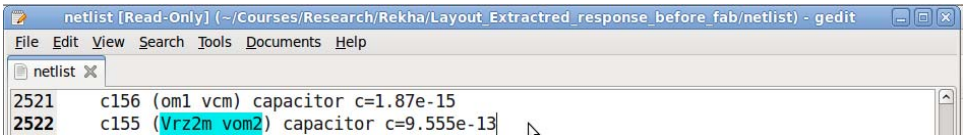
Figure E.5: Portion of the netlist showing the integrating capacitors of first integrator. (a) MIM capacitors (b) Extracted parasitic capacitance between $Vrz1p$ and $vop1$ (c) Extracted parasitic capacitance between $Vrz1m$ and $vom1$.



(a)

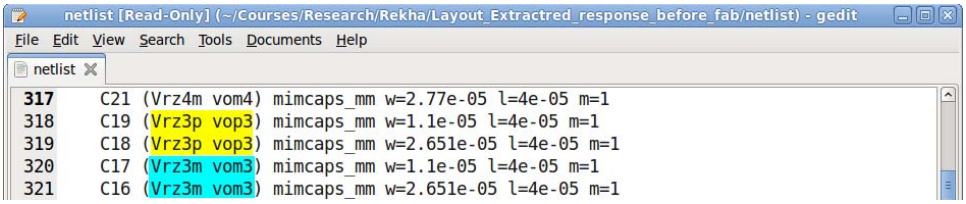


(b)

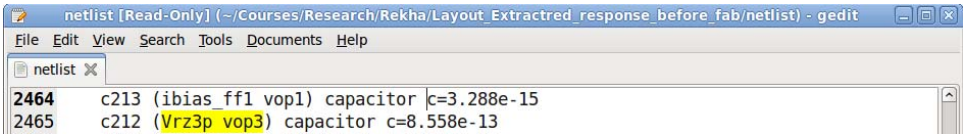


(c)

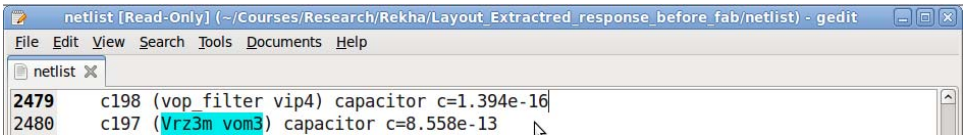
Figure E.6: Portion of the netlist showing the integrating capacitors of second integrator. (a) MIM capacitors (b) Extracted parasitic capacitance between $Vrz2p$ and $vop2$ (c) Extracted parasitic capacitance between $Vrz2m$ and $vom2$.



(a)

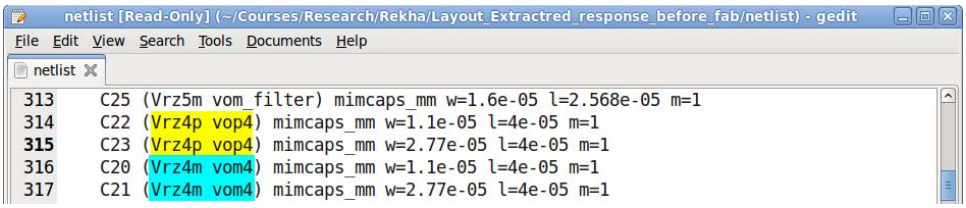


(b)

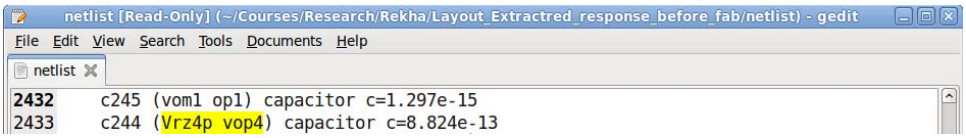


(c)

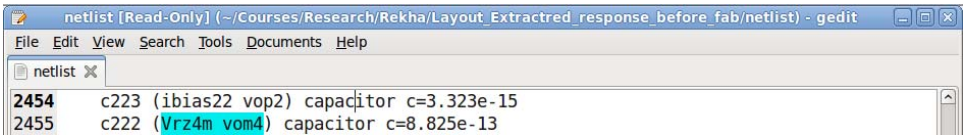
Figure E.7: Portion of the netlist showing the integrating capacitors of third integrator. (a) MIM capacitors (b) Extracted parasitic capacitance between $Vrz3p$ and $vop3$ (c) Extracted parasitic capacitance between $Vrz3m$ and $vom3$.



(a)

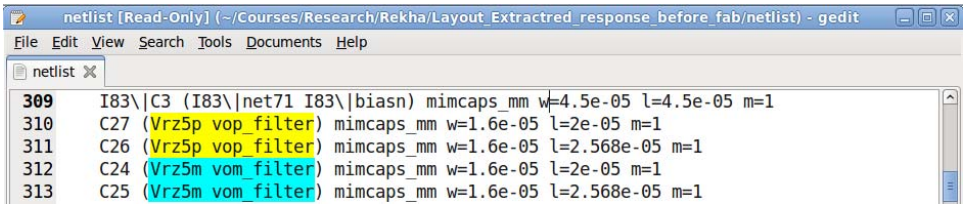


(b)

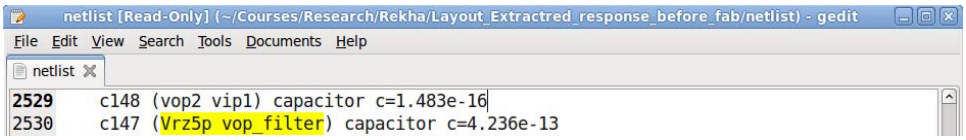


(c)

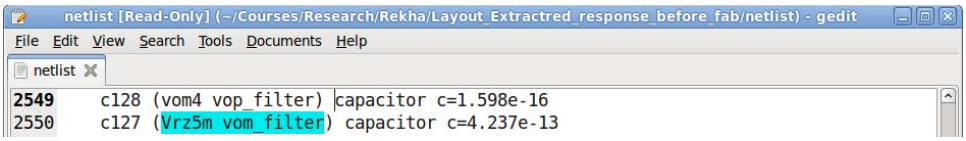
Figure E.8: Portion of the netlist showing the integrating capacitors of fourth integrator. (a) MIM capacitors (b) Extracted parasitic capacitance between $Vrz4p$ and $vop4$ (c) Extracted parasitic capacitance between $Vrz4m$ and $vom4$.



(a)



(b)



(c)

Figure E.9: Portion of the netlist showing the integrating capacitors of fifth integrator. (a) MIM capacitors (b) Extracted parasitic capacitance between $Vrz5p$ and vop_filter (c) Extracted parasitic capacitance between $Vrz5m$ and vom_filter.

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PUBLICATIONS BASED ON THIS THESIS

Journal Papers

1. Rekha S., Laxminidhi T., "Low voltage, Low power Chebyshev filter in 0.18 μm CMOS Technology", *Journal of Circuits, Systems and Computers, World Scientific Publishing Company, ISSN: 0218-1266*, Vol.22, No.7, August 2013.

2. Rekha S. and Laxminidhi T., "A low power, fully differential bulk driven OTA in 180 nm CMOS Technology", *International Journal of Computer and Electrical Engineering(IJCEE) ISSN: 1793-8163*, Vol. 4, No. 3, June 2012.

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1. Rekha S. and Laxminidhi T., "Ultra low power Active-RC filter in 180 nm CMOS technology", *Proc.of 11th International Workshop IEEE on Electronics, Control, Measurement, Signals and their application to Mechatronics (ECMSM)*, Toulouse, France, June 21-23, 2013.

2. Rekha S. and Laxminidhi T., "Effect of Finite gain and Bandwidth of feed-forward compensated OTA on Active-RC integrators: A case study", *International Symposium of Electronic System Design (ISED) 2012*, Kolkata, December 19-22, 2012.

3. Rekha S. and Laxminidhi T., "Effect of parasitics of feed-forward compensated OTA on Active-RC integrators", *3rd international conference on Advances in Power Electronics and Instrumentation Engineering (PEIE 2012)*, Bangalore, Aug.03-04, 2012.

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5. Rekha S. and Laxminidhi T., "A low power, fully differential bulk driven OTA in 180 nm CMOS Technology", *Proc. 3rd international conference on Signal acquisition and Processing*, Singapore, Feb. 26-28, 2011.

Journal Paper Communicated

1. Rekha S., Laxminidhi T.,"Common Mode Feedback circuits for Low Voltage Fully Differential Amplifiers" to *Journal of Analog IC and signal processing, Springer Publications.*

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