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Single-Phase DVR with Semi-Z-Source Inverter for Power Distribution Network

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Abstract A novel topology of single-phase dynamic voltage restorer (DVR) is proposed to compensate the load voltage during voltage sag and voltage swell events. The semi-Z-source converter is utilised in its inverter operating mode for this proposed topology. The reduction in the number of active switches in the inverter and also in the current conduction path without compromising the output voltage range is the merit of the semi-Z-source inverter-based DVR against the commonly used full-bridge inverter-based DVR. The load voltage contains harmonics within the permissible limits when the compensation is performed by the semi-Z-source inverter-based DVR. The need for the filter circuit is eliminated; hence, the magnitude difference and the phase shift in the inverter output voltage due to the filter circuit are not present in the semi-Z-source inverter-based DVR. The proposed topology is cheap compared to the full-bridge inverter-based DVR topology. The simulations performed in MATLAB/Simulink environment are presented to validate the performance of the proposed topology. A comparison between the semi-Z-source inverter-based DVR and full-bridge inverter-based DVR is presented in this paper. The novel topology of DVR using semi-Z-source inverter is proved to be a better solution to the full-bridge inverter-based DVR.

Keywords Voltage sag · DVR · Semi-Z-source inverter · Modified sinusoidal pulse width modulation (MSPWM) · Feedforward controller · Feedback controller

1 Introduction

Industries have attained tremendous growth rate in recent years with the advent of computers and sophisticated equipment. Excellent product quality, reduction in manpower and financial profit obtained from this modern method of industrialisation have opened the market for sensitive equipment and control systems, automated manufacturing units and computerised process controls. The significant gain in revenue received made such systems popular in the industrial arena irrespective of their initial cost. Most of the processes involving this equipment are disturbed and sometimes even damaged by the voltage quality problems. Disturbances in the working environment and economic unbalance are experienced in the industries whenever the utility power deviates from the pre-specified quality.

Power quality (PQ) is a matter of great concern to sensitive industrial customers. The PQ issues have a great influence on the profit, end product quality and equipment wellness. Among the various PQ problems, voltage sag is the most severe issue [1]. Through temporary shutdowns, deteriorated products and damaged equipment, sags majorly affect the paper, semiconductor and chemical industries [2,3]. Voltage sag is the reduction in the rms value of the voltage from 0.9 to 0.1 p·u for a short duration of 0.5 cycles to less than one minute, usually occurring due to faults in the transmission and distribution lines. Voltage sags reported in the litera-

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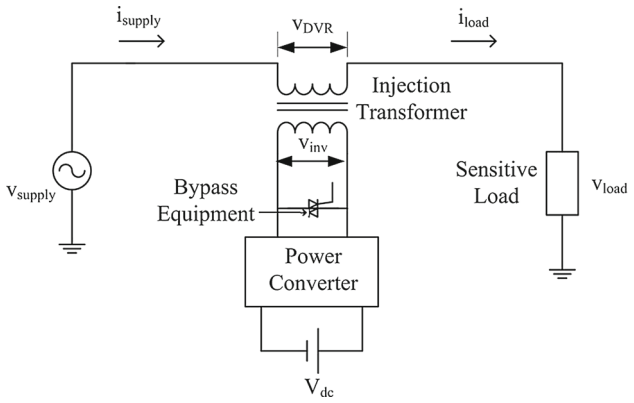

Fig. 1 Basic block diagram of DVR

ture are mostly having a reduction down to 40–50% of the nominal line voltage and lasting up to < 2 s [1]. The fault conditions mostly single-line-to-ground fault (SLGF), starting of large motor drives, energisation of the transformers and animal contact are some of the reasons for voltage sags which adversely affect the sensitive loads [4,5]. Voltage sags are characterised by magnitude, duration and phase jump, if any. The location of the fault from the sensitive load, associated impedances of the transformers, conductors and related equipment, voltage class of the feeder, the speed of response of load protection switchgear are the factors determining the magnitude and duration of the sag experienced by the sensitive loads [1,6].

A dynamic voltage restorer (DVR) protects the sensitive loads from experiencing the PQ problems and diminishes the potential losses caused by these issues. The DVR is a power quality device, which restores the load voltage during voltage quality events (particularly sags and swells) by injecting the appropriate voltage in series with the supply voltage. The DVR restores the magnitude and phase of the load voltage completely, irrespective of the utility disturbances, thereby allowing control of real and reactive power exchange between the DVR and the distribution system [1,3,7]. It is the most economical solution for mitigating upstream voltage disturbances in the distribution system [8].

Conventionally in the DVR system, the inverter output voltage (v_{inv}) is injected into the distribution line through an injection transformer, as shown in Fig. 1. The basic DVR structure consists of energy storage for real power injection, the inverter for synthesising the required voltage to be injected into the power line, the filter for removing switching harmonics from injected voltage and the injection transformer for voltage boosting and galvanic isolation between the inverter and the line [9]. The voltage requirement of the inverter can be reduced by choosing proper turns ratio 'n' of the transformer, and it also prevents the input dc source of the inverter from being short circuited through the switches in the different inverter legs [10]. A bypass equipment or crowbar circuit is provided to protect the DVR from the abnormally high downstream load and fault currents [11].

Usually for cost-effectiveness, the DVR installation is performed with 50% voltage injection capability. The voltage rating of the DVR depends on the maximum voltage injection capability and the nominal line voltage of the utility supply. The existing load and the future expansion of the load are considered while selecting the current rating of the DVR. Either DVR must be rated to handle the higher currents during load expansion or the system should be protected using the bypass equipment [6].

The DVR load voltage compensation is associated with the exchange of active power and reactive power with the utility grid. The active power supply to the load demands the need of a source for this energy. Based on this consideration, DVR is classified into one with stored energy and another with no stored energy. The DVR topologies with stored energy exhibit improved performance for certain types of sags when compared to its counterpart. The current drawn from the utility grid remains unchanged, and hence, the strain on the utility grid is lower in the case of the energy storage-based DVR. The two categories in energy storage-based DVR are (a) variable dc-link voltage DVR where energy is stored in the dc-link capacitors and (b) constant dc-link voltage DVR. The battery, Superconducting Magnetic Energy Storage (SMES) or supercapacitors are some of the direct storage methods used in the constant dc-link voltage DVR [12].

The DVR topologies with no storage offer cost benefits due to the elimination of the energy storage system. In DVR topologies with no energy storage, a passive shunt converter is used to charge the dc-link capacitor from the grid, and according to the location of the shunt converter, the subclassifications are named as (a) supply-side-connected shunt converter-based DVR and (b) load-side-connected shunt converter-based DVR. These topologies draw more current from the grid during sag conditions, and hence, the sensitive loads will experience a higher voltage drop. On the other hand, the nonlinear currents drawn by the load-side-connected shunt converter can even disturb the load [12].

A capacitor with voltage control can be used to realise the dc source of the voltage source inverter (VSI) of the DVR. As the compensating voltage is injected in quadrature with the line currents, the capacitor-supported DVR neither supplies nor absorbs active power during the steady-state operation [13,14]. As the restored voltage is not in-phase with the pre-sag/swell voltage, the performance is limited to the certain sag conditions where the phase jump caused by the quadrature voltage injection is affordable [13,15].

The way in which the compensation is conducted to maintain the load voltage constant depends on the type of the load—whether it is magnitude sensitive, phase sensitive or both. The load reaction to magnitude variation and phase disturbance during the sag events are studied and analysed.

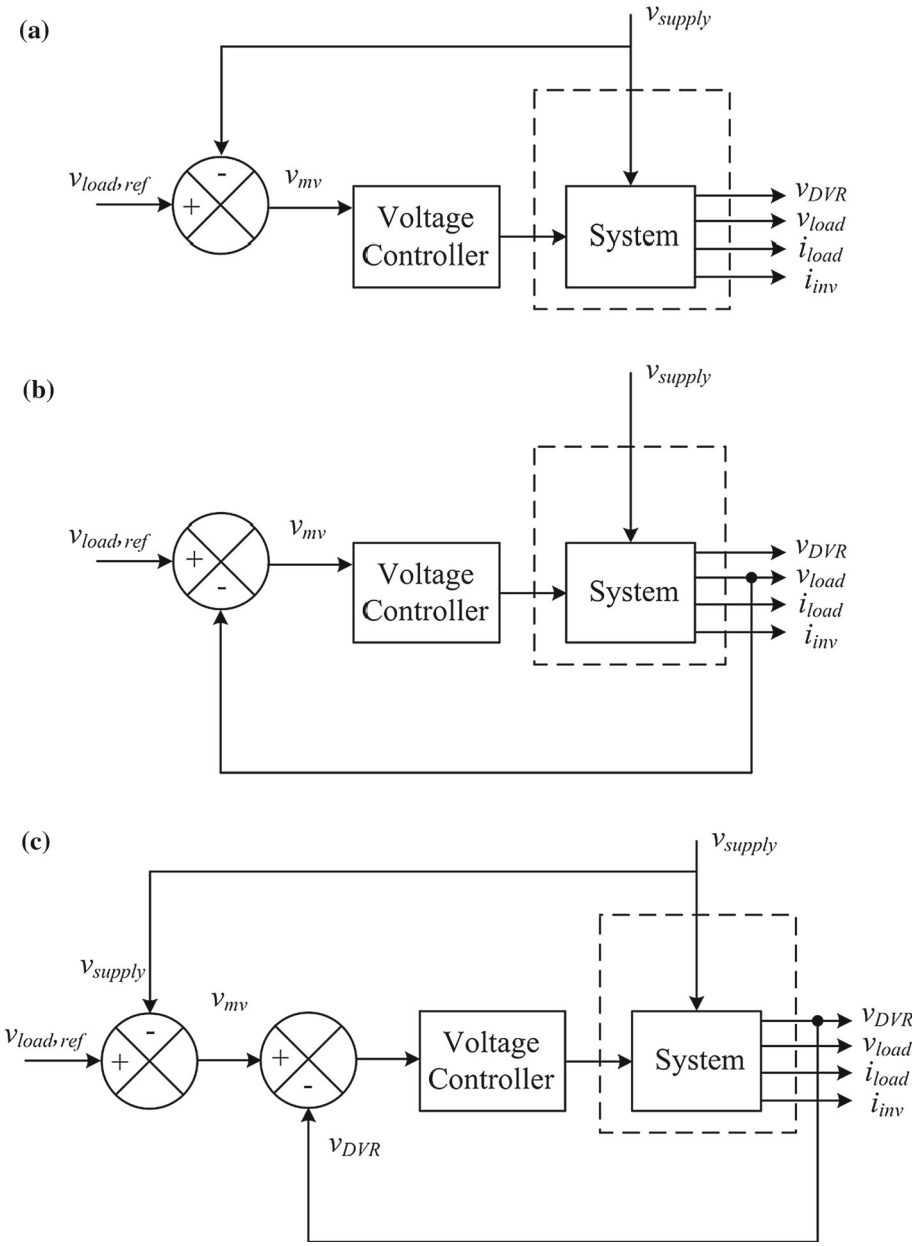

Fig. 2 DVR voltage controllers. **a** Feedforward voltage controller, **b** feedback voltage controller, **c** modified feedback voltage controller

The compensation method is selected according to the severity of the disturbance on the load. The conventional voltage injection schemes are in-phase compensation, pre-sag compensation and energy optimised compensation, as elaborated in the literature [16].

For the appropriate injection of the DVR voltage, voltage controllers are used. The most commonly used DVR voltage controllers are feedforward, feedback and modified feedback voltage controllers [17,18]. Due to its simplicity and robustness, the feedforward controller given in Fig. 2a is widely used. In this control method, the DVR reference voltage is determined by comparing the supply voltage with the load reference voltage. The response of the feedback control is quick and more accurate as it uses either the load voltage or DVR voltage in the feedback loop as given in Fig. 2b, c, respectively. The modified feedback control which uses the DVR voltage in the feedback loop is more accurate compared to the feedback control.

The VSI is the most essential element of the DVR. The performance of the DVR system is influenced by the inverter topology. The switching frequency, number of power switches in the current path, the number of active and passive devices, the harmonic content in the inverter output voltage and the need for the filter are some of the parameters to be considered while selecting the inverter topology [17]. Table 1 compares the commonly used inverters in the single-phase and three-phase DVR system [19–30]. The three-phase inverter and four-switching leg inverter for three-phase DVR

Table 1 Comparison of commonly used inverter topologies in the DVR

Sl. no.	Inverter	Merits	Demerits
1	Half-bridge inverter	Reduced switch count and low cost	Harmonic content present in the voltage is high. Filter is required
2	Full-bridge or H-bridge inverter	Used in high-voltage distribution system. Independent single-phase connection available	Harmonic content is high. Filter is required
3	Three-phase inverter	Lower cost and simpler control	Filtering scheme is required due to harmonics in the inverter output. Presence of differential and common mode EMI
4	Four-switching leg inverter	No dc-link capacitor balancing problem	Presence of differential and common mode EMI
5	Multilevel inverter	Low switching frequency, low device stress, low THD and low switching losses	Increase in number of switching devices. Complex structure after level 5
6	Cascaded multilevel inverter	Medium and high-voltage applications, simpler filter design, low harmonics and less losses	Increase in number of switching devices. Complex control and structure

applications and half-bridge and full-bridge inverters used in both single-phase and three-phase DVR systems require filter circuits. The inverter-side filtering scheme in the DVR system introduces a magnitude difference due to the passive filter component voltage drop and the phase shift between the inverter output voltage and the reference voltage waveform. Figure 3 shows the phase shift in the inverter output voltage in a single-phase full-bridge inverter-based DVR when it is compensating a sag of 40% depth. The phase shift due to the presence of filter inductance and its equivalent series resistance (ESR) prevents the DVR from the exact tracking of the reference voltages generated. The magnitude and phase difference in the fundamental component of voltage before and after the filter circuit may even jeopardise the DVR control [31]. The lag/lead compensators are introduced in the control strategy to compensate for the phase shift [24]. However, the lag/lead compensator demands an adaptive nature due to the temperature dependence of the ESR. The alternative line-side filtering scheme can make use of the leakage reactance of the secondary winding of the injection transformer as a filter inductance along with a capacitor. Nevertheless, the penetration of higher-order harmonics from the inverter to the transformer and its effect cannot be neglected in the line-side filtering scheme [31].

To avoid this phase shift and the consequences resulting from the phase shift, multilevel and cascaded multilevel inverters are incorporated into the DVR structure. Even though the filtering scheme is eliminated by increasing the levels of inverter output voltage, the increase in the number of switching devices and its control make the system more complex [32,33]. The demand for an inverter topology without a filtering scheme giving a sinusoidal output voltage which matches exactly with the reference inverter voltage both in magnitude and in phase motivated to introduce the semi-Z-source inverter into the DVR system.

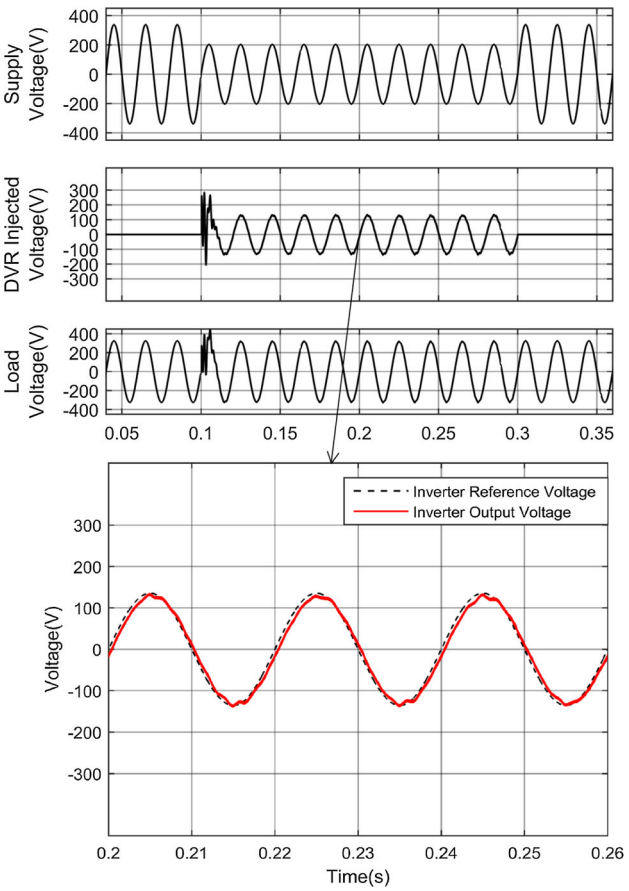

Fig. 3 Load voltage compensation using single-phase full-bridge inverter- based DVR and its phase shift in inverter output voltage

Considering the above-mentioned parameters, the semi-Z-source inverter is identified as a new inverter configuration for the DVR. It can replace the most commonly used full-bridge inverter in the DVR system [15]. The semi-Z-source inverter shares the same output voltage range as the conventional full-bridge inverter but with only two active switches. The Z-source network is present in the ac side, and hence, the size of the same is reduced [34]. The semi-Z-source inverter is found to be an effective alternative for the full-bridge inverter in the DVR systems.

This paper proposes a new topology of DVR based on the semi-Z-source inverter for mitigating the voltage sag. A detailed description of the semi-Z-source inverter, its modulation technique and comparison with the single-phase and three-phase inverters are given in the next section. The feed-forward control scheme for the semi-Z-source inverter-based DVR is given in Sect. 4 of the paper. The modified feedback control is implemented in the proposed topology using the proportional integral (PI) controller. The simulation results and the total harmonic distortion (THD) analysis of the compensated system validate the performance of the novel single-phase DVR topology.

2 Semi-Z-Source Inverter

Conceptually, the semi-Z-source inverter shown in Fig. 4 is a dc–dc converter which can output both positive and negative voltages with a continuous voltage gain curve. The duty cycle of S_1 is taken as D, and the voltage gain curve is shown in Fig. 5. From the continuous voltage gain curve, it is clear that the semi-Z-source converter can be transformed into the semi-Z-source inverter by providing a proper pulse width modulation (PWM) strategy with duty cycle D varying from 0 to 2/3. The output voltage range of the semi-Z-source inverter matches that of the full-bridge inverter even though the total number of switches is reduced to half of the latter. IGBT and MOSFET are the two choices for the switching device in

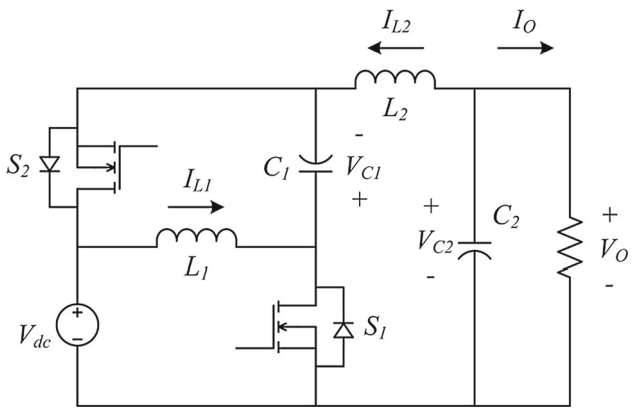

Fig. 4 Semi-Z-source inverter

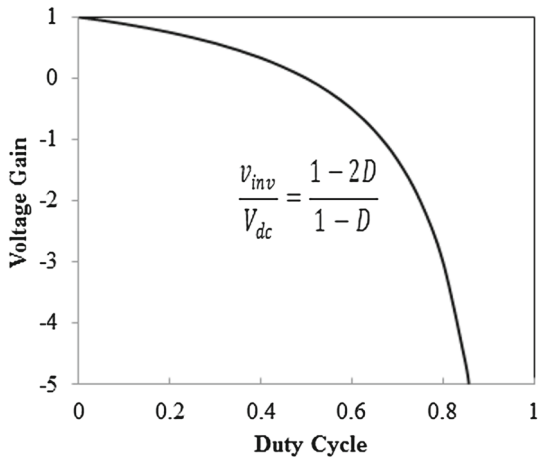

Fig. 5 Voltage gain of semi-Z-source inverter

the semi-Z-source inverter as they cater for the bidirectional current conduction and unidirectional voltage blocking characteristics. Because of the nonlinear nature of the voltage gain curve of the semi-Z-source inverter, a modified sinusoidal PWM (MSPWM) is required to output the sinusoidal voltage [34,35].

The switching pulses for the two switches S_1 and S_2 in the semi-Z-source inverter are complementary in nature. The duty cycle D of switch S_1 of the semi-Z-source converter when varied from 0 to 2/3 makes it operate as an inverter [27]. The output range of the semi-Z-source inverter ($+V_{dc}$ to $-V_{dc}$) is the same as the full-bridge inverter. The positive half cycle of the output ac voltage is obtained by varying the duty cycle of S_1 from (0–0.5). The semi-Z-source inverter gives the negative half cycle when the duty cycle of S_1 is varied from (0.5–2/3). The output voltage is zero when the duty cycle of S_1 is equal to 0.5 [34,35].

Figure 6 shows the equivalent circuit of the semi-Z-source inverter for the two states of operation in one switching period. Figure 6a shows the mode of operation at state I where the switch S_1 is conducting. During this mode of operation, the input dc source and the capacitor C_1 charge the inductors L_1 and L_2. Figure 6b shows the mode of operation at state II where switch S_2 is conducting. During this mode of operation, the two inductors act as the source and the inductor current is decreased. The steady-state equations of the semi-Z-source inverter are given in Eqs. (1)–(4), assuming the direction of the inductor current references and the capacitor voltage references as given in Fig. 6a, b.

$$\frac{V_o}{V_{dc}} = \frac{1-2D}{1-D} \tag{1}$$

$$V_{c_1} = \frac{D}{1-D} V_{dc} \tag{2}$$

$$I_{L_2} = -I_o \tag{3}$$

$$I_{L_1} = -\frac{D}{1-D} I_o \tag{4}$$

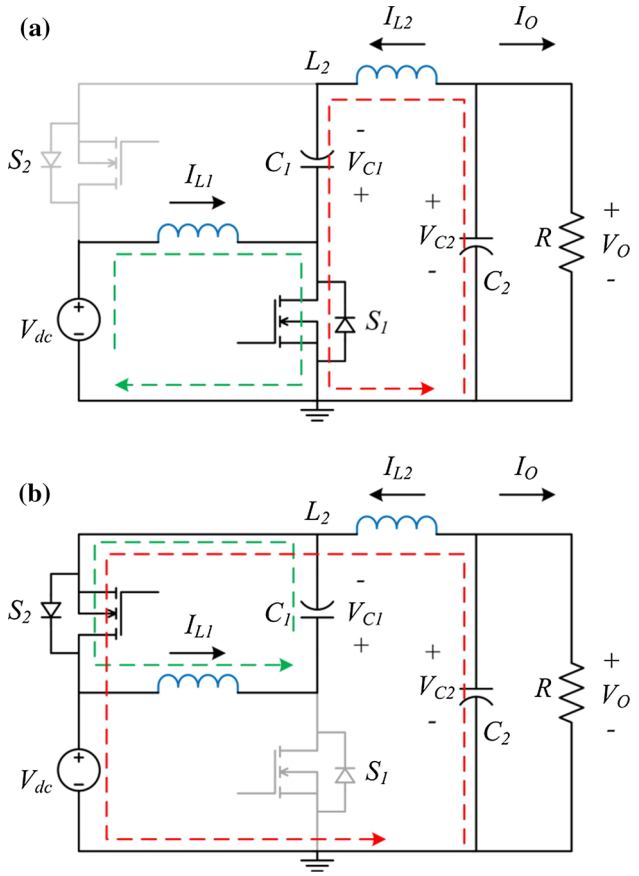

Fig. 6 Semi-Z-source operating modes. **a** Mode of operation at state I, S_1 is on. **b** Mode of operation at state II, S_2 is on

The output voltage of the inverter can be represented as Eq. (5) and the modulation index M can be given by Eq. (6).

$$V_o = V \sin \omega t \tag{5}$$

$$M = \frac{V}{V_{dc}} \tag{6}$$

Substituting Eqs. (5) into (1):

$$\frac{V \sin \omega t}{V_{dc}} = \frac{1-2D}{1-D} \tag{7}$$

Plugging Eqs. (6) into (7) gives:

$$M \sin \omega t = \frac{1-2D}{1-D} \tag{8}$$

From Eq. (8), the duty cycle D and 1-D for switches S_1 and S_2 are obtained as Eqs. (9) and (10), respectively.

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{9}$$

$$1 - D = \frac{1}{2 - M \sin \omega t} \tag{10}$$

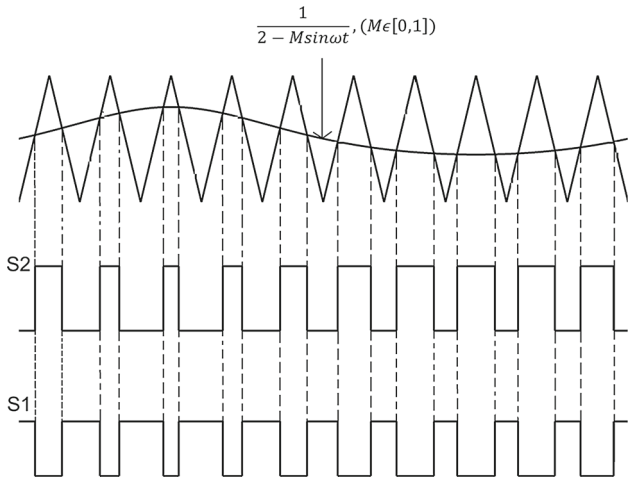

Fig. 7 MSPWM technique for semi-Z-source inverter

Figure 7 shows the MSPWM technique of the semi-Z-source inverter. As the voltage gain curve holds a nonlinear relationship with the duty cycle D of the semi-Z-source inverter, a nonlinear SPWM method called the MSPWM is used to generate the output sinusoidal wave. A reference voltage given by Eq. (10) is used to generate the switching pulses of switch S_2. When the reference sine wave is greater than the carrier triangular wave, the switch S_2 is turned on and vice versa. Equation (9) gives the reference sine wave for switch S_1. The switching pulses of switches S_1 and S_2 are complementary in nature. The range of modulation index M is from [0–1]. The gating signal of switch S_2requires less calculation in the digital controller, so the generation of the switching pulses of S_2 is preferred over the S_1 pulses in a real-time implementation Fig. 7 shows the switching pulses of S_1 and S_2 when the modulation index M is equal to 2/3 [34,35].

Table 2 compares the semi-Z-source inverter with the single-phase full-bridge inverter and the three-phase three-leg inverter when all three are used as the DVR inverter. The three-phase DVR could be easily developed from the single-phase full-bridge inverter-based DVR and single-phase semi-Z-source inverter-based DVR by multiplying the single-phase units to other phases. In the semi-Z-source inverter, a single active switch is present in the conduction path per phase, whereas there are two in the case of the full-bridge inverter. The full-bridge inverter and the three-phase inverter exhibit the risk of short circuiting the dc source when there is a conduction overlap in the switches present in one leg. To prevent this shoot-through phenomenon, a dead time is introduced between the conduction of the switches in one leg. This will introduce fifth and seventh harmonics in the output voltage [36]. This problem is not present in the semi-Z-source inverter as the switches are not in the same leg. The SPWM technique fails to generate the unbalanced

Table 2 comparison between single-phase full-bridge inverter, three-phase inverter and semi-Z-source inverter

Sl. no.	Parameters	Single-phase full-bridge inverter	Three- phase three-leg inverter	Semi-Z-source inverter
1	Nature of the inverter	Buck	Buck	Buck
2	No. of switches per phase	4	2	2
3	No. of active switches in the current path per phase	2	1	1
4	No. of reactive components per phase	2	2	4
5	Generation of unbalanced output voltage when the sags are non-symmetrical	Possible	Difficult	Possible
6	Need for filter	Yes	Yes	No
7	Phase shift in the output voltage due to filter	Yes	Yes	No
8	Risk of short circuit condition due to conduction overlap of switches in same leg	Yes	Yes	No
9	Need of dead time control	Yes	Yes	No
10	Control	Complex with dead time control and adaptive phase shift compensation	Complex with dead time control and adaptive phase shift compensation. For unbalanced output voltages, space vector modulation is preferred	Simple
11	No. of ADC per phase	3	3	2
12	No. of voltage sensing element	3	3	2
13	Voltage overshoot due to LC filter parameters	Yes	Yes	No

three-phase output voltage in the three-phase inverter when compared to the full-bridge inverter and the semi-Z-source inverter. Since most of the sags and swells are unbalanced, this provides limitations to the three-phase inverter-based DVR during unbalanced voltage sags and swells [37]. During the transient operation of the DVR, the load terminals experience a very large voltage overshoot depending on the LC filter parameters. This may affect the DVR operation and may even result in the tripping of the load [38]. The absence of the filter circuit makes the semi-Z-source inverter-based DVR free from such voltage overshoots. In the literature [35], it is clearly mentioned that the cost of the semi-Z-source inverter is less than the single-phase full-bridge inverter. In the DVRs based on the full-bridge inverter and the three-phase inverter, an additional analogue-to-digital converter (ADC) and the voltage sensing element are required to compare the inverter output voltage and the reference voltage for removing the phase shift caused by the filters. This will increase the capital cost of the full-bridge inverter and the three-phase inverter-based DVRs compared to the semi-Z-source inverter-based DVR. The heat sinks, optocouplers and the driver circuits associated with the additional switches in the full-bridge inverter also add to the cost.

3 Proposed DVR Topology with Semi-Z-Source Inverter

Figure 8 displays the single-phase representation of the proposed topology of the DVR with the semi-Z-source inverter marked by the dashed line box. The topology consists of a dc voltage source (V_{dc}), semi-Z-source inverter and an injection transformer. The transformer provides the voltage boosting

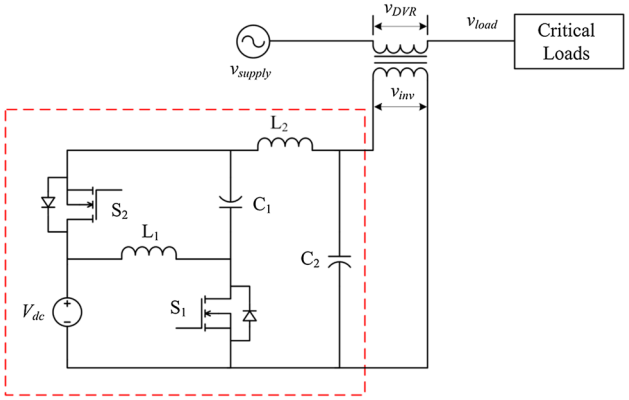

Fig. 8 Proposed DVR topology with semi-Z-source inverter

function and electrical isolation. The secondary of the injection transformer connects the DVR in series with the supply and the load. Here, in this paper, the transformer provides only electrical isolation. According to the sag depth and the phase jump, the semi-Z-source inverter injects the missing voltage through the injection transformer, and thus, the load profile is restored.

For cost-effectiveness, the common practice in DVR technology is to design the DVR with 50% voltage injection capability as most of the sags are limited to 50% sag depth [6,39]. The dc source V_{dc} is selected as 50% of the nominal line voltage peak value. A safety margin is provided to prevent the reverse power flow through the anti-parallel diodes of the switches in the inverter [40]. In the proposed topology, the margin is chosen as 20%.

This paper uses the missing voltage technique described in [41] to detect the sag and to evaluate the missing voltage. During the voltage sag conditions, the missing voltage is determined by subtracting the actual supply instantaneous voltage (v_{supply}) from the desired load instantaneous voltage ($v_{load,ref}$). The reference for DVR voltage is generated with the help of the phase-locked loops (PLL). The missing voltage (v_{mv}) obtained from Eq. (11) is taken as the reference for the DVR output voltage (v_{DVR}). The semi-Z-source inverter outputs the missing voltage, and it is injected to regulate the load profile.

$$v_{mv} = v_{load,ref} - v_{supply} \tag{11}$$

Here, in this single-phase DVR application, the voltage v_{mv} determines the range of the duty cycles D and 1-D of the semi-Z-source inverter switches S_1 and S_2, respectively. Under any sag conditions, the two switches S_1 and S_2 are operated in complementary manner such that the load voltage (v_{load}) matches the load reference voltage ($v_{load,ref}$). The semi-Z-source inverter output (v_{inv}) is equal to v_{DVR} since the turns ratio 'n' of the injection transformer is 1:1. The DVR output voltage $v_{DVR}$is equal to the missing voltage v_{mv} when the load voltage V_{load} is restored to 100%. The modulation index M is dependent on the peak value of the voltage to be injected (V_{mv}) and V_{dc}.

$$v_{mv} = V_{mv} \sin \omega t \tag{12}$$

$$M = \frac{V_{mv}}{V_{dc}} \tag{13}$$

Equations (5) and (6) can be co-related with Eqs. (12) and (13), respectively. The duty cycle D and 1-D of the switches S_1 and S_2 are determined in the same way as given by Eqs. (9) and (10), respectively. The v_{mv} decides the range of modulation index M and the duty cycle D and 1-D of the switches S_1 and S_2, respectively. With MSPWM, the semi-Z-source inverter gives the sinusoidal output voltage with permissible

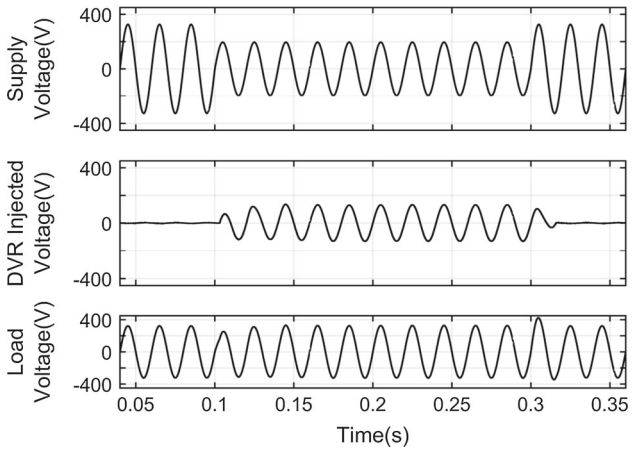

Fig. 9 Load compensation using transformerless DVR based on semi-Z-source inverter

harmonic content. The harmonics present in the semi-Z-source inverter output voltage are within the limits given by IEEE Standard 519-2014. The sinusoidal output voltage from the semi-Z-source inverter is injected in series with the supply and load with the help of an injection transformer. By selecting the injection transformer with appropriate turns ratio 'n', the voltage requirement of the semi-Z-source inverter can be reduced further.

The presence of only a permissible amount of harmonics in the output voltage, even without any additional filter components, makes the semi-Z-source inverter suitable for the transformerless topology of the DVR. Figure 9 shows the load voltage compensation during the sag condition for a single-phase transformerless DVR based on the semi-Z-source inverter. The THD of the load voltage is determined to be only 0.82% without using any of the filtering schemes. The filter circuit is indispensable in a full-bridge inverter-based DVR system. The absence of additional filter components and the Z-source network present in the ac side can be considered as the merits of the semi-Z-source inverter when used in the DVR system.

4 DVR Controller and Modulation Technique

The small-signal modelling of the semi-Z-source inverter is performed by defining the inductor currents and the capacitor voltages as the state variables as given by:

$$x(t) = \left[i_{L_1}(t)\ i_{L_2}(t)\ v_{C_1}(t)\ v_{C_2}(t) \right]^{\mathrm{T}} \tag{14}$$

For the small-signal modelling of the semi-Z-source converter, the passive components in the impedance network are assumed to be lossless. The on resistance and the forward voltage drop of the switches S_1 and S_2 are neglected. The input voltage V_{dc} is an independent voltage source,

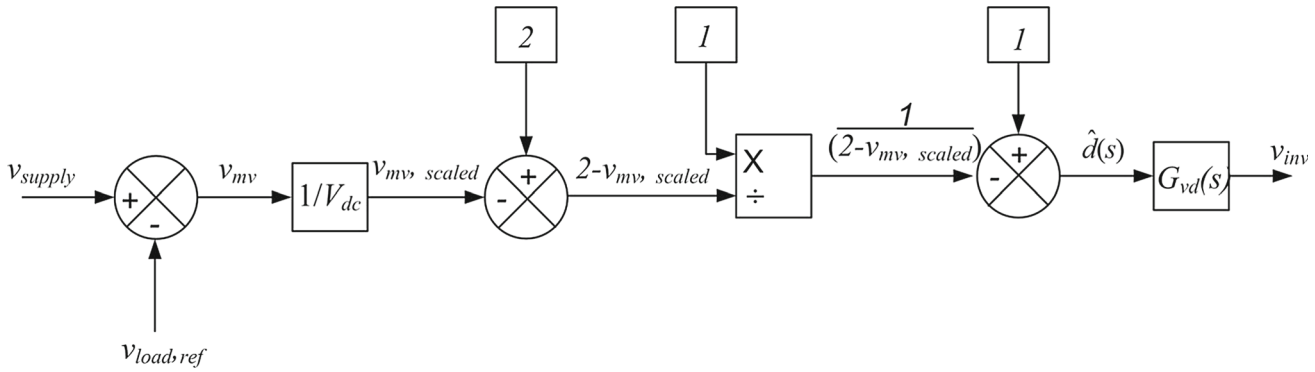

Fig. 10 Feedforward control block diagram

and the load is taken as resistive (R) [42,43]. To derive the small-signal model, perturbations $\hat{v}_{\mathrm{dc}}(t)$and $\hat{d}(t)$are added to the input voltage and the duty cycle and are given by $v_{\mathrm{dc}}(t) = V_{\mathrm{dc}} + \hat{v}_{\mathrm{dc}}(t)$ and $d(t) = D + \hat{d}(t)$, respectively.

In Eq. (19), $G_{v_{\mathrm{dc}}}(s)$ and $G_{v_d}(s)$ represent the input-to-capacitor voltage transfer function and control-to-capacitor voltage transfer function and are given by Eqs. (20) and (21), respectively:

$$G_{v_{\mathrm{dc}}}(s) = \frac{1}{C_2 s}\left[\frac{(D-1)L_1C_1s^2 + D^2(1-D) - (1-D)^3}{L_1L_2C_1s^3 + RL_1C_1s^2 + \left((1-D)^2L_2 - D^2L_1\right)s + R(1-D)^2}\right] \tag{20}$$

$$G_{v_d}(s) = \frac{1}{C_2 s}\left[\frac{\left(D + \frac{1}{1-D}L_1C_1s^2 + (1-D)\right)V_{\mathrm{dc}} + \frac{D}{1-D}L_1I_{L_2}s}{L_1L_2C_1s^3 + RL_1C_1s^2 + \left((1-D)^2L_2 - D^2L_1\right)s + R(1-D)^2}\right] \tag{21}$$

The variation in the state variables due to the perturbations is given by $x(t) = X + \hat{x}$. The small-signal state equations of the semi-Z-source inverter are given by the following equations (see "Appendix"):

$$sL_1 \cdot \hat{i}_{L_1}(s) = (D-1)\hat{v}_{C_1}(s) + D\hat{v}_{\mathrm{dc}}(s) + \frac{V_{\mathrm{dc}}}{(1-D)}\hat{d}(s) \tag{15}$$

$$sL_2 \cdot \hat{i}_{L_2}(s) = -R\hat{i}_{L_2}(s) + D\hat{v}_{C_1}(s) + (D-1)\hat{v}_{\mathrm{dc}}(s) + \frac{V_{\mathrm{dc}}}{(1-D)}\hat{d}(s) \tag{16}$$

$$sC_1 \cdot \hat{v}_{C_1}(s) = (1-D)\hat{i}_{L_1}(s) + D\hat{i}_{L_2}(s) + \frac{I_{L_2}}{(1-D)}\hat{d}(s) \tag{17}$$

$$sC_2 \cdot \hat{v}_{C_2}(s) = \hat{i}_{L_2}(s) \tag{18}$$

The output voltage v_{inv} of the semi-Z-source inverter is the same as the capacitor voltage v_{C_2}. The small-signal expression for the capacitor voltage $\hat{v}_{C_2}$ can be expressed as the linear combination of input voltage and duty cycle perturbation as:

$$\hat{v}_{C_2}(s) = G_{v_{\mathrm{dc}}}(s) \cdot \hat{v}_{\mathrm{dc}}(s) + G_{v_d}(s) \cdot \hat{d}(s) \tag{19}$$

Here, in the proposed DVR topology, the input voltage V_{dc} is considered as a stiff dc source. So, the output voltage expression is reduced to:

$$\hat{v}_{C_2}(s) = G_{v_d}(s) \cdot \hat{d}(s) \tag{22}$$

4.1 Feedforward Control of the Semi-Z-Source Inverter-Based DVR

Figure 10 shows the feedforward control block diagram of the semi-Z-source inverter-based DVR. Robustness and simplicity are the key advantages of the feedforward voltage control in the DVR system [17]. A reference load voltage $v_{\mathrm{load,ref}}$ is generated, and the instantaneous difference between the actual supply v_{supply} and reference load voltage $v_{\mathrm{load,ref}}$ is determined. This difference is equal to zero when there is no PQ problem, assuming the system is lossless. During the sag events, this difference provides the missing voltage v_{mv} as given in Eq. (11), which is the voltage to be injected by the DVR.

In the feedforward control, v_{mv} is scaled by a scaling factor equal to the dc-link voltage (V_{dc}) to obtain the scaled missing voltage ($v_{\mathrm{mv,scaled}}$) similar to the term $M\sin\omega t$ given in the description of the MSPWM technique. This scaled missing

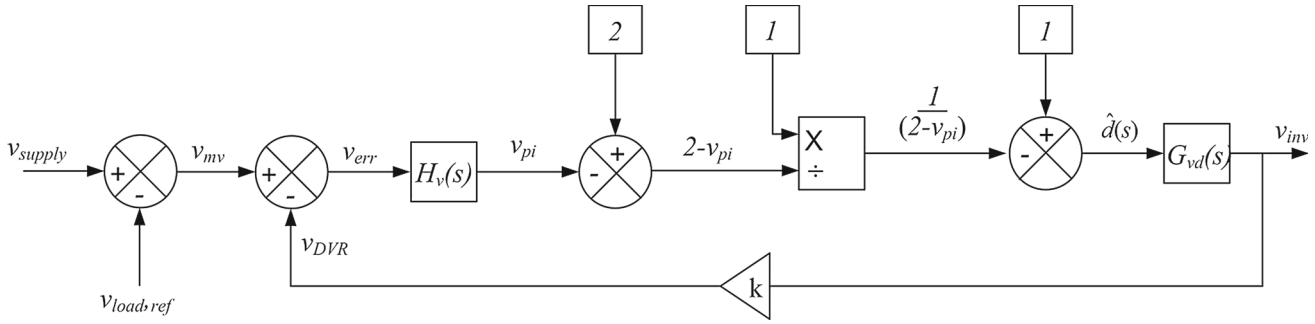

Fig. 11 Modified feedback control block diagram

voltage ($v_{\mathrm{mv,scaled}}$) is modified in the digital controller to obtain the $\hat{d}(s)$, which is analogous to the term given by Eq. (9). Due to the relationship given by Eq. (23), the output of the block $G_{v_d}(s)$ is the inverter voltage,v_{inv}

$$G_{v_d}(s) = \frac{\hat{v}_{C2}(s)}{\hat{d}(s)} \tag{23}$$

4.2 Modified Feedback Control of the Semi-Z-Source Inverter-Based DVR

In this modified feedback control of the proposed DVR topology, the DVR voltage (v_{DVR}) is taken as the feedback parameter. Generation of the missing voltage v_{mv} is the same as that in the feedforward control. In this modified feedback control, the semi-Z-source inverter is controlled in such a manner that at any instant the DVR voltage (v_{DVR}) should match the missing voltage,v_{mv}. The missing voltage v_{mv} is set as the reference for the DVR voltage (v_{DVR}), and the error between them (v_{err}) is corrected using the PI controller.

Figure 11 shows the modified feedback control block diagram for the proposed semi-Z-source inverter-based DVR. Here, as the injection transformer only provides galvanic isolation, v_{DVR} and v_{inv} are the same voltages. The PI controller handles any error between v_{DVR} and v_{mv} given by Eq. (24) [17]. Furthermore, $H_v(s)$ demonstrates the transfer function of the PI controller given by Eq. (25) and its output v_{pi} is similar to the $M\sin\omega t$ term given in the description of the MSPWM technique. From the PI controller output v_{pi}, the signal $\hat{d}(s)$ is obtained using Eq. (9).

$$v_{\mathrm{err}} = v_{\mathrm{mv}} - v_{\mathrm{DVR}} \tag{24}$$

$$H_v(s) = K_p + \frac{K_i}{s} \tag{25}$$

The modified feedback controller also follows Eq. (23), and the inverter output voltage v_{inv} is obtained. A gain 'k' equal to the turns ratio 'n' of the injection transformer (1 in this case) is given to the inverter voltage v_{inv} to obtain the DVR voltage v_{DVR}. The voltage v_{DVR} is compared with the actual reference voltage v_{mv}, and the feedback loop attempts to reduce the error to zero. This control method of the proposed DVR assures the proper tracking of the reference voltage by the semi-Z-source inverter.

5 Design and Simulation Results

The performance of the semi-Z-source inverter DVR and its control technique have been verified using MATLAB/Simulink. The simulation parameters of the single-phase semi-Z-source inverter-based DVR are given in Table 3. The missing voltage technique is used to detect the voltage sag [41]. The in-phase compensation method is adopted as the compensation technique. The feedforward and modified feedback control strategies are utilised for the simulation, and the missing voltage v_{mv} is taken as the reference for the injected voltage v_{DVR}.

Considering the maximum injection of 50% of the single-phase rms voltage, (V_{supply}) and the 20% extra given in the dc source voltage (V_{dc}), the maximum modulation index M_{max} is derived as 0.81 from:

$$M_{\mathrm{max}} = \frac{0.5 * \sqrt{2} * V_{\mathrm{supply}}}{V_{\mathrm{dc}}} \tag{26}$$

Table 3 Simulation parameters

Parameters	Values	
Rated voltage and frequency	230 V and 50 Hz	
Load	800 + j600 VA	
Injection transformer	1:1230 V, 1.6 kVA	
Semi-Z-source Inverter	Dc-link voltage, V_{dc}	200 V
	Switching frequency, f_{sw}	50 kHz
	Capacitor C_1 and C_2	3.9 μF
	Inductor L_1 and L_2	320 μH

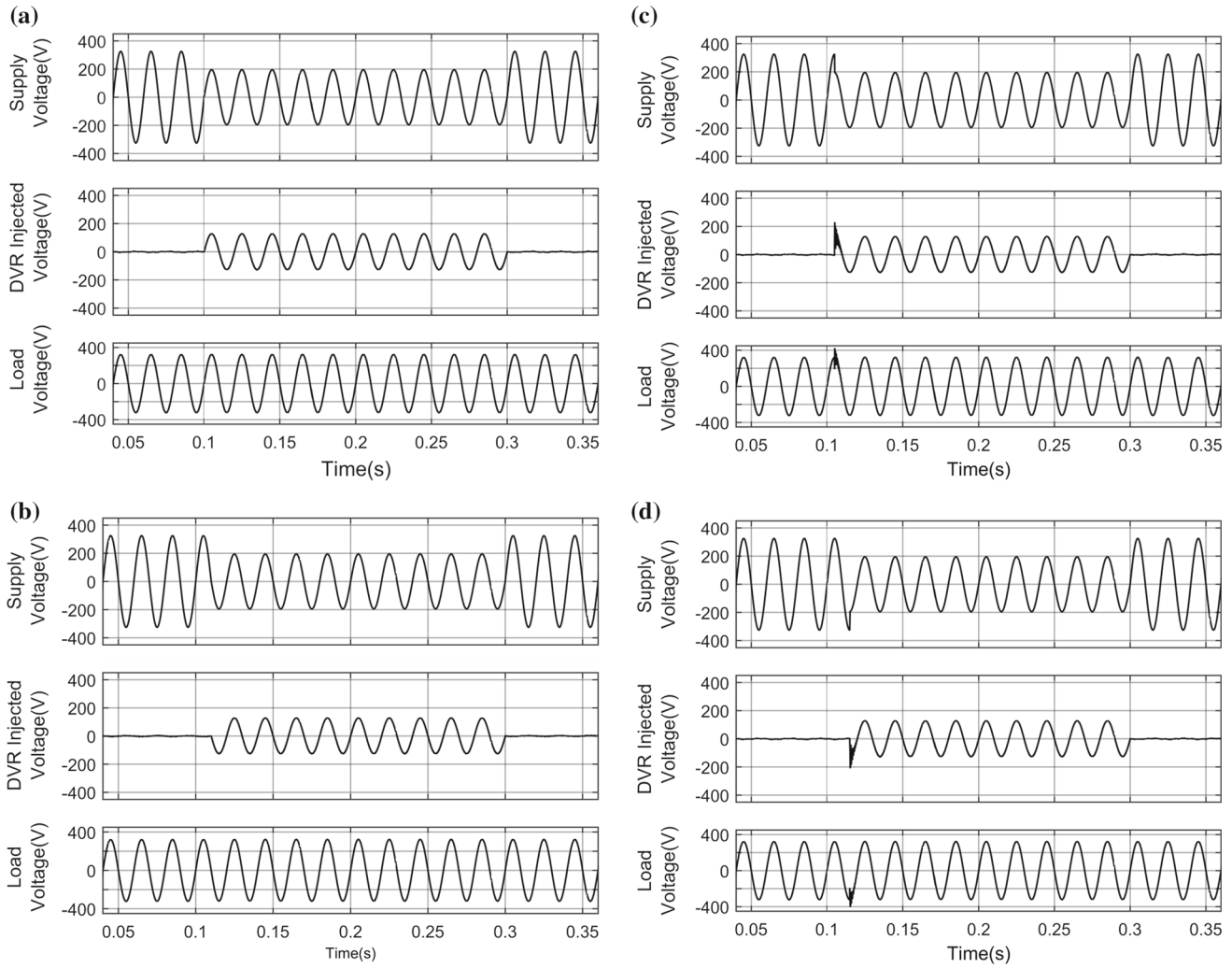

Fig. 12 Compensation using feedforward control. **a** Sag initiation at positive going zero-crossing, **b** sag initiation at negative going zero-crossing, **c** sag initiation at positive peak, **d** sag initiation at negative peak

For obtaining the output voltage range of (+ 115 to − 115 V), the duty cycle D of switch S_1 is changed from 0.16 to 0.644 according to the voltage ratio given in Fig. 5. By varying the duty cycle D from 0.16 to 0.5, the positive output voltage for the maximum injection is obtained. The negative output voltage is obtained when the duty cycle D is varied from 0.5 to 0.644. The inductor and capacitor values of the semi-Z-source inverter are designed by considering the maximum injection capability.

All the simulation results given in this paper show the response of the DVR system for 40% sag in the supply voltage. The DVR system is simulated to protect a linear load of 1 kVA. The four worst cases of the point on wave of sag initiation, namely (a) sag initiation at positive going zero-crossing, (b) sag initiation at negative going zero-crossing, (c) sag initiation at the positive peak and (d) sag initiation at the negative peak, are simulated with system parameters given in Table 3. Figure 12 shows the supply voltage, DVR injected voltage and load voltage when the proposed single-phase semi-Z-source inverter-based DVR is controlled using the feedforward control scheme given in Fig. 10. As depicted, whenever the sag event begins, the semi-Z-source inverter is operated to inject the missing voltage in series with the supply and the load. Irrespective of the sag in the supply voltage, the feedforward controlled DVR restores the load voltage without any delay by injecting the appropriate voltage by the semi-Z-source inverter.

Figure 13 illustrates the corresponding waveforms for the same four worst cases of sag conditions when the semi-Z-source inverter-based DVR is modified feedback controlled using the PI controller. The same system parameters given in Table 3 are used for the simulation of the modified feedback controlled proposed single-phase DVR with K_p and K_i values equal to 0.017 and 1.1, respectively. A half-cycle

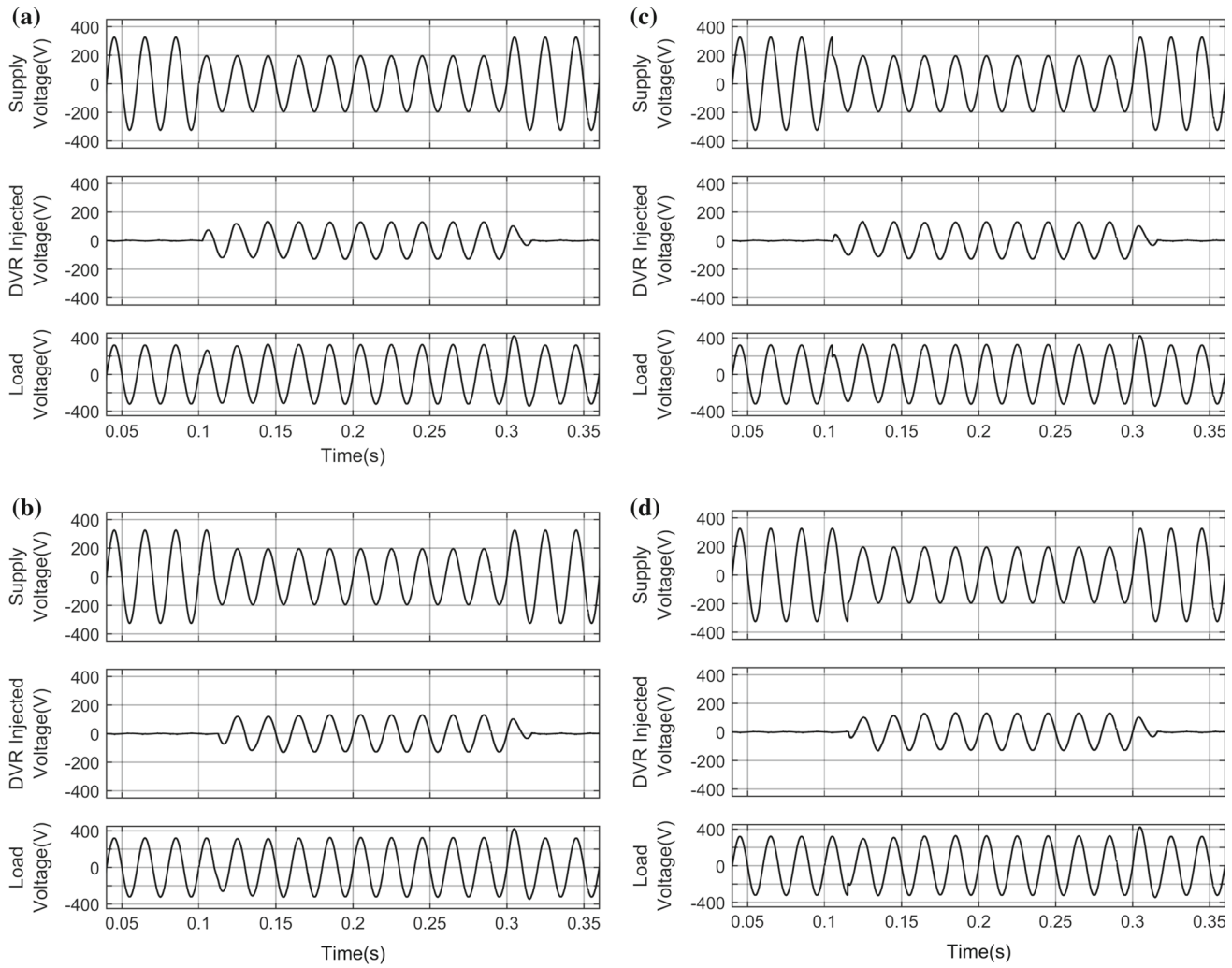

Fig. 13 Compensation using feedback control. **a** Sag initiation at positive going zero-crossing, **b** sag initiation at negative going zero-crossing, **c** sag initiation at positive peak, **d** sag initiation at negative peak

compensation delay is experienced from the point of sag occurrence in this control.

In both the feedforward and modified feedback control of the proposed DVR, the DVR output v_{DVR} tries to match the missing voltage, v_{mv}. The reference voltage is tracked exactly by the semi-Z-source inverter output voltage as given in Fig. 14. The efficiency of the semi-Z-source inverter for mitigating the sag of depth 40% is found to be around 98% from the simulation studies. The steady-state THD analysis of the load voltage for the four worst cases of sags under the feedforward and feedback control is given in Table 4. From time 0.16 s, seven cycles of the load voltage V_{load} are considered for the THD analysis.

A comparison study of the efficiency of the semi-Z-source inverter-based DVR and the full-bridge inverter-based DVR is also conducted for different sag depths. The missing voltage v_{mv} and the modulation index M hold a linear

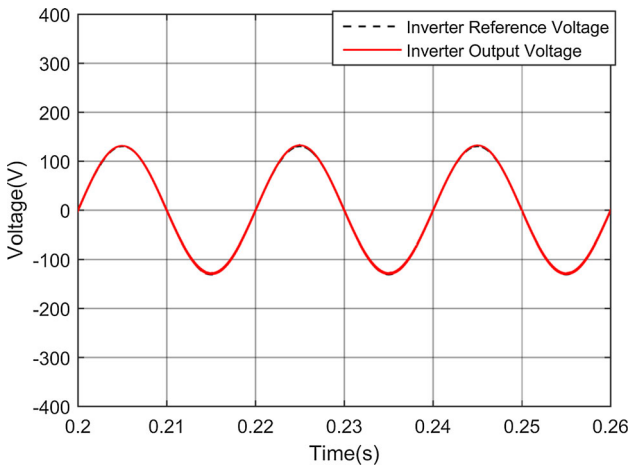

Fig. 14 Magnitude and phase comparison between reference voltage and semi-Z-Source inverter output voltage

Table 4 Load voltage THD analysis

Different cases of point on wave of sag initiation	THD of V_{load}	
	Feedforward control	Feedback control
Sag initiation at positive going zero-crossing	0.73	0.67
Sag initiation at negative going zero-crossing	0.73	0.73
Sag initiation at positive peak	0.73	0.67
Sag initiation at negative peak	0.73	0.81

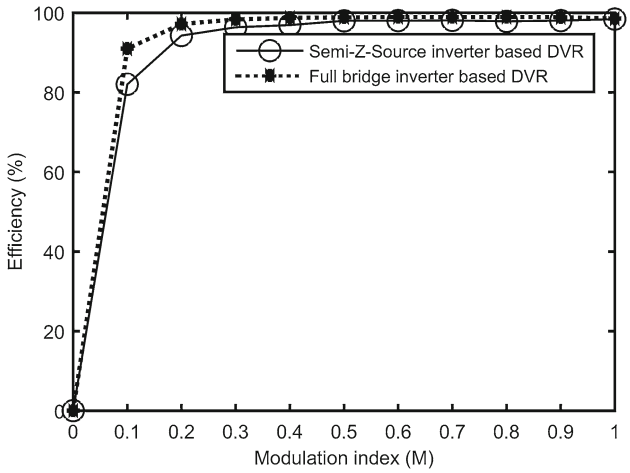

Fig. 15 Efficiency curve

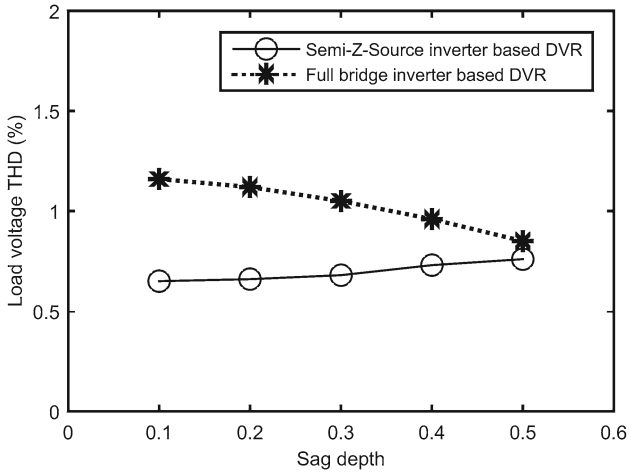

Fig. 16 Load voltage THD versus sag depth

relationship, as given by Eq. (13). The efficiency curve of the DVR based on the semi-Z-source inverter and the full-bridge inverter is plotted against the modulation index M and is illustrated in Fig. 15. The efficiency of the semi-Z-source inverter is comparable with that of the full-bridge inverter. For sag depths up to 50% of the nominal line voltage, the THD of the load voltage is compared for the semi-Z-source inverter-based DVR and the full-bridge inverter-based DVR. As shown in Fig. 16, without using any filtering scheme, the THD of the semi-Z-source inverter-based DVR is better than the full-bridge inverter-based DVR with inverter-side filtering. Altogether, considering the cost, efficiency, THD and performance of the semi-Z-source inverter, it is a better alternative to the full-bridge inverter in DVR applications.

6 Conclusion

This technical note proposes a novel topology of the single-phase DVR based on the semi-Z-source inverter and its feedforward and modified feedback control strategies. The reduced size of the Z-source network, same output voltage range as the full-bridge inverter with a reduced number of switches, the absence of filter components and only a single switch in the current path are some of the advantages of the semi-Z-source inverter. The proposed DVR is controlled using both the feedforward and the modified feedback control scheme. The small-signal modelling of the semi-Z-source inverter, the feedforward and the modified feedback control scheme for the proposed semi-Z-source inverter-based DVR are discussed in detail in Sect. 4. Both the control schemes compensate for the upstream sag conditions efficiently within 10 ms. The feasibility of the proposed topology in restoring the load voltage under sag conditions has been verified in the MATLAB/Simulink environment. The simulation results and Table 4 validate the efficacy of the new topology of the DVR.

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APPENDIX

Small-signal modelling of the semi-Z-source inverter

The inductor currents and capacitor voltages are defined as state variables which is already given in the paper as equation (14)

For state I mode of operation of the semi-Z-source inverter, the differential equations governing the system can be written

in the form $\dot{x}(t) = A_1.x(t) + B_1.u$ as given in equation (27)

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{-R}{L_2} & \frac{1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{dc} \end{bmatrix} \quad (27)$$

For state II mode of operation of the semi-Z-source inverter, the differential equations governing the system can be written in the form $\dot{x}(t) = A_2.x(t) + B_2.u$ as given in equation (28)

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & \frac{-R}{L_2} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{dc} \end{bmatrix} \quad (28)$$

Considering high switching frequency, the dc steady state equations describing the semi-Z-source converter can be written as

$$0 = (DA_1 + (1-D)\,A_2)\,X + (DB_1 + (1-D)\,B_2)\,U \quad (29)$$

By solving (29), the steady state equation of the semi-Z-source inverter given by equations (1) - (4) is obtained.

To derive the small-signal model, perturbations are added to the input voltage and duty cycle as $\hat{v}_{dc}(t)$ and $\hat{d}(t)$ respectively.

In general, small-signal state space equations represented by

$$\hat{\dot{X}} = (DA_1 + (1-D)\,A_2)\,.\hat{X} + (DB_1 + (1-D)\,B_2)\,.\hat{U} + [(A_1 - A_2)\,X + (B_1 - B_2)\,U]\,\hat{d}(t)$$

is given by equation (30)

$$\hat{\dot{X}} = \begin{bmatrix} 0 & 0 & \frac{D-1}{L_1} & 0 \\ 0 & \frac{-R}{L_2} & \frac{D}{L_2} & 0 \\ \frac{-D}{C_1} & \frac{D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix}.\hat{X} + \begin{bmatrix} \frac{D}{L_1} \\ \frac{D-1}{L_2} \\ 0 \\ 0 \end{bmatrix}.\hat{U} + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{-1}{C_1} & \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}.X + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}.U \quad (30)$$

After Laplace transformation of equation (30), equations (15) – (18) are obtained.

The control-to-capacitor voltage transfer function $G_{v_d}(s)$ is obtained by substituting $\hat{v}_{dc} = 0$ in equations (15)-(18). The equations reduce to

$$sL_1.\hat{i}_{L1}(s)|_{\hat{V}_{dc}(s)=0} = (D-1)\,.\hat{v}_{C1}(s) + \frac{V_{dc}}{(1-D)}\hat{d}(s) \quad (31)$$

$$sL_2.\hat{i}_{L2}(s)|_{\hat{V}_{dc}(s)=0} = -R.\hat{i}_{L2}(s) + D\hat{v}_{C1}(s) + \frac{V_{dc}}{(1-D)}\hat{d}(s) \quad (32)$$

$$sC_1.\hat{v}_{C1}(s)|_{\hat{V}_{dc}(s)=0} = (1-D)\,.\hat{i}_{L1}(s) + D.\hat{i}_{L2}(s) + \frac{i_{L2}}{(1-D)}\hat{d}(s) \quad (33)$$

$$sC_2.\hat{v}_{C2}(s)|_{\hat{V}_{dc}(s)=0} = \hat{i}_{L2}(s) \quad (34)$$

From the equations (31) – (34), $\hat{v}_{C2}(s)$ is found out as the product of $\hat{d}(s)$ and $G_{v_d}(s)$ where $G_{v_d}(s)$ is given by equation (21)

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