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Investigation of a family of dual-output coupled/decoupled switched capacitor converter for low-power applications

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Abstract: Here, accurate transresistance calculations for the coupled case and mathematical modelling are provided for dual input–output switched capacitor converter (SCC). This converter offers two different output voltages and produces 36 voltage conversion ratios. The dual input–output SCC is portable and operates by considering either sources or the combination of both V_{s1} and V_{s2} as input sources. The proposed dual input–output SCC has the ability to vary 54 voltage ratios. An efficient low-power SCC is designed for an input voltage range of 1.5–5 V and it gives dual-output voltages of 1–10 V. The proposed converter can operate in both buck and boost modes. The SCC has high drive capability of load current in the range of 10 μA to 100 mA that is adjusted by varying the operating frequency. The accurate equivalent resistance for both coupled and decoupled load cases is found and validated. The results are verified through PSIM simulations and validated experimentally. The mathematical, simulation, and experimental results give excellent proof for proposing the newly designed converter for applications requiring large conversion ratios eliminating inductors.

1 Introduction

Switched capacitor converter (SCC) is a power circuit that implements voltage conversion by switching capacitor elements [1, 2]. It is becoming popular due to its non-magnetic components, smaller size, and higher efficiency [3]. Owing to the employment of small area, SCC facilitates for the development of valuable products such as power-on-a-chip. Another major advantage of SCC is its configurability. Multiple voltage conversion ratios (VCRs) can be achieved with a single circuit by just changing the switching pattern of capacitor elements.

A conventional power management (CPM) IC contains both front-end and back-end DC–DC converter connections. Linear regulators and low drop-out regulators are used to provide multiple output voltages [4]. In order to reduce power losses, both front-end and back-end DC–DC converter need to be efficient. The main disadvantages of CPMs are more weight of the converter devices [5] and larger space consumption. As more filters are used, it consumes more printed board space [6]. Owing to more space consumption, all components need to be implemented using integrated circuits called as PMICs. Recently, all components such as drivers, gates, controllers, and sensing circuits are designed and wrapped in silicon circuits [7]. SCCs are developed by many researchers [6–8]. The advantages of SCCs are non-magnetic elements and it is easy for integration into ICs. Furthermore, SCC has high efficiency in open-loop conditions for fixed input and fixed output VCRs [1, 7]. Hence, portable applications preferred SCC for high-efficiency, low-efficiency drop for the technological processors [8, 9].

The major area of SCC studies is the implementation of the maximum number of VCRs with less number of switches and capacitors. Employing more number of switching and capacitor elements may result in higher losses, and hence less efficiency of SCC. The dual-output Fibonacci SCC proposed by Zhaikhan *et al*. [10] can implement six VCRs by means of ten switches and three capacitors. There are also commercial examples such as MAX integrated, which is single-input dual-output IC SCC [11], single-input SCC from Texas Instruments [12]. Texas Instruments [12] also developed power management IC with 20 regulated outputs. VCRs of the above SCCs are generated employing multiple single-output SCC circuits. Another interest of SCC research is increasing the number of converter inputs. This trend has originated in the line with the utilisation of renewable energy sources. Unreliable operation of renewable energy requires some backup element, such as battery. So, the ability to operate alternatively with battery and renewable energy sources is an important design specification of modern systems. The examples of dual input SCC is described in [13, 14] In [14], summation, subtraction, halving, and negating of inputs is implemented using five separate SCCs, each composing single flying capacitor, two switches, and two diodes. The single-circuit SCC designed by Abraham *et al*. [14] could implement 11 VCRs with 9 switches and 5 diodes. As well as dual input [15], dual output brings a major advantage for the design. This gives simultaneous powering of two loads using the single circuit. Hence, two times less number of components is utilised. An example of dual-output SCC is designed in [16] for limited fractions. This work proposes dual-input and dual-output (DIDO) SCC design which can implement 36 VCRs with 2 capacitors and 11 switches. The proposed SCC is designed as an application for light-emitting diodes (LED). LED is gaining popularity in practice due to high luminous efficiency, fast response, long life span, and high energy efficiency. To assure high efficiency of the overall system, the efficiency of LED driver is important, while the converter is part of the driver. Usually, LED driver selection is based on system power factor, total harmonic distortions, cost, galvanic isolation, and efficiency [17].

For better insight into circuit operations, proper modelling should be employed. The analysis will be based on resistance and transresistance parameters (*R*-parameters) [18]. Two cases are considered for the analysis: decoupled and coupled. Coupling is a term which gives a measure for interdependence of two loads. Mathematically, it is described with parameters R_{12} and R_{21}, which are discussed in [19]. The approach in [19] proposes to treat dual-output ternary SCC as a two-port system [18] which are shown in Figs. 1*a* and *b*.

It should be noted that this method neglects the effect of filter (load) capacitors. As a result, theoretical calculations are less complex. For simulation and experimental measurements of *R*-parameters, it is suggested to use current sources and to measure average output voltages to account for filter capacitors effects.

We considered this work as a model for power management IC. The paper is framed in the following way: Section 2 is about circuit operation principle, described in one sample VCR implementation. In Section 3, modelling of equivalent circuit and calculation of equivalent resistance (*R*-parameters) are discussed. The design is verified with PSIM simulations and hardware implementation and findings are presented in Section 4. The work conclusions and directions of future studies are outlined in Section 5.

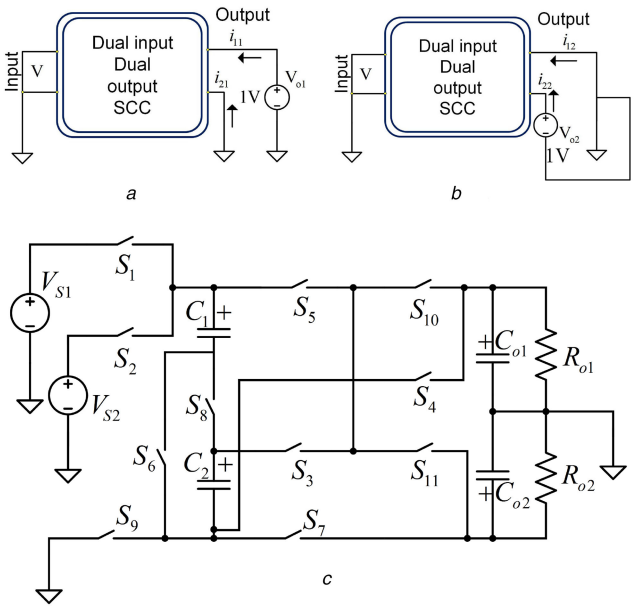


Fig. 1 *Proposed Schematic of DIDO*
(a, b) *General two-port system* [19], ***(c)*** *DIDO SCC* [19]

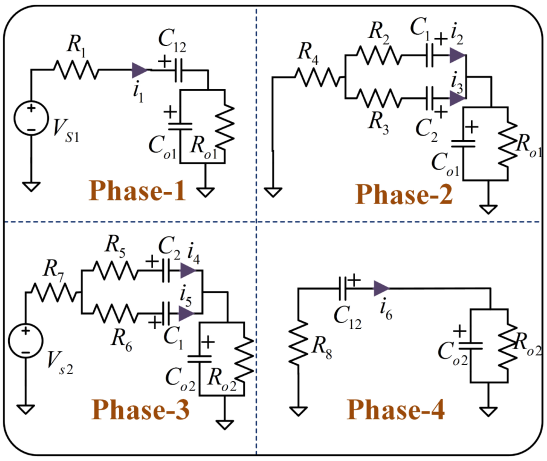


Fig. 2 *Different phases of the proposed converter* $V_{o1} = \frac{1}{3}V_{s1}$ *and* $V_{o2} = \frac{2}{3}V_{s2}$

2 Circuit description

The proposed SCC configuration is illustrated in Fig. 1*c*. It is basically a two-capacitor series–parallel SCC, modified with dual inputs and dual outputs. It can generate 54 VCRs with limited number of switches and capacitors. In total, 2 capacitors and 11 switches are used. The main principle of operation is based on two phase (parallel or series) charging and discharging of flying capacitors. In dual output, the number of phases is doubled, so each of the output VCR implementation is characterised with separate charging and discharging states. Separate implementation of each output VCR reduces the possibility of the cross-coupling effect [10]. For better insight into design, let us consider the implementation of VCR $V_{o1} = (1/3)V_{s1}$ and $V_{o2} = (2/3)V_{s2}$. For configuring to this VCR, four phases ($\phi_1, \phi_2, \phi_3, \phi_4$) are required as shown in Fig. 2. In the phase ϕ_1, two flying capacitors (C_1 and C_2) and load capacitor (C_{o1}) are charged in series. These result in voltage of $(V_{s1} - V_o)/2$ across each of flying capacitors. In the phase ϕ_2, flying capacitors are discharged parallel with the load, which gives $(V_{s1} - V_o)/2 = V_o$ and hence $V_{o1} = (1/3)V_{s1}$. The gain of (2/3) is obtained in similar way, but with parallel charging first and in series discharging (ϕ_3 and ϕ_4). Switching pattern is given in Table 1. All other VCRs are given in Table 2. All the VCRs in Table 2 are explained in the general form, where k, n denote dual input and i, j denote dual-output terminals.

Authors in [14] implemented 11 VCRs using 2 capacitors and 9 switches and 5 diodes. They could obtain gains of 1, 0.5 and 1.5 and 2. Authors in [13] could implement doubling, halving, and inversion. So, the proposed design, apart general advantages of the dual-output system, claims also new non-unity converter gains. It is possible to generate even more number of VCRs such as $V_{o1} = (0.5{*}V_{s1}) + (0.5{*}V_{s2})$ and $V_{o2} = 0.5{*}V_{s1}$. However, such kind of implementations require two outputs to appear in one topology, which may arise cross-regulation phenomenon at the loads [1]. Hence, Zhaikhan *et al.* [1] considered only decoupled VCR implementations. In this paper, coupled case are also considered and verified mathematically.

3 Analysis and modelling of multiple VCRs DIDO SCC

Equivalent resistance analysis is discussed separately for two cases coupled and decoupled by upcoming sections. Configuration is called as decoupled if parameters R_{12} and R_{21}, called 'transresistances', are relatively small. With decoupled loads, dual-output SCC can be treated as two separate single-output SCCs. For coupled case, on the contrary, outputs cross-regulation becomes more apparent. The implementation of VCR $V_{o1} = (1/3)V_{s1}$ and $V_{o2} = (2/3)V_{s2}$ is predetermined as decoupled, since two outputs never appear together in one topology, as shown in Fig. 2. As Fig. 3 shows, topologies of VCR $V_{o1} = 2V_{s1}$ and $V_{o2} = (2V_{s1} + 2V_{s2})$ include phases with simultaneous switching of both loads. Following the same logic, this case is defined as coupled. For both cases, accurate equivalent resistance analysis is solved using a two-port system approach explained in Section 1. Further calculations will validate that for VCR predefined as

Table 1 Pulse pattern of coupled and decoupled VCRs

VCR	Phase	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
$V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$	phase 1	1	0	0	1	0	0	0	1	0	0	0
$V_{o2} = \frac{1}{3}V_{s1}$ and $V_{o1} = \frac{2}{3}V_{s2}$	phase 2	0	0	1	0	1	1	0	0	1	1	0
	phase 3	0	1	1	0	1	1	1	0	0	0	0
	phase 4	0	0	0	0	1	0	0	1	1	0	1
$V_{o1} = 2{*}V_{s1}$	phase 1	0	1	1	0	1	1	0	0	1	0	0
$V_{o2} = (2{*}V_{s1}) + (2{*}V_{s2})$	phase 2	0	0	0	0	1	0	0	1	1	1	0
	phase 3	1	0	1	0	1	1	0	0	1	0	0
	phase 4	0	0	0	1	1	0	0	1	0	0	1

Table 2 All VCRs

*VCRs	No. of VCRs	Remarks
$V_{ok} = V_{si}$ and $V_{on} = 0.5*V_{sj}$.	8	—
$V_{o1} = 1/3*V_{si}$ and $V_{o2} = 1/3*V_{sj}$.	2	$i \neq j$
$V_{o1} = 2/3*V_{si}$ and $V_{o2} = 2/3*V_{sj}$.	2	$i \neq j$
$V_{ok} = 1/3*V_{si}$ and $V_{on} = 2/3*V_{sj}$.	8	—
$V_{ok} = V_{si}$ and $V_{on} = 1/3*V_{sj}$.	8	—
$V_{ok} = V_{si}$ and $V_{on} = 2/3*V_{sj}$.	8	—
$V_{ok} = V_{si}$; $V_{on} = (0.5*V_{s1}) + (0.5*V_{s2})$.	4	—
$V_{ok} = 2*V_{si}$; $V_{on} = (2*V_{s1}) + (2*V_{s2})$.	4	—
$V_{ok} = 2*V_{si}$ and $V_{on} = 1.5*V_{sj}$.	4	—
$V_{ok} = 2*V_{si}$ and $V_{on} = V_{sj}$.	4	—

*V_{ok}/V_{on} = output voltage; V_{si}/V_{sj} = input voltage; where, $i, j, n, k = 1, 2$; $n \neq k$.

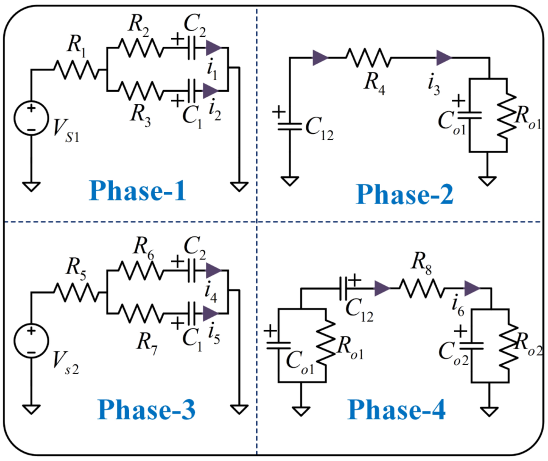


Fig. 3 *Different phases of the proposed converter* $V_{o1} = 2V_{in1}$ *and* $V_{o2} = (2V_{in1}) + (2V_{in2})$

decoupled transresistances are, indeed, practically negligible, while coupling in VCR $V_{o1} = 2V_{s1}$ and $V_{o2} = (2V_{s1} + 2V_{s2})$ is large enough to be accounted in cross-regulation and the detailed discussion is followed in the upcoming sections.

3.1 Decoupled case

In this accurate methodology, for deriving R_{eq}, few steps to be assumed as follows:

i. equal switch resistance (r), equal capacitance of the flying capacitor (C), equal equivalent series resistance (ESR) of the flying capacitor (ESR),
ii. filter (load) capacitors effect is neglected.

Using Table 1 and above assumptions, (1)–(4) and (37)–(40) were derived using different phases that are shown in Fig. 2. Similarly, for the coupled case, different phases and equations are discussed in Section 3.2. Time constants for different phases (phase 1 – T_1; phase 2 – T_2, T_3; phase 3 – T_4, T_5; phase 4 – T_6) are found using Fig. 2 and are given in (5)–(8). Owing to the symmetry of phases 2 and 3, the corresponding time constants are similar to each other

$$R_1 = 3r + 2\text{ESR}; \quad R_2 = 2r + \text{ESR}; \quad R_3 = r + \text{ESR}; \tag{1}$$

$$R_4 = 2r; \quad R_5 = 2r + \text{ESR}; \quad R_6 = r + \text{ESR}; \tag{2}$$

$$R_7 = 2r; \quad R_8 = 4r + 2\text{ESR}; \tag{3}$$

$$C_1 = C; \quad C_2 = C; \quad C_{12} = C/2. \tag{4}$$

$$T_1 = \frac{C(2\text{ESR} + 3r)}{2}; \tag{5}$$

$$T_2 = T_4 = \frac{2C(\text{ESR}^2 + 7\text{ESR}r + 8r^2)}{2\text{ESR} + 7r + (\sqrt{17})r}; \tag{6}$$

$$T_3 = T_5 = \frac{2C(\text{ESR}^2 + 7\text{ESR}r + 8r^2)}{2\text{ESR} + 7r - (\sqrt{17})r}; \tag{7}$$

$$T_6 = C(\text{ESR} + 2r)\,. \tag{8}$$

A voltage source (V) is applied at output 1 (input voltages and output 2 are short-circuited) as shown in Fig. 1*a*. Capacitor voltage expressions for each phase as discussed in Fig. 2 are given below

$$V_{1C12}(t) = -V + (V_{1C12}(0) + V)\mathrm{e}^{(-t/T_1)}; \tag{9}$$

$$V_{2C1}(t) = V + a_{11}\mathrm{e}^{(-t/T_2)} + a_{12}\mathrm{e}^{(-t/T_3)}; \tag{10}$$

$$V_{2C2}(t) = V + a_{21}\mathrm{e}^{(-t/T_2)} + a_{22}\mathrm{e}^{(-t/T_3)}; \tag{11}$$

$$V_{3C1}(t) = a_{31}\mathrm{e}^{(-t/T_4)} + a_{32}\mathrm{e}^{(-t/T_5)}; \tag{12}$$

$$V_{3C2}(t) = a_{41}\mathrm{e}^{(-t/T_4)} + a_{42}\mathrm{e}^{(-t/T_5)}; \tag{13}$$

$$V_{4C12}(t) = V_{4C12}(0)\mathrm{e}^{(-t/T_6)}. \tag{14}$$

To find unknown coefficients, a set of ten linear equations need to be derived. Among that, five equations are from capacitor voltage continuity principle which are given below

$$V_{1C12}(T/4) = V_{2C1}(0) + V_{2C2}(0); \tag{15}$$

$$V_{2C1}(T/4) = V_{3C1}(0); \quad V_{2C2}(T/4) = V_{3C2}(0); \tag{16}$$

$$V_{3C1}(T/4) + V_{3C2}(T/4) = V_{4C12}(0); \tag{17}$$

$$V_{4C12}(T/4) = V_{1C12}(0), \tag{18}$$

where T is a switching period.

The other two equations are from partial KVL (only exponential terms) of phase 2 are given below

$$i_2(t)R_2 - V_{2C1}(t) = i_3(t)R_3 - V_{2C2}(t); \tag{19}$$

$$\left(\frac{R_2C_1}{T_2} - 1\right)a_{11} = \left(\frac{R_3C_2}{T_2} - 1\right)a_{21}; \tag{20}$$

$$\left(\frac{R_2C_1}{T_3} - 1\right)a_{12} = \left(\frac{R_3C_2}{T_3} - 1\right)a_{22}\,. \tag{21}$$

The other two equations are from partial KVL (only exponential terms) of phase 3 are given below

$$i_4(t)R_2 - V_{3C2}(t) = i_3(t)R_6 - V_{3C1}(t); \tag{22}$$

$$\left(1-\frac{R_5C_1}{T_4}\right)a_{41}=\left(1-\frac{R_6C_1}{T_4}\right)a_{31}; \tag{23}$$

$$\left(1-\frac{R_5C_1}{T_5}\right)a_{42}=\left(1-\frac{R_6C_1}{T_5}\right)a_{32}. \tag{24}$$

Further one equation is from charge conservation between two capacitor plates C_1 and C_2 during phases 1 and 4 is given in the below equation

$$C_2V_{3C2}(T/4)-C_1V_{3C1}(T/4)=C_2V_{2C2}(0)-C_1V_{2C1}(0). \tag{25}$$

Average currents from the loads (I_{11} and I_{21}) are given by

$$I_{11}=-\frac{1}{T}\left(\int_0^{(T/4)}i_1(t)\mathrm{d}t+\int_0^{(T/4)}(i_2(t)+i_3(t))\mathrm{d}t\right); \tag{26}$$

$$I_{21}=-\frac{1}{T}\left(\int_0^{(T/4)}i_6(t)\mathrm{d}t+\int_0^{(T/4)}(i_4(t)+i_5(t))\mathrm{d}t\right). \tag{27}$$

Y-parameters (Y_{11} and Y_{21}) are calculated as

$$Y_{11}=\frac{I_{11}}{V};\quad Y_{21}=\frac{I_{21}}{V}. \tag{28}$$

A voltage source (V) is applied at output 2 (input voltages and output 1 are short-circuited) as shown in Fig. 1*b*. Capacitor voltage expressions for each phase are given below

$$V_{1C12}(t)=(V_{1C12}(0)+V)\mathrm{e}^{(-t/T_1)}; \tag{29}$$

$$V_{2C1}(t)=a_{11}\mathrm{e}^{(-t/T_2)}+a_{12}\mathrm{e}^{(-t/T_3)}; \tag{30}$$

$$V_{2C2}(t)=a_{21}\mathrm{e}^{(-t/T_2)}+a_{22}\mathrm{e}^{(-t/T_3)}; \tag{31}$$

$$V_{3C1}(t)=-V+a_{31}\mathrm{e}^{(-t/T_4)}+a_{32}\mathrm{e}^{(-t/T_5)}; \tag{32}$$

$$V_{3C2}(t)=-V+a_{41}\mathrm{e}^{(-t/T_4)}+a_{42}\mathrm{e}^{(-t/T_5)}; \tag{33}$$

$$V_{4C12}(t)=V+(V_{4C12}(0)-V)\mathrm{e}^{(-t/T_6)}. \tag{34}$$

Similar steps are followed for solving the set of ten linear equations as discussed in previous equations. The derivation of average currents from the loads I_{12} is similar to I_{11}, while I_{22} is similar to I_{21}. Y-parameters (Y_{12} and Y_{22}) are calculated as given in the below equation

$$Y_{12}=\frac{I_{12}}{V};\quad Y_{22}=\frac{I_{22}}{V}. \tag{35}$$

R-parameters are reciprocal to Y-parameters as given by

$$\begin{bmatrix}R_{11} & R_{12}\\ R_{21} & R_{22}\end{bmatrix}=\begin{bmatrix}Y_{11} & Y_{12}\\ Y_{21} & Y_{22}\end{bmatrix}^{-1}. \tag{36}$$

The final expression of R-parameters is quite long and cannot be added in this paper due to page constraints. The calculations were made symbolically in Matlab software. The final results of the decoupled case are discussed in Section 4.

3.2 Coupled case

Coupling is one of the major issues of dual-output converter, but for the proposed converters, it is an issue for only certain number of VCRs. Zhaikhan *et al.* in [1] discussed that VCRs with cross-regulation of outputs are a topic of future studies. For low-power and low current converters, the coupling effect will be too minimum, so it is negligible. The coupled case boost VCRs are discussed in Table 2. To solve the coupling case, the R-parameters are derived using the following analytical process, i.e. RC network and partial KVL methods. For simplicity, $V_{o1}=(2{*}V_{\mathrm{in1}})+(2{*}V_{\mathrm{in2}})$ and $V_{o2}=2{*}V_{\mathrm{in1}}$ VCR are considered for upcoming R-parameters analysis. The same assumptions, which are discussed in Section 3.1, are followed. From Fig. 3, phases 2 and 4 are the first-order RC circuits, while phases 1 and 3 are the higher order ones. Therefore, phases 2 and 4 have one time constant (T_3 and T_6, respectively), whereas phases 1 and 3 have two time constants (T_1 and T_2; T_4 and T_5, respectively). In addition, time constant values for phases 1 and 3 (as well as phases 2 and 4) are similar due to the equivalence of topologies

$$R_1=2r;\quad R_2=2r+\mathrm{ESR};\quad R_3=r+\mathrm{ESR}; \tag{37}$$

$$R_4=4r+2\mathrm{ESR};\quad R_5=2r;\quad R_6=2r+\mathrm{ESR}; \tag{38}$$

$$R_7=r+\mathrm{ESR};\quad R_8=4r+2\mathrm{ESR}; \tag{39}$$

$$C_1=C;\quad C_2=C;\quad C_{12}=C/2; \tag{40}$$

$$T_1=T_4=2C\frac{(\mathrm{ESR}^2+7\mathrm{ESR}r+8r^2)}{(2\mathrm{ESR}+7r+(\sqrt{17})r)}; \tag{41}$$

$$T_2=T_5=2C\frac{(\mathrm{ESR}^2+7\mathrm{ESR}r+8r^2)}{(2\mathrm{ESR}+7r-(\sqrt{17})r)}; \tag{42}$$

$$T_3=T_6=C(\mathrm{ESR}+2r). \tag{43}$$

From Fig. 1*a*, voltage source (V) is applied at output 1 (input voltages and output 2 are short-circuited). Capacitor voltage expressions for each phase are given by

$$V_{1C1}(t)=a_{11}\mathrm{e}^{(-t/T_1)}+a_{12}\mathrm{e}^{(-t/T_2)}; \tag{44}$$

$$V_{1C2}(t)=a_{21}\mathrm{e}^{(-t/T_1)}+a_{22}\mathrm{e}^{(-t/T_2)}; \tag{45}$$

$$V_{2C12}(t)=V+(V_{2C12}(0)-V)\mathrm{e}^{(-t/T_3)}; \tag{46}$$

$$V_{3C1}(t)=a_{31}\mathrm{e}^{(-t/T_4)}+a_{32}\mathrm{e}^{(-t/T_5)}; \tag{47}$$

$$V_{3C2}(t)=a_{41}\mathrm{e}^{(-t/T_4)}+a_{42}\mathrm{e}^{(-t/T_5)}; \tag{48}$$

$$V_{4C12}(t)=-V+(V_{4C12}(0)+V)\mathrm{e}^{(-t/T_6)}. \tag{49}$$

To find unknown coefficients, a set of ten linear equations need to be derived. Among that, five equations are from capacitor voltage continuity principle that are given in (15)–(18)

$$V_{1C1}(T/4)+V_{1C2}(T/4)=V_{2C12}(0); \tag{50}$$

$$V_{2C12}(T/4)=V_{3C1}(0)+V_{3C2}(0); \tag{51}$$

$$V_{3C1}(T/4)+V_{3C2}(T/4)=V_{4C12}(0); \tag{52}$$

$$V_{4C12}(T/4)=V_{1C1}(0)+V_{1C2}(0). \tag{53}$$

Other two equations are from charge conservation between two capacitor plates C_1 and C_2 during phases 2 and 4 which are given by

$$C_2V_{1C2}(T/4)-C_1V_{1C1}(T/4)=C_2V_{3C2}(0)-C_1V_{3C1}(0); \tag{54}$$

$$C_2V_{3C2}(T/4)-C_1V_{3C1}(T/4)=C_2V_1C2(0)-C_1V_{1C1}(0). \tag{55}$$

The other two equations are from partial KVL (only exponential terms) of phase 1 which are given by

$$i_1(t)R_2+V_{1C2}(t)=i_2(t)R_3+V_{1C1}(t); \tag{56}$$

Table 3 Modelling and analysis comparison of VCR (decoupled and coupled)

Decoupled case: $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$								
***f*, kHz**	**Modelling**				**Simulation**			
	$R_{11}(\Omega)$	$R_{21}(\Omega)$	$R_{12}(\Omega)$	$R_{22}(\Omega)$	$R_{11}(\Omega)$	$R_{21}(\Omega)$	$R_{12}(\Omega)$	$R_{22}(\Omega)$
10	2.50	−0.18	−0.32	2.61	2.49	−0.16	−0.29	2.60
50	2.01	0.02	−0.05	2.17	2.01	0.02	−0.05	2.17
100	1.99	0.01	−0.03	2.15	1.99	0.01	−0.03	2.15
Coupled case: $V_{o1} = (2{*}V_{s1}) + (2{*}V_{s2})$ and $V_{o2} = 2{*}V_{s1}$								
10	14.75	21.28	21.28	42.56	14.69	21.12	21.12	42.38
50	12.69	19.67	19.67	39.34	12.58	19.46	19.46	38.96
100	12.62	19.62	19.62	39.23	12.51	19.41	19.41	38.85

Table 4 Parameter for DIDO converter

Sl. no	Parameters	Quantity
1	MAX4678 switch $(S_1 - S_{11})$	11
2	flying capacitor(C_1 and C_2)	22 μF
3	output capacitor(C_{o1} and C_{o2})	220 μF
4	load resistance (R_{o1} and R_{o2})	200 Ω to 200 kΩ
5	ESR (C_1 and C_2)	100 mΩ
6	switch on resistance (r_{on})	0.3
7	input voltage range (V_{s1} and V_{s2})	1–5 V
8	output voltage range (V_{o1} and V_{02})	0.1–10 V

$$\left(1 - \frac{R_2C_2}{T_1}\right)a_{21} = \left(1 - \frac{R_3C_1}{T_1}\right)a_{11}; \tag{57}$$

$$\left(1 - \frac{R_2C_2}{T_1}\right)a_{22} = \left(1 - \frac{R_3C_1}{T_1}\right)a_{12}. \tag{58}$$

The last two equations are from partial KVL of phase 3 which are given by

$$i_4(t)R_6 + V_{3C2}(t) = i_5(t)R_7 + V_{3C1}(t); \tag{59}$$

$$\left(1 - \frac{R_6C_2}{T_4}\right)a_{41} = \left(1 - \frac{R_7C_1}{T_4}\right)a_{31}; \tag{60}$$

$$\left(1 - \frac{R_6C_2}{T_5}\right)a_{42} = \left(1 - \frac{R_7C_1}{T_5}\right)a_{32}. \tag{61}$$

Average currents from the loads (I_{11} and I_{21}) are given by

$$I_{11} = \frac{1}{T}\left(\int_0^{(T/4)} i_6(t)\mathrm{d}t - \int_0^{(T/4)} i_3(t)\mathrm{d}t\right); \tag{62}$$

$$I_{21} = -\frac{1}{T}\int_0^{(T/4)} i_6(t)\mathrm{d}t. \tag{63}$$

Similarly, *Y*-parameters (Y_{11} and Y_{21}) are calculated as

$$Y_{11} = \frac{I_{11}}{V}; \quad Y_{21} = \frac{I_{21}}{V}. \tag{64}$$

From Fig. 1*b*, voltage source (V) is applied at output 2 (input voltages and output 1 are short-circuited). Capacitor voltage expressions for each phase [same as previous except $V_{2C12}(t)$ and $V_{4C12}(t)$] are given by

$$V_{2C12}(t) = V_{2C12}(0)\mathrm{e}^{(-t/T_3)}; \tag{65}$$

$$V_{4C12}(t) = V + (V_{4C12}(0) - V)\mathrm{e}^{(-t/T_6)}. \tag{66}$$

The set of ten linear equations are similar to the previous case. The derivation of average currents from the loads I_{12} is similar to I_{11}, while I_{22} is similar to I_{21}. *Y*-parameters (Y_{12} and Y_{22}) are calculated as it is shown in the below equation

$$Y_{12} = \frac{I_{12}}{V}; \quad Y_{22} = \frac{I_{22}}{V}. \tag{67}$$

Using (36), we can easily find the *R*-parameters. The final expression of *R*-parameters is quite long and cannot be expressed in this paper due to paper constraints. Symbolic calculations were made in Matlab software. The final results are discussed in Section 4.

4 Validation of equivalent resistance

Analysis is performed with voltage sources at the outputs, whereas simulations (and also experiment) with current sources. The use of current sources accounts the filter capacitors effect, while the use of voltage sources neglects it. The results almost coincide. The deviation of the results is caused by the filter capacitors. For the *decoupled case*, R_{eq} values are validated based on the *R*-parameters. Table 3 (decoupled case) shows output voltages simulation results for 5 V input sources and load resistances equal to their corresponding equivalent resistances. Table 3 shows that the results of simulation are in good agreement with rated values of the proposed converter. As can be observed from calculation and simulation results of the decoupled case (Table 3), transresistances (R_{12} and R_{21}) have very small values as was expected. In addition, it should be noted that in some cases, transresistance values are negative, i.e. from the model developed in [18, 19], output voltage values will be increased such that the cross-regulation effect is positive. For the *coupled case*, modelling and simulation comparison are discussed in Table 3 (coupled case) where it shows agreement to each other.

5 Simulation results, experimental results, and discussion

The simulation, experimental simulation, experimental results are discussed for validation real-time parameters are chosen which is shown in Table 4. For simplicity and better understanding, coupled and decoupled analyses are performed for different VCRs. For the *decoupled case*, $[V_{o1} = (1/3)V_{s1}$ and $V_{o2} = (2/3)V_{s2}]$ is chosen and solved mathematically, and it is validated by simulation and

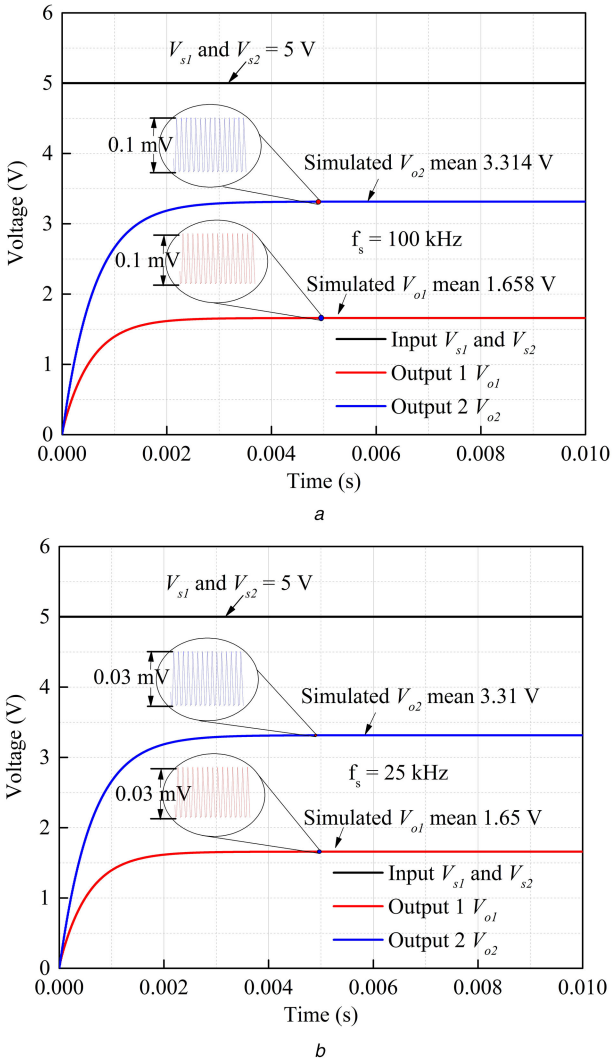


Fig. 4 *Simulation results of* $V_{o1} = \frac{1}{3}V_{s1}$ *and* $V_{o2} = \frac{2}{3}V_{s2}$

(a) Output voltage, input voltage, and voltage ripple of V_{o1} and V_{o2} of $f_s = 25$ kHz, ***(b)*** Output voltage, input voltage, and voltage ripple of V_{o1} and V_{o2} of $f_s = 100$ kHz

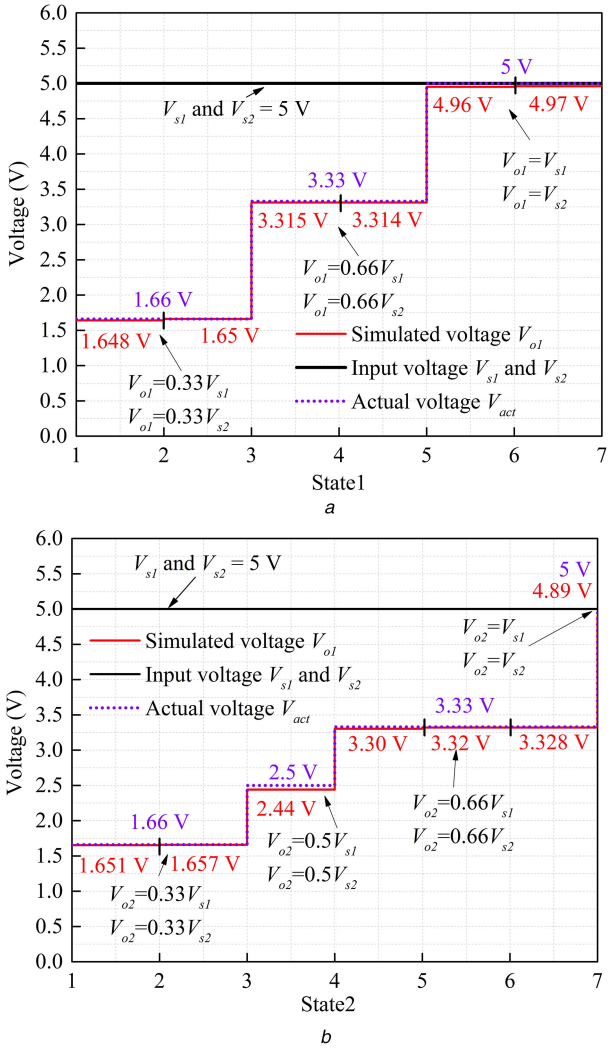


Fig. 5 *Comparison of simulated and actual output voltages of different VCRs*

(a) Output voltage V_{o1} VCRs, ***(b)*** Output voltage V_{o2} VCRs

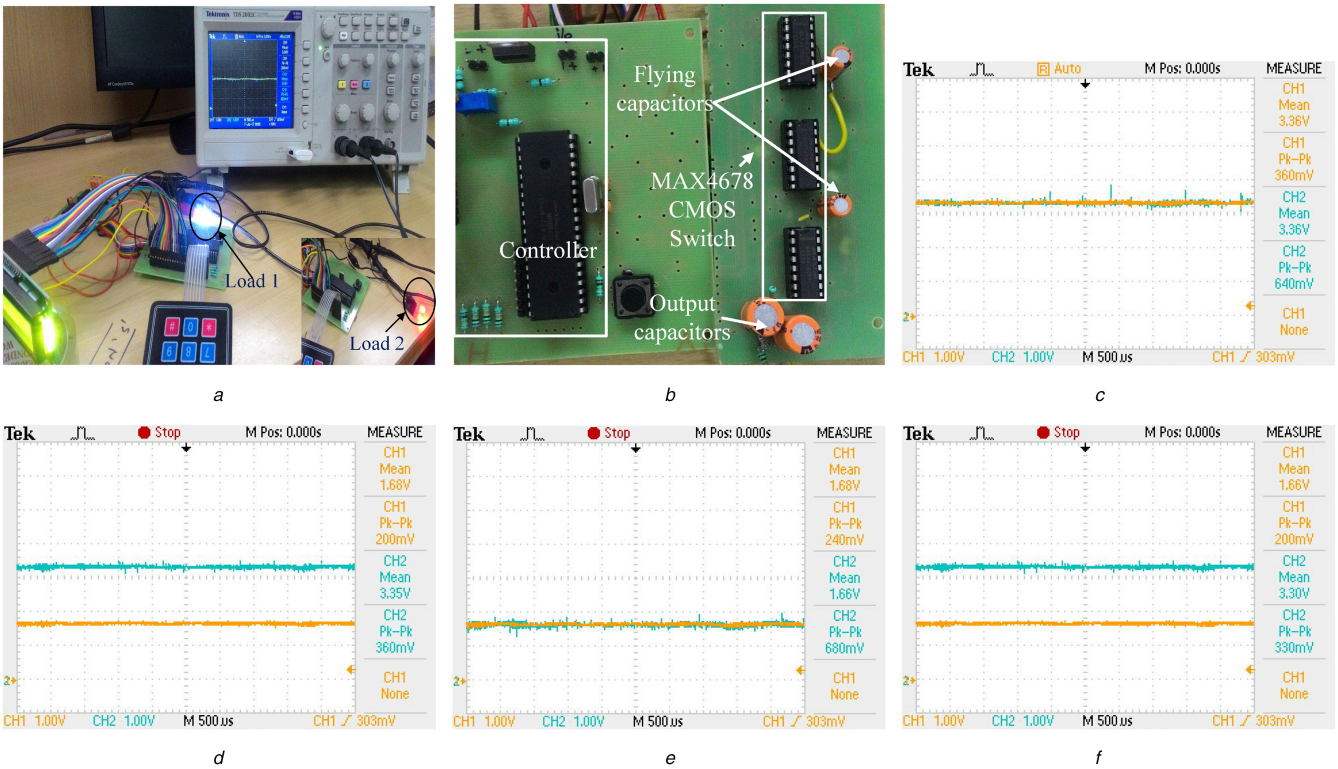
Table 5 Modelled, simulated, and experimental comparison of VCRs (all the values in the table are rounded to nearest points)

VCRs	Frequency, kHz	V_{o1}			V_{o2}		
		Model, V	Simulated, V	Hardware, V	Model, V	Simulated, V	Hardware, V
decoupled	50	1.66	1.66	1.57	3.32	3.32	2.98
	100	1.66	1.66	1.6	3.32	3.32	3.01
coupled	50	2.98	2.97	2.52	5.97	5.95	5.12
	100	2.98	2.98	2.59	5.97	5.96	5.25

experimental results which are shown in Table 3 (decoupled). To verify the design, PSIM simulation tool was used. Figs. 4*a* and *b* illustrate the output voltages of V_{o1} and V_{o2} VCR ($V_{o1} = (1/3)V_{s1}$ and $V_{o2} = (2/3)V_{s2}$) and voltage ripples are plotted for frequency 25 and 100 kHz, respectively. Similarly, Fig. 4*b* illustrates the output voltages and voltage ripples of VCR ($V_{o1} = (1/3)V_{s1}$) and ($V_{o2} = (2/3)V_{s2}$) of frequency 100 kHz. Table 5 shows the compared results of model, simulated, and experimental results which are in good agreement to verify the proposed converter. Finally, comparison of all VCRs is discussed using Fig. 5 and Table 6. Figs. 6*a* and *b* show the proposed SCC prototype. Figs. 6*c–f* show the output voltage of V_{o1} and V_{o2} for a VCR of ($V_{o1} = (1/3)V_{s1}$) and ($V_{o2} = (2/3)V_{s2}$) and ($V_{o1} = (2/3)V_{s1}$ and $V_{o2} = (2/3)V_{s2}$) for different load current of 10 and 100 mA. Fig. 7*a* shows various load conditions of the proposed SCC. Fig. 7*b* shows good agreement for hardware and simulation output. For hardware set-up, input (V_{s1} and V_{s2}) are treated as ≅ 5.1 V. The load change for different voltages is performed as given in Fig. 8*a*. Switching frequency (f_s) is varied accordingly to verify the proposed converter efficiency. In the *coupled case*, boost converter usage is very low compared to buck converter for low-power applications, i.e. whenever boost converter is required, V_{s2} source is used. For simplicity, $V_{o1} = (2*V_{s1}) + (2*V_{s2})$ and $V_{o2} = 2*V_{s1}$ VCR is considered for simulation, modelling, and experimental verification. The VCRs are solved mathematically and it is validated by simulation and experimental results which are shown in Table 3 (coupled case). Fig. 8*b* shows the coupled case VCRs of the proposed converter and validates by comparing with hardware and simulation results. The input voltage used for coupled VCRs is 1.5–3 V because MAX4567 switch [15] has limitation of 10 V. Finally, Table 5 discusses modelled, simulated, and experimental comparison of coupled and decoupled VCR, which shows that values are in good agreement to each other. The comparison results of the previous work based on switching DIDO converters are

Table 6 Comparison table for different VCRs

VCRs	State 1	State 2	Actual V_{o1}, V	Simulated V_{o1}, V	Actual V_{o2}, V	Simulated V_{o2}, V
$V_{o1}=\frac{1}{3}V_{s1}$ and $V_{o2}=\frac{1}{3}V_{s2}$	1	1	1.66	1.65	1.66	1.65
$V_{o1}=\frac{1}{3}V_{s2}$ and $V_{o2}=\frac{1}{3}V_{s1}$	2	2	1.66	1.65	1.66	1.66
$V_{o1}=\frac{1}{3}V_{s1}$ and $V_{o2}=\frac{2}{3}V_{s2}$	1	4	1.66	1.65	3.33	3.30
$V_{o1}=\frac{1}{3}V_{s2}$ and $V_{o2}=\frac{2}{3}V_{s1}$	2	5	1.66	1.65	3.33	3.32
$V_{o1}=\frac{2}{3}V_{s1}$ and $V_{o2}=\frac{2}{3}V_{s2}$	3	4	3.33	3.32	3.33	3.30
$V_{o1}=\frac{2}{3}V_{s2}$ and $V_{o2}=\frac{2}{3}V_{s1}$	4	5	3.33	3.31	3.33	3.32
$V_{o1}=V_{s1}$ and $V_{o2}=\frac{1}{2}V_{s2}$	5	3	5.00	4.96	2.50	2.44
$V_{o1}=V_{s2}$ and $V_{o2}=\frac{1}{2}V_{s1}$	6	3	5.00	4.97	2.50	2.44
$V_{o1}=V_{s1}$ and $V_{o2}=\frac{1}{3}V_{s2}$	5	1	5.00	4.96	1.66	1.65
$V_{o1}=V_{s2}$ and $V_{o2}=\frac{1}{3}V_{s1}$	6	2	5.00	4.97	1.66	1.66
$V_{o1}=V_{s1}$ and $V_{o2}=\frac{2}{3}V_{s2}$	5	5	5.00	4.96	3.33	3.32
$V_{o1}=V_{s2}$ and $V_{o2}=\frac{1}{3}V_{s1}$	6	6	5.00	4.97	3.33	3.33



a *b* *c*

d *e* *f*

Fig. 6 *Experimental results for different VCRs for 10 and 100 mA. This experimental set-up is for validating the prototype model of DIDO converter using hardware components. With the help of this model, we can easily design a PMIC*

(a) Prototype of DIDO SCC with different load condition, ***(b)*** Prototype of DIDO SCC, ***(c)*** Output voltage of V_{o1} and V_{o2}, $V_{o1}=(2/3)V_{s1}$ and $V_{o2}=(2/3)V_{s2}$ for 10 mA, ***(d)*** Output voltage of V_{o2} and V_{o1}, $V_{o1}=(2/3)V_{s1}$ and $V_{o2}=(1/3)V_{s2}$ for 100 mA, ***(e)*** Output voltage of V_{o1} and V_{o2}, $V_{o1}=(1/3)V_{s1}$ and $V_{o2}=(1/3)V_{s2}$ for 100 mA, ***(f)*** Output voltage of V_{o1} and V_{o2}, $V_{o1}=(1/3)V_{s1}$ and $V_{o2}=(2/3)V_{s2}$ for 10 mA

discussed in detail and are shown in Table 7. The DIDO converter provides high efficiency and maximum VCRs can be generated. The major advantage of the proposed converter is that VCRs can be generated independently in each output terminals. The capacitor ESR and ESL (effective series inductance) may degrade the SCC performance by increasing its equivalent resistance. ESR may be accounted for by combining it with a series switch (MAX4678) resistance(s). The deteriorating effect for ESL (stray inductance) manifests itself starting from relatively high switching frequency (above FSL). The load or filter capacitance may have an impact on equivalent resistance for relatively slow switching frequencies (near SSL). To have this effect ignorable, the filter capacitance must be larger than switched capacitances by an order of magnitude. On the other hand, it is known that the effect of not sufficiently large filter capacitance is equivalent to resistance reduction. Therefore, equivalent resistance calculated in the

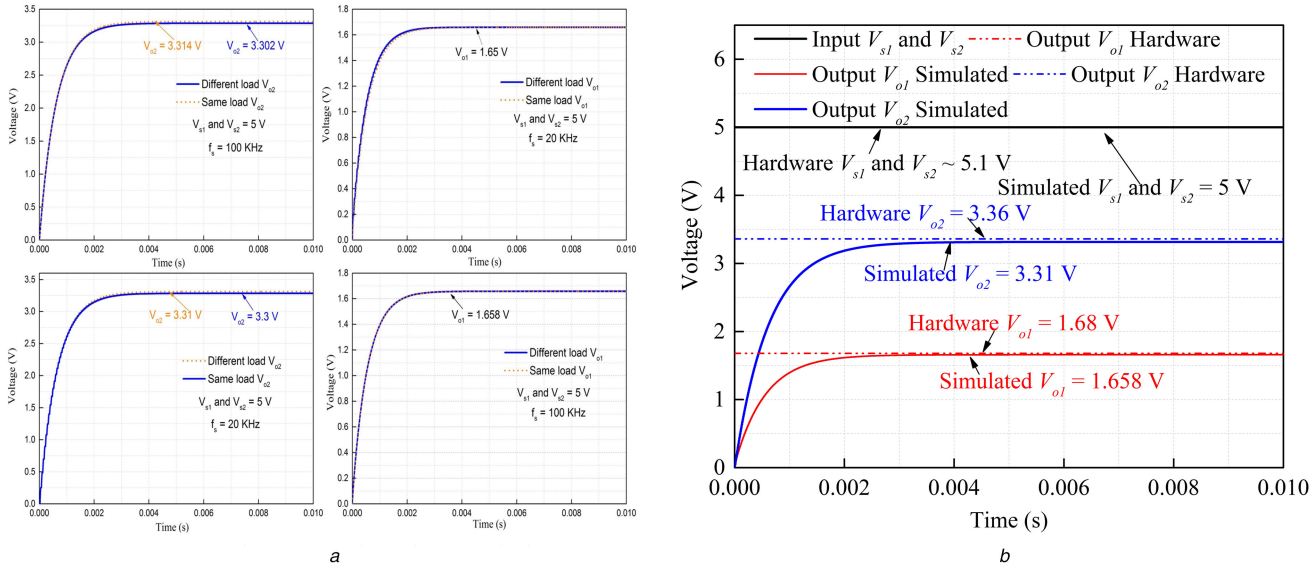


Fig. 7 *Experimental and simulation results of the proposed converter*

(a) Simulation result of different load condition with different frequency, ***(b)*** Comparison of experimental and simulation results of load 10 mA VCRs

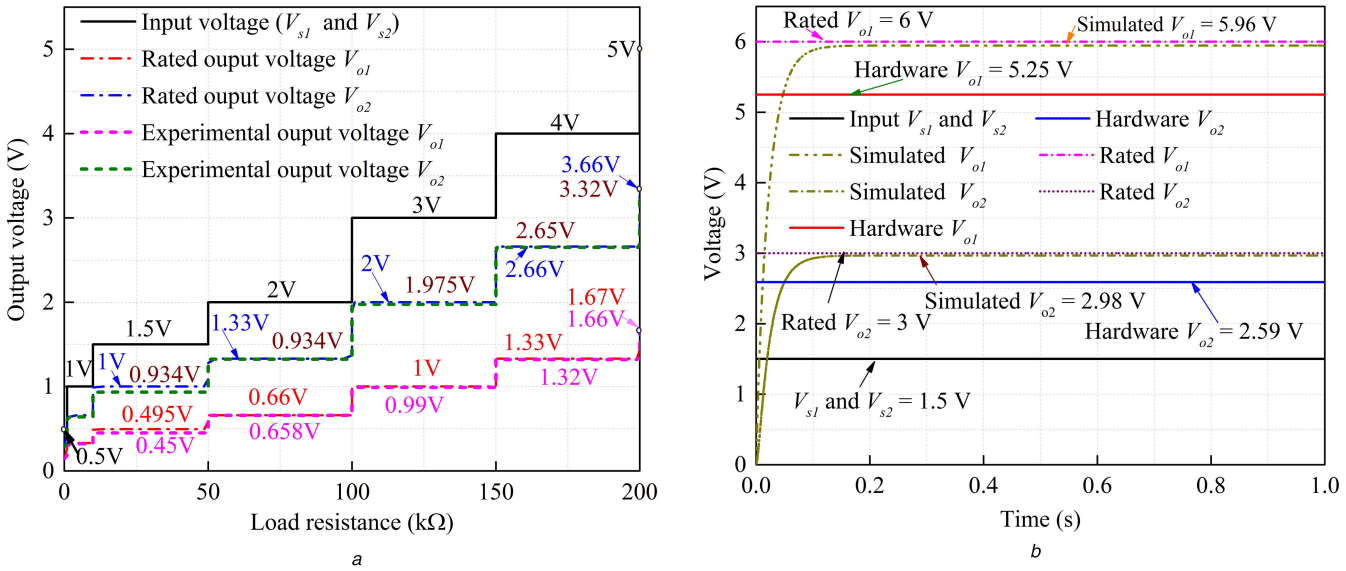


Fig. 8 *Comparison results of proposed converter*

(a) Load variations of the proposed converter for different inputs, ***(b)*** Simulation, experimental, modelling voltage of V_{o1} and V_{o2} of VCRs $V_{o1} = (2*V_{s1}) + (2*V_{s2})$ and $V_{o2} = 2*V_{s1}$

Table 7 Comparison of previous SC VCRs

Authors	Number of switches	No. of input	No. of output	No. of capacitors	VCRs	Efficiency	Specification
[20]	15	1	1	5	2	NA	1 V, <250 mA
[13, 21]	4	2	1	2	1	93%	36 V, <120 mA
[11]	7	1	1	3	2	NA	5.4 V, <120 mA
[14]	14 (include diodes)	2	1	3	11	80–90%	9 V, <120 mA
this work	11	2	2	4	36	>90%	10 V, <100 mA

manuscript assuming (infinitely) large filter capacitance can be considered as an upper bound and in real life, it can be only smaller.

6 Conclusions

The proposed design for DIDO SCC is implemented and validated using *R*-parameters. The converter can implement 36 VCRs some of which are defined as coupled and it is validated by simulation, modelling, and experimental results that are in coincidence to each other. In this designed converter, detailed analysis and modelling were performed for both decoupled and coupled cases. Modelling is based on *R*-parameters coming from two-port network approach. VCR implementation which has series connection of loads is found to have large coupling resistances, which affects to the regulation of outputs. A mathematical model for output voltage cross-regulation is provided and verified with simulations and experimentally. The decoupled case was also analysed with *R*-parameters. The effect of transresistances is practically negligible for this case. Therefore, with decoupled outputs, mathematical modelling can be simplified by treating dual-output SCC as two separate single-output SCCs.

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