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Fast start crystal oscillator design with negative resistance control

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ABSTRACT

Clock is an essential part of most of the integrated circuits as time base reference. It must be very accurate, highly reliable and readily available as soon as it is enabled. In all types of oscillator architectures, crystal oscillator is the most accurate and stable clock generator. But usually the crystal oscillator circuit suffers from slow startup. Therefore, it is essential to improve the startup time with optimally controlled crystal drive such that crystal drive power rating is not compromised. We propose a method that discusses about increasing the negative resistance during startup, using a startup circuit for fast start. Once the reliable startup is achieved, the negative resistance is decreased and the startup circuit is disconnected. The reduction in negative resistance is done with current steps and there are two ways in which it is achieved, the Digital control method and Analog control method. In digital control method, the current steps are timed at regular intervals and in analog control method, oscillator output amplitude is given as feedback to the startup circuit there by reducing the negative resistance. In the 32768 Hz real time clock generating oscillator, the startup time can be improved from 330 ms to 220 ms using the conventional startup method. With the proposed digital control method, lesser startup time of 160 ms is achieved and in analog control method it is further reduced to 120 ms.

1. Introduction

Electronic circuits especially in low-power Micro Controller Unit (MCU) and watch systems need clocks with an accurate and stable frequency. Accurate frequency generation circuits consume a lot of power which is a major concern in battery operated portable devices. Also accurate clock available as soon as the clock system is enabled will reduce the wait time in MCU units for Real Time Clocks (RTC). In most systems where different power modes are defined, along with other circuit systems, the clock oscillators also have dutycycled operation. Usually a low power low frequency RC oscillator is used for quick start the basic operation and then the more stable and accurate clock source is enabled. In some applications where deep sleep mode of operation exists, entire clock system is shutdown to conserve power, retaining the digital logic status as it is, till external event like interrupt wakes it up.

In the sensor/transceiver application, if the transmission message is preceded with a header of a specified length, then it is possible to turn on the receiver periodically to detect a transmission and not miss the transmitted data. This type of operation is known as Sniff Mode [1]. By sniffing at regular interval and then powering down the mixed signal system between successive sniffs, battery life can be improved. During the off time, the digital domain will still have its power supply and retain its logical states and memory without consuming power. The faster the system can be powered up, performs its function and powers down, the lesser is the power that is needed [2].

Generating the clock that is reliable, accurate and available as soon as enabled is very essential for any application that requires the time base reference. In real time clock applications where accuracy and power are very important, crystal oscillator is the most suited circuit [3]. Usually the crystal oscillator circuit suffers from slow startup. If the integrated circuit requires a crystal oscillator circuit, which most do, then the ability to quickly start the crystal to produce a valid stable clock signal is very important without compromising on power rating of the crystal specified in datasheet. Therefore, it is required to address the trade-off between the fast startup and crystal power and reliability. Hence, it is essential to improve the startup time with optimally controlled crystal drive such that crystal drive power rating is not compromised.

Many circuit techniques have been listed in the literature for fast startup of the clock. Some of them include injecting the noise/signal, starting the clock in sync with another ring oscillator [2,4]. These methods need extra circuit to generate the noise or starting clocks. Also these methods can start the clock fast, but may not ensure the stable clock output. The crystal power dissipation is very important factor in

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determining the stability and reliability of the oscillator. Most of the time, power dissipation is limited by external resistor in series with crystal. This external resistor drop reduces the voltage across the crystal. But, this requires extra resistor and also may contribute to failure in some corners. To reduce the crystal drive power, supply voltage can be reduced. This requires added LDO to reduce the supply voltage and may affect the performance of the oscillator across process corners [5,6]. In Ref. [7], author proposes a startup improvement method with periodically switching off the amplifier to avoid the saturation. With the saturation of oscillation, the stored energy in the crystal's equivalent inductor and capacitor is saturated. After the saturation, if the amplifier is disabled, the oscillation will start decaying; and if we enable it again, it will start growing again. Fast startup can also be achieved with large currents [8,9] thereby affecting the transconductance. But for normal operation, these currents have to be reduced later to control the power dissipation across the crystal.

Some authors used multiple startup improving techniques combining noise injection with load capacitor reduction [10,11] and precisely timed energy induction [12]. Though these combined techniques improve the startup time of the oscillator, they require complicated external circuits. These external circuits need time and energy to stabilize, thereby limiting the combined startup time. Although load capacitor reduction method can improve the startup time, it increases the frequency sensitivity and decreases the stability. Hence it is not recommended by crystal manufacturers.

In this paper, a novel method has been proposed to get fast startup by increasing the negative resistance across the crystal terminals. The amount of negative resistance to be increased and the time duration to which it has to be kept active, will decide the startup time and also the crystal drive. Two methods, Digital and Analog, are proposed to control the crystal drive and startup. In the digital method, the control is based on the number of clock cycles generated. For a fixed duration, the negative resistance is applied in steps to avoid the crystal overdrive. A digital feedback circuit is designed to control the startup. In analog control, instead of a fixed number of cycles, the crystal drive voltage amplitude is sensed and it is used to control the startup. Rest of the paper is organized as follows. Section 2 describes the basics of the crystal oscillator circuit and the negative resistance. Crystal oscillator system model is explained in section 3. Design of the circuit is proposed in Section 4. Sections 5 and 6 explain the Digital and Analog startup circuits respectively. Results are discussed in section 7. Section 8 concludes the paper.

2. Crystal oscillator basics

The principle behind any oscillator is a positive feedback loop satisfying the Barkhausen criterion. In the case of crystal oscillator, accuracy of the generated clock depends on the reference element used. There are a number of crystalline materials available as the basic reference element. But Quartz has many characteristics such as good mechanical strength, less variation of size and shape with temperature etc., hence it is most widely and commercially used crystalline element. Fig. 1 shows the simplified electrical equivalent model that describes the quartz crystal, where C_O is the shunt capacitance, L_M is motional inductance, C_M is motional capacitance and R_M is the motional resistance some times also referred to as Equivalent Series Resistance (ESR). For 32768 Hz frequency crystal, the values are as shown in Table 1.

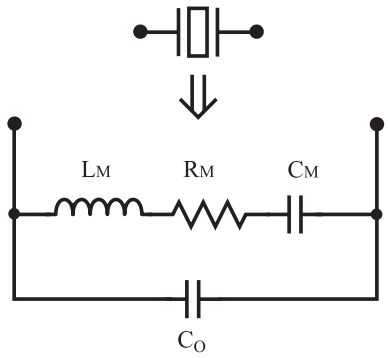

Fig. 1. Quartz crystal electrical model.

Table 1
Crystal model parameters for 32768 Hz frequency crystal.

Parameter	Value	Unit
C_0	1.2	pF
C_M	3.4	fF
L_M	6.9	kH
R_M	70	kΩ

Fig. 2 shows the plots of Phase, Impedance and Reactance variation as frequency varies. The slope of phase curve shows that the crystal has two resonant frequencies denoted by zero phase angle, the first is the series resonant frequency and second is parallel resonant frequency or anti-resonance frequency. The slope of the reactance against frequency shows that below series resonance f_s and above parallel resonance f_p, the crystal appears capacitive. Between frequencies f_s and f_p, the crystal appears inductive as the two parallel capacitances cancel out.

The formula for the crystal's series resonance frequency, f_s is given as in (1) [2].

$$f_s = \frac{1}{2\pi\sqrt{L_M C_M}} \tag{1}$$

The parallel resonance frequency (f_p) occurs when the reactance of the series LC leg equals the reactance of the parallel capacitor, and it is given as in (2).

$$f_p = \frac{1}{2\pi\sqrt{L_M\left(\frac{C_p C_M}{C_p + C_M}\right)}} \tag{2}$$

where C_p is total parallel capacitance. C_p is given by Eq. (3).

$$C_p = C_0 + \left(\frac{C_1 C_2}{C_1 + C_2}\right) \tag{3}$$

where C_0 is the parasitic capacitance between the terminals. C_1 and C_2 are the load capacitances for a specified parallel resonant frequency and their values are specified in the data sheets and denoted as C_L.

As specified in the data sheet of the crystal, the frequency of oscillation lies between the two resonance frequencies as shown in (4).

$$f_s < f_{XTAL} < f_p \tag{4}$$

The oscillator block diagram shown in Fig. 3 is a general architecture usually found in Integrated oscillators in MCUs. The architecture shown is of the pierce oscillator [13].

Bias generator generates the reference current and voltage. Gm-stage is the negative resistance generator along with parallel capacitors across the crystal. The resistance shown across the inverting amplifier is a large resistance used for biasing the inverting amplifier. The Gm-stage can be a single transistor (MOSFET or BJT) or in integrated circuits it could be an inverter. Voltage buildup at the output of the Gm-stage is sinusoidal in nature. To use it as a clock in digital circuits, this must be converted into full logic swing. Clock generation circuit does this function. Startup current generation circuit is the current mirror with switches to control the amount of current given to Gm-stage.

Startup circuit is used for reducing the crystal clock generation and stabilization time. There are many types of startup circuits that are

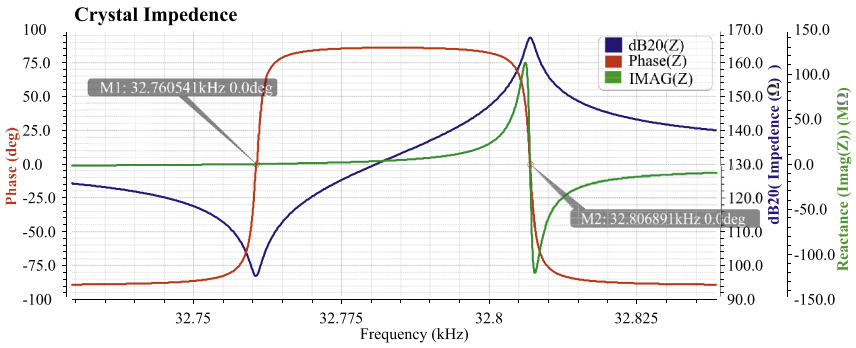

Fig. 2. Crystal electrical model impedance plot.

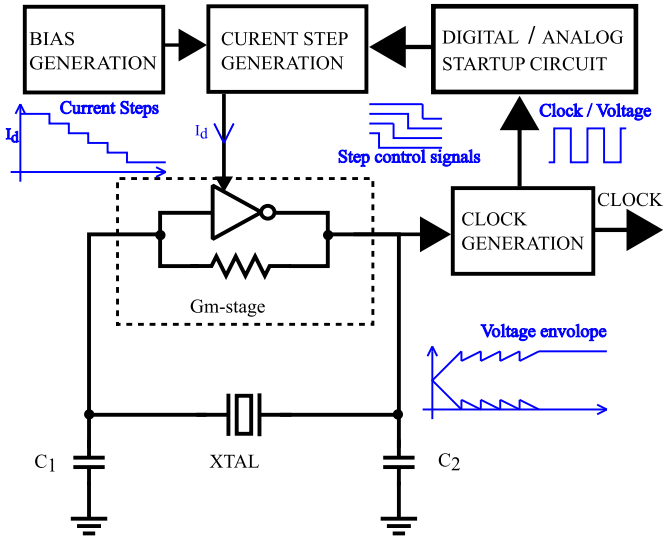

Fig. 3. Block diagram of the oscillator.

being used. In this work, we are proposing two different methods to control the startup time - Digital and Analog. Usually the startup circuit is switched off to save power once stable clock is obtained.

3. System model

As shown in Fig. 3, Gm-stage is the negative resistance generator along with parallel capacitors at terminals XI and XO, across which crystal is connected. As shown in detailed Fig. 4, CMOS transistors MP0 and MN0 are connected in inverter configuration and forms the inverting gain stage. The resistance Rb shown across the inverting amplifier is a large resistance (>1 MΩ) used for DC biasing of the inverting amplifier and implemented with transistors biased in linear region.

3.1. Small signal analysis

Small signal analysis of the Gm-stage shown in Fig. 4 using the small signal model as in Fig. 5, gives the gain equation of the amplifier as in (5).

$$A = A_0 \left[\frac{1 - \frac{s}{z}}{1 + \frac{s}{p}} \right] \tag{5}$$

From the gain equation we can derive the Gain Bandwidth product as given in (6). Detailed derivation is shown in Table 2.

$$GB = \frac{(gm_{MP0} + gm_{MN0})}{C_L} \tag{6}$$

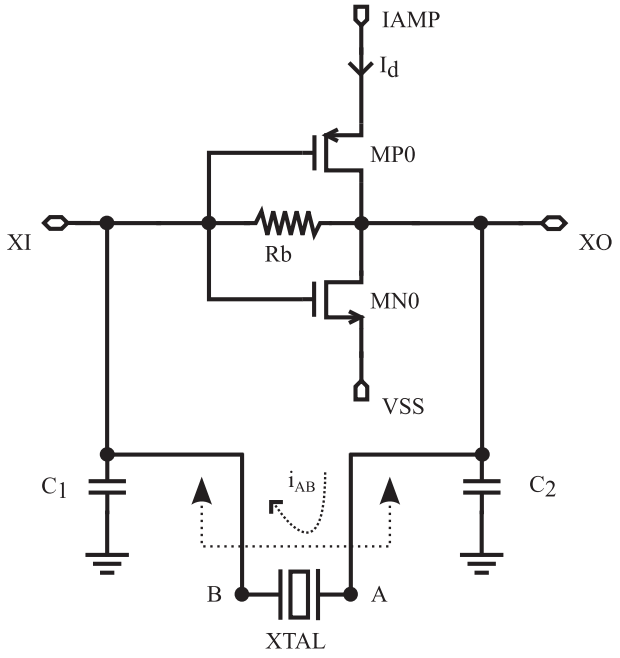

Fig. 4. Gm-stage amplifier circuit.

Gain-Bandwidth product is directly proportional to the sum of transconductances of both the transistors and inversely proportional to the load capacitance (C_L). Plots of sum of the transconductances and the gain of the amplifier are shown in Figs. 6 and 7.

Fig. 6 shows the variation of gm with amplifier current (I_d). A current variation of approximately 10 μA causes a change of 100 μS in the sum of the transconductances. Amplifier current is varied to change the

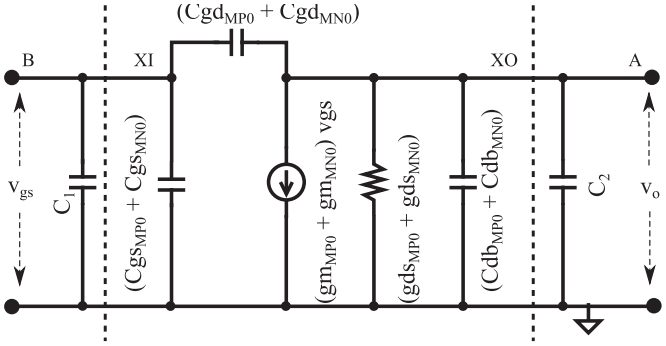

Fig. 5. Small signal model of amplifier.

Table 2
Derivation of equation for Gain-Bandwidth (Eq. (6)).

$$A = A_0 \left[\frac{1-\frac{s}{z}}{1+\frac{s}{p}}\right]$$

At the frequency of interest, the impedance of Cgd and Cdb capacitors of the devices are very large compared to the impedance offered by C_L. Hence,

$$A_0 = -(gm_{MP0} + gm_{MN0})R_0,\ R_0 = \frac{1}{(gds_{MP0} + gds_{MN0})},\ z = \frac{(gm_{MP0} + gm_{MN0})}{(Cgd_{MP0} + Cgd_{MN0})}$$

$$C_0 = (Cgd_{MP0} + Cgd_{MN0} + Cdb_{MP0} + Cdb_{MP0} + C_L)$$

$$p = -\frac{(gds_{MP0} + gds_{MN0})}{(Cgd_{MP0} + Cgd_{MN0} + Cdb_{MP0} + Cdb_{MP0} + C_L)} = -\frac{1}{R_0 C_0} \approx -\frac{(gds_{MP0} + gds_{MN0})}{C_L}$$

Zero occurs at very high frequency, hence it is a single pole system in the region of interest. Gain Bandwidth product (GB) is a constant and is given by the following.

$$GB = A_0 \times p = (-(gm_{MP0} + gm_{MN0})R_0) \times \left(-\frac{1}{R_0 C_0}\right) = \frac{(gm_{MP0} + gm_{MN0})}{C_L}$$

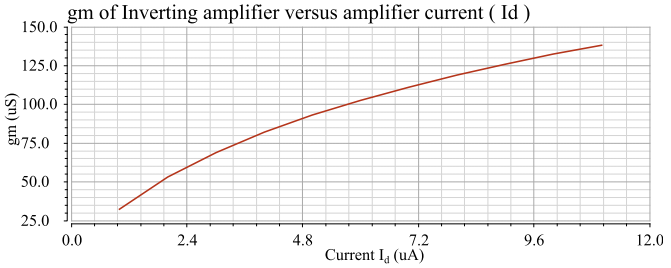

Fig. 6. AC Simulation - $(gm_{MP0} + gm_{MN0})$ of the amplifier versus amplifier current.

negative resistance. Fig. 7 shows the small signal gain of amplifier for max. 11 μA (Full startup current) and min. 1 μA (normal mode current). It is observed that gain bandwidth product is varied as total gm changes (as C_L is held constant). Since gain bandwidth is different, gains are different at 32768 Hz frequency for normal mode and startup mode currents. This I_d variation in amplifier, changes the negative resistance and hence the gain in the loop, which causes faster startup.

3.2. Negative resistance

To obtain the stable oscillation, there should be a balance between the reference element (crystal) and rest of the oscillator circuit. To find the impedance presented to the reference element by the oscillator, the circuit (Fig. 3) can be replaced by a small signal current source as shown in Fig. 8.

The impedance presented to the reference element by C_1, C_2 and the inverter can be denoted as Z_{IN}. It is the effective series combination of the capacitors in series with inverter amplifier. Choosing appropriate values of C_1 and C_2 from the crystal, we can set the crystal's load capacitance. This will set the negative resistance part which is independent of the Gm-stage gain. This analysis suggests that an arbitrary negative resistance can be synthesized for an oscillator using the appropriate transfer characteristic of Gm-stage and capacitor values [14].

$$Z_{IN} = \frac{V}{I} = \frac{V_{AB}}{I_{AB}} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_1} - \frac{g_m}{\omega^2 C_1 C_2} \tag{7}$$

$$\text{Negative resistance } (R_N) = -\frac{g_m}{\omega^2 C_1 C_2} = -g_m X_{C1} X_{C2} \tag{8}$$

The negative resistance can be modeled as shown in Fig. 9.

To ensure robust startup of the crystal oscillator, the magnitude of the negative resistance must be at least 5 times greater than Equivalent Series Resistance (ESR) during the initial start-up of the crystal but can be 2 to 3 times greater than ESR after start-up and during steady state operation. Fig. 10 shows the plot of negative resistance versus amplifier current (I_d).

It is observed that the negative resistance reduces as current is reduced in startup circuit. From Fig. 6 and from Eq. (8) we can infer that negative resistance reduces as the amplifier current is reduced.

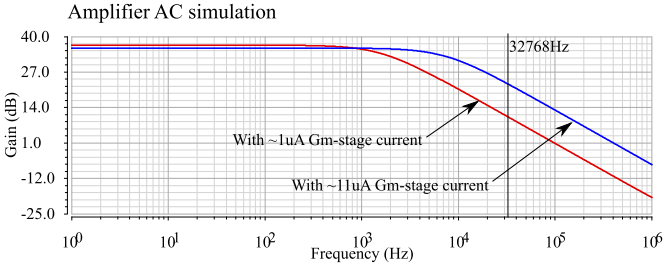

Fig. 7. AC Simulation - Gain plot of the amplifier.

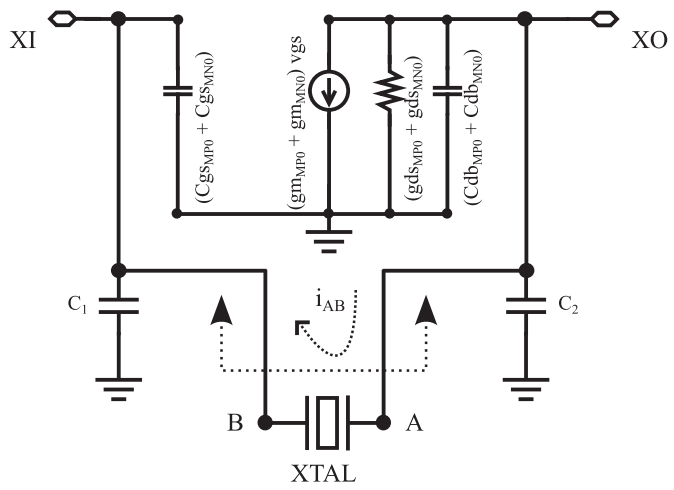

Fig. 8. Oscillator negative resistance analysis.

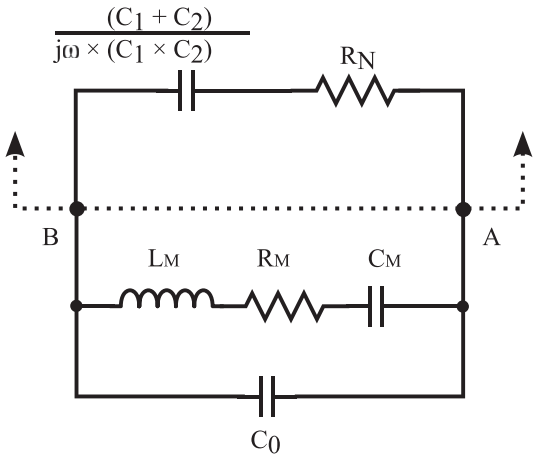

Fig. 9. Crystal oscillator negative resistance model.

Also it is observed that minimum negative resistance is well above 2–3 times of ESR (70 kΩ).

3.3. Startup time

The requirement for startup time varies from system to system, based on how the clock is used. For a microprocessor, the clock should be available as soon as the initial power is applied and in this case startup time is defined as the time to achieve the sustained clock from enable signal. The clock in a phase locked loop circuit must, not only be sustained but also be within the defined accuracy. The startup time of a crystal oscillator is determined by the noise or transient conditions at turn on, small signal envelope expansion due to negative resistance and large signal final amplitude limiting [15].

As shown in Fig. 9, the simplified equivalent series RLC circuit contains the motional inductance (L_M), the sum of the applied negative resistance of the oscillator and the motional resistance of the crystal (R_S) and the effective series capacitance of the entire network dominated by the motional capacitance (C_M). The equation of the un-driven network model of the crystal (refer Fig. 9) can be written as below [15].

$$s \times L_M + R_S + \frac{1}{s \times C_M} = 0 \tag{9}$$

Solving this equation, we can see that, as the net resistance R_S is negative, the poles lie in the right half of the s-plane. The resulting time domain solution for the differential equation can be written as in Eq. (10).

$$V(t) = K_i \times e^{\left(-\frac{R_S}{2L_M}\right)\times t} \times \sin\left[2\pi t\sqrt{\frac{1}{L_M C_M}} + \phi_i\right] \tag{10}$$

where K_i is a constant and ϕ_i is an arbitrary phase, both related to the initial startup conditions. The exponential expansion is valid only for small signal conditions as the power available to the circuit is limited. The envelope expansion is only a function of total negative resistance and the motional inductance of the crystal.

The time constant of the envelope expansion is proportional to the startup time of the oscillator given by

$$\tau = -\frac{2L_M}{R_S} = -\frac{2L_M}{(R_M + R_N)} \approx \frac{2L_M}{|R_N|} \tag{11}$$

Since $|R_N| > > |R_M|$

The time constant for envelope expansion is positive. It is inversely proportional to the net negative resistance of the oscillator and the motional resistance. Also directly proportional to the motional inductance. Due to the large motional inductance of crystals and the limited net negative resistance, crystal oscillators have long startup times.

3.4. Crystal drive level

The drive level of a crystal refers to the power dissipated in the crystal. The maximum drive level of a crystal is often specified in the data sheet of the crystal in μW. Drive level is the maximum power the crystal can handle where all the electrical parameters are guaranteed. Drive level of the crystal is given by

$$\mathrm{DL} = R_M \times 2 \times \left(\pi f_{XTAL}\left(C_M + C_L\right) V_{pp}\right)^2 \tag{12}$$

Where.

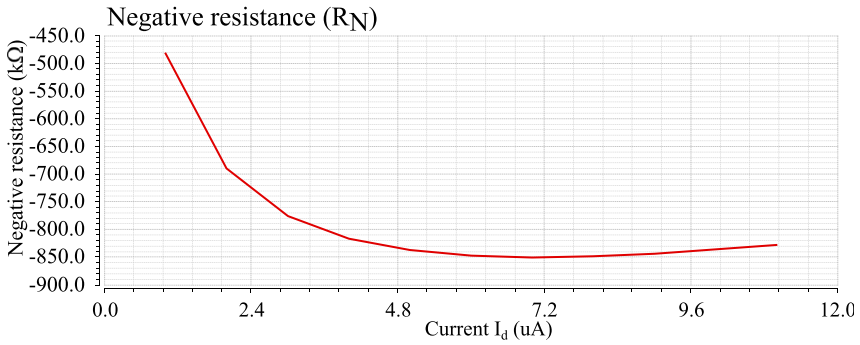

Fig. 10. Negative resistance vs. I_d plot.

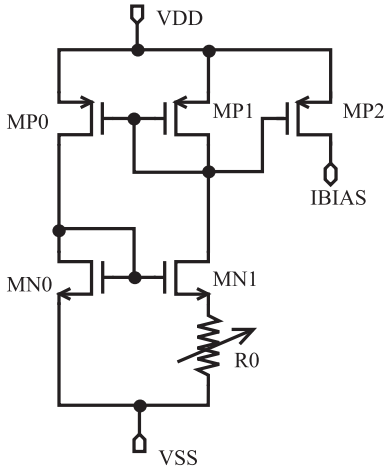

Fig. 11. Bias generation circuit.

C_L is load capacitance for the specified crystal frequency ($C_L = C_1 = C_2$).
f_{XTAL} is crystal oscillator parallel resonance frequency.
V_{pp} is peak to peak voltage across the crystal.

Drive level is defined in crystal datasheet to avoid a number of problems such as high EM emission, reliability issues like physical damage to the crystal, attempting to start at an overtone or failing to start at all etc. It also affects the thermal stability and premature aging of the crystal.

4. Proposed design

Based on the theory discussed in previous section, a fully integrated circuit is designed and simulated in 180 nm CMOS process. The blocks shown in Fig. 3 are explained below. Bias generator, shown in Fig. 11, is a Widlar self biased current generator circuit. The circuit is used for generating small currents without needing large resistor value, which is difficult to fabricate with precision. With MN1 in source degeneration configuration, current is limited to gate to source voltage difference of MN0 and MN1 divided by the resistor value. Thus the small value of resistor will generate the current reference.

Voltage buildup at the output of the gm-stage is sinusoidal in nature. To use the clock in digital circuits we need to convert it into full logic swing. Clock generator in Fig. 12 is a self referenced Schmitt trigger circuit. It is used for converting the sinusoidal waveform to full swing square waveform. Transistors are biased for lower reference trigger. As shown in Fig. 12, circuit has two stages, first stage converts the limited amplitude sinusoidal swing to clock. Second stage consists of inverter that gives the drive strength to output.

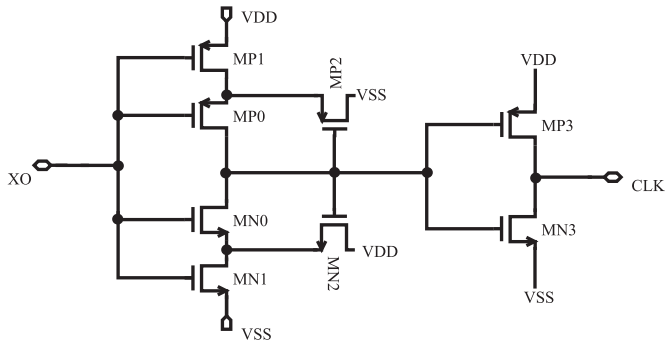

Fig. 12. Clock generation circuit.

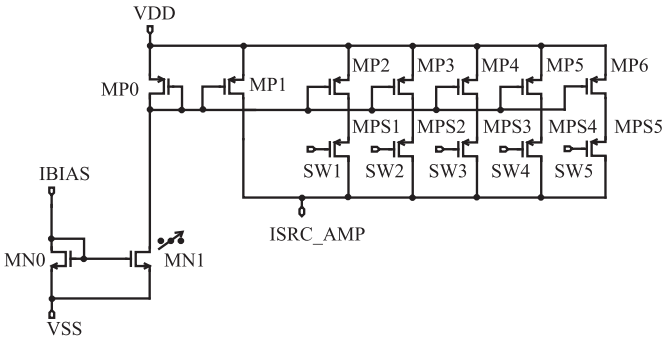

Fig. 13. Startup current step generation circuit.

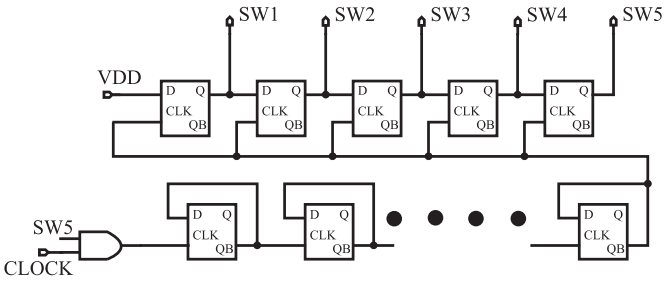

Fig. 14. Digital control generation circuit.

Startup current step generation circuit is used for reducing the crystal clock generation and stabilization time. As shown in Fig. 13, current in the Gm stage is increased with five mirrored stages. The switches (SW1-SW5) are used for controlling the current in each leg. Once the clock starts, it is counted for definite number of cycles or to the point when crystal voltage reaches a set voltage. Then each current mirror is cutoff in sequence, effectively reducing the current in the inverter amplifier.

5. Startup circuit - digital control

Startup time is improved by increasing the current in Gm-stage. However, to avoid the overdrive of crystal, the time duration for which the current is increased is controlled by the timer circuit. The digital timer circuit controls the current reduction in linear and equal intervals. As shown in Fig. 14, a series of D-latches count for specified clock periods before cutting off the current mirrors.

6. Startup circuit - analog control

In order to remove the startup drive current in steps, we can also use a feedback mechanism in analog domain. This will allow us to control the voltage buildup across the crystal and get the optimum startup time, that is better than the digital control method, but at the expense of added circuit. Different circuit blocks designed for the analog control method are explained in the following sub-sections.

6.1. Amplitude detector circuit

First step of the analog control method is to detect the amplitude of the crystal output. For detecting the amplitude, maximum and minimum values of the signal are determined. This is done by the peak and valley detection circuits. Once the maximum and minimum are found, the amplitude is determined using add and subtract circuit. The output of the add and subtract circuit or amplitude measuring circuit is compared with a threshold level using Schmitt trigger circuit with upper

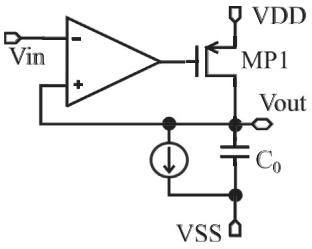

Fig. 15. Peak detector circuit.

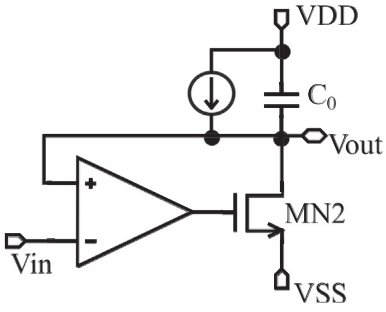

Fig. 16. Valley (Negative peak) detector circuit.

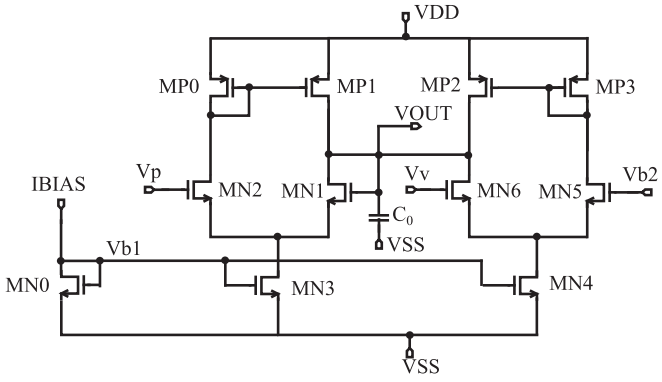

Fig. 17. Signal amplitude detector circuit.

threshold set at the maximum signal amplitude allowed as per the crystal drive voltage specification. The hysteresis of the schmitt trigger circuit is kept low for detection of the reduction in amplitude as the startup current is switched off in steps. Instead of schmitt trigger circuit we can use the comparator as well, but that requires the additional voltage reference circuit. Finally, the digital signal output of the schmitt trigger circuit when amplitude reaches a certain level is given as input to the startup current generation circuit which in turn will cut off the startup currents in steps. Unlike the digital control method where the cut off of currents is done at constant interval of time, in analog control method, these steps are triggered by amplitude of the oscillator output, hence improving the startup time.

6.1.1. Peak and valley detector circuits

The maximum and minimum of the oscillator output voltage is determined by the peak and valley detector circuits.

As shown in Figs. 15 and 16, Peak and Valley detection circuits find the envelope of the oscillator output waveform. These circuits produce the output contouring the peak and valley of the input waveform. The difference of the output voltages of these two circuits gives the amplitude of the oscillator swing.

6.1.2. Amplitude value detector

From the peak and valley detector circuits, the magnitude of oscillator swing can be obtained by subtracting the valley voltage (Vv) from the peak voltage (Vp). An analog add subtract circuit is used as shown in Fig. 17 [16]. The circuit will produce the output waveform which is the difference of the two inputs, Vp and Vv, with a DC level of the third input, Vb2.

Add subtract circuit has two amplifiers, first one acts as a unity gain buffer and second as difference current generator. Both the amplifiers are biased by the reference current from bias generator. First amplifier has same current (half of bias current) in both the legs and both inputs and output are at same voltage value which is equal to the input, Vp. The second amplifier gives an output current which is proportional to the difference between the two inputs Vb2 and Vv. Since the outputs of both amplifiers are connected together, capacitor connected at this node gets current which is sum of first and second amplifier output currents, which in turn generates a voltage proportional to Vp − Vv + Vb2.

7. Results and analysis

7.1. Oscillator performance analyses

It is of equal importance to analyze the oscillator parameters for stability, sustainability and accuracy as getting it started fast. These parameters are analyzed across supply (1.8 V ± 10%) and temperature (−40 to 85 °C) corners using Monte-Carlo simulations with device mismatch.

7.1.1. Negative resistance

Once the oscillator is started, the current is reduced. The reduced current should produce enough negative resistance to overcome the losses in crystal and other parasitics. As discussed earlier, the negative resistance should be approximately 2–3 times of the crystal motional

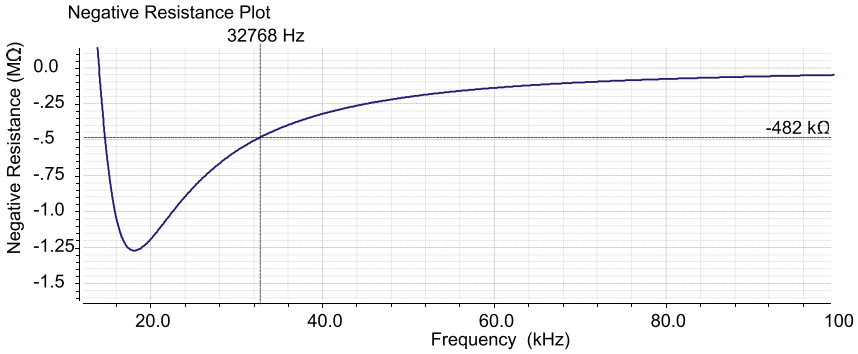

Fig. 18. Simulation results of negative resistance at typical condition.

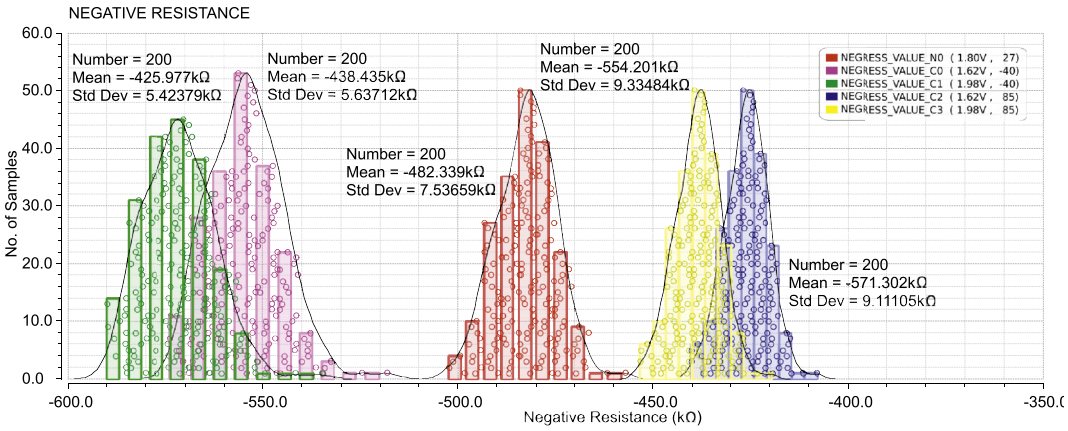

Fig. 19. Montecarlo Simulations - Negative resistance at 32768 Hz.

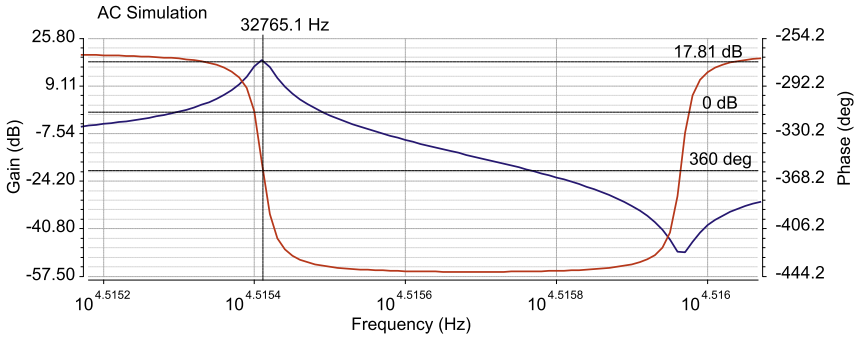

Fig. 20. Simulation results of frequency analysis zoomed at the region of interest.

resistance. As shown in Figs. 18 and 19, the simulation results show that, there is sufficient negative resistance at the required resonance frequency for sustained oscillations.

Montecarlo simulations with device mismatch across supply and temperature corners (Fig. 19) show variation between − 408 kΩ (Min) and −589.8 kΩ (Max). The minimum value is greater than 5 times the ESR (70 kΩ) as required by design.

7.1.2. AC simulation

The AC simulation shows the stability and accuracy of the circuit. To meet the Barkhausen criterion for oscillation, the circuit must show 360° phase shift in loop and gain at this point must be greater than 1.

Fig. 20 shows the AC simulation (gain and phase analysis) at typical corner condition. It can be seen that a phase shift of 360° is observed at the resonance frequency. Other point to note is, there are two frequencies at which phase shift is 360°. But at the second frequency, the gain is less than one and hence oscillations will not sustain at this frequency and hence this can be ignored.

Montecarlo simulation results with device mismatch across supply and temperature corners are shown in Figs. 21 and 22. Frequency variation between 32764.8 Hz (min) and 32766.3 Hz (max) and a Gain variation between 15.94 dB (min) and 19.98 dB (max) are observed.

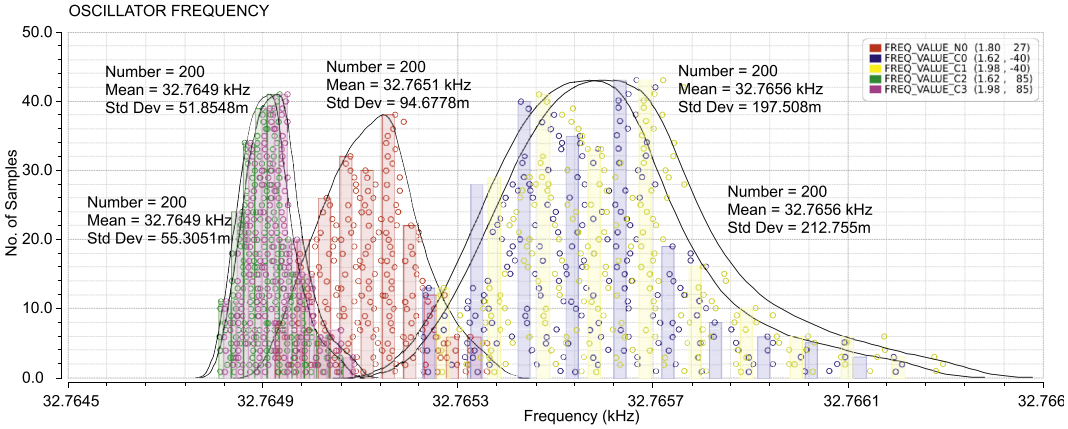

Fig. 21. Montecarlo simulation - Frequency variation.

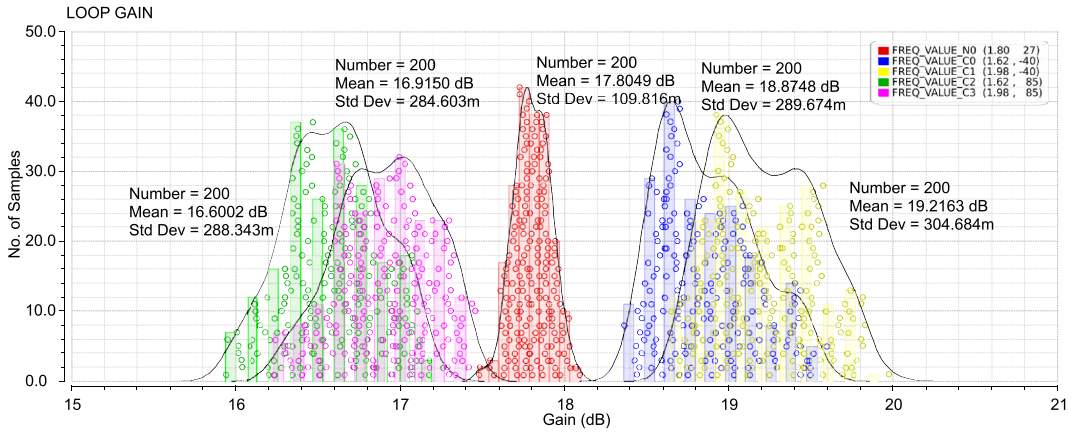

Fig. 22. Montecarlo simulation - Gain variation.

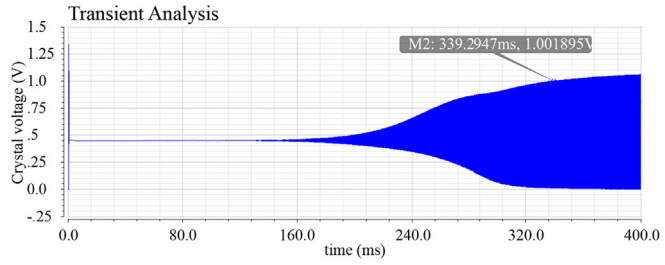

Fig. 23. Voltage buildup across the crystal without startup improvement circuit.

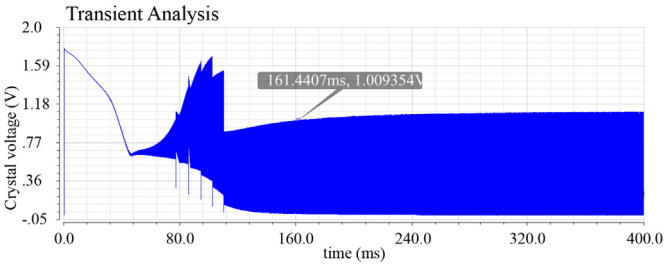

Fig. 26. Voltage buildup with digital control.

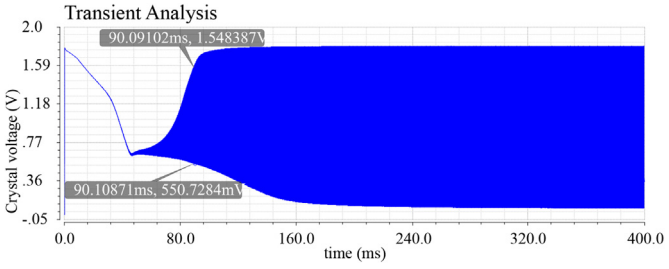

Fig. 24. Voltage buildup of high power mode.

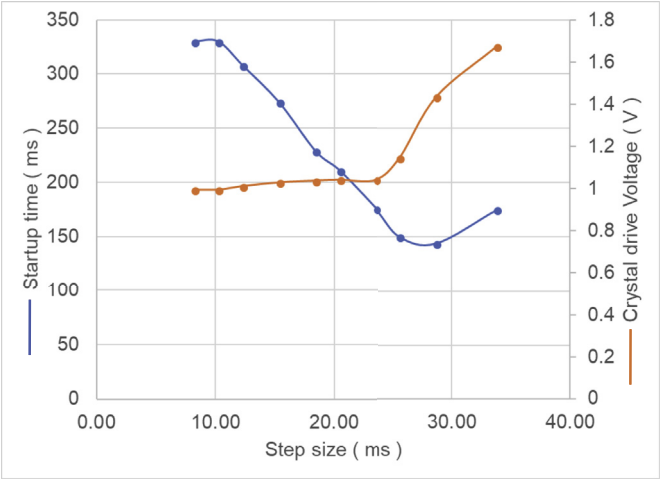

Fig. 27. Plots of Startup time and Crystal Drive voltage vs. Step size.

7.2. Oscillator startup behavior analyses

The circuit is simulated and results are compared for startup behavior, without startup circuit and with conventional single step startup circuit with that of proposed step wise negative resistance reduction method.

Fig. 23 shows the simulation result of the voltage buildup of crystal without startup improvement circuit. Gm-stage current is approxi-

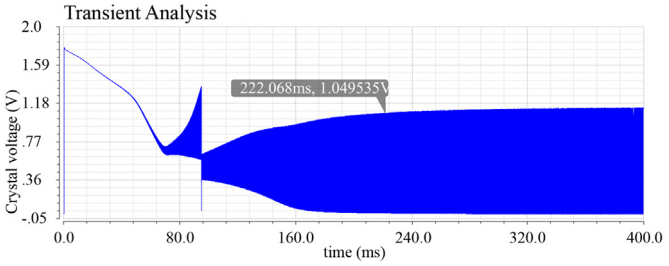

Fig. 25. Voltage buildup with switch to low power mode.

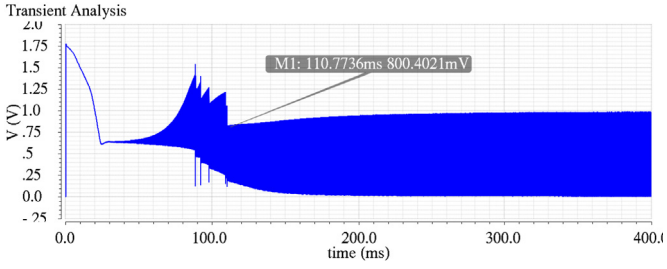

Fig. 28. Simulation results of analog control.

Table 3
Comparison of startup time (simulated) with other published works (measured).

	Frequency	Process	Startup time	Number of cycles	Power Consumption
[17]	39 MHz	40 nm	208 μs	8112	9.2 μW
[18]	39 MHz	180 nm	158 μs	6162	181 μW
[19]	4.19 MHz	180 nm	800 μs	3355	–
[20]	32.768 kHz	–	1 s	32768	–
[21]	32.768 kHz	–	400 ms	13107	450 μW
This Work	32.768 kHz	180 nm	120/160 ms	3840	11 μW

mately 1 μA (Current is representation of the Negative resistance). It can be observed that the crystal oscillation buildup to a set voltage (90% of final settling amplitude, approximately 1 V) is taking long time, approximately 330 ms.

One method of improving the startup time is by giving the startup current for a long time to ensure quick startup, then at arbitrary large time, it may be switched off when external controller decides. This circuit is simulated with a higher current of approx 11 μA (same as the peak current when startup circuit is active). As shown in Fig. 24, with increased current, the startup time is reduced to approximately 90 ms. But in this case, the voltage buildup across the crystal is beyond the set voltage and this increases the power dissipation in crystal and goes beyond the rated drive power of the crystal. For the crystal we referred (FC135) with a specification of 1 μW max power dissipation, from Eq. (12), the value of voltage (Vpp) comes to 1.0385 V.

From theory and the previous simulation result as in Fig. 24, it has been found that the startup time can be improved by increasing the current in amplifier. Conventionally to avoid the overdrive of the crystal, it is switched to low power mode after the oscillations are built up sufficiently or to the set level of voltage (approx 1 V). However, sudden change of the drive will alter the crystal voltage buildup and may cause the clock instability. As shown in Fig. 25, it is required to wait till approx 220 ms for the voltage to buildup again. This method no doubt will improve the startup time, but the improvement is very small. With this, crystal drive limit will not get exceeded.

7.2.1. Startup circuit - digital control

In the proposed method to improve the startup time, the high current mode is held till the voltage across the crystal is built up sufficiently and remove the current drive in multiple steps than in a single step. This way, extra drive is provided just long enough for startup process to happen. As shown in Fig. 26, the steps are kept at regular time apart and faster startup of 160 ms is observed.

The timing of the step size is limited such that the crystal drive limit is not exceeded. As shown in Fig. 27, as the timing is reduced, the startup time will increase whereas increase in the step time beyond certain limit will exceed the crystal drive limit. The best suited step timing can be determined by observing the crystal voltage. This can be done easily while doing post-silicon measurements.

7.2.2. Startup circuit - analog control

As discussed in previous digital control method, once the clock starts, the startup current is removed in steps with regular interval. This interval is fixed and kept at minimum across the corner so that crystal is not overdriven. There is risk of this interval becoming too small to sustain the oscillation or too large where the crystal is over driven. This timing is critical, hence it should be adjusted properly.

Analog control method relies on the amplitude feedback. Once the current is reduced in startup circuit, it will wait for the oscillator to reach the designated voltage, before cutting off the next current step. If oscillator output increases faster, all the current steps are cut off quickly. On the other hand, if amplitude reduces too low the feedback circuit waits for more time for oscillator to stabilize. This was not possible in digital control method.

As shown in Fig. 28, the startup time is improved with amplitude control method and a startup time of 120 ms is achieved.

7.2.3. Power consumption

For fast startup of the crystal oscillator we need to increase the negative resistance which will in turn take energy. Power consumption in steady state is almost the same for both digital and analog startup methods as startup improvement circuits are shutdown once the oscillator is stable, which is approx 11 μW. The startup energy consumed by entire oscillator for the digital startup method is 3.2 μJ and for analog startup method it is 3.9 μJ. The startup energy required by only the startup circuits is 2.4 nJ in digital startup method and 1.2 μJ in analog startup method.

7.3. Comparison of results with literature

Crystal oscillator startup time is simulated using the proposed methods and the results are compared with published works and commercially available devices. Startup time in higher frequency crystal oscillator is inherently better than the lower frequency due to the low quality factor. Thus startup time improvement is very essential in the case of low frequency crystal oscillator. Table 3 shows the startup time normalized for number of cycles. We can observe that the present work gives better startup time compared to other RTC (Real Time Clock) oscillators.

Although the work of [19] has slightly better startup time result than the present work, the crystal used in this work is of higher frequency (Low quality factor, hence easier to start). Also in this work ([19]) multiple startup improvement methods like noise injection, capacitor cutting are used, which in turn require additional circuitry.

8. Conclusions

In this paper, a novel approach to improve the startup time of the crystal is proposed. The theory provides necessary insight to synthesize the optimum solution with respect to frequency stability, power consumption and crystal drive limit. The overall startup method and factors affecting the startup time are discussed with relevant equations. Analysis and simulations show the relation between Gm-stage current and negative resistance. Fully integrated circuit shows the practicability of the proposed method of startup. The simulation and analysis show that the proposed method results in much better startup behavior in comparison with conventional startup circuit and without startup circuit.

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